THE DATASHEET OF

ADP1828ACPZ-R7

Synchronous Buck PWM, Step-Down, DC-to-DC Controller

Data Sheet **ADP1828**

FEATURES

- Wide bias voltage range 3.0 V to 20 V
- Wide power stage input range 1 V to 24 V
- Wide output voltage range: 0.6 V to 85% of input voltage
- ±0.85% accuracy at 0°C to 70°C
- All N-channel MOSFET design for low cost
- Fixed-frequency operation at 300 kHz, 600 kHz, or resistor adjustable 300 kHz to 600 kHz
- Clock output for synchronizing other controllers
- No current sense resistor required
- Internal linear regulator
- Voltage tracking for sequencing
- Soft start and thermal overload protection
- Overvoltage and undervoltage power-good indicator
- 15 µA shutdown supply current
- Available in a 20-lead QSOP and 20-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- Telecom and networking systems
- Base station power
- Set-top boxes, game consoles
- Printers and copiers
- Medical imaging systems
- DSP and microprocessor core power supplies
- DDR termination

GENERAL DESCRIPTION

The ADP1828 is a versatile and synchronous PWM voltage mode buck controller. It drives an all N-channel power stage to regulate an output voltage as low as 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators. The ADP1828 is ideal for a wide range of high power applications, such as DSP and processor core I/O power, and general-purpose power in telecommunications, medical imaging, PC, gaming, and industrial applications. It operates from input bias voltages of 3 V to 20 V with an internal LDO that generates a 5 V output for input bias voltages greater than 5.5 V.

The ADP1828 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, or at any frequency between 300 kHz and 600 kHz with a resistor. The switching frequency can also be synchronized to an external clock up to 2× the nominal oscillator frequency of the device The clock output can e used for synchronizing additional ADP1828s (or the ADP1829 controllers), thus eliminating the need for an external clock source. The ADP1828 includes soft start protection to limit any inrush current from the input supply during startup, reverse current protection during soft start for a precharged output, as well as a unique adjustable lossless current-limit scheme utilizing external MOSFET R_{DSON} sensing.

For applications requiring power-supply sequencing, the ADP1828 provides a tracking input that allows the output voltage to track during startup, shutdown, and faults. The additional supervisory and control features include thermal overload, undervoltage lockout, and power good.

The ADP1828 operates over the −40°C to +125°C junction temperature range and is available in a 20-lead QSOP and 20-lead, 4 mm × 4 mm LFCSP.

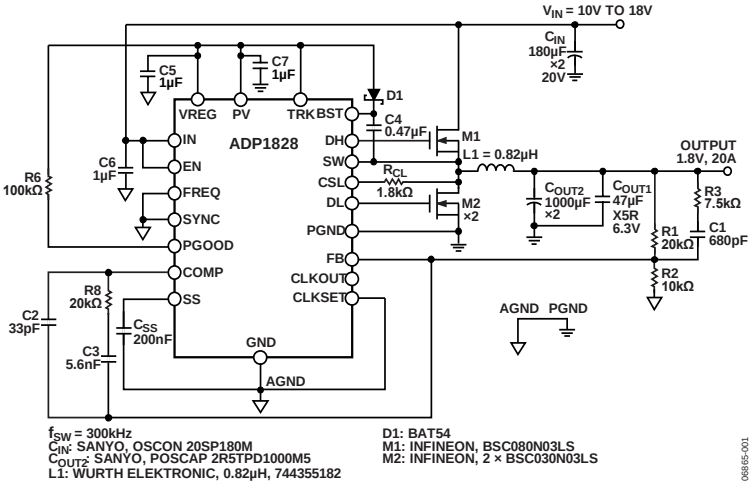

Figure 1. Typical Application Circuit with 20 A Output

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9/2007—Revision 0: Initial Version

SPECIFICATIONS

IN = 12 V, PV = V_{EN} = V_{TRK} = 5 V, SYNC = GND, unless otherwise specified. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). T_J = −40°C to +125°C, unless otherwise specified. Typical values are at T_A = 25°C.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
IN Input Voltage	PV is tied to VREG, IN is not tied to VREG (using internal regulator)	5.5		20	V
IN Input Voltage	IN = PV = VREG, IN is tied to VREG (not using internal regulator)	3.0		5.5	V
IN Quiescent Current	Not switching, I_{VREG} = 0 mA		1.5	3.0	mA
IN Shutdown Current	EN = GND		5	15	µA
VREG-to-GND Shutdown Impedance	EN = GND, IN is not tied to VREG		1.6		MΩ
VREG Undervoltage Lockout Threshold	VREG rising	2.4	2.7	3.0	V
VREG Undervoltage Lockout Hysteresis	VREG falling		0.125		V
ERROR AMPLIFER					
FB Regulation Voltage	T_A = 25°C, TRK > 700 mV	597	600	603	mV
	T_A = 0°C to +70°C, TRK > 700 mV	595		605	mV
	T_J = −40°C to +125°C, TRK > 700 mV	591		609	mV
FB Input Bias Current			5	100	nA
Open-Loop Voltage Gain			70		dB
Gain-Bandwidth Product			20		MHz
COMP Sink Current			600		µA
COMP Source Current			120		µA
COMP Clamp High Voltage	IN = VREG = 3 V		2.4		V
	IN = 12 V		3.6		V
COMP Clamp Low Voltage			0.75		V
LINEAR REGULATOR					
VREG Output Voltage	IN = 5 V+ dropout voltage to18 V, I_{VREG} = 100 mA T_J = −40°C to +125°C	4.75	5.0	5.25	V
VREG Load Regulation	I_{VREG} = 0 mA to 100 mA, IN = 5.25 V to 18 V		−10		mV
VREG Line Regulation	IN = 5 V+ dropout voltage to 18 V, no load		1		mV
VREG Current Limit	VREG drops to 4 V		220		mA
VREG Short-Circuit Current	VREG drops to 0.4 V	60	140	200	mA
IN to VREG Dropout Voltage[1]	I_{VREG} = 100 mA, IN < 5 V		0.6	1.0	V
VREG Minimum Output Capacitance		1			µF
PWM CONTROLLER					
VRAMP Peak-to-Peak Voltage[2]		0.7	1.0	1.45	V
DH Maximum Duty Cycle	FREQ = GND (300 kHz)	91	93		%
DH Minimum On Time	Any frequency		100		ns
DL Minimum On Time	Any frequency		200		ns
SOFT START					
SS Pull-Up Resistance	SS = GND		90		kΩ
SS Pull-Down Resistance	SS = 0.6 V		6		kΩ
SS to FB Offset Voltage	SS = 0 mV to 500 mV		−45		mV
SS Pull-Up Voltage			0.8		V
TRACKING					
TRK Common-Mode Input Voltage Range		0		600	mV
TRK to FB Offset Voltage	TRK = 0 mV to 500 mV	−5.5		+5	mV
TRK Input Bias Current				100	nA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OSCILLATOR					
Oscillator Frequency	SYNC = FREQ = GND	240	300	360	kHz
	SYNC = GND, FREQ = VREG	480	600	720	kHz
	R_{FREQ} = 57.6 kΩ	240	300	360	kHz
	R_{FREQ} = 35.7 kΩ	370	450	530	kHz
	R_{FREQ} = 24.9 kΩ	480	600	720	kHz
SYNC Synchronization Range	FREQ = GND	300		600	kHz
	FREQ = VREG	600		1200	kHz
SYNC Input Pulse Width		200			ns
SYNC Pin Capacitance			5		pF
CURRENT SENSE					
CSL Threshold Voltage	Relative to PGND	−17	−38	−58	mV
CSL Output Current	CSL = PGND	42	50	56	µA
Current Sense Blanking Period			100		ns
GATE DRIVERS					
DH Rise Time	C_{DH} = 3 nF, $V_{BST} - V_{SW}$ = 5 V		15		ns
DH Fall Time	C_{DH} = 3 nF, $V_{BST} - V_{SW}$ = 5 V		10		ns
DL Rise Time	C_{DL} = 3 nF		15		ns
DL Fall Time	C_{DL} = 3 nF		10		ns
DH or DL Driver R_{ON}, Sourcing Current[3, 4]	Sourcing 1.5 A with a 0.1 µs pulse		2		Ω
DH or DL Driver R_{ON}, Sinking Current[3, 4]	Sinking 1.5 A with a 0.1 µs pulse		1.5		Ω
DH or DL Driver R_{ON}, Sourcing Current	IN = VREG = 3 V; sourcing 1 A with a 0.1 µs pulse		2.3		Ω
DH or DL Driver R_{ON}, Sinking Current	IN = VREG = 3 V; sinking 1 A with a 0.1 µs pulse		2		Ω
DH to DL, DL to DH Dead Time			40		ns
CLOCK OUT					
CLOCKOUT Pulse Width			360		ns
CLKOUT Rise or Fall Time	C_{CLKOUT} = 47 pF		10		ns
SYNC to CLKOUT Propagation Delay, t_{PD}	C_{CLKOUT} = 47 pF, C_{SYNC} = 5 pF		40		ns
SYNC to CLKOUT Propagation Delay, t_{PD}	C_{CLKOUT} = 47 pF, C_{SYNC} = 5 pF, IN < 5 V		52		ns
LOGIC THRESHOLDS					
SYNC, CLKSET, FREQ Logic High		1.8			V
SYNC, CLKSET Logic Low				0.4	V
FREQ Logic Low				0.25	V
CLKSET, SYNC, FREQ Input Leakage Current	CLKSET, SYNC, FREQ = 0 V or VREG			1	µA
EN Input Threshold		1.1	1.5	1.8	V
EN Input Threshold Hysteresis			0.2		V
EN Current Source	EN = 0 V to 3.0 V	−0.1	−0.6	−1.5	µA
EN Input Impedance to 5 V Zener	EN = 5.5 V to 20 V		100		kΩ
THERMAL SHUTDOWN					
Thermal Shutdown Threshold[4]			145		°C
Thermal Shutdown Hysteresis[4]			15		°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER GOOD					
FB Overvoltage Threshold	V_{FB} rising	700	750	810	mV
FB Overvoltage Hysteresis			50		mV
FB Undervoltage Threshold	V_{FB} falling	500	550	585	mV
FB Undervoltage Hysteresis			50		mV
PGOOD Propagation Delay			8		µs
PGOOD Off Leakage Current	V_{PGOOD} = 5.5 V			1	µA
PGOOD Output Low Voltage	I_{PGOOD} = 10 mA		150	500	mV

[1] Connect IN to VREG when IN < 5.5 V. For applications with IN < 5.5V and IN not connected to VREG, keep in mind that VREG = V_{IN} – dropout. VREG must be ≥ 3 V for proper operation.
[2] V_{RAMP} = 1.0 V × f_{OSC}/f_{SW}, where f_{OSC} is the natural oscillator frequency and f_{SW} is the actual switching frequency. If SYNC is not used, then $f_{OSC} = f_{SW}$. If SYNC is used, then $f_{SW} = f_{SYNC}$.
[3] With a 5 V drive, the peak source or sink current can be up to 2.5 A and 3.3 A, respectively, when driving external power MOSFETs. The duration of the peak current pulse is generally in the order of 10 ns.
[4] Guaranteed by design and characterization. Not subject to production test.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN	−0.3 V to +20.5 V
EN	−0.3 V < IN + 0.3 V
PV, SYNC, FREQ, COMP, SS, FB, PGOOD, CLKSET, CLKOUT, VREG, TRK	−0.3 V to +6 V
BST-to-GND, SW-to-GND	−0.3 V to +30 V
BST-to-SW	−0.3 V to +6 V
BST-to-GND, SW-to-GND, 50 ns transients	+38 V
SW-to-GND, 30 ns negative transients	−7 V
CSL-to-GND	−1 V to +30 V
DH-to-GND	(SW − 0.3 V) to (BST + 0.3 V)
DL-to-PGND	−0.3 V to (PV + 0.3 V)
PGND-to-GND	±2 V
θ_{JA}, 20-Lead QSOP on a Multilayer PCB (Natural Convection)[1]	83°C/W
θ_{JA}, 20-Lead LFCSP on a Multilayer PCB (Natural Convection)[1]	35.6°C/W
Operating Junction Temperature[2]	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Maximum Soldering Lead Temperature	260°C

[1] Junction-to-ambient thermal resistance (θ_{JA}) of the package was calculated or simulated on a multilayer PCB.

[2] The junction temperature, T_J, of the device is dependent on the ambient temperature, T_A, the power dissipation of the device, P_D, and the junction-to-ambient thermal resistance of the package, θ_{JA}. Maximum junction temperature is calculated from the ambient temperature and power dissipation using the formula $T_J = T_A + P_D \times \theta_{JA}$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SIMPLIFIED BLOCK DIAGRAM

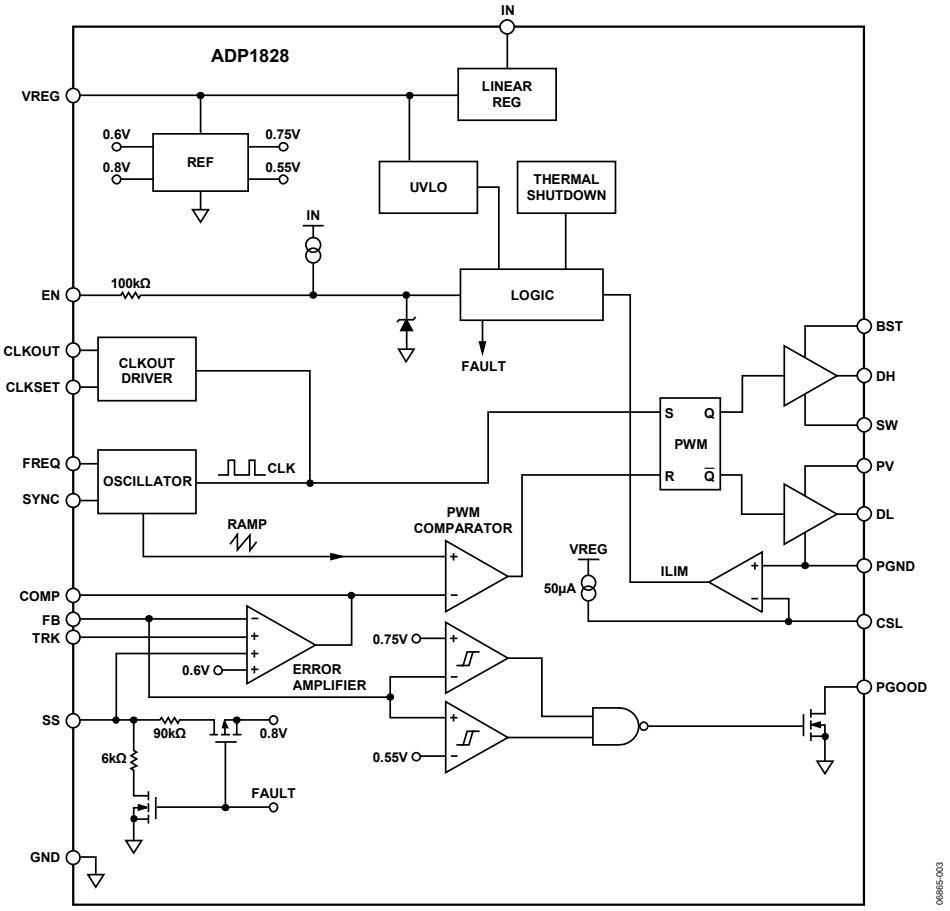


Figure 2. Simplified Block Diagram

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

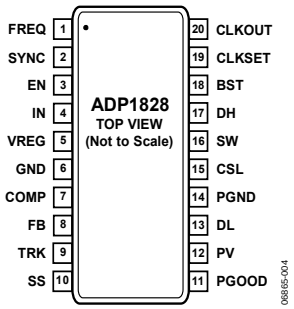


Figure 3. 20-Lead QSOP Pin Configuration

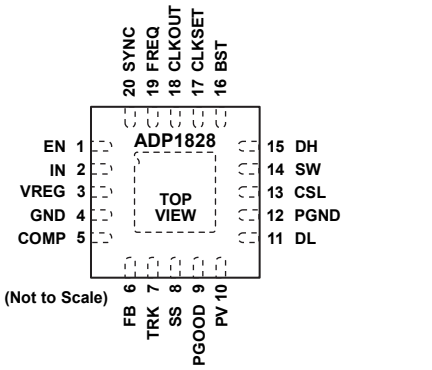


Figure 4. 20-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

QSOP Pin No.	LSCSP Pin No.	Mnemonic	Description
1	19	FREQ	Frequency Control Input. Low for 300 kHz, high for 600 kHz, or connect a resistor from FREQ to GND to set the free-running frequency between 300 kHz and 600 kHz.
2	20	SYNC	Frequency Synchronization Input. Accepts external signals between 300 kHz and 600 kHz if FREQ is set to low, or between 600 kHz and 1.2 MHz if FREQ is set to high. If f_{OSC} is set by R_{FREQ}, then the synchronization frequency range is from f_{OSC} up to 600 kHz. If SYNC is not used, connect SYNC to GND or VREG. V_{SYNC} can be driven up to 6 V even when V_{IN} is less than 6 V.
3	1	EN	Enable Input. Drive EN high or tristate EN to turn on the ADP1828 controller, and drive it low to turn off. Connect EN to IN for automatic startup.
4	2	IN	Input Supply to the Internal Linear Regulator. Drive IN with 5.5 V to 20 V to power the ADP1828 from LDO, VREG; tie PV to VREG. For input voltages between 3 V and 5.5 V, tie IN, PV, and VREG together.
5	3	VREG	Output of the Internal Linear Regulator (LDO). The internal circuitry and gate drivers are powered from VREG. Bypass VREG to AGND plane with 1 µF ceramic capacitor for stable operation, for example, a 10 V X5R 1 µF ceramic capacitor is sufficient. The VREG output is 5 V when IN = 5 V + dropout. Connect IN to VREG and PV when IN = 3 V to 5.5 V. For applications with IN < 5.5 V and IN not connected to VREG, keep in mind that VREG = VIN – dropout. VREG needs to be ≥3 V for proper operation.
6	4	GND	Ground for Internal Circuits. Tie the bottom of the feedback dividers to this GND.
7	5	COMP	Error Amplifier Output. Connect an RC network from COMP to FB for loop compensation.
8	6	FB	Voltage Feedback. Connect a resistor divider from the buck regulator output to GND and tie the tap to FB to set the output voltage.
9	7	TRK	Tracking Input. To track a master voltage, drive TRK from a voltage divider from the master voltage. If the tracking function is not used, connect TRK to VREG.
10	8	SS	Soft Start Control Input. Connect a capacitor from SS to GND to set the soft start period.
11	9	PGOOD	Open-Drain Power-Good Output. Sinks current when FB is out of regulation. Connect a pull-up resistor from PGOOD to VREG.
12	10	PV	Positive Input Voltage for Gate Driver DL. When IN is 3 V to 5.5 V, connect IN to VREG and PV. Connect a 1 µF bypass capacitor from PV to PGND. When IN = 5.5 V to 20 V, connect PV to VREG.
13	11	DL	Low-Side (Synchronous Rectifier) Gate Driver Output.
14	12	PGND	Power GND. Ground for gate driver.
15	13	CSL	Current Sense Comparator Inverting Input. Connect a resistor between CSL and SW to set the current-limit offset.
16	14	SW	Switch Node Connection.
17	15	DH	High-Side (Switch) Gate Driver Output.
18	16	BST	Boost Capacitor Input. Powers the high-side gate driver DH. Connect a 0.22 µF to 0.47 µF ceramic capacitor from BST to SW and a Schottky diode from PV to BST.

QSOP Pin No.	LSCSP Pin No.	Mnemonic	Description
19	17	CLKSET	Clock Set Input. Setting CLKSET to logic high (connect CLKSET to VREG) sets the CLKOUT to 2× the internal oscillator frequency and is in phase with the oscillator. Setting CLKSET to logic low sets the CLKOUT to 1× the oscillator frequency and 180° out of phase.
20	18	CLKOUT	Clock Output. The CLKOUT frequency, f_{CLKOUT}, is either 1× or 2× the oscillator frequency. CLKOUT can 0be used to synchronize another ADP1828 or ADP1829 controllers. Set f_{CLKOUT} to 1× when synchronizing another ADP1828, or to 2× when synchronizing the ADP1829. If SYNC is used, $f_{SYNC} = f_{CLKOUT}$ independent of the CLKSET voltage. CLKOUT is able to drive a 100 pF load.
N/A[1]	EPAD	EPAD	Exposed Pad. Connect the bottom exposed pad of the LFCSP package to system AGND plane.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

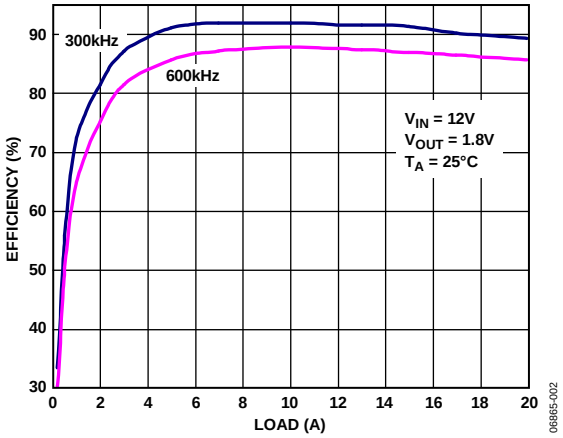


Figure 5. Efficiency vs. Load Current of Figure 1

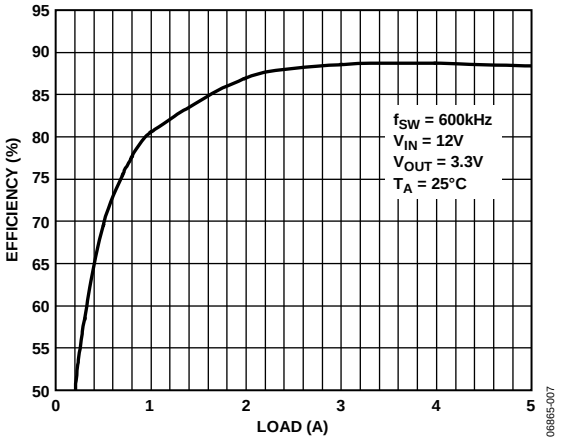


Figure 8. Efficiency vs. Load Current of Figure 55

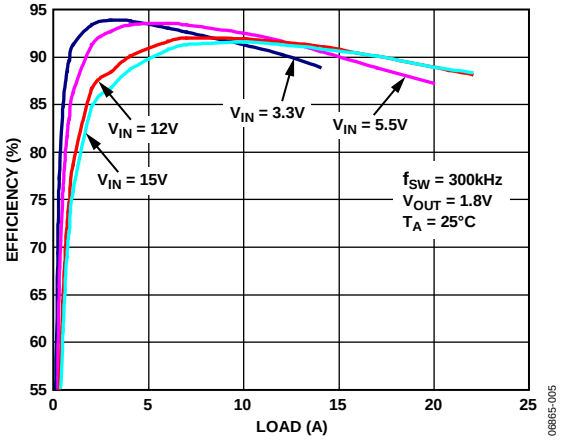


Figure 6. Efficiency vs. Load Current of Figure 1

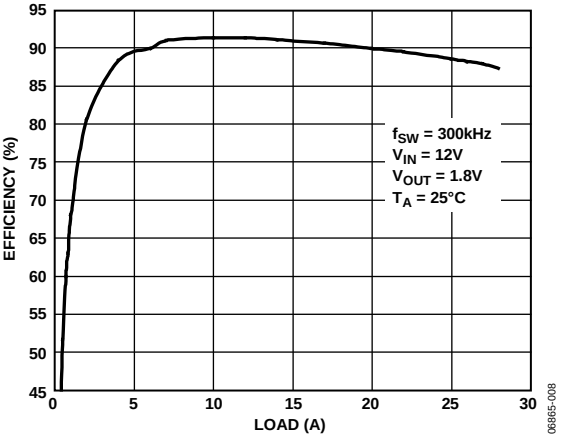


Figure 9. Efficiency vs. Load Current of Figure 57

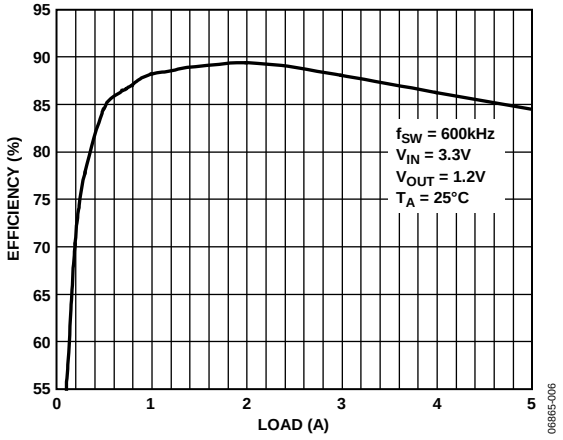


Figure 7. Efficiency vs. Load Current of Figure 54

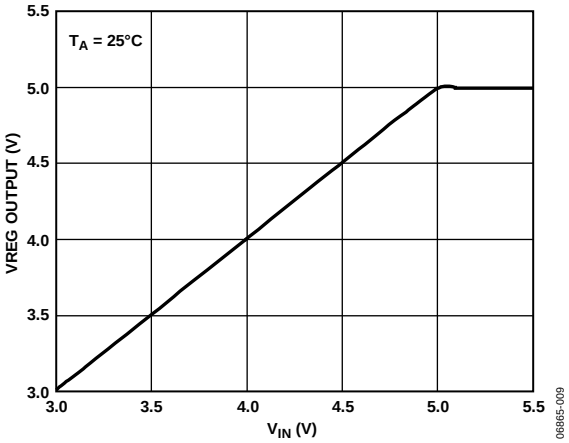


Figure 10. VREG in Dropout, No Load

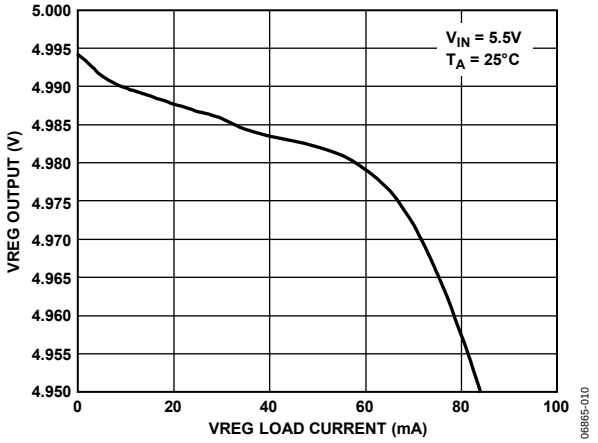


Figure 11. VREG vs. Load Current

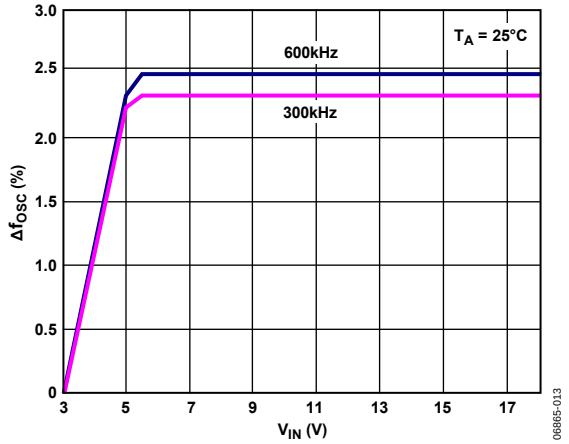


Figure 14. Δf_{OSC} vs. V_{IN}, Referenced at V_{IN} = 3 V

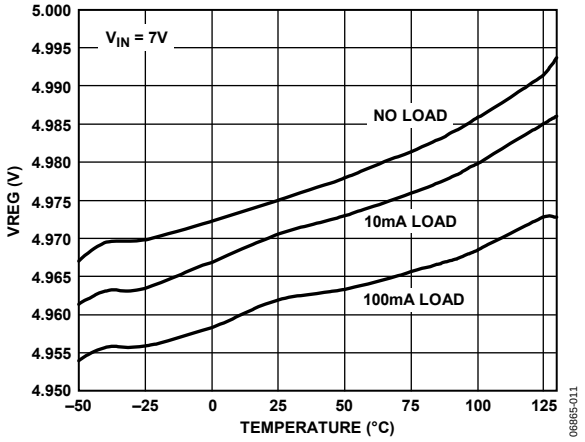


Figure 12. VREG Voltage vs. Temperature

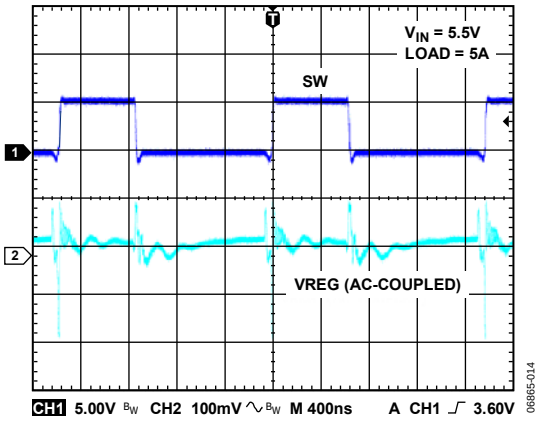


Figure 15. VREG Output of Figure 55

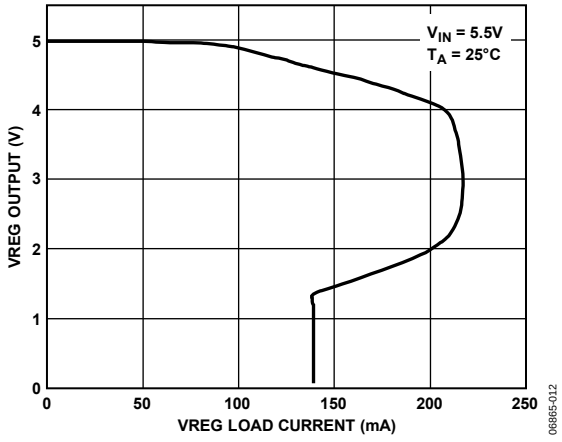


Figure 13. VREG Current-Limit Foldback

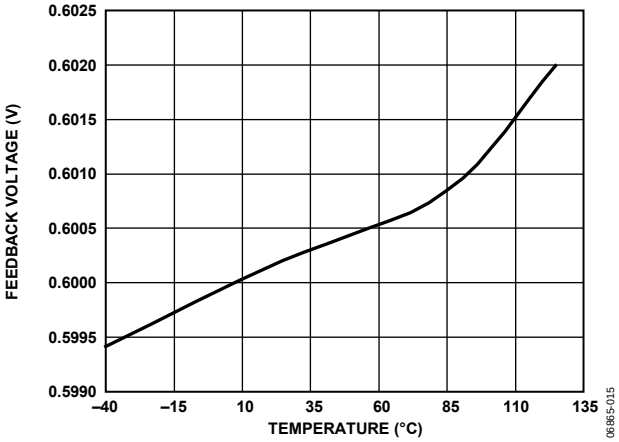


Figure 16. Feedback Voltage vs. Temperature, V_{IN} = 12 V

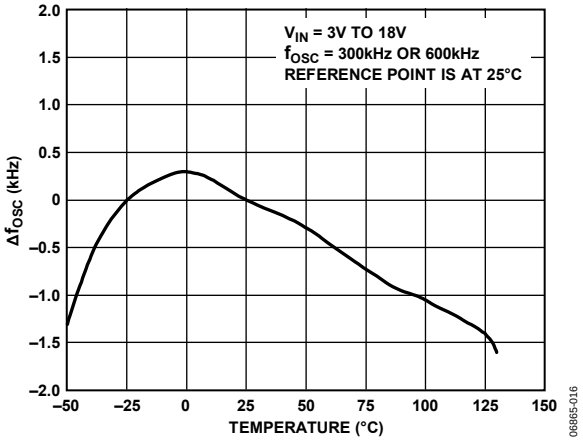


Figure 17. Δ f_{OSC} vs. Temperature

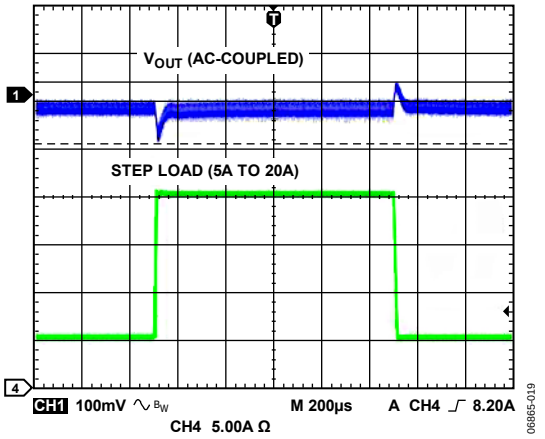


Figure 20. Load Transient Response of Figure 1, 5 A to 20 A, V_{IN} = 12 V

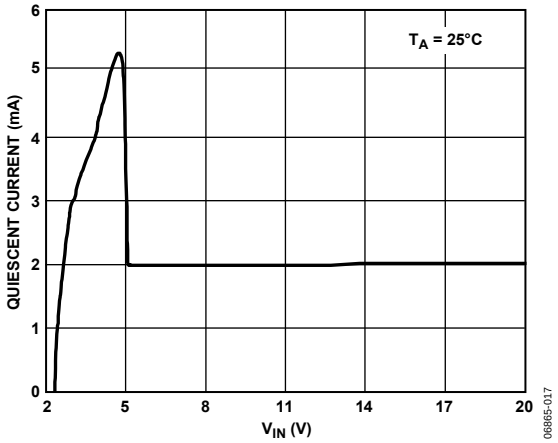


Figure 18. Supply Current vs. Input Voltage

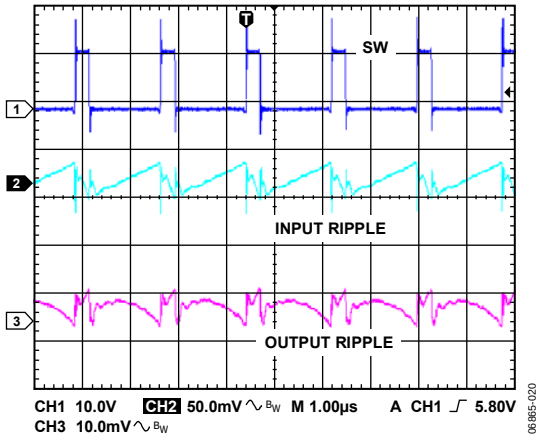


Figure 21. Input and Output Ripple of Figure 55, 4 A Load

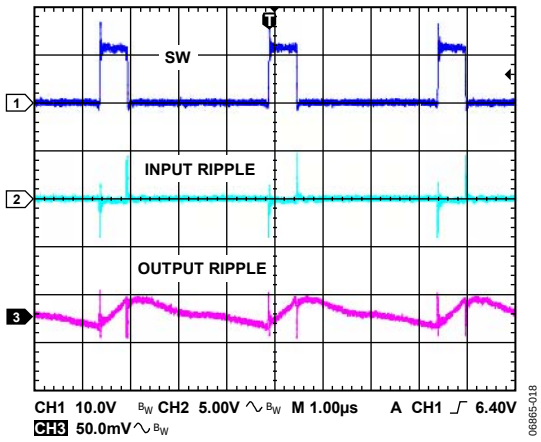


Figure 19. Input and Output Ripple of Figure 1, 22 A Load

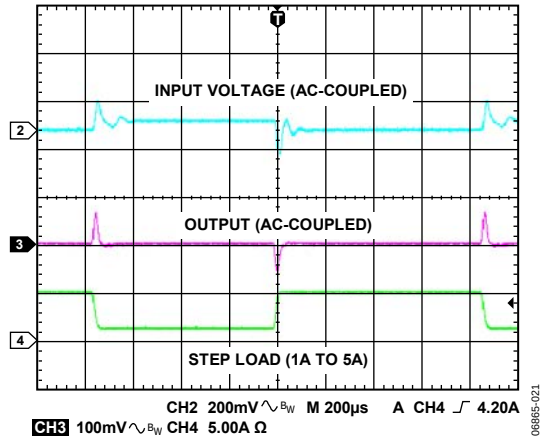


Figure 22. Load Transient Response of Figure 55, 1 A to 5 A, V_{IN} = 12 V

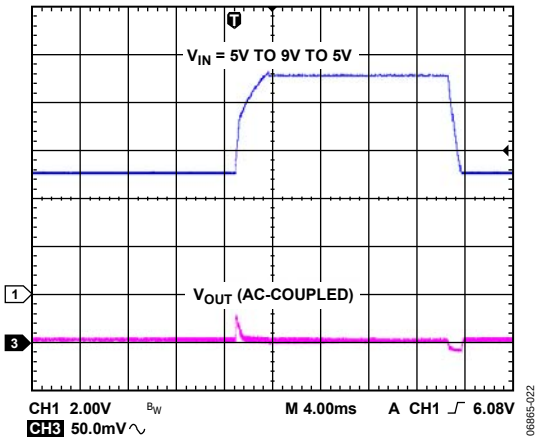


Figure 23. Line Transient Response of Figure 1, No Load

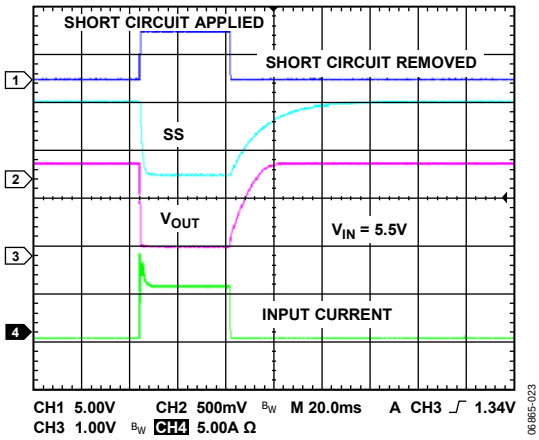


Figure 24. Output Short-Circuit Response

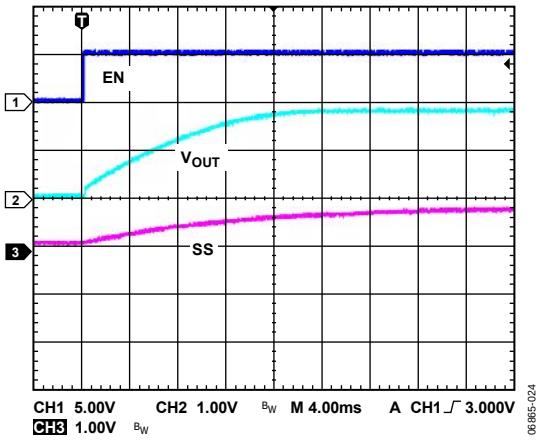


Figure 25. Soft Start and Inrush Current of Figure 1

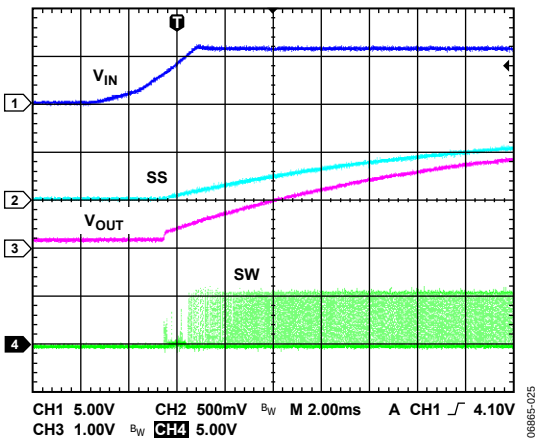


Figure 26. Power-On Response, EN Tied to V_{IN}

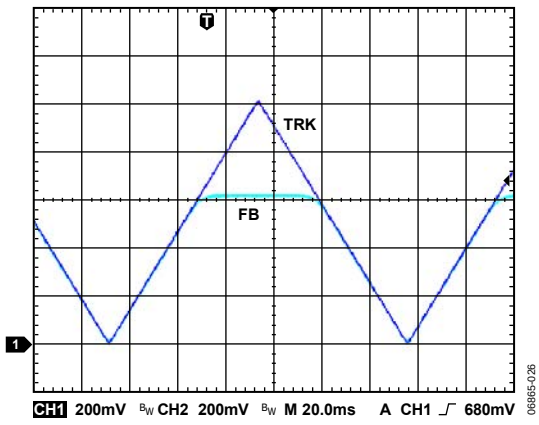


Figure 27. Tracking, TRK from 0 V to 1 V

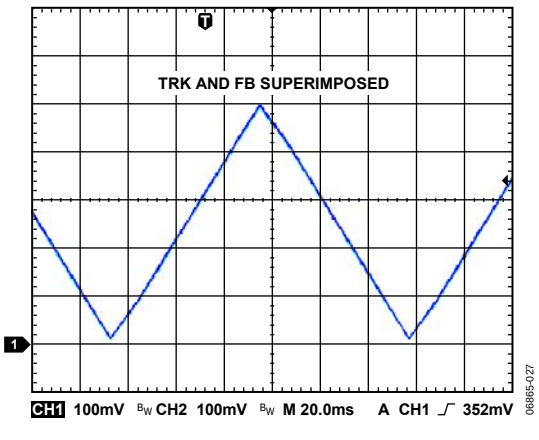


Figure 28. Tracking, TRK from 0 V to 0.5 V

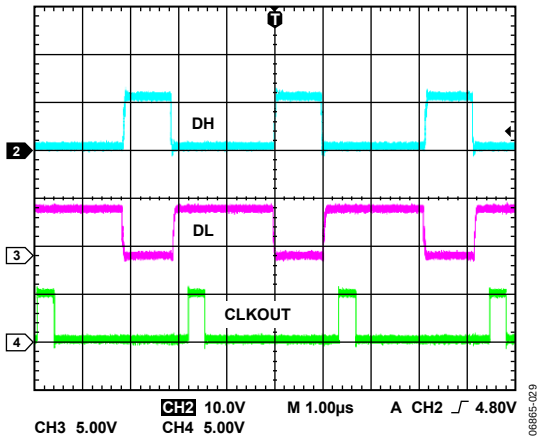


Figure 29. CLKOUT, CLKSET = 0 V

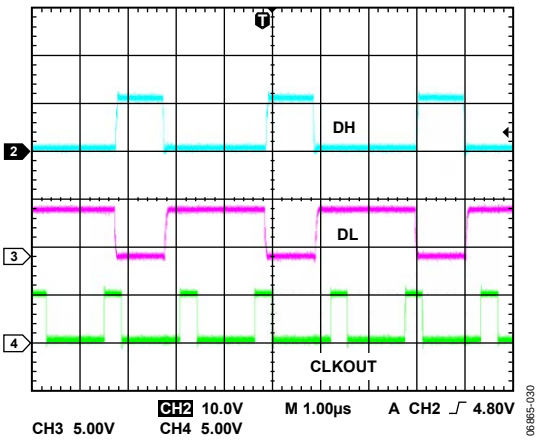


Figure 30. CLKOUT, CLKSET = 5 V

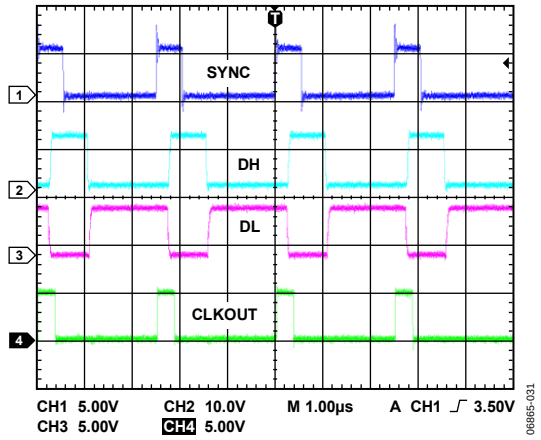


Figure 31. SYNC

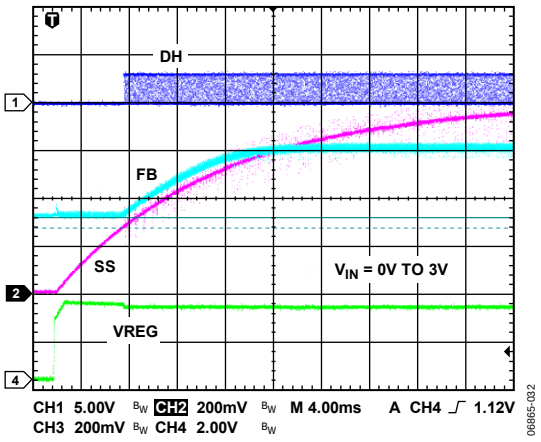


Figure 32. Start into Precharged Output

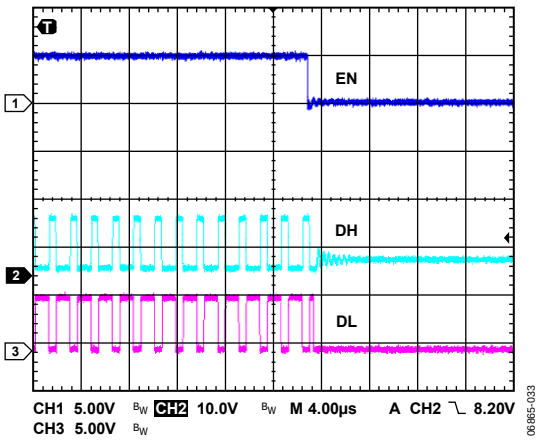


Figure 33. EN, Shutdown

THEORY OF OPERATION

The ADP1828 is a versatile, synchronous-rectified, fixed-frequency, pulse-width modulation (PWM), voltage mode, step-down controller capable of generating an output voltage as low as 0.6 V to 85% of the input voltage. It is ideal for a wide range of applications, such as DSP and processor core input/output supplies, general-purpose power in telecom, medical imaging, gaming, PCs, set-top boxes, and industrial controls. The ADP1828 controller operates directly from 3 V to 20 V, and includes fully integrated MOSFET gate drivers and a linear regulator for internal and gate drive bias.

The ADP1828 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, or operates at any frequency between 300 kHz and 600 kHz by connecting a resistor between FREQ and GND. The switching frequency can also be synchronized to an external clock up to 2× the nominal oscillator frequency of the device. The built-in clock output can be used for synchronizing the ADP1829 and other ADP1828 controllers, thus eliminating the need for an external clock source. The ADP1828 also includes clockout, voltage tracking, thermal overload protection, undervoltage lockout, power good, soft start to limit inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, and an adjustable lossless current-limit scheme utilizing external MOSFET R_{DSON} sensing. The ADP1828 operates over the −40°C to +125°C junction temperature range and is available in a 20-lead QSOP.

INPUT POWER

The ADP1828 is powered from the IN pin from 3.0 V up to 20 V. The internal low dropout linear regulator, regulates the IN voltage down to 5 V when IN is between 5.5 V and 20 V. The output of the LDO is denoted as VREG. The control circuits, gate drivers, and the external boost capacitor operate from the LDO output for IN between 5.5 V and 20 V. PV powers the low-side MOSFET gate drive (DL), and IN powers the internal control circuitry. Bypass PV to PGND with a 1 µF or greater capacitor, and bypass IN to GND with a 0.1 µF or greater capacitor. Bypass the power input to PGND with a suitably large capacitor.

The VREG output is sensed by the undervoltage lockout (UVLO) circuit to be certain that enough voltage headroom is available to run the controllers and gate drivers. As VREG rises above about 2.7 V, the controllers are enabled. The IN voltage is not directly monitored by the UVLO circuit. If the IN voltage is insufficient to allow VREG to be above the UVLO threshold, the controllers are disabled, but the LDO continues to operate. The LDO is enabled and cannot be turned off whenever EN is high, even if VREG is below the UVLO threshold.

For a supply voltage between 5.5 V and 20 V, connect IN to the supply voltage, and tie VREG to PV. For a supply voltage between 3 V and 5.5 V, connect IN, PV, and VREG to the supply voltage. In this case, the input supply voltage directly powers the low-side gate driver.

While IN is limited to 20 V, the switching stage can run from up to 24 V and the BST pin can go to 30 V to support the gate drive. This can provide an advantage, for example, in the case of high frequency operation from high input voltage. Power dissipation in the ADP1828 can be limited by running IN from a low voltage rail while operating the switches from the high voltage rail.

INTERNAL LINEAR REGULATOR

The internal linear regulator has low dropout, meaning it can regulate its output voltage (VREG) close to the input voltage. It powers up the internal control circuitry and provides bias for the gate drivers when VREG is tied to PV. It is guaranteed to have more than 100 mA of output current capability, which is sufficient to handle the gate drive requirements of typical logic threshold MOSFETs driven at up to 1.2 MHz. Bypass VREG to AGND with a 1 µF or greater capacitor.

Because the LDO supplies the gate drive current, the output of VREG is subjected to sharp transient currents as the drivers switch and the boost capacitors recharge during each switching cycle. The LDO has been optimized to handle these transients without overload faults. Due to the gate drive loading, using the VREG output for other auxiliary system loads is not recommended.

The LDO includes a current limit well above the expected maximum gate drive load. This current limit also includes a short-circuit fold back to further limit the VREG current in the event of a short-circuit fault.

SOFT START

The ADP1828 employs a programmable soft start that reduces input current transients and prevents output overshoot. SS drives an auxiliary positive input to the error amplifier; thus, the voltage at this pin regulates the voltage at the feedback control pin.

Program the soft start by connecting a capacitor from SS to GND. On startup, the capacitor charges from an internal 90 kΩ resistor to 0.8 V. The dc-to-dc converter output voltage rises with the voltage at the soft start pin, allowing the output voltage to rise slowly and reducing the inrush current.

If the output voltage is precharged prior to turn-on, the ADP1828 prevents reverse inductor current, which would discharge the output capacitor. When the voltage at SS exceeds the regulation voltage (typically 0.6 V), the reverse current is re-enabled to allow the output voltage regulation to be independent of load current.

When a controller is disabled or experiences any form of fault condition, the soft start capacitor is discharged through an internal 6 kΩ resistor, so that at restart or recovery from fault the output voltage soft starts again.

ERROR AMPLIFIER

The ADP1828 error amplifier is an operational amplifier. The ADP1828 senses the output voltage through an external resistor divider at the FB pin. The FB pin is the inverting input to the error amplifier. The error amplifier compares this feedback voltage to the internal 0.6 V reference, and the output of the error amplifier appears at the COMP pin. The COMP pin voltage then directly controls the duty cycle of the switching converter.

A series/parallel RC network is tied between the FB pin and the COMP pin to provide the compensation for the buck converter control loop. A detailed design procedure for compensating the system is provided in the Compensating the Voltage Mode Buck Regulator section.

The error amplifier output is clamped between a lower limit of about 0.75 V and a higher limit of up to about 3.6 V, depending on the VREG voltage. When the COMP pin is low, the switching duty cycle goes to 0%, and when the COMP pin is high, the switching duty cycle goes to the maximum.

The SS and TRK pins are auxiliary positive inputs to the error amplifier. Whichever voltage is lowest (SS, TRK, or the internal 0.6 V reference) controls the FB pin voltage and the output. Consequently, if two of these inputs are close to each other, a small offset is imposed on the error amplifier.

CURRENT-LIMIT SCHEME

The ADP1828 employs a programmable, cycle-by-cycle lossless current-limit circuit that uses an inexpensive resistor to set the threshold. Every switching cycle, the synchronous rectifier turns on for a minimum time and the voltage drop across the MOSFET R_{DSON} is measured to determine if the current is too high.

This measurement is done by an internal current-limit comparator and an external current-limit setting resistor. The resistor is connected between the switch node (that is the drain of the rectifier MOSFET) and the CSL pin. The CSL pin, which is the inverting input of the comparator, forces 50 μA through the resistor to create an offset voltage drop across it.

When the inductor current is flowing in the MOSFET rectifier, its drain is forced below PGND by the voltage drop across its R_{DSON}. If the R_{DSON} voltage drop exceeds the preset drop on the current-limit resistor, the inverting comparator input is similarly forced below PGND and an overcurrent fault is flagged.

The normal transient ringing on the switch node is ignored for 100 ns after the synchronous rectifier turns on, so the overcurrent condition must also persist for 100 ns for a fault to be flagged.

When the ADP1828 senses an overcurrent condition, the next switching cycle is suppressed, the soft start capacitor is discharged through an internal 6 kΩ resistor, and the error amplifier output voltage is pulled down. The ADP1828 remains in this mode for as long as the overcurrent condition persists.

Note that the current-limit scheme in the ADP1828 is not the same as a short-circuit protection. The ADP1828 does not go into current foldback in the event of a short circuit. The short-circuit output current is the current limit set by the R_{CL} resistor and is monitored cycle by cycle. When the overcurrent condition is removed, operation resumes in soft start mode.

MOSFET DRIVERS

The DH pin drives the high-side switch MOSFET. This is a boosted 5 V gate driver that is powered by a bootstrap capacitor circuit. This configuration allows the high-side, N-channel MOSFET gate to be driven above the input voltage, allowing full enhancement and a low voltage drop across the MOSFET. The bootstrap capacitor is connected from the SW pin to the BST pin. A bootstrap Schottky diode connected from the PV pin to the BST pin recharges the boost capacitor every time the SW node goes low. Use a bootstrap capacitor value greater than 100× the high-side MOSFET input capacitance.

In practice, the switch node can run up to 24 V of input voltage, and the boost nodes can operate more than 5 V above this to allow full gate drive. The IN pin can be run from 3 V to 20 V.

The switching cycle is initiated by the internal clock signal. The high-side MOSFET is turned on by the DH driver, and the SW node goes high, pulling up on the inductor. When the internally generated ramp signal crosses the COMP pin voltage, the switch MOSFET is turned off and the low-side synchronous rectifier MOSFET is turned on by the DL driver. Active break-before-make circuitry as well as a supplemental fixed dead time are used to prevent cross-conduction in the switches.

The DL pin provides the gate drive for the low-side MOSFET synchronous rectifier. Internal circuitry monitors the external MOSFETs to ensure break-before-make switching to prevent cross-conduction. An active dead-time reduction circuit reduces the break-before-make time of the switch to limit the losses due to current flowing through the synchronous rectifier body diode.

The PV pin provides power to the low-side drivers. It is limited to 5.5 V maximum input and must have a local decoupling capacitor to PGND.

The synchronous rectifier is turned on for a minimum time of about 200 ns on every switching cycle in order to sense the current. This minimum off time plus the nonoverlap dead time puts a limit on the maximum high-side switch duty cycle based on the selected switching frequency. Typically, this maximum duty cycle is about 90% at 300 kHz switching. At 1.2 MHz switching, it reduces to about 70% maximum duty cycle.

SETTING THE OUTPUT VOLTAGE

The output voltage is set using a resistive voltage divider from the output to FB. The voltage divider splits the output voltage to the 0.6 V FB regulation voltage to set the regulation output voltage. The output voltage can be set to as low as 0.6 V and as high as 85% of the power input voltage.

SWITCHING FREQUENCY CONTROL AND SYNCHRONIZATION

The ADP1828 has a logic controlled frequency select input, FREQ, which sets the switching frequency to 300 kHz or 600 kHz. Drive FREQ low at 300 kHz and high at 600 kHz. The frequency can also be set to between 300 kHz and 600 kHz by connecting a resistor between FREQ and GND. A 24.9 kΩ sets the frequency to 600 kHz, 35.7 kΩ to 450 kHz, and 57.6 kΩ to 300 kHz. Figure 34 shows f_{OSC} as a function of R_{FREQ}.

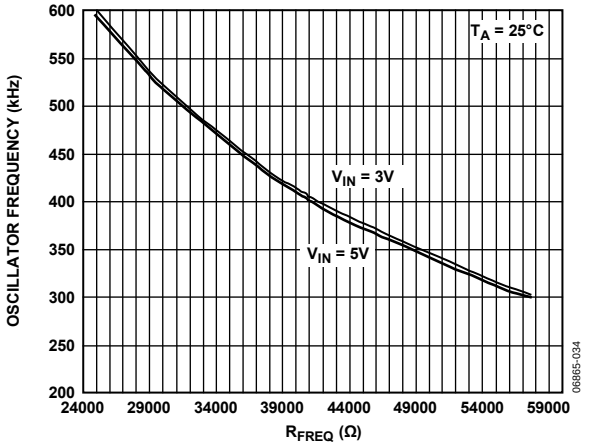


Figure 34. f_{OSC} vs. R_{FREQ}

The SYNC input is used to synchronize the converter switching frequency to an external signal. This allows multiple ADP1828 converters to be operated at the same frequency to prevent frequency beating or other interactions. The ADP1828 has a clock output (CLKOUT), which can be used for synchronizing the ADP1829 and other ADP1828 controllers, thus eliminating the need for an external clock source. Pulling CLKSET low sets the frequency at CLKOUT to 1× the internal oscillator frequency, f_{OSC}, and is 180° out of phase with f_{OSC}.

The 1× output is suitable for synchronizing other ADP1828s. Setting CLKSET high (connect to VREG) sets the frequency to 2× f_{OSC} and is in phase with f_{OSC}. The 2× output is suitable for synchronizing the dual channel ADP1829 controller (see Table 4).

Table 4. CLKOUT Truth Table[1]

EN	CLKSET	SYNC	CLKOUT	Comment
H	L	H/L	1× f_{OSC}	180° out of phase with f_{OSC}
H	H	H/L	2× f_{OSC}	In phase with f_{OSC}
H	X	Clock in	Clock	CLKOUT in-sync with clock in
L	X	X	L	CLKOUT is low

[1] X: don't care, H: Logic high, L: Logic low.

To synchronize the ADP1828 switching frequency to an external signal, drive the SYNC input with an external clock or with the CLKOUT signal from another ADP1828. The ADP1828 can be synchronized to between 1× and 2× the internal oscillator frequency. If f_{OSC} is set by R_{FREQ}, then the synchronization frequency range is from f_{OSC} up to 600 kHz. Driving SYNC faster than recommended for the FREQ setting results in a small ramp signal, which can affect the signal-to-noise ratio and the modulator gain and stability.

When an external clock is detected at the first SYNC edge, the internal oscillator is reset and the clock control shifts to SYNC. The SYNC edges then trigger subsequent clocking of the PWM outputs. The high-side MOSFET turn-on follows the rising edge of the sync input by approximately 320 ns (see Figure 35 for an illustration). If the external SYNC signal disappears during operation, the ADP1828 reverts to its internal oscillator and experiences a delay of no more than a single cycle of the internal oscillator.

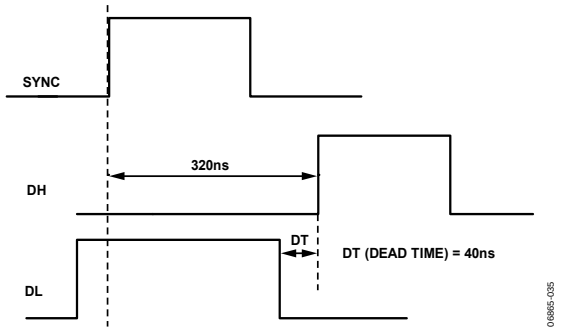


Figure 35. Synchronization

COMPENSATION

The control loop is compensated by an external series RC network from COMP to FB and sometimes requires a series RC in parallel with the top voltage divider resistor. COMP is the output of the internal error amplifier.

The internal error amplifier compares the voltage at FB to the internal 0.6 V reference voltage. The difference between the FB voltage and the 0.6 V reference voltage is amplified by the open-loop voltage 1000 volt-to-volt gain of the error amplifier. To optimize the ADP1828 for stability and transient response for a given set of external components and input/output voltage conditions, choose the compensation components carefully. For more information on choosing the compensation components, see the Compensating the Voltage Mode Buck Regulator section.

POWER-GOOD INDICATOR

The ADP1828 features an open-drain power-good output (PGOOD) that sinks current when the output voltage drops 8.3% below or rises 25% above the nominal regulation voltage. Two comparators measure the voltage at FB to set these thresholds. The PGOOD comparator directly monitors FB, and the threshold is fixed at 0.55 V for undervoltage and 0.75 V for overvoltage. The PGOOD output also sinks current if an overtemperature or input undervoltage condition is detected and is operational with power-input voltage as low as 1.0 V.

Use this output as a logical power-good signal by connecting a pull-up resistor from PGOOD to an appropriate supply voltage.

THERMAL SHUTDOWN

In most applications, the ADP1828 controller itself does not generate a significant amount of heat under normal conditions, even when driving relatively large MOSFETs. However, the surrounding power components or other circuits on the same PCB can heat up the PCB to an unsafe operating temperature. A thermal shutdown protection circuit on the ADP1828 shuts off the LDO and the controllers if the die temperature exceeds approximately 145°C, but this is a gross fault protection only and must not be depended on for system reliability.

SHUTDOWN CONTROL

The ADP1828 dc-to-dc converter features a low power shutdown mode that reduces the quiescent supply current to 20 μA, or 40 μA when IN is tied to VREG. To shut down the ADP1828, drive EN low. To turn it on, drive EN high or tristate EN. For automatic startup, connect EN to IN.

TRACKING

The ADP1828 features a tracking input, TRK that makes the output voltage track another voltage, that is, the master voltage. This feature is especially useful in core and input/output voltage sequencing applications where the output of the ADP1828 can be set to track and not exceed another voltage.

The internal error amplifier includes three positive inputs: the internal 0.6 V reference voltage, and the SS and TRK pins. The error amplifier regulates the FB pin to the lowest of the three inputs. To track a supply voltage, tie the TRK pin to a resistor divider from the voltage to be tracked. If the TRK function is not used, tie the TRK pin to VREG.

APPLICATION INFORMATION

SELECTING THE INPUT CAPACITOR

The input current to a buck converter is a pulse waveform. It is zero when the high-side switch is off and approximately equal to the load current when it is on. The input capacitor carries the input ripple current, allowing the input power source to supply only the dc current. The input capacitor needs sufficient ripple current rating to handle the input ripple as well as an ESR that is low enough to mitigate input voltage ripple. For the usual current ranges for these converters, it is good practice to use two parallel capacitors placed close to the drains of the high-side switch MOSFETs (one bulk capacitor of sufficiently high current rating as calculated in Equation 2 along with a 10 µF ceramic capacitor).

Select an input bulk capacitor based on its ripple current rating. First, determine the duty cycle of the output with the larger load current:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

The input capacitor ripple current is approximately

$$I_{RIPPLE} \approx I_L \sqrt{D(1-D)} \quad (2)$$

where:
I_L is the maximum inductor or load current.
D is the duty cycle.

OUTPUT LC FILTER

The output LC filter smoothes the switched voltage at SW, making the dc output voltage. Choose the output LC filter to achieve the desired output ripple voltage. Because the output LC filter is part of the regulator negative-feedback control loop, the choice of the output LC filter components affects the regulation control loop stability.

Choose an inductor value such that the inductor ripple current is approximately 1/3 of the maximum dc output load current. Using a larger value inductor results in a physical size larger than required and using a smaller value results in increased losses in the inductor and/or MOSFET switches.

Choose the inductor value by the following equation:

$$L = \frac{1}{f_{SW} \times \Delta I_L} V_{OUT} \left[1 - \frac{V_{OUT}}{V_{IN}} \right] \quad (3)$$

where:
L is the inductor value.
f_{SW} is the switching frequency.
V_{OUT} is the output voltage.
V_{IN} is the input voltage.
ΔI_L is the inductor ripple current, typically 1/3 of the maximum dc load current.

Choose the output bulk capacitor to set the desired output voltage ripple. The impedance of the output capacitor at the switching frequency multiplied by the ripple current gives the output voltage ripple. The impedance is made up of the capacitive impedance plus the nonideal parasitic characteristics, including the equivalent series resistance (ESR) and the equivalent series inductance (ESL). The output voltage ripple can be approximated with:

$$\Delta V_{OUT} = \Delta I_L \sqrt{ESR^2 + \left(\frac{1}{8 f_{SW} C_{OUT}} \right)^2 + (4 f_{SW} ESL)^2} \quad (4)$$

where:
ΔV_{OUT} is the output ripple voltage.
ΔI_L is the inductor ripple current.
ESR is the equivalent series resistance of the output capacitor (or the parallel combination of ESR of all output capacitors).
ESL is the equivalent series inductance of the output capacitor (or the parallel combination of ESL of all capacitors).

Note that the factors of 8 and 4 in Equation 4 would normally be 2π for sinusoidal waveforms, but the ripple current waveform in this application is triangular. Parallel combinations of different types of capacitors, for example, a large aluminum electrolytic in parallel with MLCCs, can give different results.

Usually the impedance is dominated by ESR at the switching frequency, as stated in the maximum ESR rating on the capacitor data sheet, so this equation reduces to

$$\Delta V_{OUT} \cong \Delta I_L \, ESR \quad (5)$$

Electrolytic capacitors have significant ESL also, on the order of 5 nH to 20 nH, depending on type, size, and geometry, and PCB traces contribute some ESR and ESL as well. However, using the maximum ESR rating from the capacitor data sheet usually provides some margin such that measuring the ESL is not usually required.

In the case of output capacitors, the impedance of the ESR and ESL at the switching frequency are small, for instance, where the effective output capacitor is a bank of parallel MLCC capacitors, the capacitive impedance dominates and the ripple equation reduces to

$$\Delta V_{OUT} \cong \frac{\Delta I_L}{8 C_{OUT} f_{SW}} \quad (6)$$

Make sure that the ripple current rating of the output capacitors is greater than the maximum inductor ripple current.

During a load step transient on the output, the output capacitor supplies the load until the control loop has a chance to ramp the inductor current. This initial output voltage deviation, due to a change in load, is dependent on the output capacitor characteristics. Again, usually the capacitor ESR dominates this response, and the ΔV_{OUT} in Equation 6 can be used with the load step current value for ΔI_L.

SELECTING THE MOSFETS

The choice of MOSFET directly affects the dc-to-dc converter performance. The MOSFET must have low on resistance to reduce I^2R losses and low gate charge to reduce transition losses. In addition, the MOSFET must have low thermal resistance to ensure that the power dissipated in the MOSFET does not result in excessive MOSFET die temperature.

The high-side MOSFET carries the load current during on-time and usually carries most of the transition losses of the converter. Typically, the lower the MOSFET's on resistance, the higher the gate charge and vice versa. Therefore, it is important to choose a high-side MOSFET that balances the two losses. The conduction loss of the high-side MOSFET is determined by the equation

$$P_C \cong (I_{LOAD})^2 R_{DSON}\left(\frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

where:
P_C is the conduction power loss.
R_{DSON} is the MOSFET on resistance.

The gate charging loss is approximated by the equation

$$P_G \cong V_{PV} Q_G f_{SW} \quad (8)$$

where:
P_G is the gate charging loss power.
V_{PV} is the gate driver supply voltage.
Q_G is the MOSFET total gate charge.
f_{SW} is the converter switching frequency.

The high-side MOSFET transition loss is approximated by the equation

$$P_T = \frac{V_{IN} I_{LOAD} (t_R + t_F) f_{SW}}{2} \quad (9)$$

where:
P_T is the high-side MOSFET switching loss power.
t_R is the MOSFET rise time.
t_F is the MOSFET fall time.

The total power dissipation of the high-side MOSFET is the sum of all the previous losses, or

$$P_{HS} \cong P_C + P_G + P_T \quad (10)$$

where P_{HS} is the total high-side MOSFET power loss.

The conduction losses can need an adjustment to account for the MOSFET R_{DSON} variation with temperature. Note that MOSFET R_{DSON} increases with increasing temperature. The MOSFET data sheet must list the thermal resistance of the package, θ_{JA}, along with a normalized curve of the temperature coefficient of the R_{DSON}. For the power dissipation estimated in Equation 10, calculate the MOSFET junction temperature rise over the ambient temperature of interest:

$$T_J = T_A + \theta_{JA} P_D \quad (11)$$

Then, calculate the new R_{DSON} from the temperature coefficient curve and the R_{DSON} specification at 25°C. An alternate method to calculate the MOSFET R_{DSON} at a second temperature, T_J, is

$$R_{DSON} \text{ at } T_J = R_{DSON} \text{ at } 25°C\ (1 + T_C(T_J - 25°C)) \quad (12)$$

where T_C is the temperature coefficient of the MOSFET's R_{DSON}, and its typical value is 0.004/°C.

Then the conduction losses can be recalculated and the procedure iterated until the junction temperature calculations are relatively consistent.

The synchronous rectifier, or low-side MOSFET, carries the inductor current when the high-side MOSFET is off. The low-side MOSFET transition loss is small and can be neglected in the calculation. For high input voltage and low output voltage, the low-side MOSFET carries the current most of the time. Therefore, to achieve high efficiency, it is critical to optimize the low-side MOSFET for low on resistance. In cases where the power loss exceeds the MOSFET rating or lower resistance is required than is available in a single MOSFET, connect multiple low-side MOSFETs in parallel. The equation for low-side MOSFET power loss is

$$P_{LS} \cong (I_{LOAD})^2 R_{DSON}\left[1 - \frac{V_{OUT}}{V_{IN}}\right] \quad (13)$$

where:
P_{LS} is the total low-side MOSFET power loss.
R_{DSON} is the total on resistance of the low-side MOSFET(s).

Check the gate charge losses of the synchronous rectifier using Equation 8 to be sure it is reasonable. If multiple low-side MOSFETs are used in parallel, then use the parallel combination of the on resistances for determining RDSON to solve this equation.

SETTING THE CURRENT LIMIT

The current-limit comparator measures the voltage across the low-side MOSFET to determine the load current.

The current limit is set through the current-limit resistor, R_{CL}. The current sense pin, CSL, sources 50 µA through the external current-limit setting resistor, R_{CL}. This creates an offset voltage of R_{CL} multiplied by the 50 µA CSL current. When the drop across the low-side MOSFET R_{DSON} is equal to or greater than this offset voltage, the ADP1828 flags a current-limit event.

Because the CSL current and the MOSFET R_{DSON} vary over process and temperature, the minimum current limit must be set to ensure that the system can handle the maximum desired load current. To do this, use the peak current in the inductor, which is the desired current-limit level plus the ripple current, the maximum R_{DSON} of the MOSFET at its highest expected temperature, and the minimum CSL current:

$$R_{CL} = \frac{I_{LPK} R_{DSON(MAX)} - 38\text{ mV}}{42\,\mu\text{A}} \quad (14)$$

where:
I_{LPK} is the peak inductor current.
−38 mV is the CSL threshold voltage.

Because the buck converters are usually running a fairly high current, PCB layout and component placement can affect the current-limit setting. An iteration of the R_{CL} value can be required for a particular board layout and MOSFET selection. If alternate MOSFETs are substituted at some point in production, these resistor values can need an iteration.

ACCURATE CURRENT-LIMIT SENSING

The R_{DSON} of the external low-side MOSFET can vary by more than 50% over the temperature range. Accurate current-limit sensing can be achieved by adding a current sense resistor from the source of the low-side MOSFET to PGND. Make sure that the power rating of the current sense resistor is adequate for the application. Apply Equation 14 to calculate R_{CL} and replace $R_{DSON(MAX)}$ with R_{SENSE}.

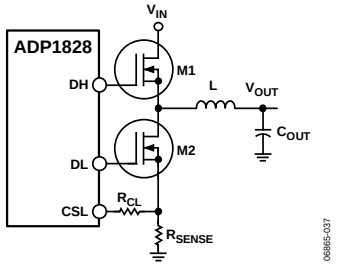


Figure 36. Accurate Current-Limit Sensing

FEEDBACK VOLTAGE DIVIDER

The output regulation voltage is set through the feedback voltage divider. The output voltage is divided down through the voltage divider and drives the FB feedback input. The regulation threshold at FB is 0.6 V. The maximum input bias current into FB is 100 nA. For a 0.15% degradation in regulation voltage and with 100 nA bias current, the low-side resistor, R_{BOT}, needs to be less than 9 kΩ, which results in 67 µA of divider current. For R_{BOT}, use a 1 kΩ to 10 kΩ resistor. A larger value resistor can be used, but results in a reduction in output voltage accuracy due to the input bias current at the FB pin, while lower values cause increased quiescent current consumption. Choose R_{TOP} to set the output voltage by using the following equation:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right) \quad (15)$$

where:
R_{TOP} is the high-side voltage divider resistance.
R_{BOT} is the low-side voltage divider resistance.
V_{OUT} is the regulated output voltage.
V_{FB} is the feedback regulation threshold, 0.6 V.

COMPENSATING THE VOLTAGE MODE BUCK REGULATOR

Assuming the LC filter design is complete, the feedback control system can then be compensated. Good compensation is critical to proper operation of the regulator. Calculate the quantities in Equation 16 through Equation 44 to derive the compensation values. The goal is to guarantee that the voltage gain of the buck converter crosses unity at a slope that provides adequate phase margin for stable operation. Additionally, at frequencies above the crossover frequency (f_{CO}), guaranteeing sufficient gain margin and attenuation of switching noise are important secondary goals. For initial practical designs, a good choice for the crossover frequency is one tenth of the switching frequency, calculate first

$$f_{CO} = \frac{f_{SW}}{10} \quad (16)$$

This gives sufficient frequency range to design a compensation scheme that attenuates switching artifacts, while also giving sufficient control loop bandwidth to provide a good transient response.

The output LC filter is a resonant network that inflicts two poles upon the response at a frequency (f_{LC}). Next, calculate

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \quad (17)$$

Generally speaking, the LC corner frequency is about two orders of magnitude below the switching frequency, and therefore about one order of magnitude below crossover. To achieve sufficient phase margin at crossover to guarantee stability, the design must compensate for the two poles at the LC corner frequency with two zeros to boost the system phase prior to crossover. The two zeros require an additional pole or two above the crossover frequency to guarantee adequate gain margin and attenuation of switching noise at high frequencies.

Depending on component selection, one zero might already be generated by the ESR of the output capacitor. Calculate this zero corner frequency, f_{ESR}, as

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}} \quad (18)$$

Figure 37 shows a typical Bode plot of the LC filter by itself.

The gain of the LC filter at crossover can be linearly approximated from Figure 37 as

$$A_{FILTER} = A_{LC} + A_{ESR}$$

$$A_{FILTER} = -40\text{ dB} \times \log\left(\frac{f_{ESR}}{f_{LC}}\right) - 20\text{ dB} \times \log\left(\frac{f_{CO}}{f_{ESR}}\right) \quad (19)$$

If $f_{ESR} \approx f_{CO}$, then add another 3 dB to account for the local difference between the exact solution and the linear approximation in Equation 19.

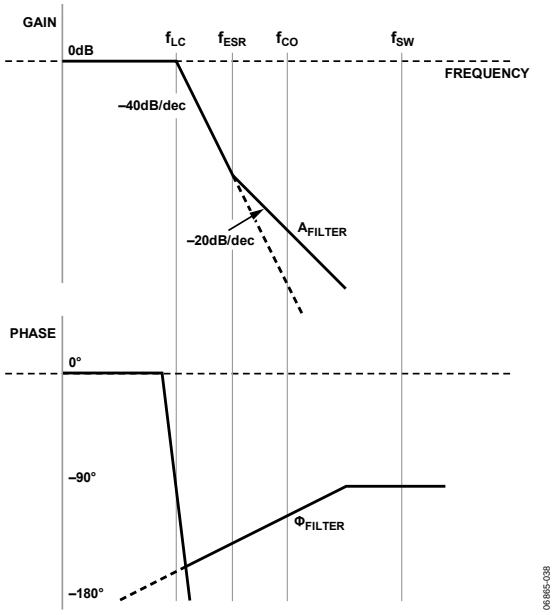


Figure 37. LC Filter Bode Plot

To compensate the control loop, the gain of the system must be brought back up so that it is 0 dB at the desired crossover frequency. Some gain is provided by the PWM modulation itself.

$$A_{MOD} = 20 \log\left(\frac{V_{IN}}{V_{RAMP}}\right) \quad (20)$$

For systems using the internal oscillator, this becomes

$$A_{MOD} = 20 \log\left(\frac{V_{IN}}{1.0\text{ V}}\right) \quad (21)$$

Note that if the converter is being synchronized, the ramp voltage, V_{RAMP}, is lower than 1.0 V by the percentage of frequency increase over the nominal setting of the FREQ pin:

$$V_{RAMP} = 1.0\text{ V}\left(\frac{f_{FREQ}}{f_{SYNC}}\right) \quad (22)$$

For example, if FREQ is grounded or connected to VREG, then f_{FREQ} is 300 kHz or 600 kHz, respectively. If the frequency is set by a resistor, then f_{FREQ} is 300 kHz and f_{SYNC} is the frequency set by the resistor. V_{RAMP} is greater than 1.0 V if f_{SYNC} is less than f_{FREQ}. The rest of the system gain needs to reach 0 dB at crossover. The total gain of the system, therefore, is given by

$$A_T = A_{MOD} + A_{FILTER} + A_{COMP} \quad (23)$$

where:

A_{MOD} is the gain of the PWM modulator.
A_{FILTER} is the gain of the LC filter including the effects of the ESR zero.
A_{COMP} is the gain of the compensated error amplifier.

Additionally, the phase of the system must be brought back up to guarantee stability. Note from the Bode plot of the filter that the LC contributes −180° of phase shift (see Figure 37). Because the error amplifier is an integrator at low frequency, it contributes an initial −90°. Therefore, before adding compensation or accounting for the ESR zero, the system is already down −270°. To avoid loop inversion at crossover, or −180° phase shift, a good initial practical design is to require a phase margin of 60°, which is therefore an overall phase loss of −120° from the initial low frequency dc phase. The goal of the compensation is to boost the phase back up from −270° to −120° at crossover.

Two common compensation schemes are used, which are sometimes referred to as Type II or Type III compensation, depending on whether the compensation design includes two or three poles (see the Type II Compensator and Type III Compensator sections). Dominant-pole compensation, or single-pole compensation, is referred to as Type I compensation, but it is not very useful for dealing successfully with switching regulators.

If the zero produced by the ESR of the output capacitor provides sufficient phase boost at crossover, Type II compensation is adequate. If the phase boost produced by the ESR of the output capacitor is not sufficient, another zero is added to the compensation network, and thus Type III is used.

In Figure 38, the location of the ESR zero corner frequency gives a significantly different net phase at the crossover frequency.

Use the following guidelines for selecting between Type II and Type III compensators:

If $f_{ESRZ} \le \frac{f_{CO}}{2}$, use Type II compensation.

If $f_{ESRZ} > \frac{f_{CO}}{2}$, use Type III compensation.

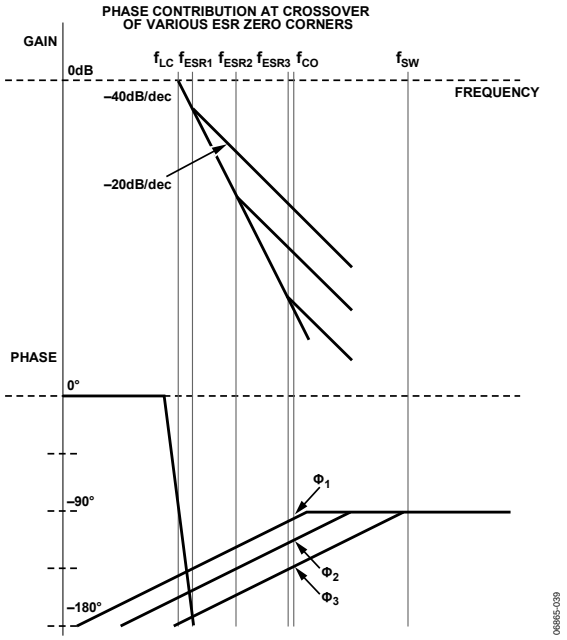


Figure 38. LC Filter Bode Plot

The following equations are used for the calculation of the compensation components as shown in Figure 39 and Figure 40:

$$f_{Z1} = \frac{1}{2\pi R_Z C_I} \quad (24)$$

$$f_{Z2} = \frac{1}{2\pi C_{FF}(R_{TOP} + R_{FF})} \quad (25)$$

$$f_{P1} = \frac{1}{2\pi R_Z \dfrac{C_I C_{HF}}{C_I + C_{HF}}} \quad (26)$$

$$f_{P2} = \frac{1}{2\pi R_{FF} C_{FF}} \quad (27)$$

where:
f_{Z1} is the zero produced in the Type II compensation.
f_{Z2} is the zero produced in the Type III compensation.
f_{P1} is the pole produced in the Type II compensation.
f_{P2} in the pole produced in the Type III compensation.

Type II Compensator

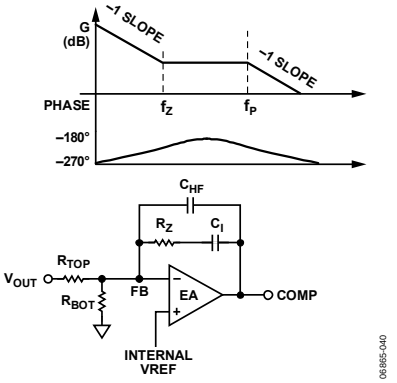


Figure 39. Type II Compensation

If the output capacitor ESR zero frequency is sufficiently low (≤½ of the crossover frequency), use the ESR to stabilize the regulator. In this case, use the circuit shown in Figure 39. Calculate the compensation resistor, R_Z, with the following equation:

$$R_Z = \frac{R_{TOP} V_{RAMP} f_{ESR} f_{CO}}{V_{IN} {f_{LC}}^2} \quad (28)$$

where:
f_{CO} is chosen to be 1/10 of f_{SW}.
V_{RAMP} is 1.0 V.

Next, choose the compensation capacitor to set the compensation zero, f_{Z1}, to the lesser of ¼ of the crossover frequency or ½ of the LC resonant frequency

$$f_{Z1} = \frac{f_{CO}}{4} = \frac{f_{SW}}{40} = \frac{1}{2\pi R_Z C_I} \quad (29)$$

or

$$f_{Z1} = \frac{f_{LC}}{2} = \frac{1}{2\pi R_Z C_I} \quad (30)$$

Solving for C_I in Equation 29 yields

$$C_I = \frac{20}{\pi R_Z f_{SW}} \quad (31)$$

Solving for C_I in Equation 30 yields

$$C_I = \frac{1}{\pi R_Z f_{LC}} \quad (32)$$

Use the larger value of C_I from Equation 31 or Equation 32. Because of the finite output current drive of the error amplifier, C_I needs to be less than 10 nF. If it is larger than 10 nF, choose a larger R_{TOP} and recalculate R_Z and C_I until C_I is less than 10 nF.

Next, choose the high frequency pole, f_{P1}, to be ½ of f_{SW}.

$$f_{P1} = \frac{1}{2} f_{SW} \tag{33}$$

Because $C_{HF} << C_I$, Equation 26 is simplified to

$$f_{P1} = \frac{1}{2\pi R_Z C_{HF}} \tag{34}$$

Combine Equation 33 and Equation 34, and solve for C_{HF},

$$C_{HF} = \frac{1}{\pi f_{SW} R_Z} \tag{35}$$

Type III Compensator

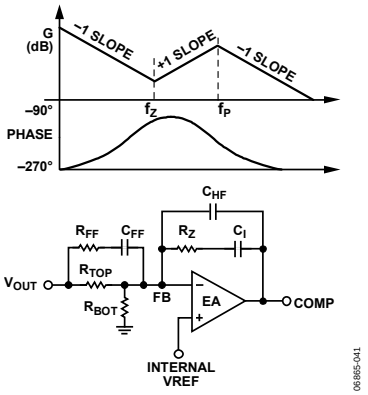


Figure 40. Type III Compensation

If the output capacitor ESR zero frequency is greater than ½ of the crossover frequency, use the Type III compensator as shown in Figure 40. Set the poles and zeros as follows:

$$f_{P1} = f_{P2} = \frac{1}{2} f_{SW} \tag{36}$$

$$f_{Z1} = f_{Z2} = \frac{f_{CO}}{4} = \frac{f_{SW}}{40} = \frac{1}{2\pi R_Z C_I} \tag{37}$$

or

$$f_{Z1} = f_{Z2} = \frac{f_{LC}}{2} = \frac{1}{2\pi R_Z C_I} \tag{38}$$

Use the lower zero frequency from Equation 37 or Equation 38. Calculate the compensator resistor, R_Z

$$R_Z = \frac{R_{TOP} V_{RAMP} f_{Z1} f_{CO}}{V_{IN} {f_{LC}}^2} \tag{39}$$

Next, calculate C_I,

$$C_I = \frac{1}{2\pi R_Z f_{Z1}} \tag{40}$$

Because of the finite output current drive of the error amplifier, C_I needs to be less than 10 nF. If it is larger than 10 nF, choose a larger R_{TOP} and recalculate R_Z and C_I until C_I is less than 10 nF.

Because $C_{HF} << C_I$, combining Equation 26 and Equation 36 yields

$$C_{HF} = \frac{1}{\pi f_{SW} R_Z} \tag{41}$$

Next, calculate the feedforward capacitor C_{FF}. Assuming $R_{FF} << R_{TOP}$, then Equation 25 is simplified to

$$f_{Z2} = \frac{1}{2\pi C_{FF} R_{TOP}} \tag{42}$$

Solving C_{FF} in Equation 42 yields

$$C_{FF} = \frac{1}{2\pi R_{TOP} f_{Z2}} \tag{43}$$

where f_{Z2} is obtained from Equation 37 or Equation 38.

The feedforward resistor, R_{FF}, can be calculated by combining Equation 27 and Equation 36

$$R_{FF} = \frac{1}{\pi C_{FF} f_{SW}} \tag{44}$$

Check that the calculated component values are reasonable. For instance, capacitors smaller than about 10 pF must be avoided. In addition, the ADP1828 error amplifier has a finite output current drive, so R_Z values less than 3 kΩ and C_I values greater than 10 nF must be avoided. If necessary, recalculate the compensation network with a different starting value of R_{TOP}. If R_Z is too small or C_I is too big, start with a larger value of R_{TOP}. This compensation technique can yield a good working solution.

In general, aluminum electrolytic capacitors have high ESR, and Type II compensation is adequate. However, if several aluminum electrolytic capacitors are connected in parallel, and produce a low effective ESR, then Type III compensation is needed. In addition, ceramic capacitors have very low ESR (only a few milliohms) making Type III compensation a better choice. Type III compensation offers better performance than Type II in terms of more low frequency gain and more phase margin and less high frequency gain at the crossover frequency.

SOFT START

The ADP1828 uses an adjustable soft start to limit the output voltage ramp-up period, limiting the input inrush current. The soft start is selected by setting the capacitor, C_{SS}, from SS to GND. The ADP1828 charges C_{SS} to 0.8 V through an internal 90 kΩ resistor. The voltage on the soft start capacitor while it is charging is

$$V_{CSS} = 0.8\ \text{V}\left(1 - e^{\frac{t}{90\ \text{k}\Omega C_{SS}}}\right) \quad (45)$$

The soft start period ends when the voltage on the soft start pin reaches 0.6 V. Substituting 0.6 V for V_{SS} and solving for the soft start time t_{SS}:

$$0.6\ \text{V} = 0.8\ \text{V}\left(1 - e^{\frac{t}{90\ \text{k}\Omega C_{SS}}}\right) \quad (46)$$

$$t_{SS} = 1.386\,RC_{SS} \quad (47)$$

Because R = 90 kΩ:

$$C_{SS} = t_{SS} \times 8\,\mu\text{F/ sec} \quad (48)$$

where t_{SS} is the desired soft start time in seconds.

SWITCHING NOISE AND OVERSHOOT REDUCTION

In any high speed step-down regulator, high frequency noise (generally in the range of 50 MHz to 100 MHz) and voltage overshoot are always present at the gate, the switch node (SW), and the drains of the external MOSFETs. The high frequency noise and overshoot are caused by the parasitic capacitance, C_{gd}, of the external MOSFET and the parasitic inductance of the gate trace and the packages of the MOSFETs. When the high current is switched, electromagnetic interference (EMI) is generated, which can affect the operation of the surrounding circuits. To reduce voltage ringing at the drain of the MOSFET, an RC snubber can be added between SW and PGND, as illustrated in Figure 41. In most applications, R_{SNUB} is about 2 Ω, and C_{SNUB} about 1.2 nF. R_{SNUB} and C_{SNUB} can be calculated using the following equations:

$$R_{SNUB} = \frac{1}{2\pi f C_{OSS}} \quad (49)$$

$$C_{SNUB} = C_{OSS} \quad (50)$$

where:
f is the high frequency ringing measured at the SW node.
C_{OSS} is the total output capacitance of the top-side and low-side MOSFETs, given in the MOSFET data sheet.

The size of the RC snubber components need to be chosen correctly to handle the power dissipated in R_{SNUB} is:

$$P_{SNUB} = V_{IN}{}^2 C_{SNUB} f_{SW}$$

In most applications, a size 0805 component is sufficient. The use of the RC snubber reduces the overall efficiency, generally by an amount in the range of 0.1% to 0.5%. However, the RC snubber cannot reduce the voltage overshoot. A resistor, shown as R_{RISE} in Figure 41, at the BST pin can help to reduce overshoot and is generally between 1 Ω and 5 Ω.

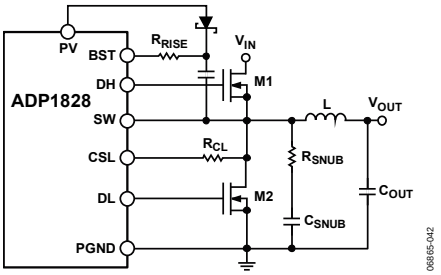


Figure 41. Application Circuit with a Snubber

VOLTAGE TRACKING

The ADP1828 includes a feature that tracks a master voltage. This feature is especially important when multiple ADP1828s (or other controllers such as the ADP1829) are powering separate power supply voltages, such as the core and input/output voltages of a DSP or microcontroller. In these cases, improper sequencing can cause damage to the load.

The ADP1828 tracking input is an additional positive input to the error amplifier. The feedback voltage is regulated to the lower of the 0.6 V reference, the SS voltage, or the voltage at TRK, so a lower voltage on TRK limits the output voltage. This feature allows implementation of two different types of tracking: coincident tracking, where the output voltage is the same as the master voltage until the master voltage reaches regulation, or ratiometric tracking, where the output voltage is limited to a fraction of the master voltage.

In all tracking configurations, the final value of the master voltage must be higher than the slave voltage.

Note that the soft start time setting of the master voltage must be longer than the soft start of the slave voltage. This forces the rise time of the master voltage to be imposed on the slave voltage. If the soft start setting of the slave voltage is longer, the slave comes up more slowly and the tracking relationship is not seen at the output. The slave channel must still have a soft start capacitor to give a small but reasonable soft start time to protect the device in case of restart after a current-limit event.

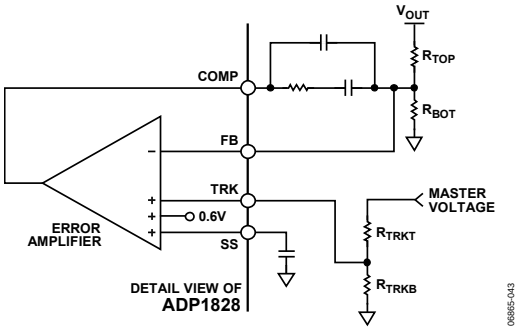


Figure 42. Voltage Tracking

COINCIDENT TRACKING

The most common application is coincident tracking, used in core vs. I/O voltage sequencing and similar applications. Coincident tracking limits the slave output voltage to be the same as the master voltage until it reaches regulation. Connect the slave TRK input to a resistor divider from the master voltage that is the same as the divider used on the slave FB pin. This forces the slave voltage to be the same as the master voltage.

For coincident tracking, use the following equation:

$$R_{TRKT} = R_{TOP} \text{ and } R_{TRKB} = R_{BOT}$$

where:

R_{TOP} and R_{BOT} are the values chosen in the Compensating the Voltage Mode Buck Regulator section.

See Figure 43 for an example of a coincident tracking circuit.

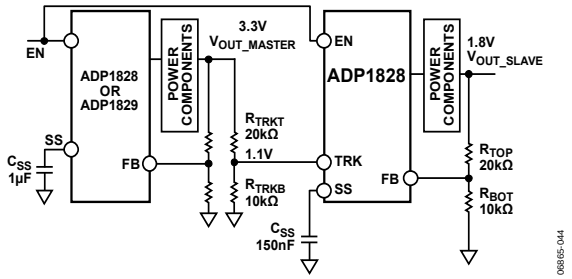


Figure 43. Example of a Coincident Tracking Circuit

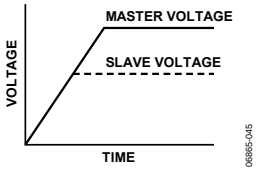


Figure 44. Coincident Tracking

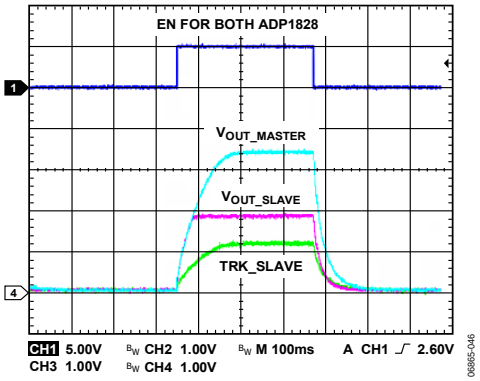


Figure 45. Coincident Tracking of Figure 43

As the master voltage rises, the slave voltage also rises in the same pattern. Eventually, the slave voltage reaches its regulation voltage, where the internal reference takes over the regulation while the TRK input continues to increase and thus removes itself from influencing the output voltage. To ensure that the output voltage accuracy is not compromised by the TRK pin being too close in voltage to the 0.6 V reference, make sure that the final value of the master voltage is greater than the slave regulation voltage by at least 10%, or 60 mV as seen at the FB node (the higher, the better). A difference of 60 mV between TRK and the 0.6 V reference produces about 3 mV of offset in the error amplifier, or 0.5%, at room temperature, while 100 mV between them produces only 0.6 mV or 0.1% offset. For accurate tracking, set the final voltage at TRK to less than or equal to 0.5 V. However, this condition would trip the PGOOD signal.

RATIOMETRIC TRACKING

Ratiometric tracking limits the output voltage to a fraction of the master voltage. For example, the termination voltage for DDR memories (VTT) is set to half the VDDQ voltage.

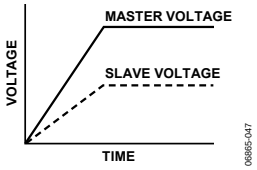


Figure 46. Ratiometric Tracking

For ratiometric tracking, the simplest configuration is to tie the TRK pin of the slave channel to the FB pin of the master channel. The advantage of this is having the fewest components, but the accuracy suffers as the TRK pin voltage becomes equal to the internal reference voltage and an offset is imposed on the error amplifier of about −18 mV at room temperature.

A more accurate solution is to provide a divider from the master voltage that sets the TRK pin voltage to be something lower than 0.6 V at regulation, for example, 0.5 V. The slave channel can be viewed as having a 0.5 V external reference supplied by the master voltage. Keep in mind that PGOOD is tripped when the TRK voltage is set to less than 0.55 V.

When this is complete, the FB divider for the slave voltage is designed as in the Compensating the Voltage Mode Buck Regulator section except to substitute the 0.5 V reference for the V_{FB} voltage. The ratio of the slave output voltage to the master voltage is a function of the two dividers:

$$\frac{V_{OUT}}{V_{MASTER}} = \frac{\left(1+\frac{R_{TOP}}{R_{BOT}}\right)}{\left(1+\frac{R_{TRKT}}{R_{TRKB}}\right)} \quad (51)$$

Figure 47 shows an example of ratiometric tracking circuit and Figure 48 shows its voltage tracking waveforms.

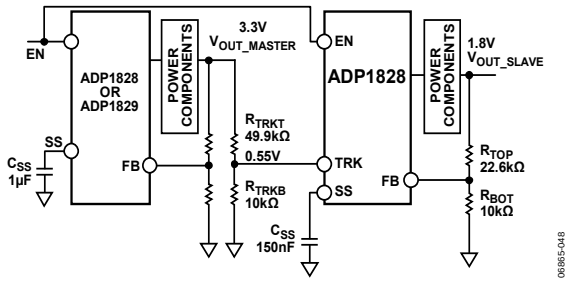


Figure 47. An Example of a Ratiometric Tracking Circuit

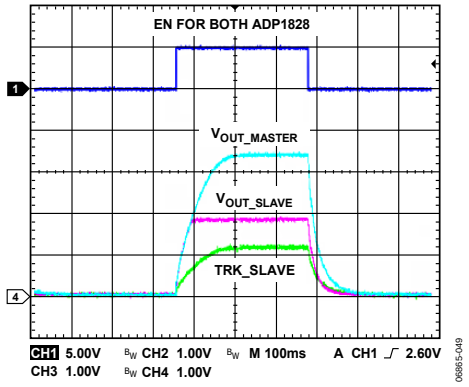


Figure 48. Ratiometric Tracking of Figure 47

Another option is to add another tap to the divider for the master voltage. Split the R_{BOT} resistor of the master voltage into two pieces, with the new tap at 0.5 V when the master voltage is in regulation. This saves one resistor, but be aware that Type III compensation on the master voltage causes the feedforward signal of the master voltage to appear at the TRK input of the slave channel.

Figure 49 shows an example of DDR memory termination application circuit, where the DDR memory termination voltage, VTT, is ½ of VDDQ. VTT can sink current during the off cycle of the ADP1828. The output waveform in Figure 50 shows that VTT changes by one-half of the output change in VDDQ.

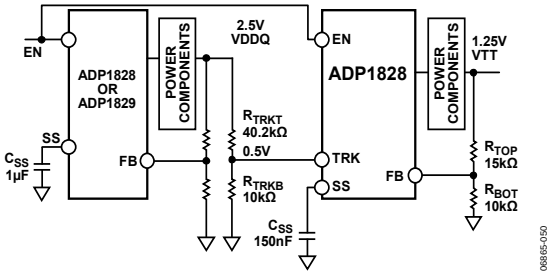


Figure 49. An Example of a DDR Termination Circuit

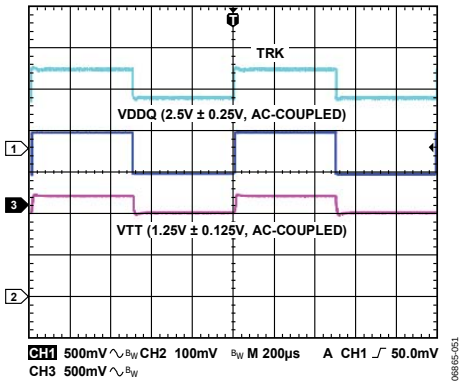


Figure 50. DDR Termination; Output Waveforms of Figure 49

In addition, by selecting the resistor values in the divider carefully, Equation 51 shows that the slave voltage output can be made to have a faster ramp rate than that of the master voltage by setting the TRK voltage at the slave larger than 0.6 V and R_{TRKB} greater than R_{TRKT}. Make sure that the master SS period is long enough (that is, use a sufficiently large SS capacitor) such that the input inrush current does not run into the current limit of the power supply during startup.

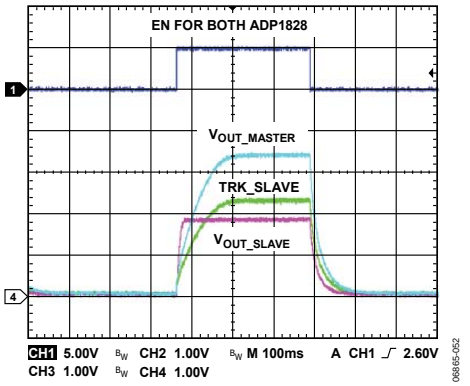


Figure 51. Ratiometric Tracking of Figure 47 with R_{TRKT} = 5 kΩ

THERMAL CONSIDERATIONS

The current required to drive the external MOSFETs comprises the vast majority of the power dissipation of the ADP1828. The on-chip LDO regulates down to 5 V, and this 5 V supplies the drivers. The full gate drive current passes through the LDO and is then dissipated in the gate drivers. The power dissipated in the gate drivers on the ADP1828 is

$$P_D = V_{IN} f_{SW} (Q_{DH} + Q_{DL}) \quad (52)$$

where:
V_{IN} is the voltage applied to IN.
f_{SW} is the switching frequency.
Q numbers are the total gate charge specifications from the selected MOSFET data sheets.

The power dissipation heats up the ADP1828. As the switching frequency, the input voltage, and the MOSFET size increase, the power dissipation on the ADP1828 increases. Care must be taken not to exceed the maximum junction temperature. To calculate the junction temperature from the ambient temperature and power dissipation, use the following formula:

$$T_J = T_A + P_D \theta_{JA} \quad (53)$$

The thermal resistance (θ_{JA}) of the package is 83°C/W depending on board layout, and the maximum specified junction temperature is 125°C, which means that at maximum ambient temperature of 85°C without airflow, the maximum dissipation allowed is about 1 W.

A thermal shutdown protection circuit on the ADP1828 shuts off the LDO and the controllers if the die temperature exceeds approximately 145°C, but this is a gross fault protection only and must not be depended on for system reliability.

PCB LAYOUT GUIDELINE

In any switching converter, there are some circuit paths that carry high dI/dt, which can create spikes and noise. Other circuit paths are sensitive to noise. While other circuits carry high dc current and can produce significant IR voltage drops. The key to proper PCB layout of a switching converter is to identify these critical paths and arrange the components and the copper area accordingly. When designing PCB layouts, be sure to keep high current loops small. In addition, keep compensation and feedback components away from the switch nodes and their associated components.

The following is a list of recommended layout practices for the synchronous buck controller arranged by decreasing order of importance:

- The current waveform in the top and bottom FETs is a pulse with very high dI/dt, so the path to, through, and from each individual FET must be as short as possible and the two paths must be commoned as much as possible. In designs that use a pair of D-Pak or a pair of SO-8 FETs on one side of the PCB, it is best to counter-rotate the two so that the switch node is on one side of the pair and the high-side drain can be bypassed to the low-side source with a suitable ceramic bypass capacitor, placed as close as possible to the FETs in order to minimize inductance around this loop through the FETs and capacitor. The recommended bypass ceramic capacitor values range from 1 µF to 22 µF depending upon the output current. This bypass capacitor is usually connected to a larger value bulk filter capacitor and must be grounded to the PGND plane.
- The negative terminals of GND, IN bypass, and a soft start capacitor (as well as the bottom end of the output feedback divider resistors) must be tied to an almost isolated small AGND plane. All of these connections must attach from their respective pins to the AGND plane that are as short as possible. No high current or high dI/dt signals are to be connected to this AGND plane. The AGND area must be connected through one wide trace to the negative terminal of the output filter capacitors.
- The PGND pin handles a high dI/dt gate drive current returning from the source of the low-side MOSFET. The voltage at this pin also establishes the 0 V reference for the overcurrent limit protection function and the CSL pin. A PGND plane must connect the PGND pin and the PV bypass capacitor, 1 µF, through a wide and direct path to the source of the low-side MOSFET. The placement of C_{IN} is critical for controlling ground bounce. The negative terminal of C_{IN} needs to be placed very close to the source of the low-side MOSFET.
- Avoid long traces or large copper areas at the FB and CSL pins, which are low signal level inputs that are sensitive to capacitive and inductive noise pickup. It is best to position any series resistors and capacitors as closely as possible to these pins. Avoid running these traces close and/or parallel to high dI/dt traces.
- The switch node is the noisiest place in the switcher circuit with large ac and dc voltages and currents. This node must be wide to keep resistive voltage drop down. But, to minimize the generation of capacitively coupled noise, the total area must be small. Place the FETs and inductor close together on a small copper plane in order to minimize series resistance and keep the copper area small.
- Gate drive traces (DH and DL) handle high dI/dt and tend to produce noise and ringing. They must be as short and direct as possible. If possible, avoid using feedthrough vias in the gate drive traces. If vias are needed, it is best to use two relatively large ones in parallel to reduce the peak current density and the current in each via. If the overall PCB layout is less than optimal, slowing down the gate drive slightly can be very helpful to reduce noise and ringing. It is occasionally helpful to place small value resistors (such as 5 Ω or10 Ω) in between the DH and DL pins and their respective MOSFET gates. These can be populated with 0 Ω resistors if resistance is not needed. Note that the added gate resistance increases the switching rise and fall times as well as switching power loss in the MOSFET.
- The negative terminal of the output filter capacitors must be tied closely to the source of the low-side FET. Doing this helps to minimize voltage differences between GND and PGND.
- All traces must be sized according to the current that is handled as well as their sensitivity in the circuit. Standard PCB layout guidelines mainly address the heating effects of a current in a copper conductor. While these are completely valid, they do not fully cover other concerns such as stray inductance or dc voltage drop. Any dc voltage differential in connections between ADP1828 GND and the converter power output ground can cause a significant output voltage error, as it affects converter output voltage according to the ratio with the 600 mV feedback reference. For example, a 6 mV offset between ground on the ADP1828 and the converter power output causes a 1% error in the converter output voltage.

To achieve an accurate output voltage, proper grounding of the AGND and PGND planes is needed. For light to medium loads, connecting the AGND plane to the PGND plane with a trace is adequate in obtaining good output accuracy (see Figure 52). If the PGND plane is large enough and under a light to medium load, the voltage drop across the PGND plane is negligible.

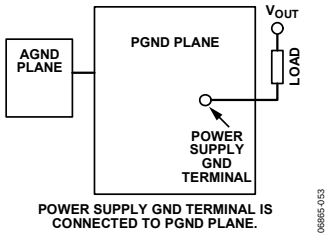


Figure 52. Grounding Technique for a Light to Medium Load

However, under a heavy load, such as at 20 A, the voltage drop across the PGND plane can be significant, thus affecting the accuracy of the output. The AGND plane would then have to be routed directly to the negative terminal of the load and the power supply, as illustrated in Figure 53. The power supply GND terminal and the load GND terminal must be placed as close as possible to each other to minimize the voltage drop across these two terminals, thus improving the output accuracy.

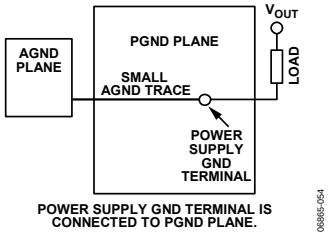


Figure 53. Proper Grounding Technique for a Heavy Load

RECOMMENDED COMPONENT MANUFACTURERS

Table 5.

Vendor	Components
AVX Corporation	Capacitors
Central Semiconductor Corp.	Diodes
Coilcraft, Inc.	Inductors
Diodes, Inc.	Diodes
International Rectifier	Diodes, MOSFETs
Murata Manufacturing Co., Ltd.	Capacitors, inductors
ON Semiconductor	Diodes, MOSFETs
Rubycon Corporation	Capacitors
Sanyo	Capacitors
Sumida Corporation	Inductors
Taiyo Yuden, Inc.	Capacitors, inductors
Toko America, Inc.	Inductors
United Chemi-Con, Inc.	Capacitors
Vishay Siliconix	Diodes, MOSFETs, resistors, and capacitors
Wurth Elektronic	Inductors

APPLICATION CIRCUITS

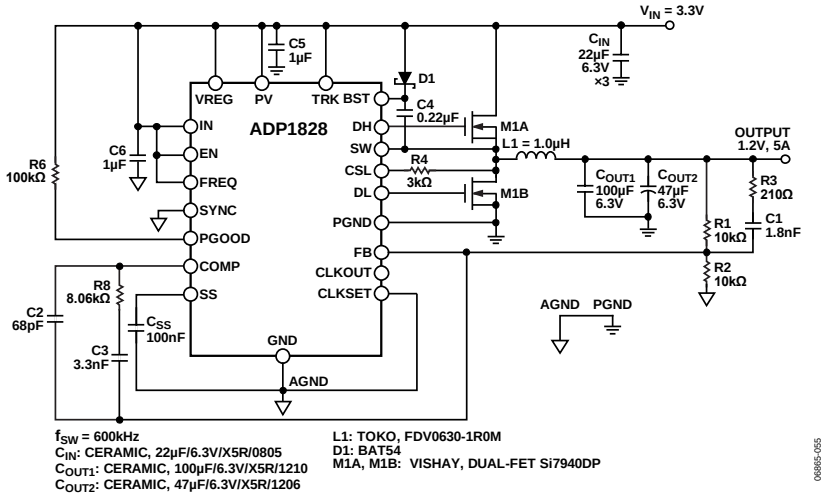


Figure 54. Application Circuit for V_{IN} = 3.3 V, All Ceramic Solution

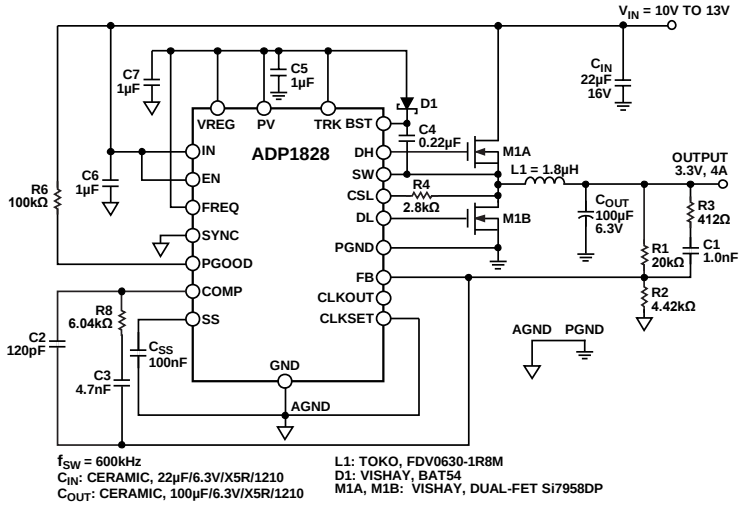


Figure 55. Application Circuit for V_{IN} = 12 V, All Ceramic Solution

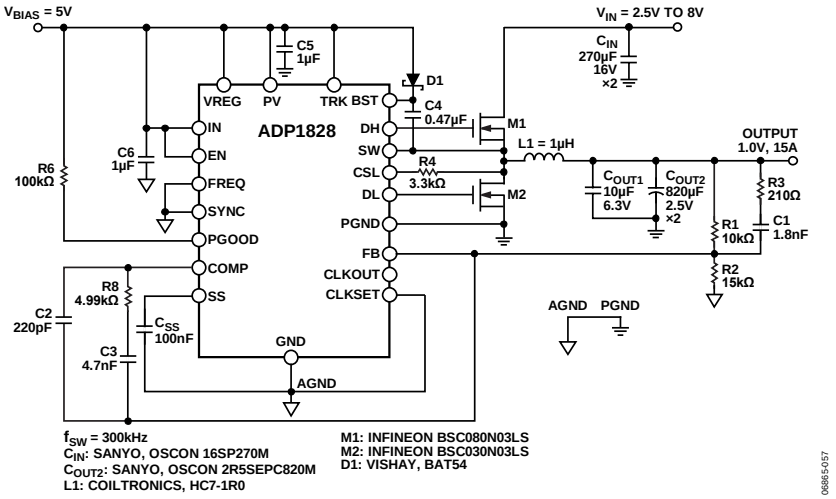


Figure 56. Application Circuit for V_{IN} = 2.5 V to 8 V

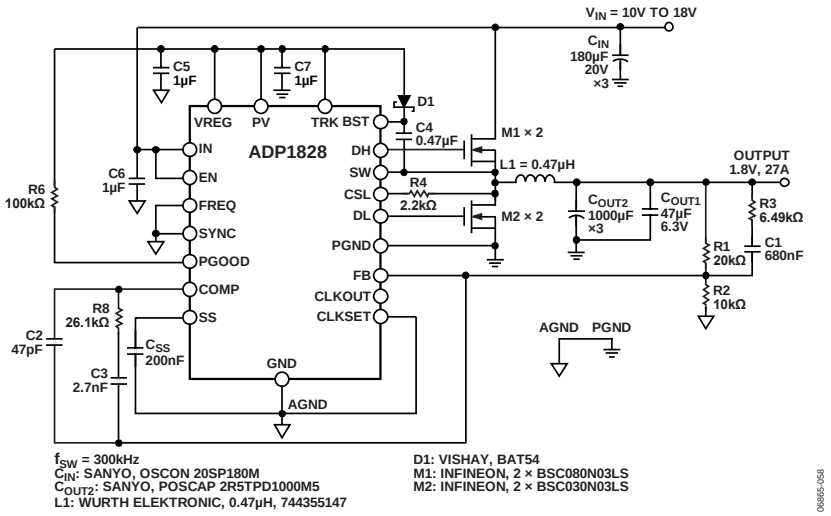
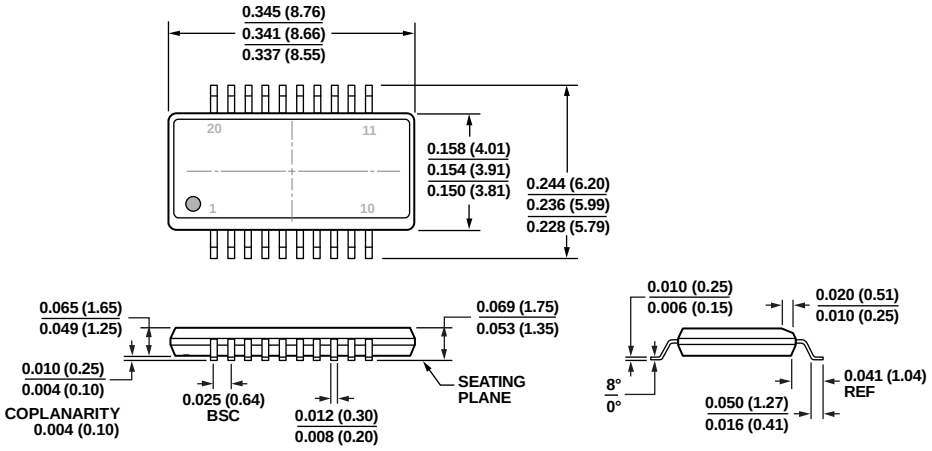


Figure 57. Application Circuit with 27 A Output

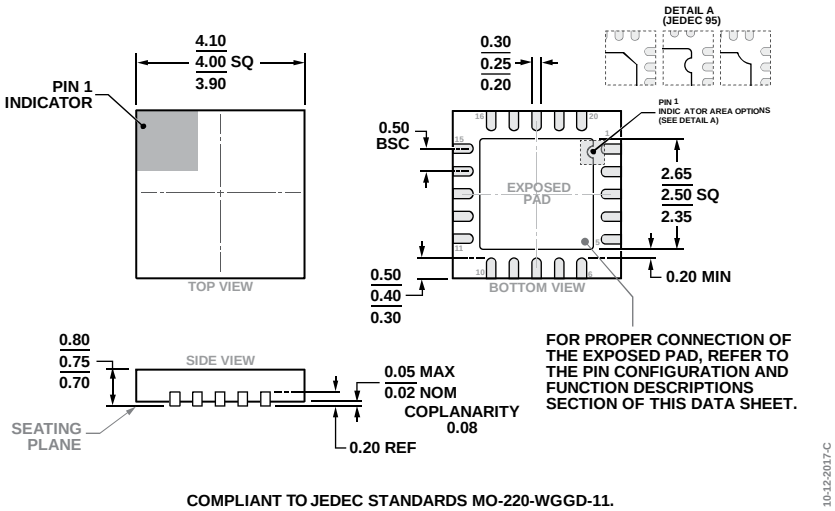
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AD
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

09-12-2014-A

Figure 58. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.

10-12-2017-C

Figure 59. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
ADP1828YRQZ-R7	−40°C to +85°C	20-Lead Shrink Small Outline Package [QSOP]	RQ-20
ADP1828ACPZ-R7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-10
ADP1828LC-EVALZ		Evaluation Board (with QSOP) with 5 A Output	
ADP1828HC-EVALZ		Evaluation Board (with QSOP) with 20 A Output	

[1] Z = RoHS Compliant Part.
[2] Operating junction temperature is −40°C to +125°C.

D06865-0-8/18(E)

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