THE DATASHEET OF

BM81810MUV-ME2

Datasheet

Power Supply IC Series for TFT-LCD Panels

Automotive Panel Power Management IC

BM81810MUV-M

General Description

BM81810MUV-M is a power management IC for TFT-LCD panels which are used in car navigation, in-vehicle center panel, and instrument cluster.
This IC incorporates VCOM amplifier, Gate Pulse Modulation (GPM) in addition to the power supply for panel driver (SOURCE, GATE, and LOGIC power supplies). Moreover, this IC has a built-in EEPROM for sequence and output voltage setting retention.

Key Specifications

- Input voltage range: 2.6V to 5.5V
- AVDD Output voltage range: 5.0V to 17.0V
- VGH Output voltage range: 8.0V to 35.0V
- VGL Output voltage range: -4.0V to -14.0V
- VDD Output voltage range: 0.9V to 3.4V
- VCOM Output current: 200 mA (Typ)
- Switching Frequency: 525KHz, 1.05MHz, 2.1MHz
- Operating temperature range: -40°C to +105°C
- Standby current: 2.0 μA (Typ)

Special Characteristics

- AVDD output voltage accuracy: ±2%
- Oscillator Frequency: ±10%

Applications

TFT-LCD Panels which are used in car navigation, in-vehicle center panel, and instrument cluster.

Features

- AEC-Q100 Qualified(Note 1)
- Alternative Synchronous Buck DC/DC converter or LDO for VDD output
- Synchronous Boost DC/DC converter for AVDD output with integrated load switch.
- VCOM amplifier with 7bit calibrator
- Positive charge pump (Integrated diode, x2/x3) for VGH output
- Negative charge pump for VGL output
- VGH and VCOM temperature compensation
- Gate Pulse Modulation(GPM)
- I^2C Interface Output Voltage Setting Control Function (Integrated EEPROM)
- Switching frequency switching function (525kHz, 1.05MHz, 2.1MHz)
- Protection circuits
  - Under-Voltage Lockout
  - Thermal Shut Down
  - Over-Current Protection
  - Over-Voltage Protection
  - Under Voltage Protection (Timer Latch type)
- Input tolerant (SCL, SDA, EN, GSIN)

(Note1: Grade 2)

Package

VQFN32SV5050

W(Typ) x D(Typ) x H(Max)

5.0mm x 5.0mm x 1.0mm

Typical Application Circuit (TOP VIEW)

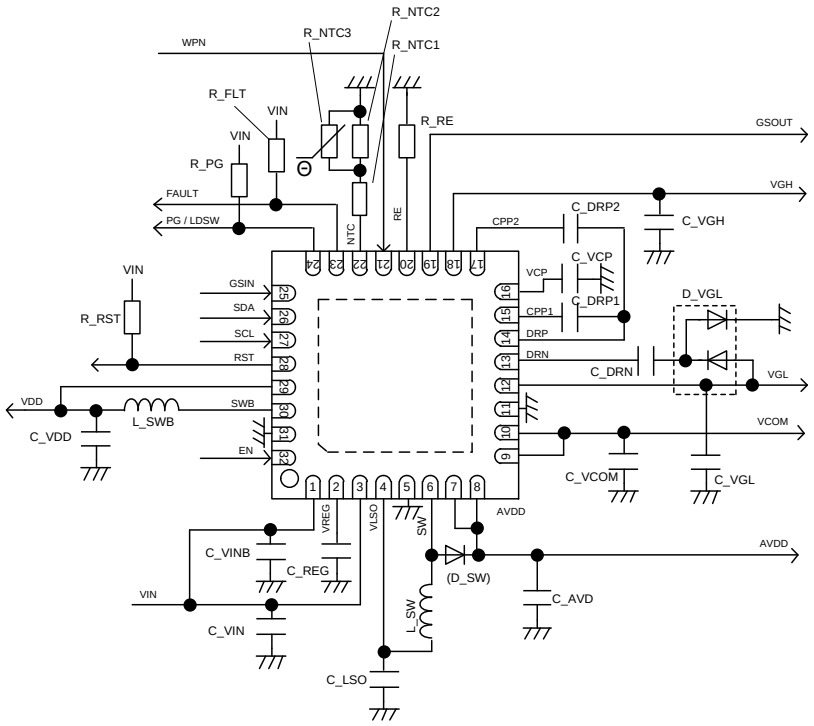

Figure 1. Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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Pin Configuration (TOP VIEW)

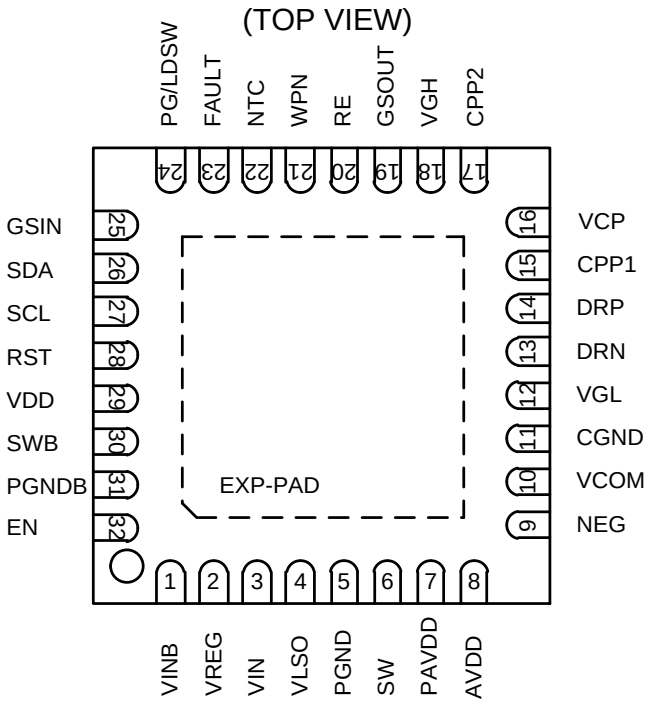

Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Function	Pin No	Pin Name	Function
1	VINB	Buck DC/DC power supply input	17	CPP2	Built-in Positive charge pump switching Di output 3
2	VREG	Inner power supply output	18	VGH	Positive charge pump feedback & Power Input of Gate Pulse Modulation
3	VIN	Boost DC/DC load switch input	19	GSOUT	Output of Gate Pulse Modulation
4	VLSO	Boost DC/DC load switch output	20	RE	Slope Setting Pin for Gate Pulse Modulation
5	PGND	Boost DC/DC ground	21	WPN	Active Low of EEPROM Writing protection.
6	SW	Boost DC/DC switching pin	22	NTC	Slope setting pin for temperature compensation of the VON and VCOM
7	PAVDD	Boost DC/DC output & output feedback Power Input of DRN	23	FAULT	FAULT signal output
8	AVDD	Power Input of VCOM , DRP	24	PG/ LDSW	Power Good signal output or Load SW of PAVDD.
9	NEG	Negative Input of VCOM Amplifier	25	GSIN	Input of Gate Pulse Modulation
10	VCOM	VCOM amplifier output	26	SDA	Serial clock data input (I2C)
11	CGND	Charge pump ground	27	SCL	Serial clock input (I2C)
12	VGL	Negative charge pump feedback	28	RST	Reset output
13	DRN	Negative charge pump driver pin	29	VDD	Buck DC/DC or LDO output feedback input
14	DRP	Positive charge pump driver pin	30	SWB	Buck DC/DC switching pin or LDO output pin
15	CPP1	Built-in Positive charge pump switching Di output 1	31	PGNDB	Buck DC/DC ground
16	VCP	Built-in Positive charge pump switching Di output 2	32	EN	Enable input
			-	EXP -PAD	Connect to Ground.

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Absolute Maximum Ratings

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Power Supply Voltage	VIN, VINB	-0.3	-	+6.5	V
Output Pin	SWB	-0.3	-	VINB+0.3	V
	VDD	-0.3	-	+6.5	V
	AVDD, PAVDD, SW	-0.3	-	+19	V
	VLSO	-0.3	-	+6.5	V
	VCOM	-0.3	-	AVDD+0.3	V
	DRP	-0.3	-	AVDD+0.3	V
	DRN	-0.3	-	PAVDD+0.3	V
	CPP1,CPP2,VCP	-0.3	-	+36	V
	VGH,GSOUT,RE	-0.3	-	+36	V
	VGL	-15	-	+0.3	V
	VREG	-0.3	-	VIN+0.3	V
	FAULT	-0.3	-	+6.5	V
	PG/LDSW	-0.3		+19	V
	RST, NTC	-0.3	-	VIN+0.3	V
Input Pin	NEG	-0.3	-	AVDD+0.3	V
Functional Pin Voltage	SCL, SDA, EN, GSIN	-0.3	-	+6.5	V
	WPN	-0.3	-	VIN+0.3	V
Maximum Junction temperature	Tjmax *(Note 1)*	-	-	+150	°C
Storage Temperature Range	Tstg	-55	-	+150	°C

(Note 1) Junction temperature at storage time.

Caution : Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

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Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
VQFN32SV5050				
Junction to Ambient	θ_{JA}	138.9	39.1	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	11	5	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air).
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mm

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 4)*Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Ratings (Ta=-40 °C to +105 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VIN,VINB	2.6	-	5.5	V
SWB Current	ISWB	-	-	1.0	A
SW Current	ISW	-	-	2.0	A
Functional Pin Voltage	EN,GSIN,WPN	-0.1	-	+5.5	V
2 Line Serial Pin Voltage	SDA, SCL	-0.1	-	+5.5	V
2 Line Serial Frequency	FCLK	-	-	400	kHz
Operating Ambient Temperature	TA	-40	-	+105	°C
Operating Junction Temperature	TJ	-40	-	+125	°C

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Electrical Characteristics (Unless otherwise specified, Ta=25°C, VIN, VINB=3.3V)

1. VDD regulator block (Alternative Buck converter or LDO)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Output Voltage Range	VDD	0.9	-	3.4	V	50 mV step
Output Voltage Accuracy 1	VDD_R1	2.462	2.5	2.538	V	VDD=2.5 V setting
Output Voltage Accuracy 2	VDD_R2	-2.0	-	+2.0	%	VDD=2.5 V to 3.4 V setting (Ta=-40 to +105 °C)
Output Voltage Accuracy 3	VDD_R3	-3.0	-	+3.0	%	VDD=0.9 V to 2.45 V setting (Ta=-40 to +105 °C)
Soft Start time	VDD_SS	0.85	1	1.15	msec	VDD=1.2 V setting
Under-Voltage Protection voltage	VDD_UVP	VDD×0.7	VDD×0.8	VDD×0.9	V	
SWB H Side ON Resistance	RONH_SWB	-	300	480	mΩ	DCDC mode
SWB L Side ON Resistance	RONL_SWB	-	300	480	mΩ	DCDC mode
SWB H Side ON Resistance	RON_SWB	-	1.0	2.0	Ω	LDO mode
SWB H Side Leak Current	IL_ SWBH	-	0	20	μA	(Ta=-40 to +105 °C)
SWB L Side Leak Current	IL_ SWBL	-	0	20	μA	(Ta=-40 to +105 °C)
Current Limit	ILMT_SWB1	1.0	1.7	2.7	A	Buck DCDC mode
Current Limit	ILMT_SWB2	0.3	0.5	0.7	A	LDO mode
Maximum Duty	DMAX_SWB	87	95	-	%	Freq=1.05 MHz (Freq=0.525 MHz:98%typ) (Freq=2.10 MHz:87%typ)
Discharge Resistance	DISR_VDD	-	25	50	Ω	

2. Boost DC/DC converter block (AVDD)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Output Voltage Range	AVDD	5.0	-	17.0	V	0.1 V step
Output Voltage Accuracy1	AVDD_R1	10.342	10.5	10.66	V	AVDD=10.5 V setting
Output Voltage Accuracy2	AVDD_R2	10.29	10.5	10.71	V	AVDD=10.5 V setting (Ta=-40 to +105 °C)
Load Switch Soft Start time	LS_SS	1.7	2	2.3	msec	
Soft Start Time	AVDD_SS	4.25	5	5.75	msec	AVDD=10.5 V setting 5 ms setting
Under-Voltage Protection voltage	AVDD_UVP	AVDD×0.7	AVDD×0.8	AVDD×0.9	V	
Over-Voltage Protection voltage	AVDD_OVP	AVDD×1.03	AVDDx1.1	AVDD×1.2	V	
SW H Side On Resistance	RON_SW	-	250	480	mΩ	
SW L Side On Resistance	RON_SW	-	200	350	mΩ	
SW H Side Leak Current	IL_SWH	-	0	20	μA	(Ta=-40 to +105 °C)
SW L Side Leak Current	IL_SWL	-	0	20	μA	(Ta=-40 to +105 °C)
Current Limit	ILMT_SW	2.0	4.0	6.0	A	AVDD OCP=2 A setting
Current Limit	ILMT_SW	1.0	2.0	2.5	A	AVDD OCP=1 A setting
Load Switch ON Resistance	RON_LS	-	200	350	mΩ	
Maximum Duty	DMAX_SW	83	90	-	%	Freq=1.05 MHz (Freq=0.525 MHz:95%typ) (Freq=2.10 MHz:80%typ)
Discharge Resistance	DISR_AVDD	-	25	50	Ω	

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Electrical Characteristics (Unless otherwise specified, Ta=25°C, VIN, VINB=3.3V) – continued

3. VCOM amplifier block (VCOM)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Output Voltage Range1	VCOM_HOT	0.5x AVDD - 4.0	0.5x AVDD	0.5x AVDD + 4.0	V	40 mV step
Output Voltage Range2	VCOM_COLD	VCOM HOT - 0.63	-	VCOM HOT	V	10 mV step
Output Voltage Range3	VCOM_CAL	VCOM HOT - 0.63	VCOM HOT	VCOM HOT +0.63V	V	10 mV step
Output Voltage Range4	VCOM_RNG	0.2xAVDD	-	0.7x AVDD	V	
Calibration Resolution	RES_CAL	-	7	-	Bit	
Integral Non-Linearity Error (INL)	INL_CAL	-1	-	+1	LSB	
Differential Non-Linearity Error (DNL)	DNLCAL	-1	-	+1	LSB	
Output Current Ability (Source)	ISOURCE	-	200	-	mA	
Output Current Ability (Sink)	ISINK	-	200	-	mA	
Load Stability	VLOAD	-	10	70	mV	Io=-15 mA to +15 mA
Slew Rate	SR	30	60	80	V/µsec	

4. Positive charge pump block (VGH)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Output Voltage Range 1	VGH_HOT	8.0	-	35	V	0.2 V step
Output Voltage Range 2	VGH_COLD	VGH HOT	-	VGH HOT +15V	V	0.2 V step *Max = 35 V
Output Voltage Accuracy 1	VGH_R1	17.46	18	18.54	V	VGH=18 V setting
Output Voltage Accuracy 2	VGH_R2	17.1	18	18.9	V	VGH=18 V setting (Ta=-40 to +105 °C)
Soft Start time	VGH_SS	4.25	5	5.75	msec	VGH=18 V setting
Under-Voltage Protection voltage	VGH_UVP	VGH×0.7	VGH×0.8	VGH×0.9	V	
DRP H Side On Resistance	RON_DRPH	-	10	20	Ω	
DRP L Side On Resistance	RON_DRPL	-	10	20	Ω	
AVDD-CPP1 On Resistance	RON_CPP1	-	10	20	Ω	
CPP1-VCP On Resistance	RON_CPP2	-	10	20	Ω	
VCP-CPP2 On Resistance	RON_CPP3	-	10	20	Ω	
CPP2-VGH On Resistance	RON_CPP4	-	10	20	Ω	
Discharge Resistance	DISR_VGH	-	150	300	Ω	

5. Negative charge pump block (VGL)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Output Voltage Range	VGL	-14.0	-	-4.0	V	0.1 V step
Output Voltage Accuracy 1	VGL_R1	-6.18	-6	-5.82	V	VGL=-6.0 V setting
Output Voltage Accuracy 2	VGL_R2	-6.3	-6	-5.7	V	VGL=-6.0 V setting (Ta=-40 to +105 °C)
Soft Start time	VGL_SS	4.25	5	5.75	msec	
Under-Voltage Protection voltage	VGL_UVP	VGL×0.7	VGL×0.8	VGL×0.9	V	
DRN H Side On Resistance	RON_DRNH	-	10	20	Ω	
DRN L Side On Resistance	RON_DRNN	-	10	20	Ω	
Discharge Resistance	DISR_VGL	-	250	500	Ω	

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Electrical Characteristics (Unless otherwise specified, Ta=25°C, VIN, VINB=3.3V) – continued

6. Temperature compensation block (NTC)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
NTC HOT Voltage	VNTC_H	0.475	0.5	0.525	V	
NTC COLD Voltage	VNTC_H	1.1875	1.25	1.3125	V	
NTC Current	INTC	36	40	44	μA	
NTC Resolution	RES_NTC	-	4	-	Bit	

7. Gate Pulse Modulation block (GPM)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
GPM High Switch On Resistance	RON_GPMH	-	15	30	Ω	
GPM Low Switch On Resistance	RON_GPML	-	30	-	Ω	
GPM Propagation Delay1	T_GPM1	-	0.1	0.3	μsec	No Capacitive Load 0.1 μS setting
GPM Propagation Delay2	T_GPM2	-	0.5	1.0	μsec	No Capacitive Load 0.5 μS setting
GPM Propagation Delay3	T_GPM3	-	1.0	1.75	μsec	No Capacitive Load 1.0 μS setting
GPM Propagation Delay4	T_GPM4	-	1.5	2.5	μsec	No Capacitive Load 1.5 μS setting
GSIN Pull Down Resistance	RGSIN	70	100	130	kΩ	
GSIN Input High Voltage	VGSINH	1.5	-	-	V	
GSIN Input Low Voltage	VGSINL	-	-	0.6	V	

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Electrical Characteristics (Unless otherwise specified, Ta=25°C, VIN, VINB=3.3V) – continued

8. Overall (Entire device)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Inside Regulator Voltage						
VREG Output Voltage	VREG	2.15	2.3	2.45	V	
Load Stability	ΔV	-	20	100	mV	IVREG=5 mA
Oscillator Block						
Oscillating Frequency 1	FOSC1	475	525	575	KHz	
Oscillating Frequency 2	FOSC2	950	1050	1150	KHz	
Oscillating Frequency 3	FOSC3	1900	2100	2300	KHz	
Under Voltage Lock Out (UVLO) Circuit						
UVLO release voltage	VUVLO1	2.5	2.55	2.6	V	
UVLO detection voltage	VUVLO2	2.0	2.1	2.2	V	
Hysteresis	VHYS_UVL	-	0.45	-	V	
Reset Circuit Block						
Reset Voltage Range	VRST	0.6	*	3.3	V	0.1 V step
Reset Voltage Accuracy	VRST_R1	1.9	2.0	2.1	V	VRST=2.0 V setting
Hysteresis	VHYS_RST	-	0.1	-	V	
Reset Delay time Range	T_Delay2	0	-	40	msec	
FAULT/ PG / RST Signal Output Block						
Output Off Leak Current	IL	-	0	10	μA	
Output On Resistance	RON_O	-	1	2	kΩ	
Control Signal Block1 SDA, SCL, WPN						
Minimum Output Voltage	VSDA	-	-	0.4	V	ISDA=3 mA
H Level Input Voltage	VIH	1.5	-	-	V	
L Level Input Voltage	VIL	-	-	0.6	V	
WPN Pull Down Resistance	RWPN	70	100	130	kΩ	
Control Signal Block2 EN						
Pull-Down Resistance Value	REN_L	280	400	520	kΩ	EN=Low
	REN_H	420	600	780	kΩ	EN=High
H Level Input Voltage	VENH	1.5	-	-	V	
L Level Input Voltage	VENL	-	-	0.6	V	
Overall						
Standby Current1	ISTB1	-	2.0	5.0	μA	EN=GND
Standby Current2	ISTB2	-	-	20	μA	EN=GND (Ta=-40 to +105 °C)
Consumption Current	ICC1	-	2.0	5.0	mA	EN=VIN, No switching

9. EEPROM

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Rewritable cycle	Cyc	100	-	-	Times	TJ<125 °C
Programmable time	Twr	-	-	50	msec	
Data hold years	DHY	20	-	-	Years	TJ<125 °C

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Typical Performance Curves
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

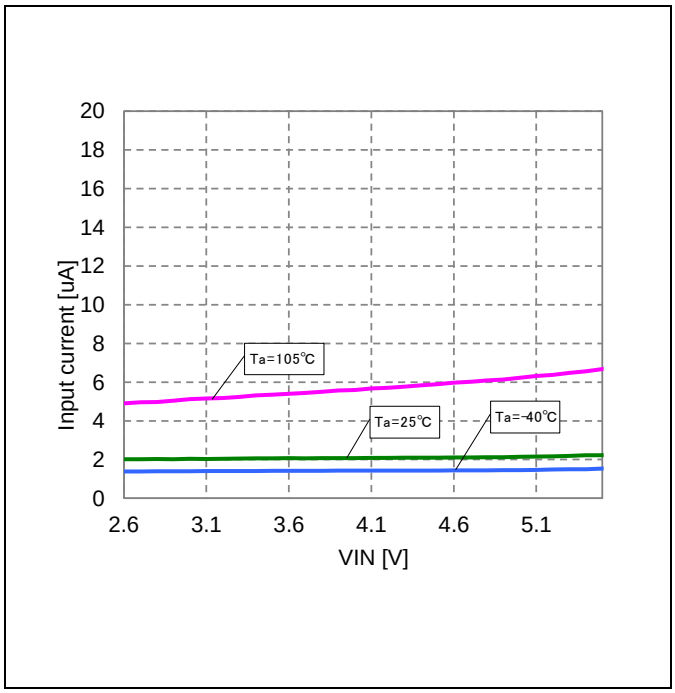

Figure 3. Standby Current(EN=L)

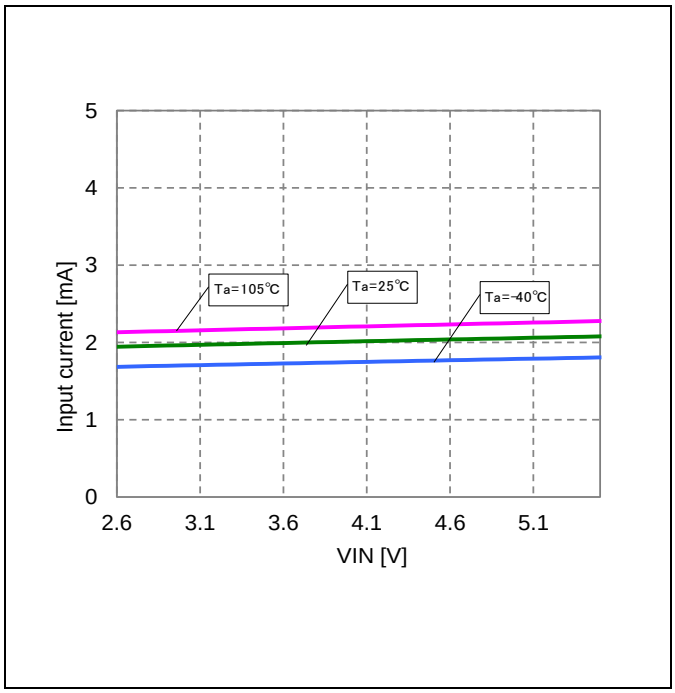

Figure 4. Circuit Current(EN=H, no switching)

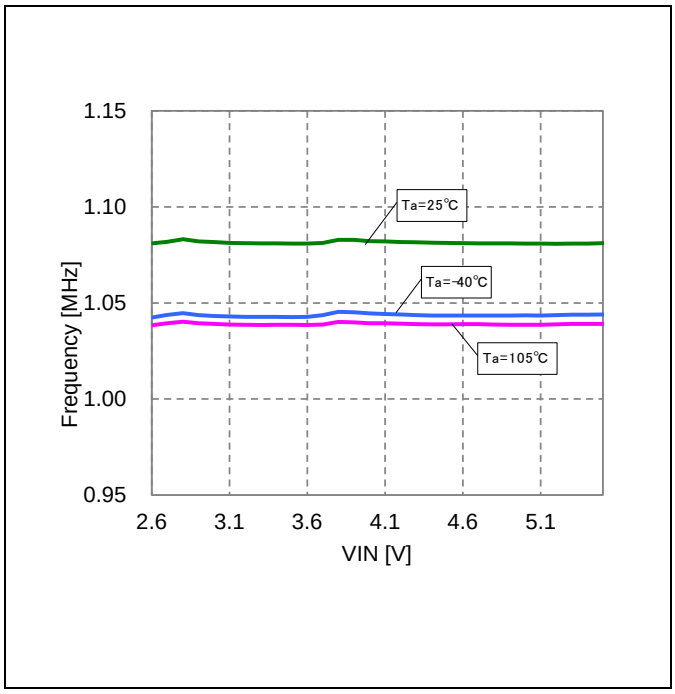

Figure 5. Switching Frequency
(Dependent on input voltage)

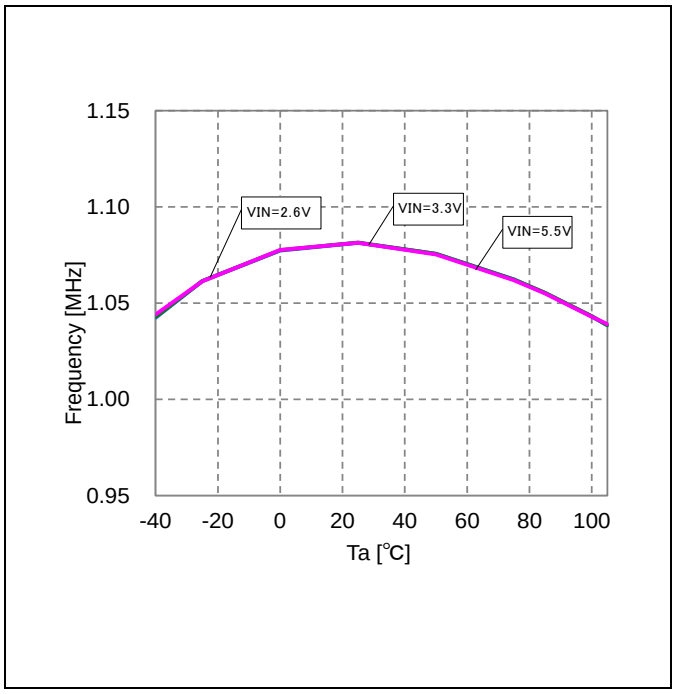

Figure 6. Switching Frequency
(Dependent on temperature)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

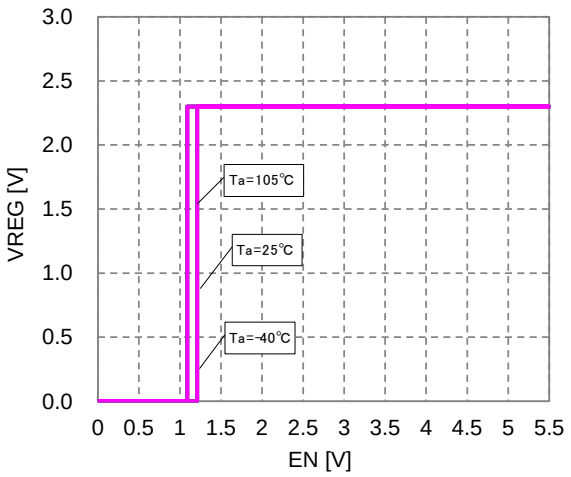

Figure 7. H/L threshold voltage
(control signals)

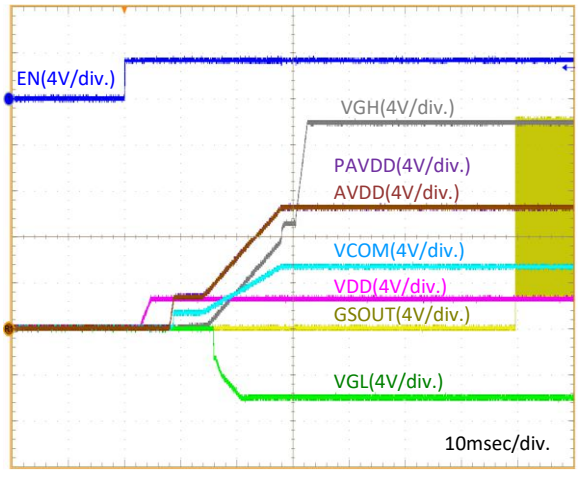

Figure 8. Power on waveform
(when operated by EN control, Function select = PG)

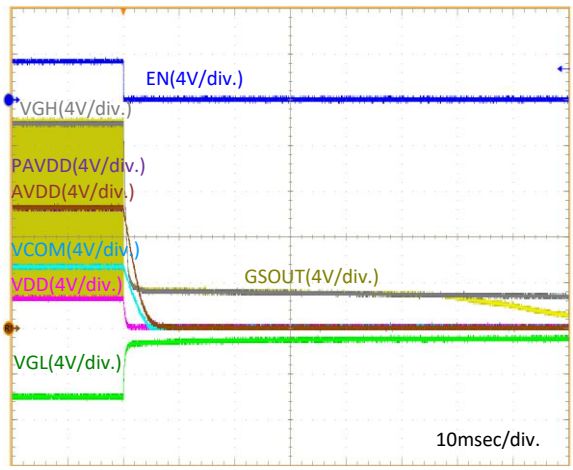

Figure 9. Power off waveform
(when operated by EN control, Function select = PG)

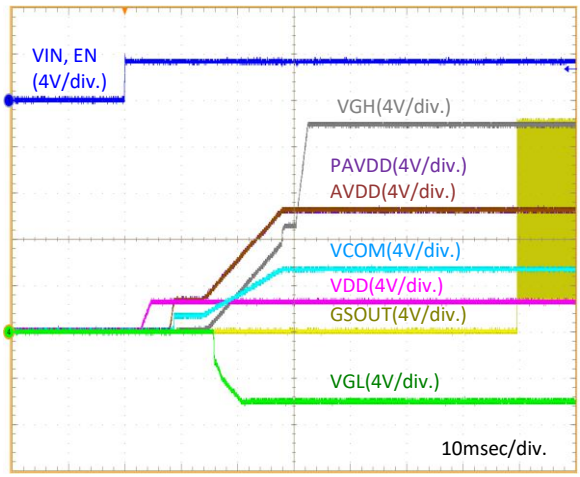

Figure 10. Power on waveform
(when operated with EN=VCC, Function select = PG)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

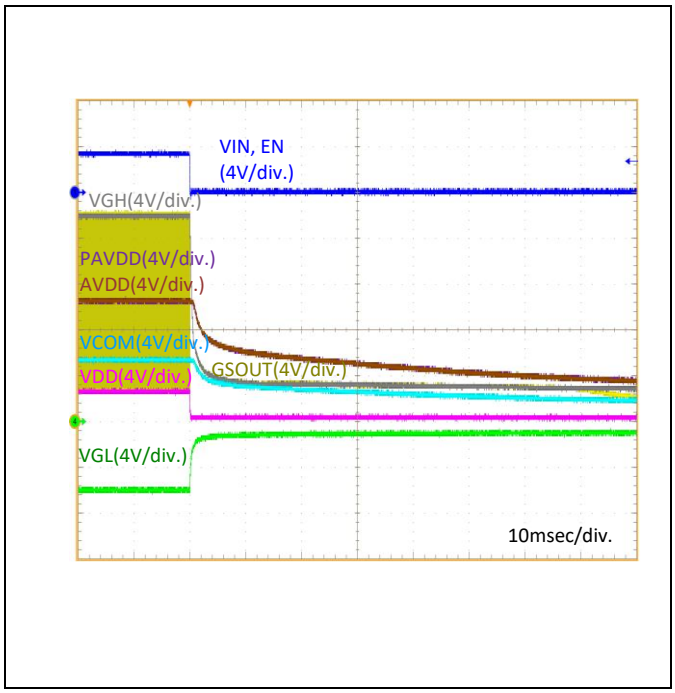

Figure 11. Power off waveform
(when operated with EN=VCC, Function select = PG)

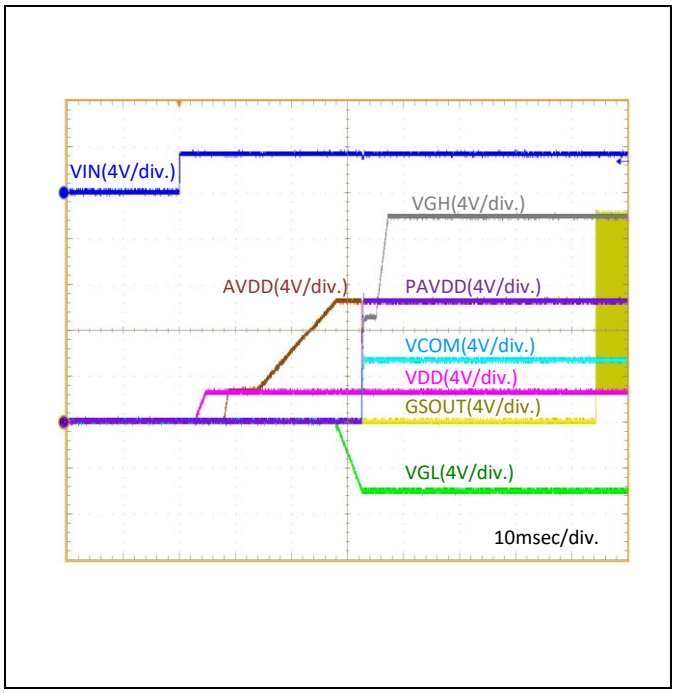

Figure 12. Power on waveform
(when operated by EN control, Function select = LDSW)

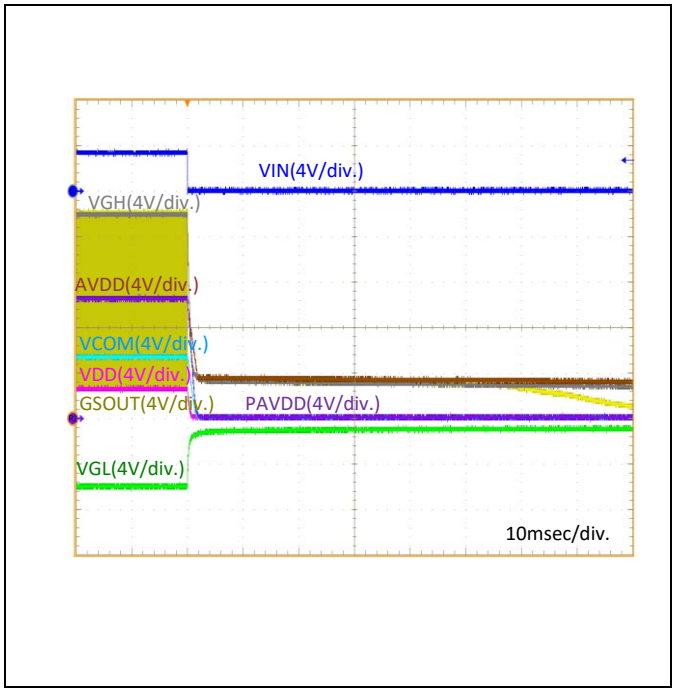

Figure 13. Power off waveform
(when operated by EN control, Function select = LDSW)

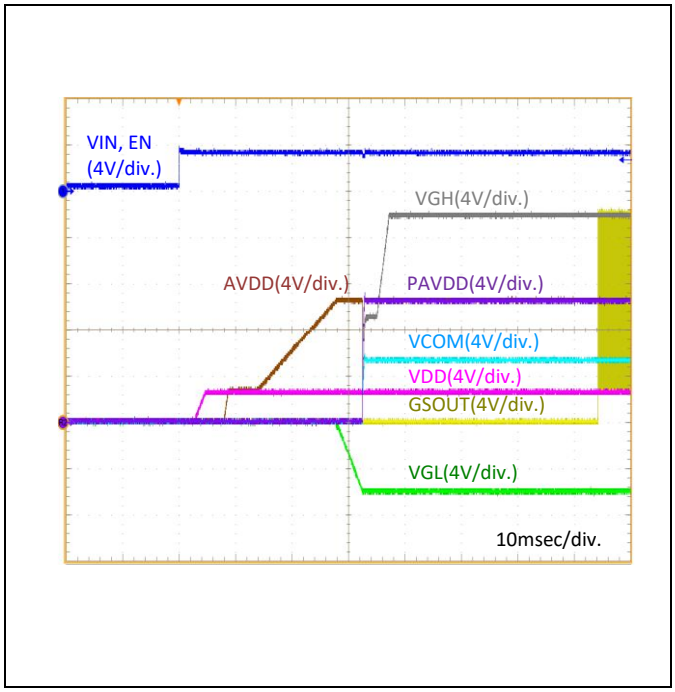

Figure 14. Power on waveform
(when operated with EN=VCC, Function select = LDSW)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

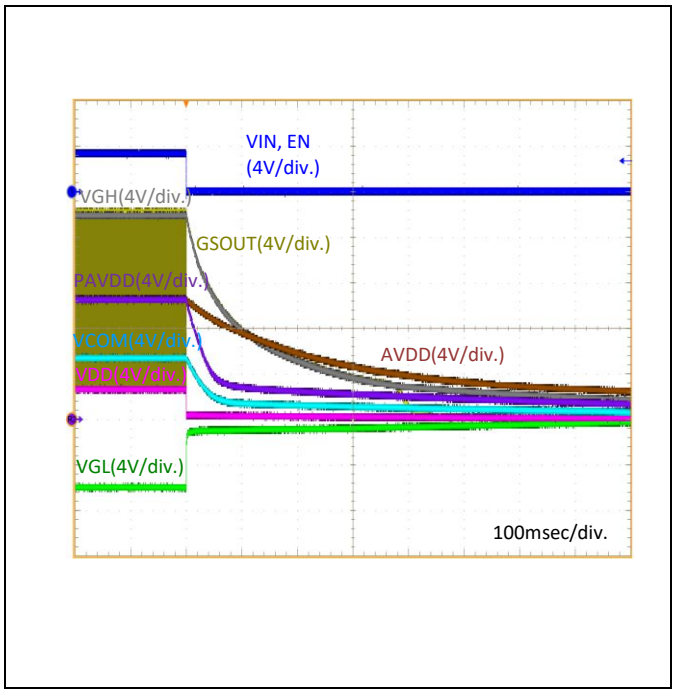

Figure 15. Power off waveform
(when operated with EN=VCC, Function select = LDSW)

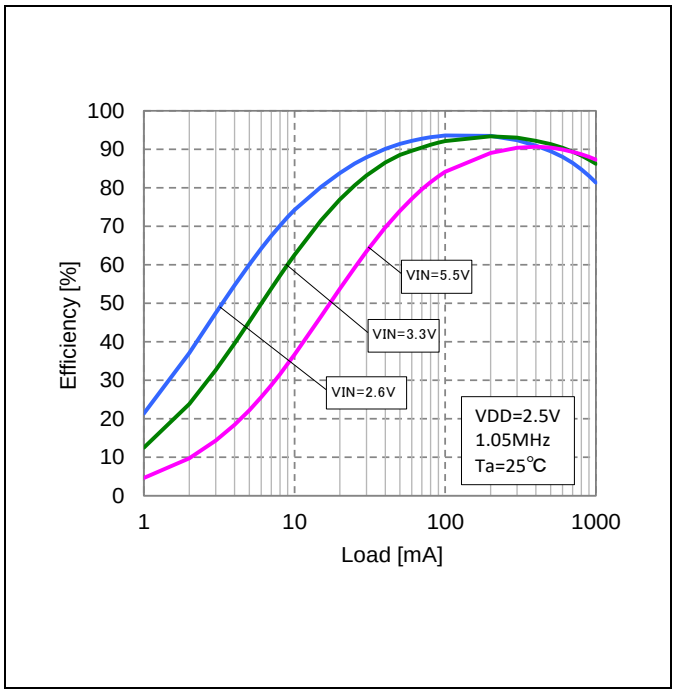

Figure 16. Efficiency
(VDD DC/DC mode)

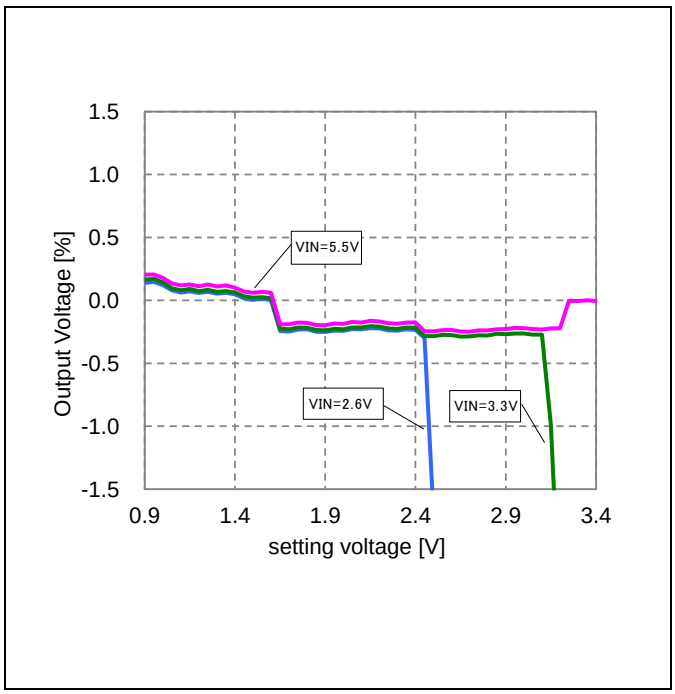

Figure 17. Output voltage accuracy
(VDD DC/DC mode, dependent on input voltage)

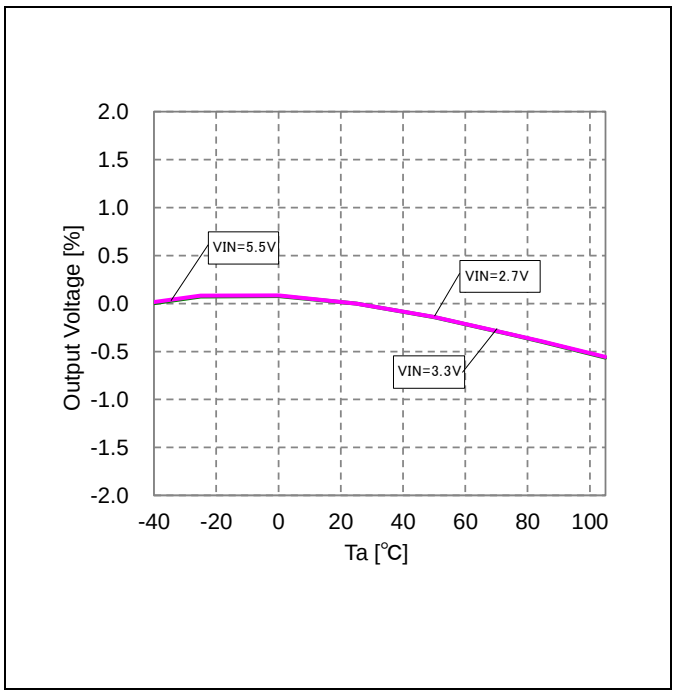

Figure 18. Output voltage accuracy
(VDD DC/DC mode, dependent on temperature)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

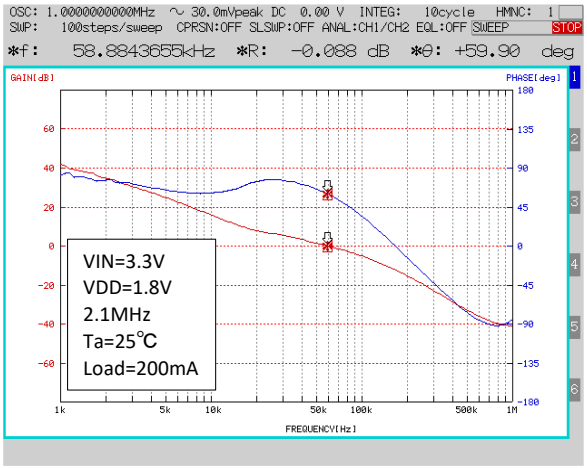

Figure 19. Phase margin
(VDD DC/DC mode)

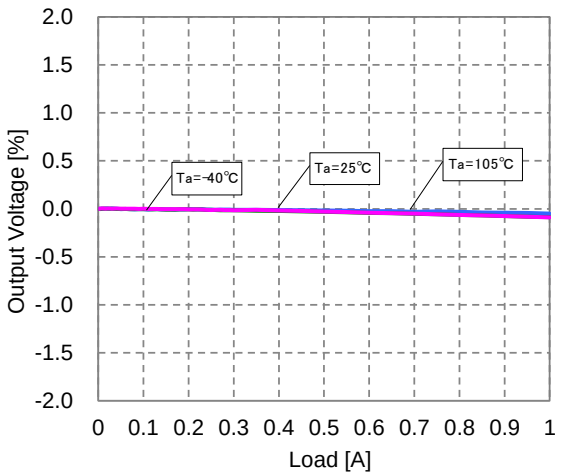

Figure 20. Load Regulation
(VDD DC/DC mode)

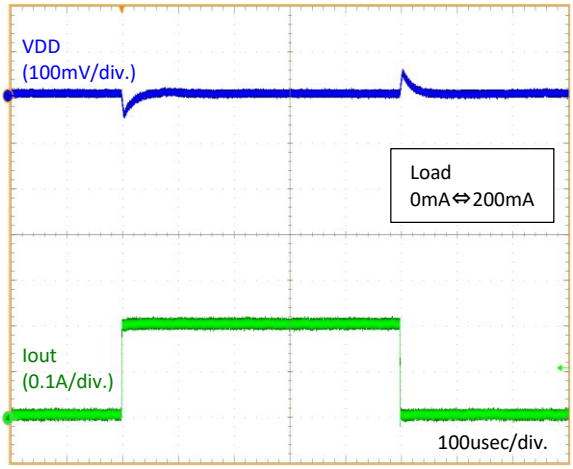

Figure 21. Load Transient
(VDD DC/DC mode)

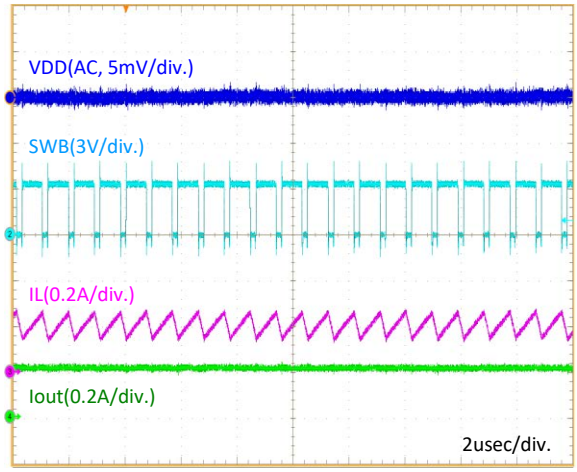

Figure 22. Switching waveform
(VDD DC/DC mode)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

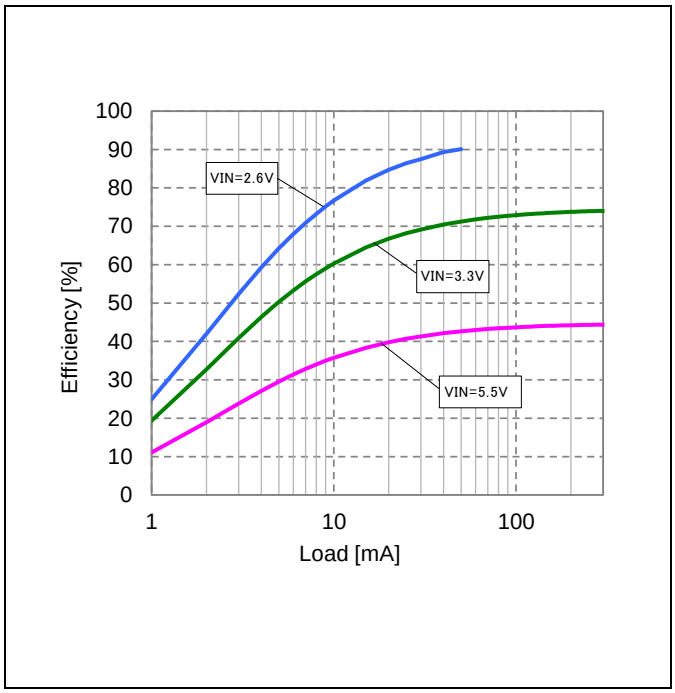

Figure 23. Efficiency
(VDD LDO mode)

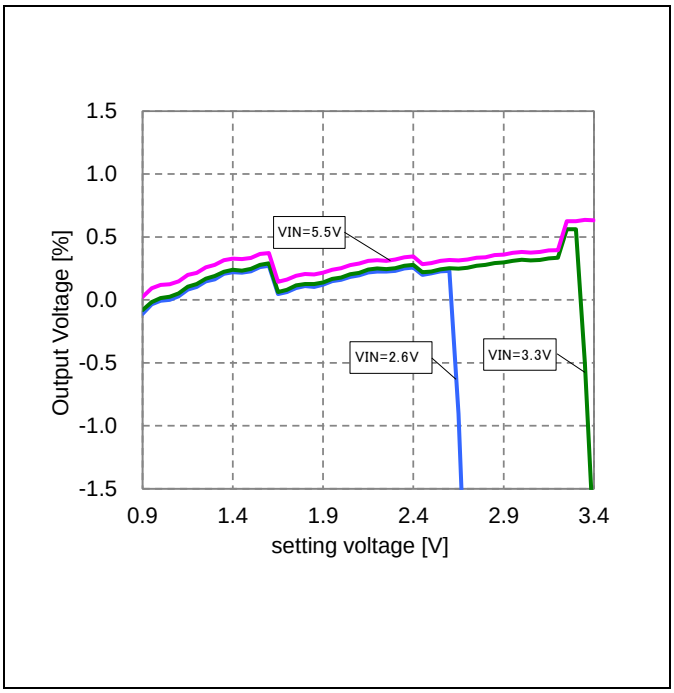

Figure 24. Output voltage accuracy
(VDD LDO mode, dependent on input voltage)

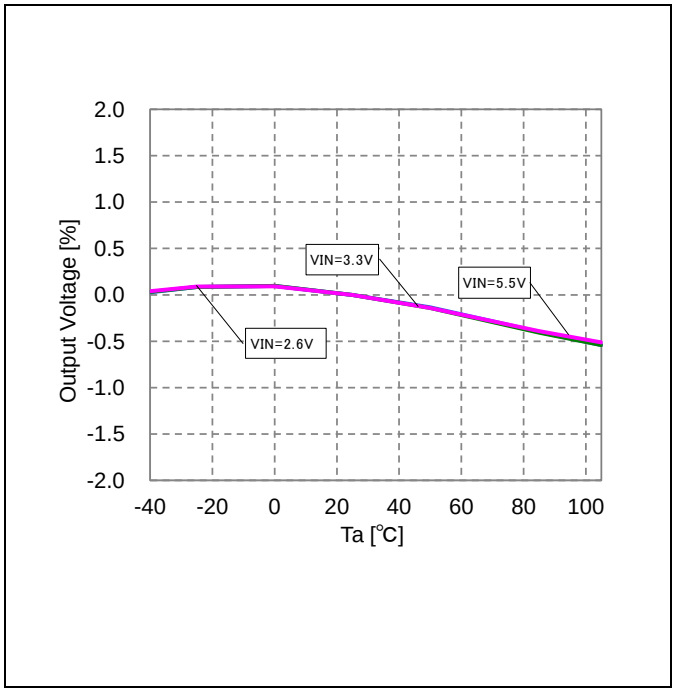

Figure 25. Output voltage accuracy
(VDD LDO mode, dependent on temperature)

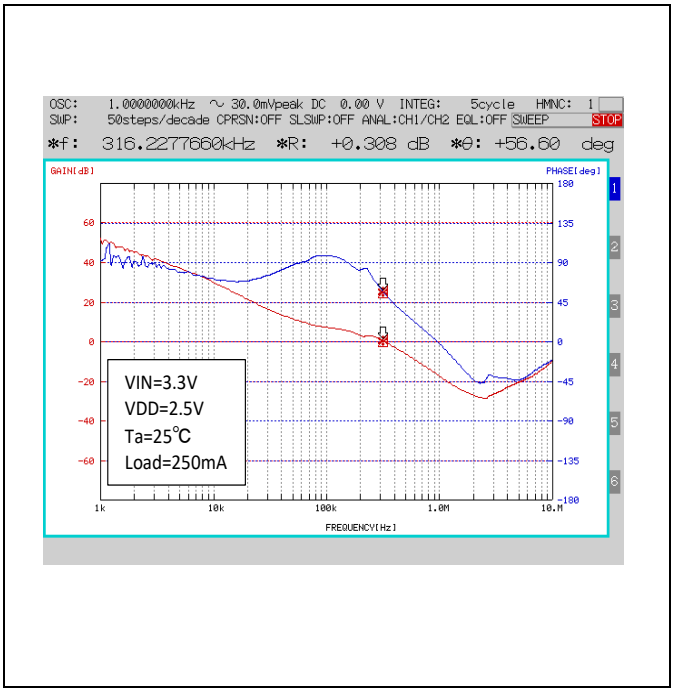

Figure 26. Phase margin
(VDD LDO mode)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

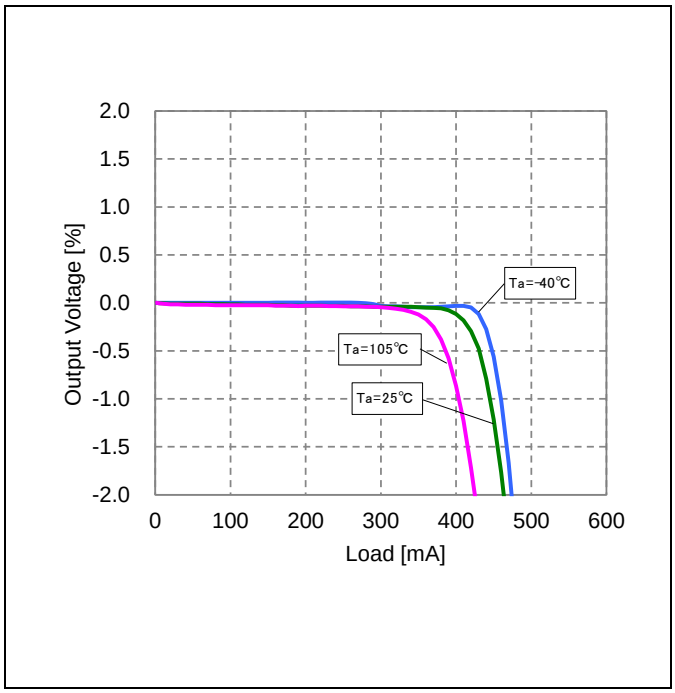

Figure 27. Load Regulation
(VDD LDO mode)

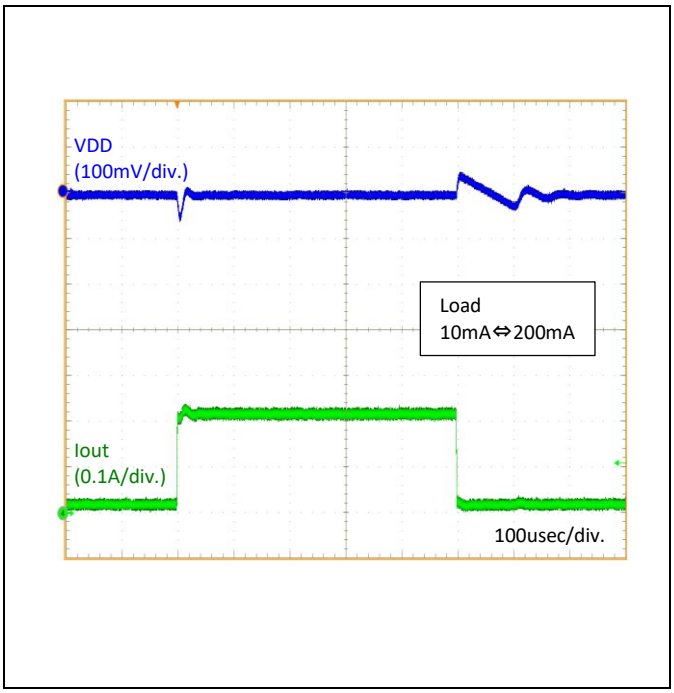

Figure 28. Load Transient
(VDD LDO mode)

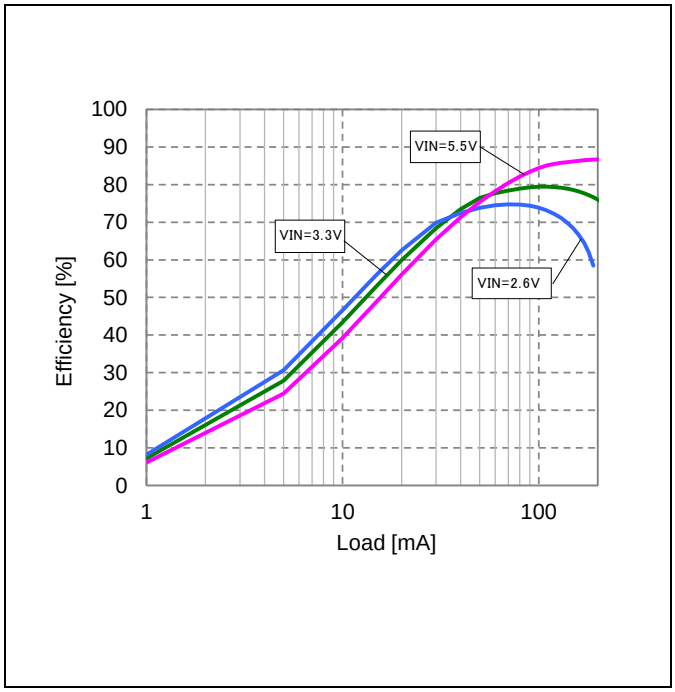

Figure 29. Efficiency
(AVDD)

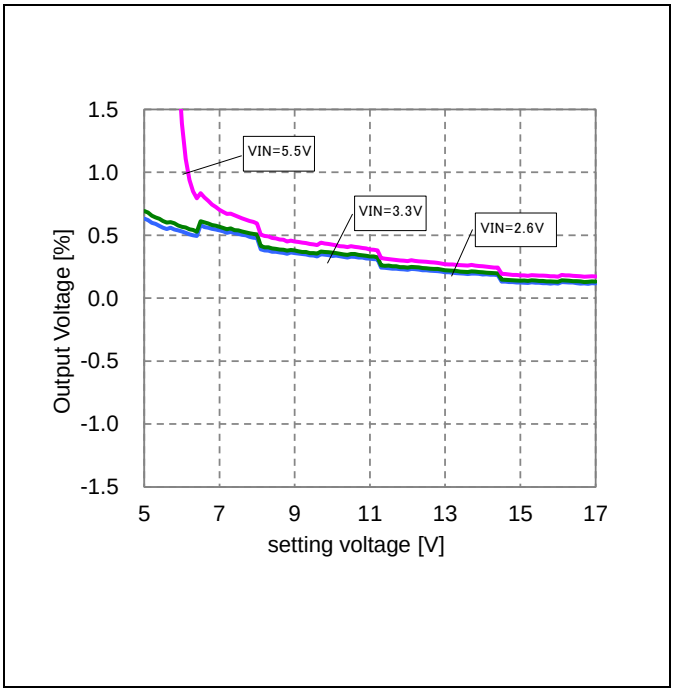

Figure 30. Output voltage accuracy
(AVDD, dependent on input voltage)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

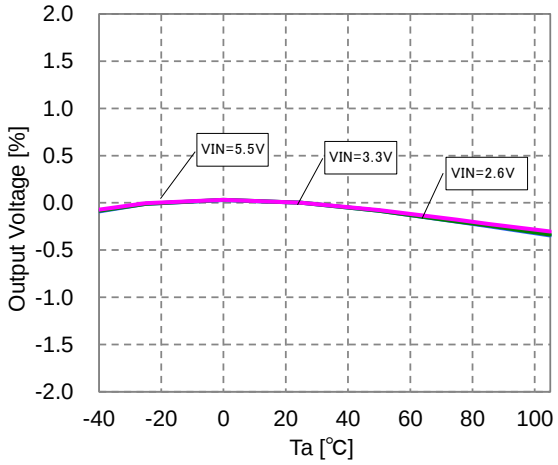

Figure 31. Output voltage accuracy
(AVDD, dependent on temperature)

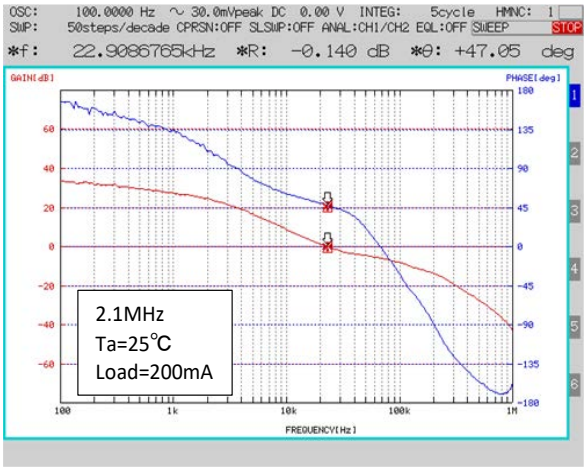

Figure 32. Phase margin
(AVDD)

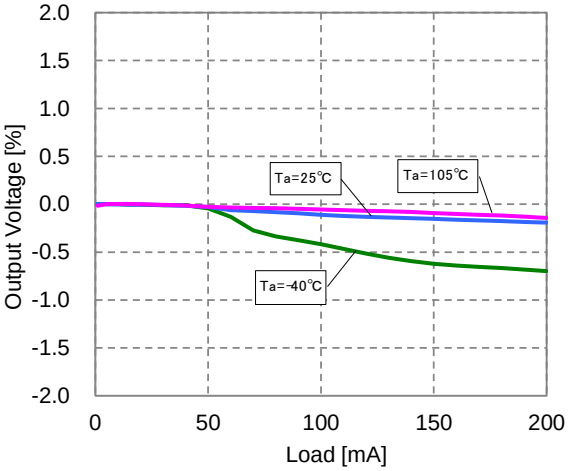

Figure 33. Load Regulation
(AVDD)

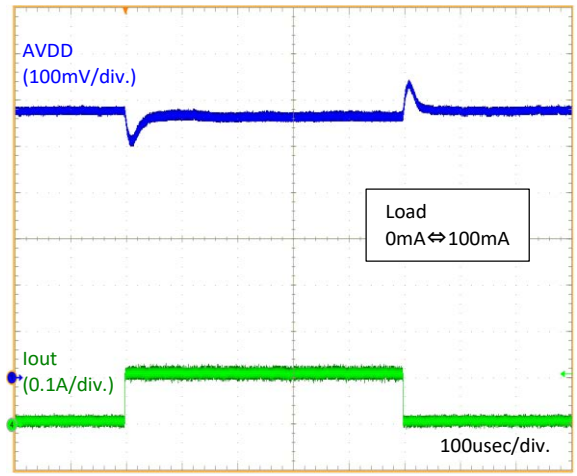

Figure 34. Load Transient
(AVDD)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

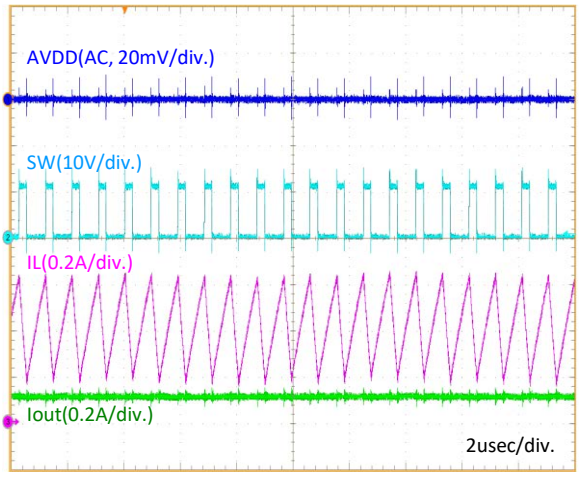

Figure 35. Switching waveform
(AVDD)

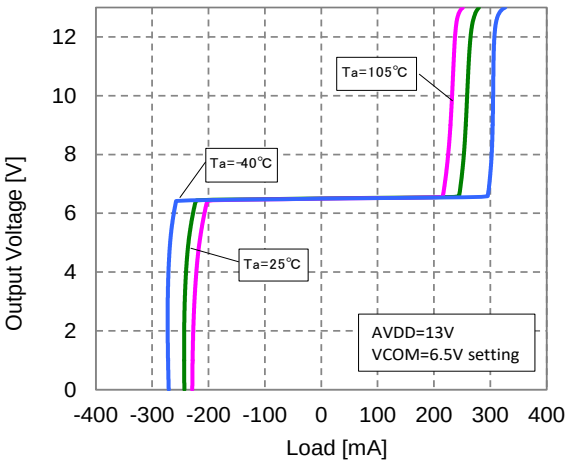

Figure 36. Output Current
(VCOM)

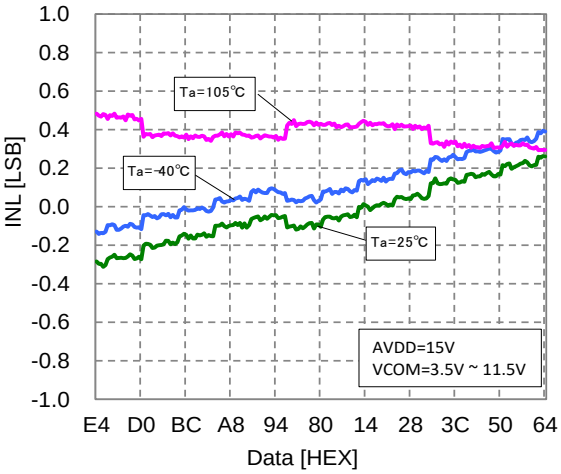

Figure 37. DAC INL
(VCOM)

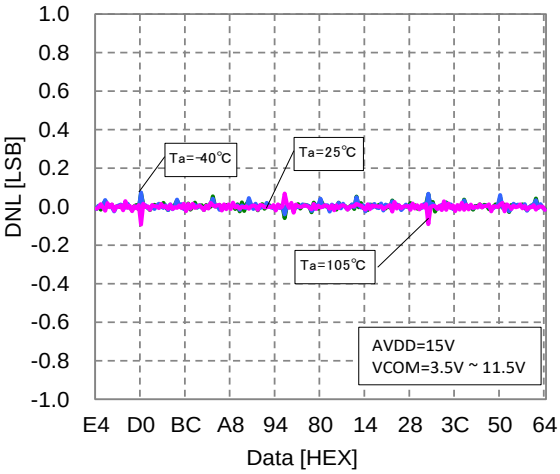

Figure 38. DAC DNL
(VCOM)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

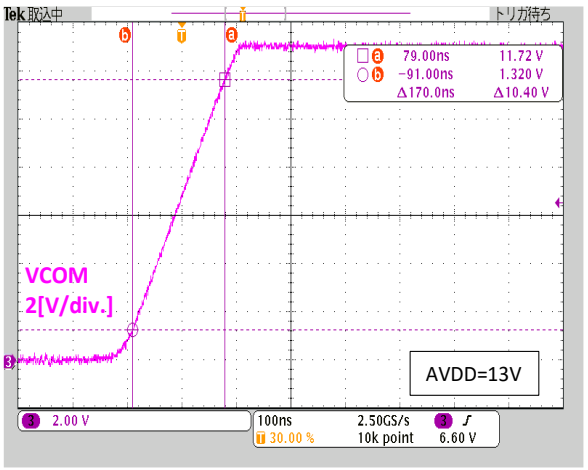

Figure 39. Slew Rate
(VCOM, rise)

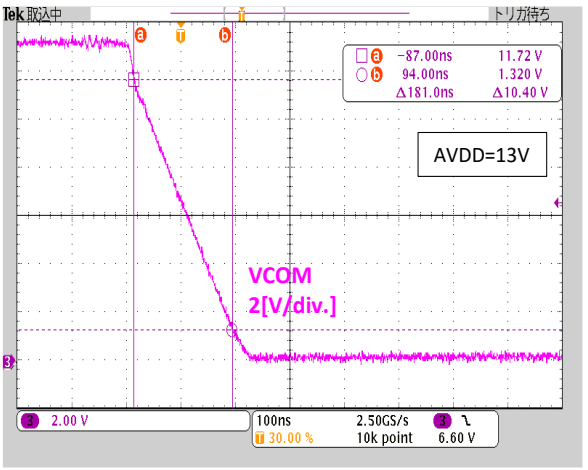

Figure 40. Slew Rate
(VCOM, fall)

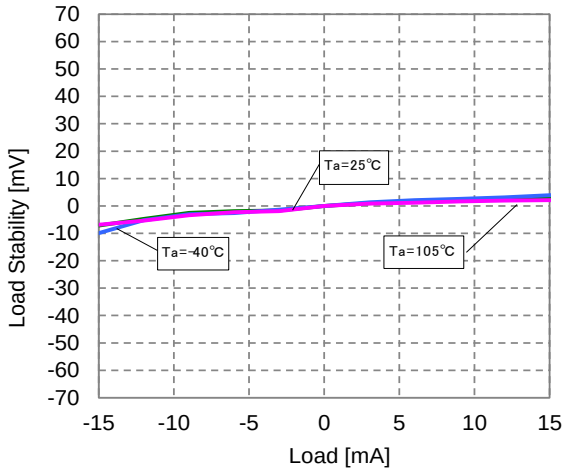

Figure 41. Load Regulation
(VCOM)

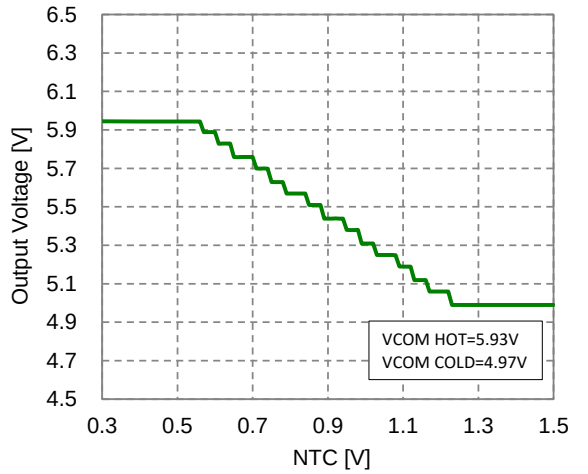

Figure 42. NTC Function
(VCOM)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

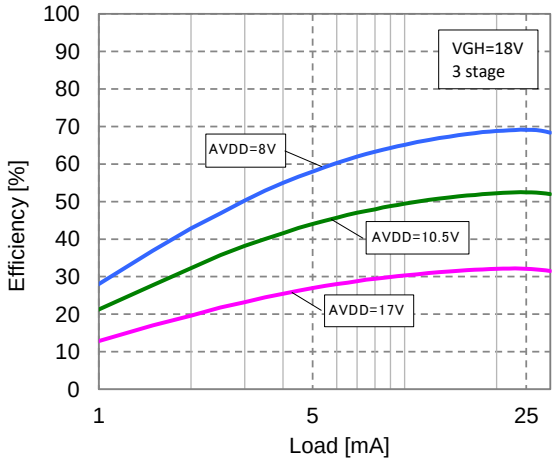

Figure 43. Efficiency
(VGH)

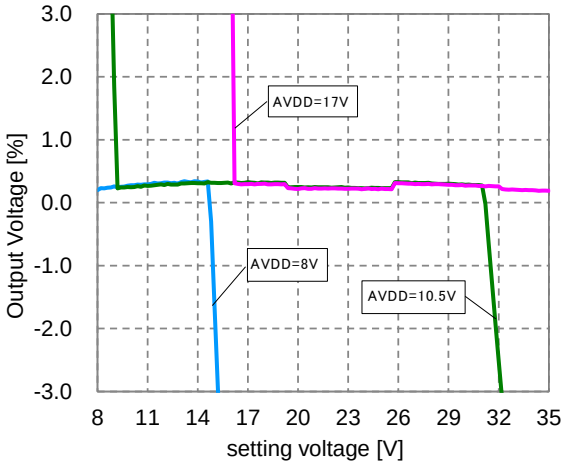

Figure 44. Output voltage accuracy
(VGH, dependent on input voltage)

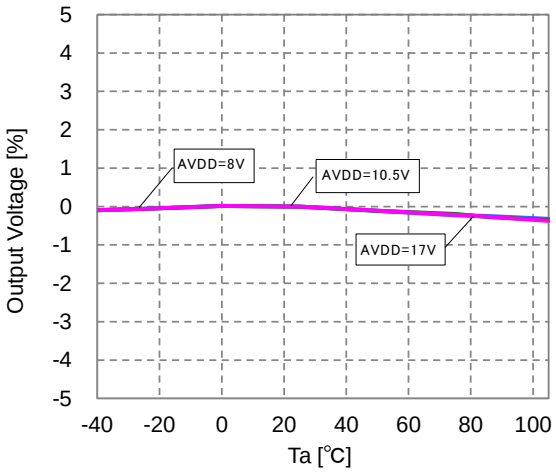

Figure 45. Output voltage accuracy
(VGH, dependent on temperature)

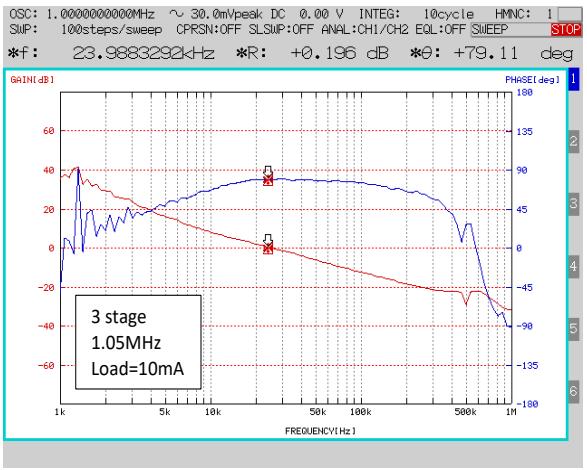

Figure 46. Phase margin
(VGH)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

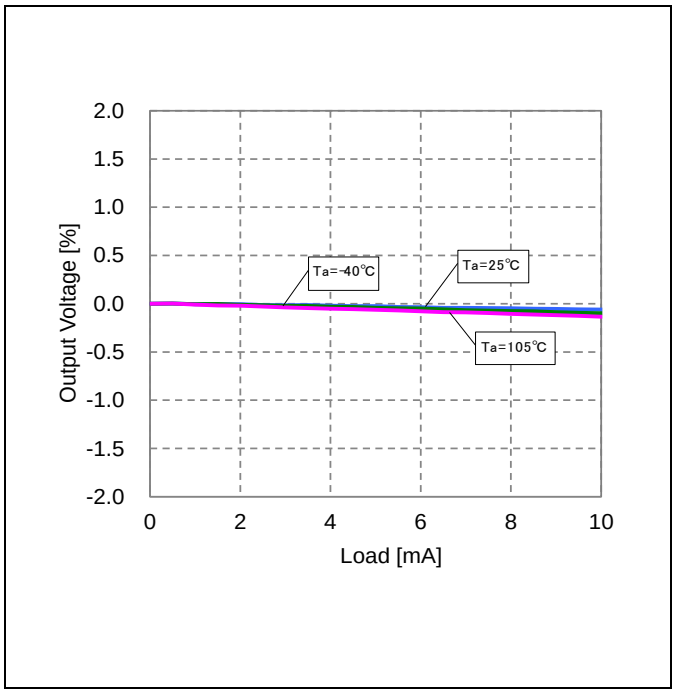

Figure 47. Load Regulation
(VGH)

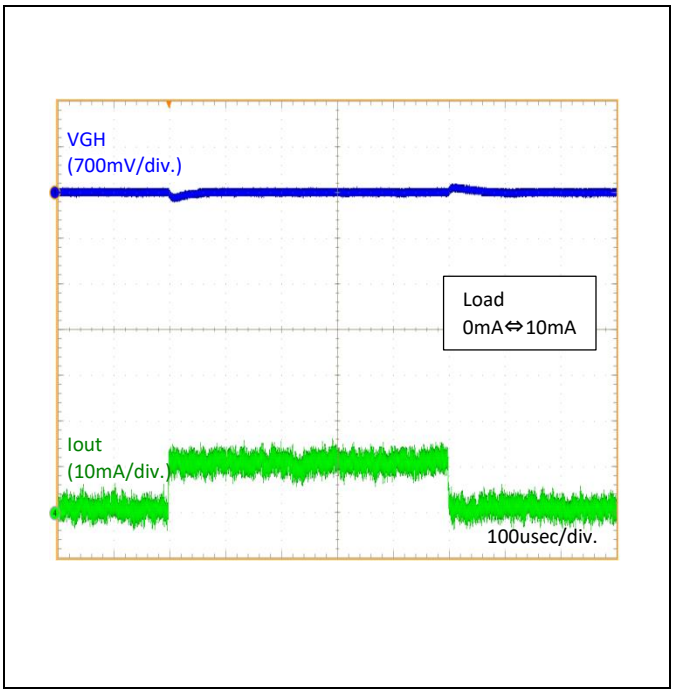

Figure 48. Load Transient
(VGH)

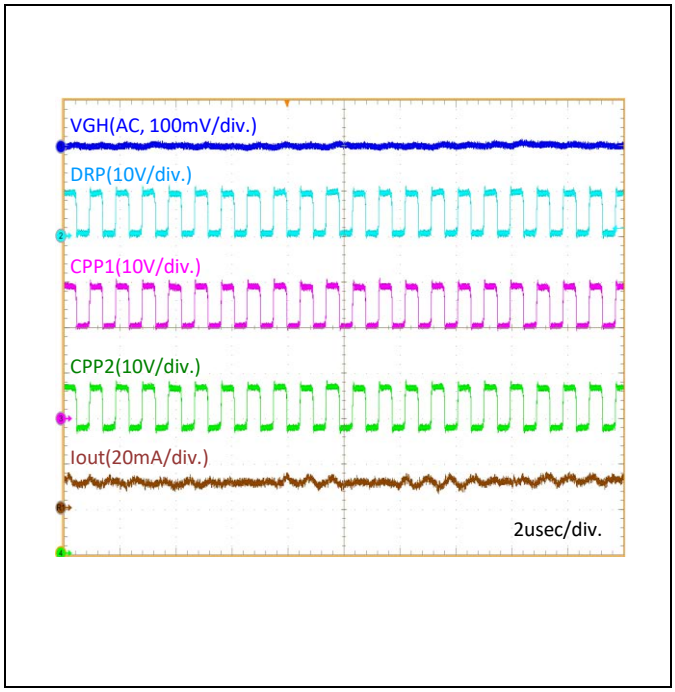

Figure 49. Switching waveform
(VGH)

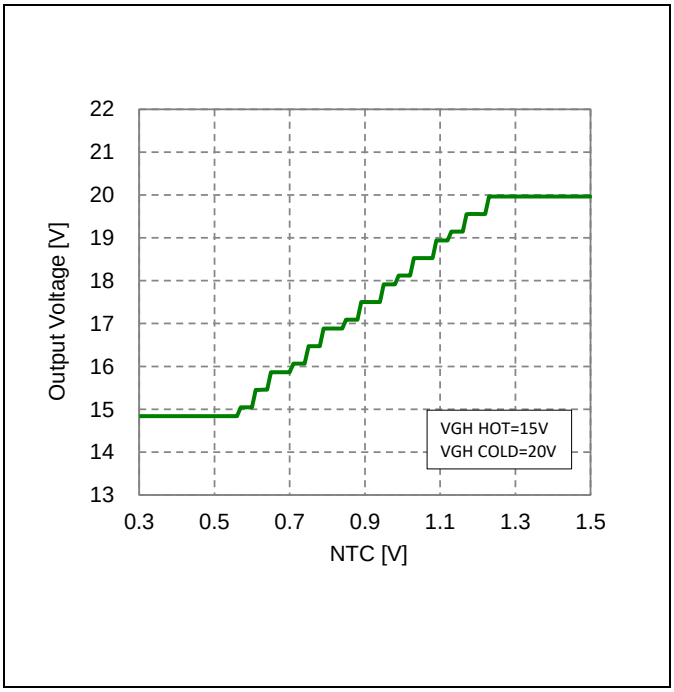

Figure 50. NTC Function
(VGH)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

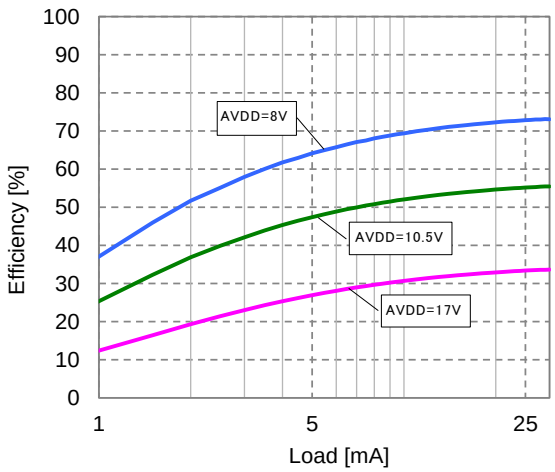

Figure 51. Efficiency
(VGL)

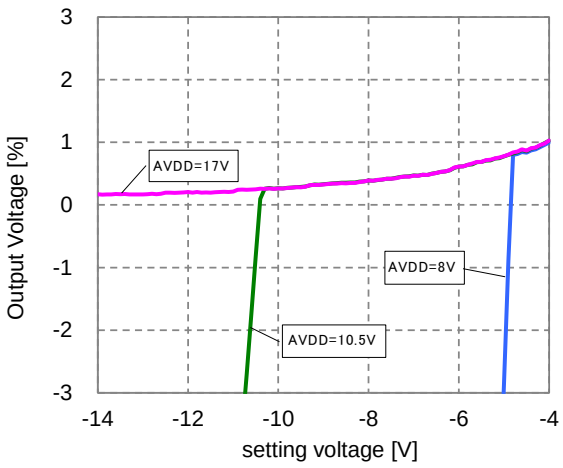

Figure 52. Output voltage accuracy
(VGL, dependent on input voltage)

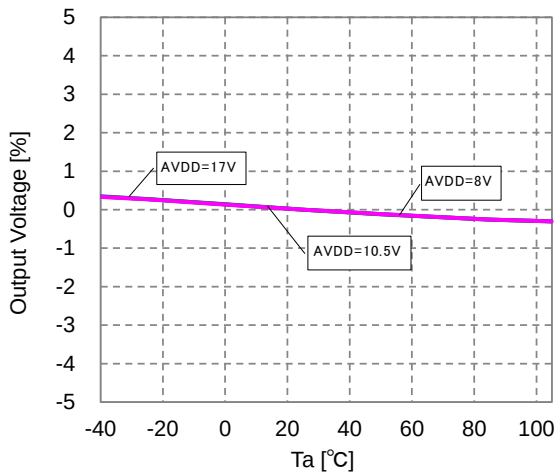

Figure 53. Output voltage accuracy
(VGL, dependent on temperature)

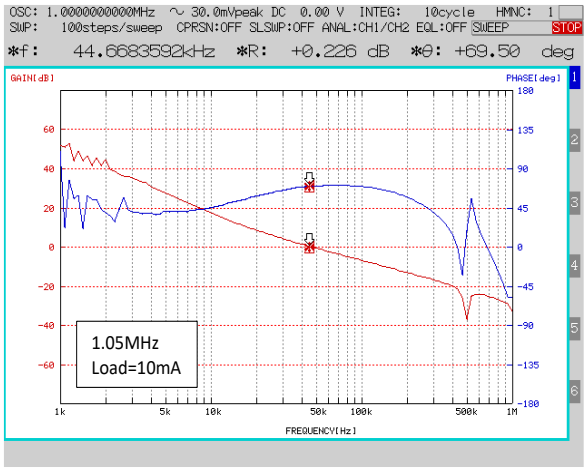

Figure 54. Phase margin
(VGL)

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

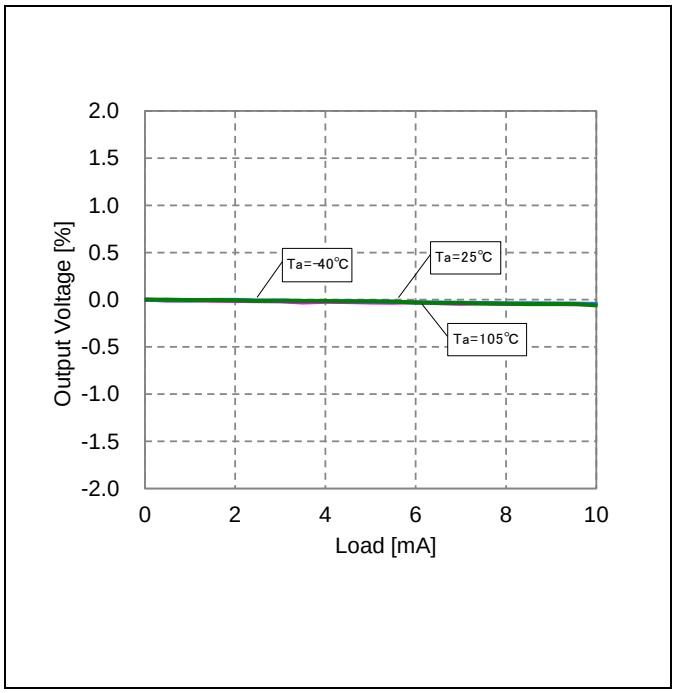

Figure 55. Load Regulation
(VGL)

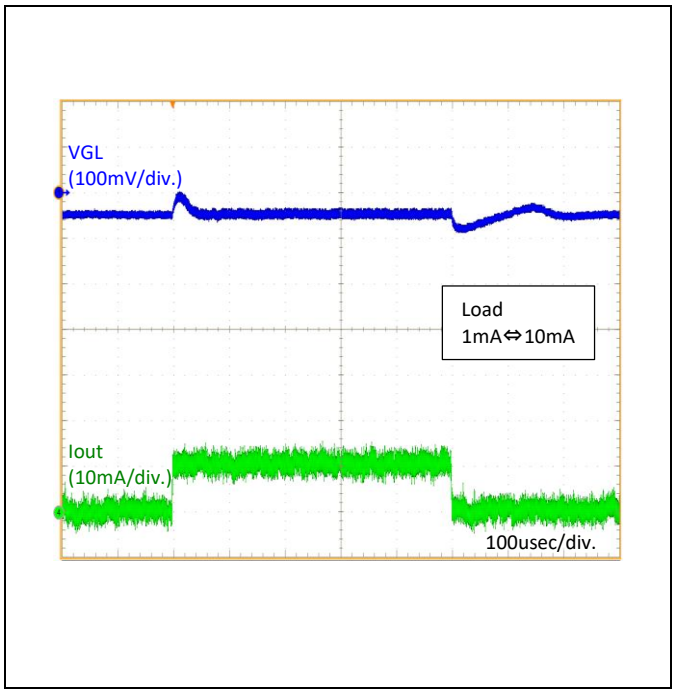

Figure 56. Load Transient
(VGL)

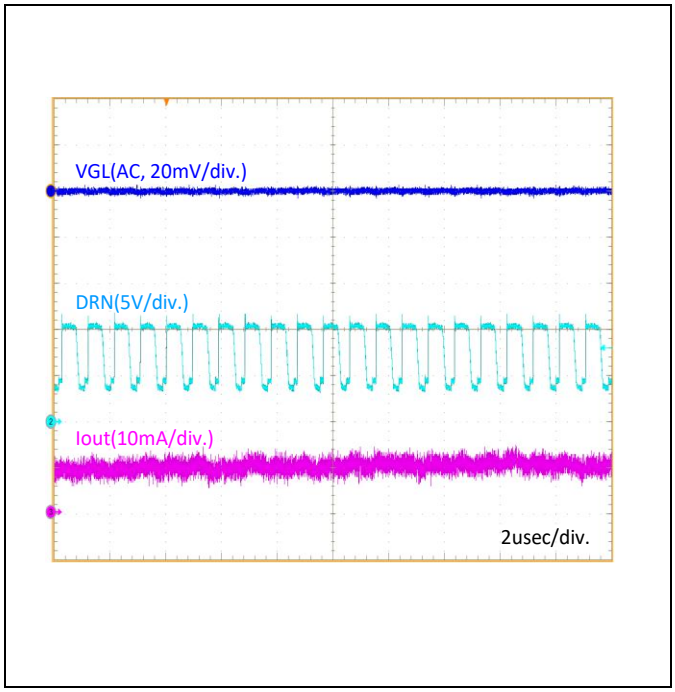

Figure 57. Switching waveform
(VGL)

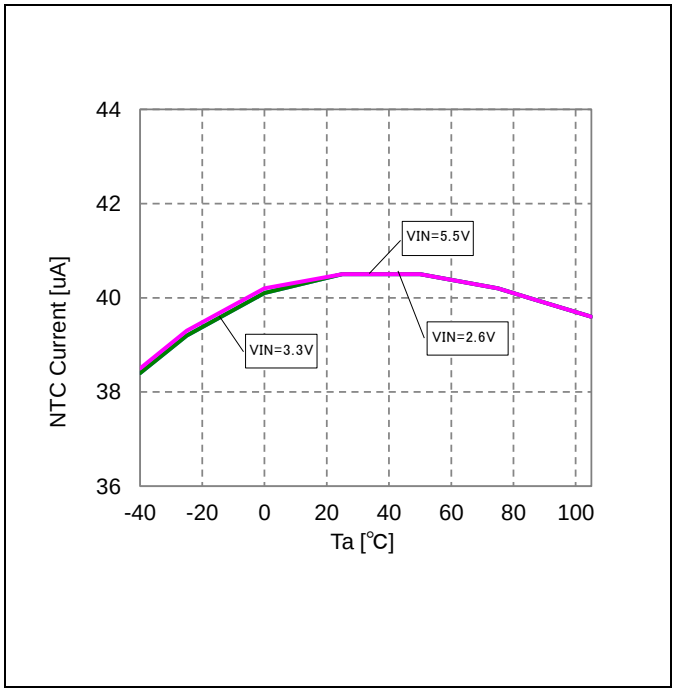

Figure 58. NTC current

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Typical Performance Curves - continued
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C)

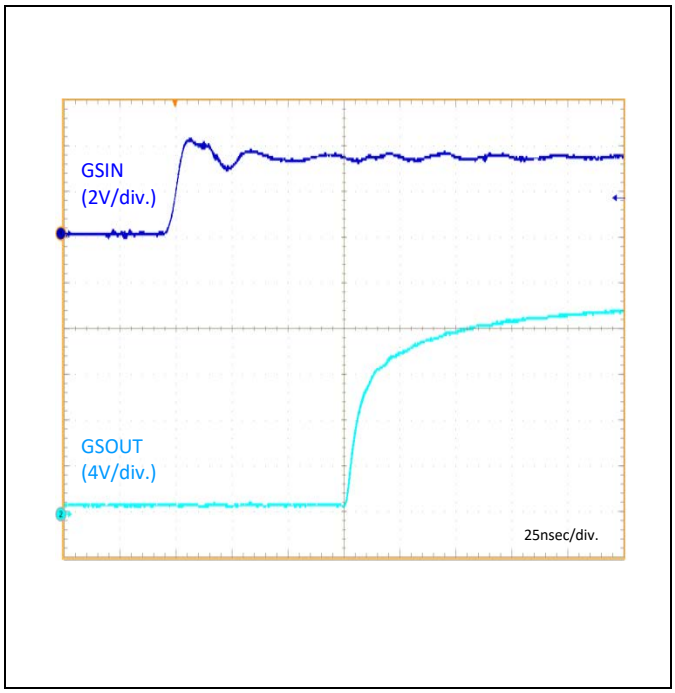

Figure 59. Propagation Delay
(GPM, rise)

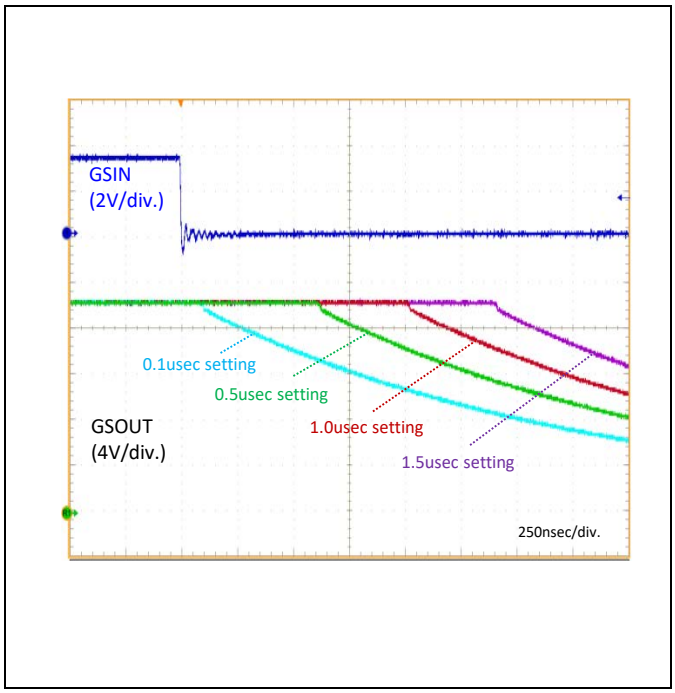

Figure 60. Propagation Delay
(GPM, fall)

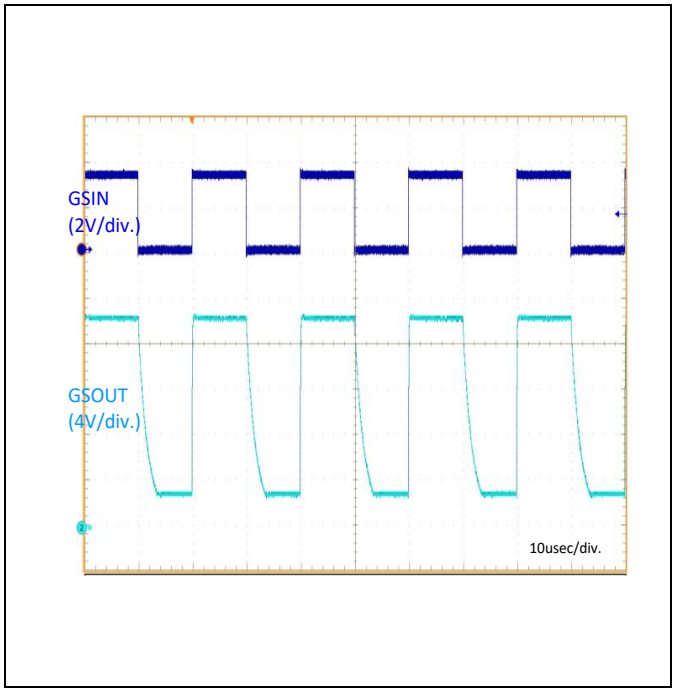

Figure 61. Waveform
(GPM)

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Application Example 1 (when operated by EN control)

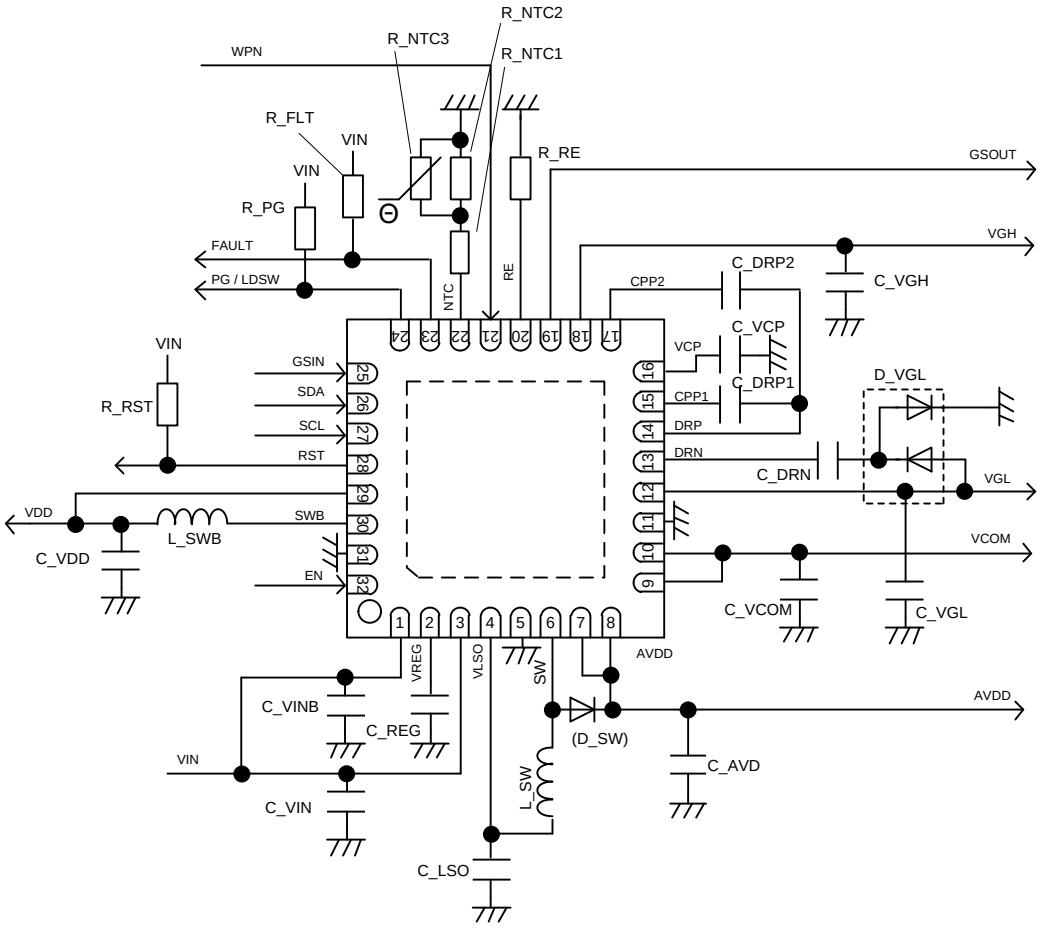

Figure 62. Application Circuit
(Function Select = PG)

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Application Example 1 (when operated by EN control) – continued

Application circuit components list
(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V)

Parts name	Value			Unit	Company	Parts Number	Comment
	Min *(Note 1)*	Typ	Max				
C_VIN	10	10 x 2	-	µF	MURATA	GRT21BC81A106KE01	
C_VINB	4.7	10	-	µF	MURATA	GRT21BC81A106KE01	No need @ VDD LDO mode
C_REG	0.047	0.1	0.47	µF	MURATA	GRT188R71H104KE13	
C_LSO	10	10 x 2	-	µF	MURATA	GRT21BC81A106KE01	
C_AVD	5.0	10 x 3	10 x 6	µF	MURATA	GRT31CC81E106KE01	See p.49 in detail.
L_SW	-	4.7	-	µH	TDK	LTF5022T-4R7N2R0-H	See p.49 in detail.
D_SW	-	-	-	-	ROHM	(RB060M-30DD)	Please insert D_SW when improving the efficiency is necessary.
C_VDD	10	10 x 2	47	µF	MURATA	GRT21BC81A106KE01	
L_SWB	-	4.7	-	µH	TDK	LTF5022T-4R7N2R0-H	
C_VCOM	-	-	-	µF	MURATA	-	
C_VGL	0.47	1.0	4.7	µF	MURATA	GRT21BC81E105KE13	
C_DRN	-	0.1	-	µF	MURATA	GRT188R71H104KE13	
D_VGL		-		-	ROHM	RB558WFH	
C_VGH	0.47	2.2	4.7	µF	MURATA	GRT21BC8YA225KE13	
C_CPP1	-	0.1	-	µF	MURATA	GRT188R71H104KE13	
C_VCP	-	1.0	-	µF	MURATA	GRT188C81E105KE13	
C_CPP2	-	0.1	-	µF	MURATA	GRT188R71H104KE13	
R_RE	0.2	2.0	-	kΩ	ROHM	MCR03	
R_NTC1	-	4.7	-	kΩ	ROHM	MCR03	
R_NTC2	-	33	-	kΩ	ROHM	MCR03	
R_NTC3	-	10	-	kΩ	MURATA	NCU18XH103F6SRB	
R_FLT	47	100	200	kΩ	ROHM	MCR03	
R_PG	47	100	200	kΩ	ROHM	MCR03	
R_RST	47	100	200	kΩ	ROHM	MCR03	

*(Note 1)*Please set in consideration of temperature properties and DC bias properties not to become less than the minimum.
Please consider it based on enough evaluations with the actual model.

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Application Example 1 (when operated by EN control) – continued
Timing Chart1

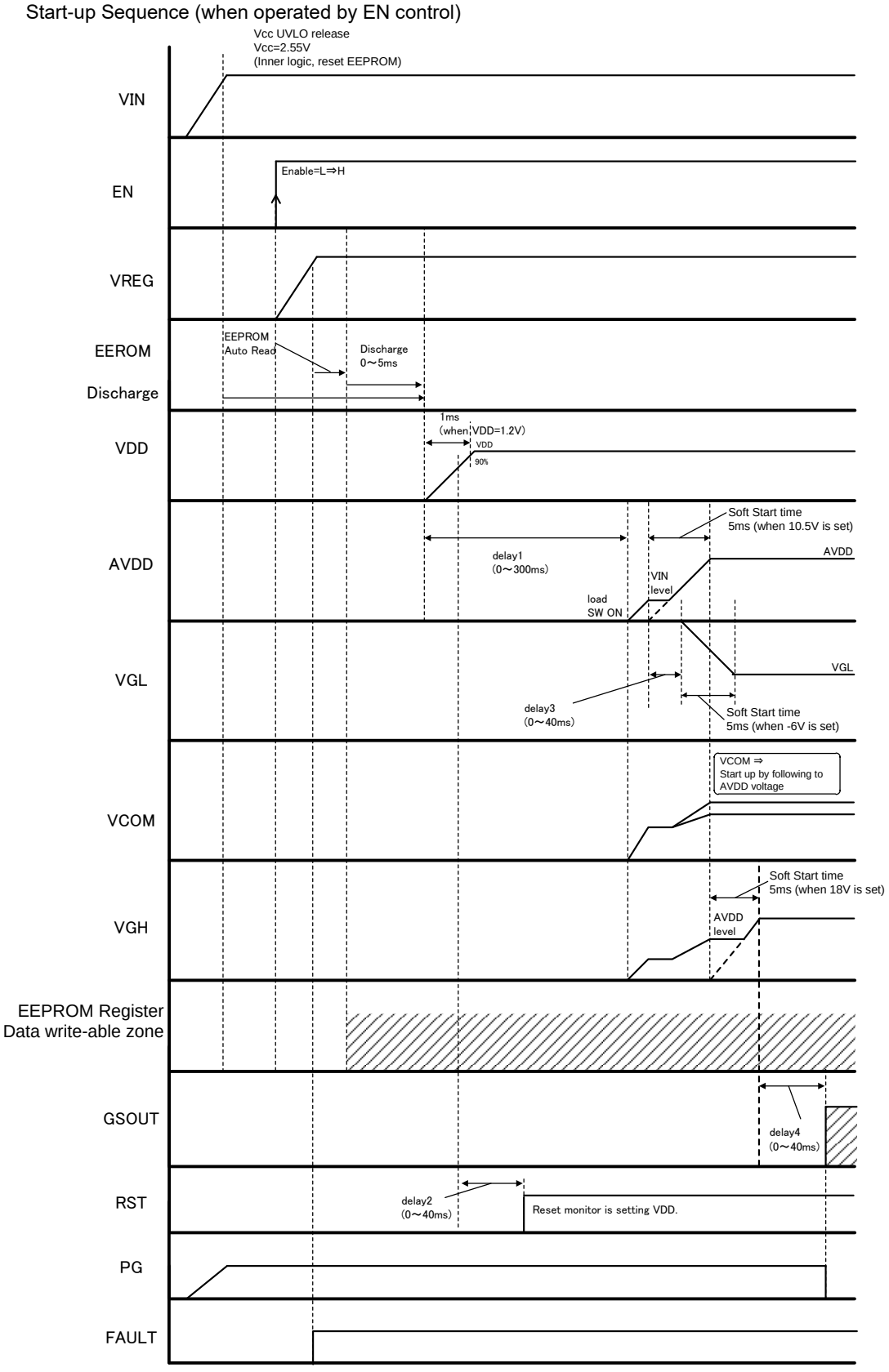

Figure 63. Start-Up Sequence Diagram (when operated by EN control)

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Application Example 1 (when operated by EN control) – continued

OFF Sequence (when operated by EN control)

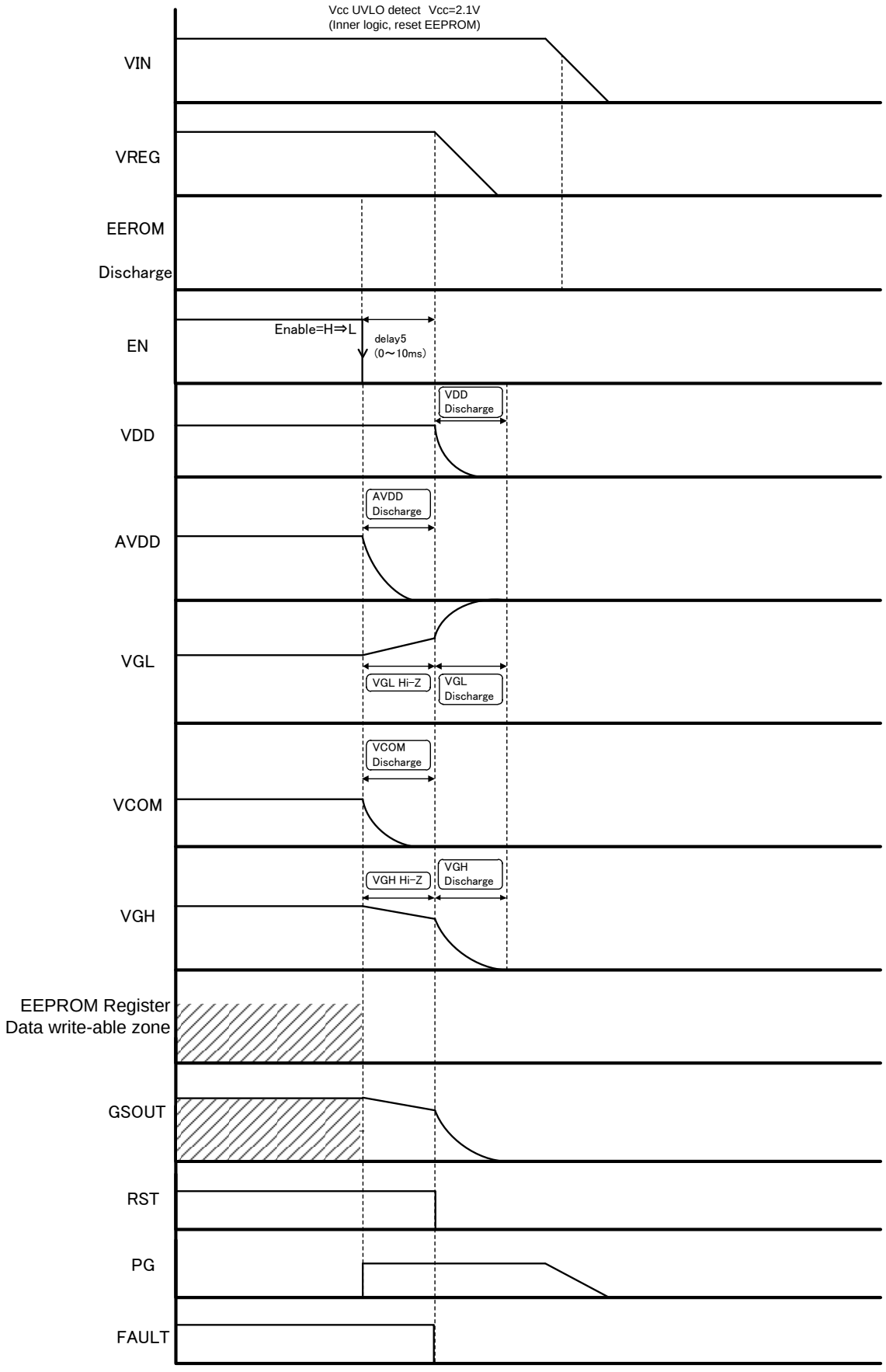

Figure 64. OFF Sequence Block (when operated by EN control)

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Application Example 2 (when operated with EN= VCC condition)
Timing Chart2

Start-up Sequence (when operated with EN= VCC condition)

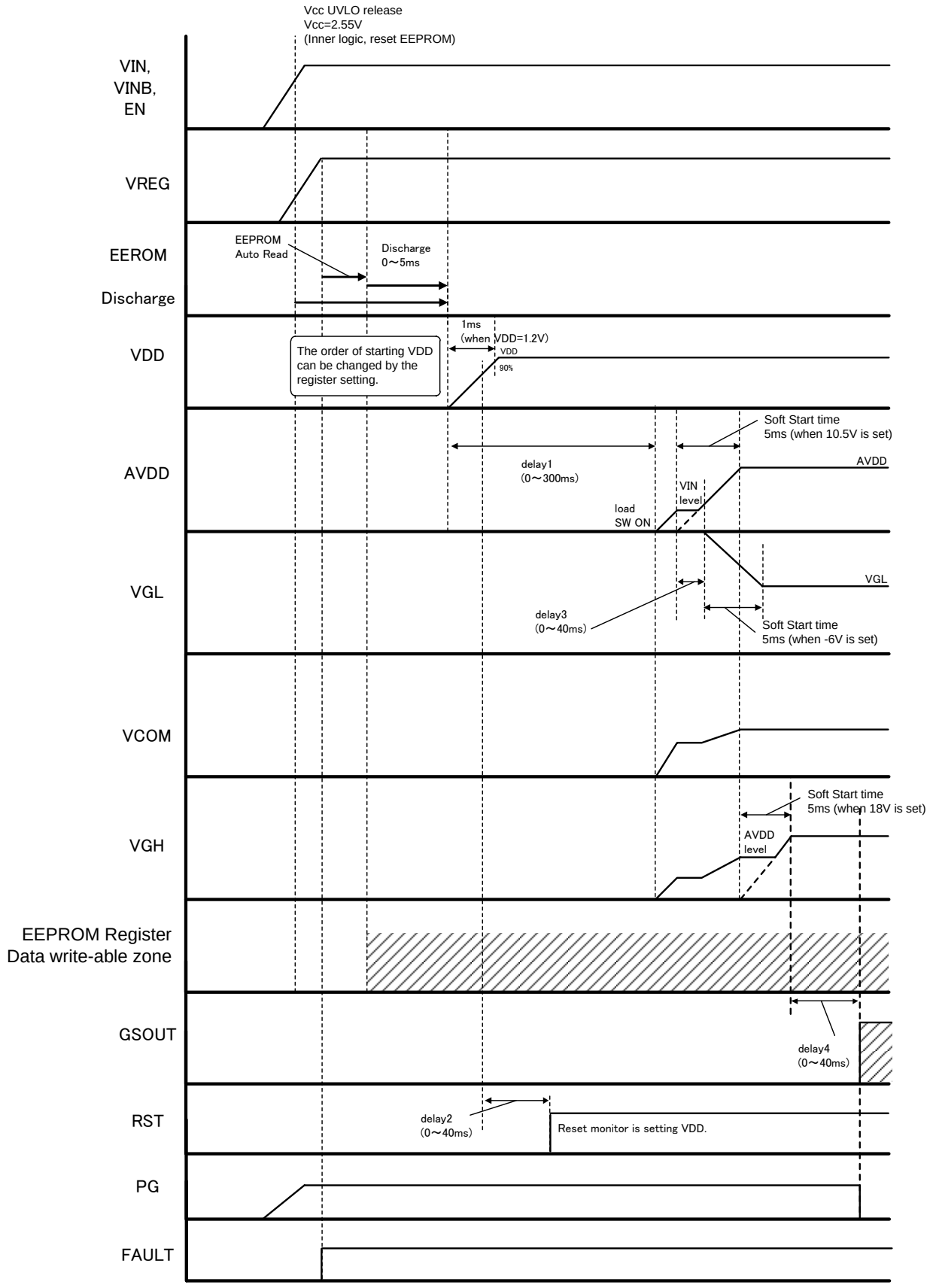

Figure 65. Start-Up Sequence Diagram (when operated with EN= VCC condition)

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Timing Chart2 - continued

OFF Sequence (when operated with EN= VCC condition)

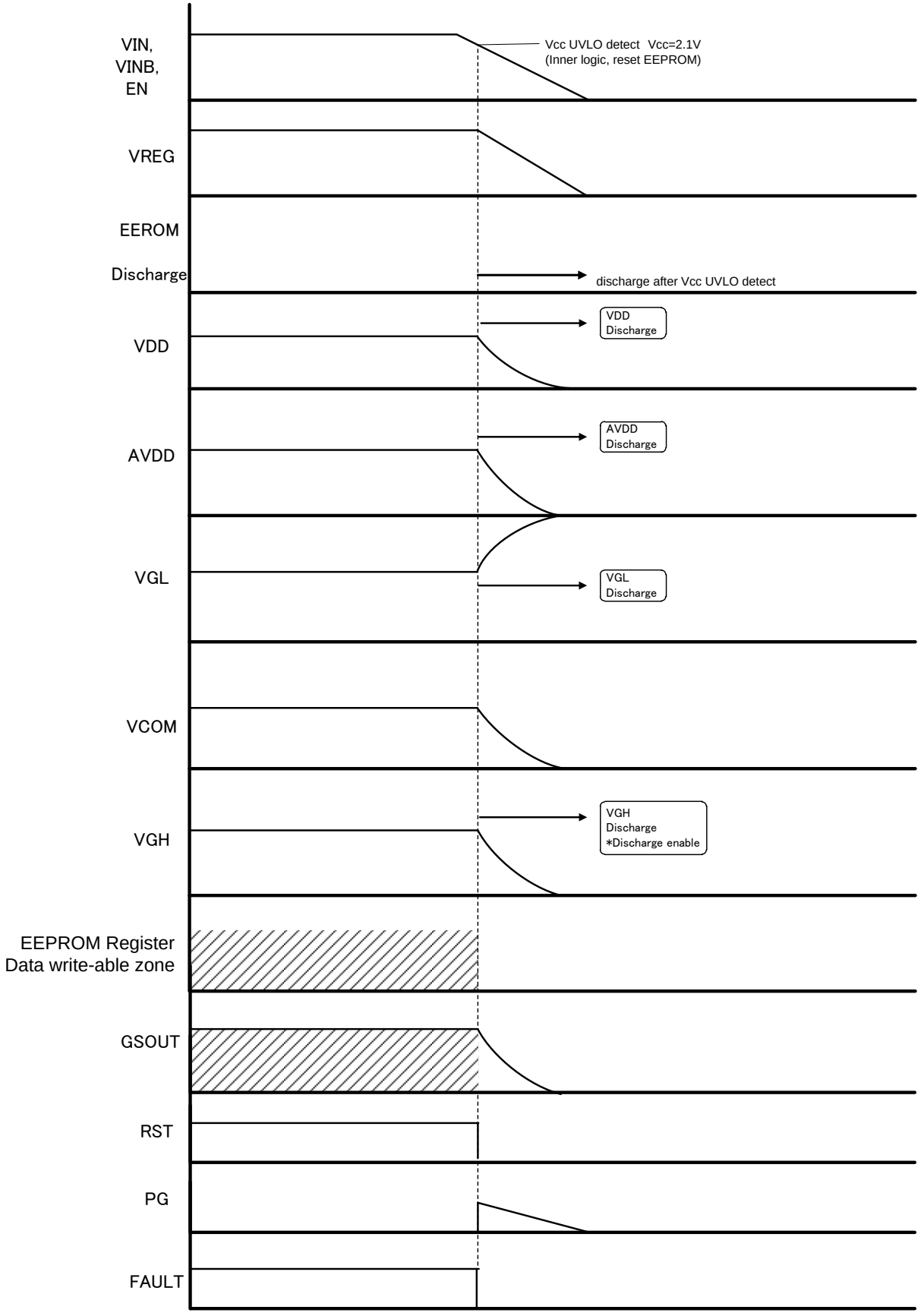

Figure 66. OFF Sequence Diagram (when operated with EN= VCC condition)

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Application Example 3 (using LDSW mode)

In case of activating in order of VGL => AVDD => VGH, changing the application contracture to following make is possible. In this case please set Register08h (Function Select) of the EEPROM to "1".

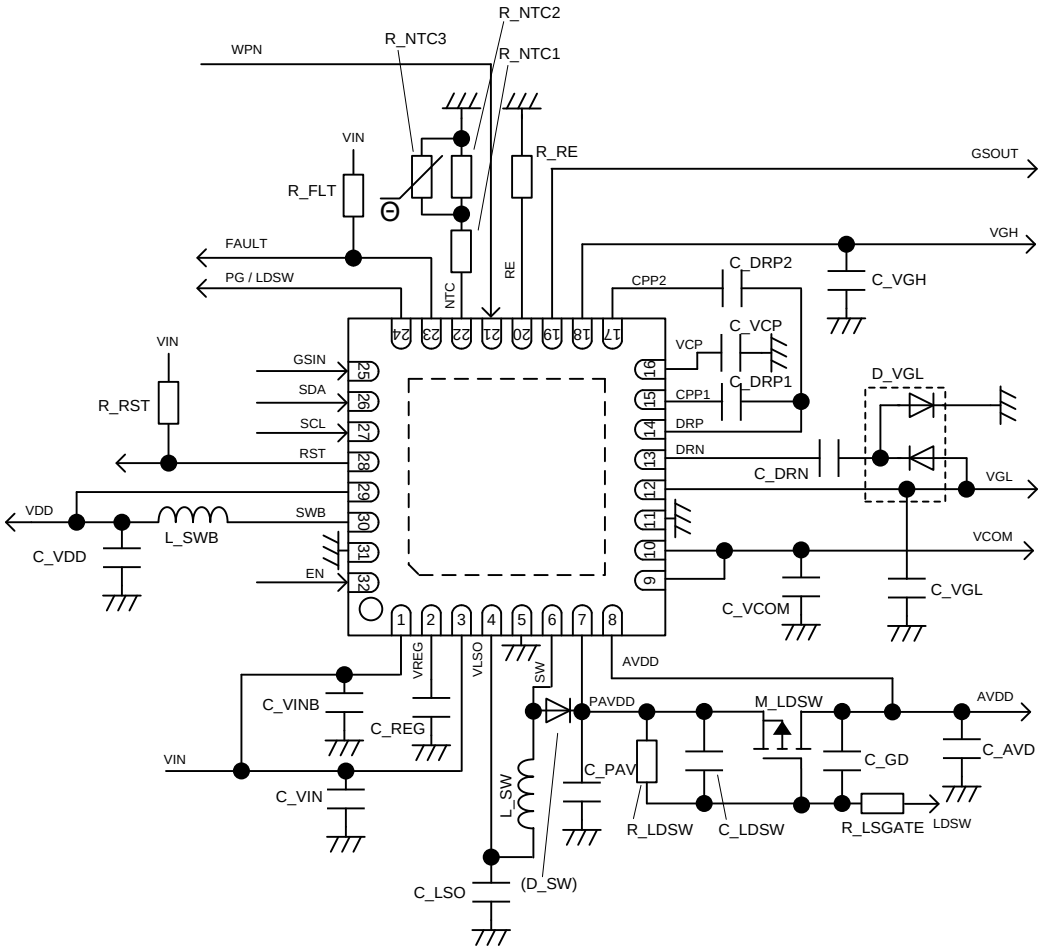

Figure 67. Application Circuit
(Function Select = LDSW)

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Application Example 3 (using LDSW mode) - continued

Application circuit components list

(Unless otherwise specified VIN=3.3V, VDD=2.5V, AVDD=10.5V, VGH=18V, VGL=-6.0V, VCOM=5.25V and Ta=25°C**)**

Parts name	Value			Unit	Company	Parts Number	Comment
	Min *(Note 1)*	Typ	Max				
C_VIN	10	10 x 2	-	µF	MURATA	GRT21BC81A106KE01	
C_VINB	4.7	10	-	µF	MURATA	GRT21BC81A106KE01	No need @ VDD LDO mode
C_REG	0.047	0.1	0.47	µF	MURATA	GRT188R71H104KE13	
C_LSO	10	10 x 2	-	µF	MURATA	GRT21BC81A106KE01	
C_PAVD	5.0	10 x 2	10 x 5	µF	MURATA	GRT31CC81E106KE01	See p.49 in detail.
C_AVD	2.2	4.7	10	µF	MURATA	GRT31CC81E475KE01	See p.49 in detail.
L_SW	-	4.7	-	µH	TDK	LTF5022T-4R7N2R0-H	See p.49 in detail.
D_SW	-	-	-	-	ROHM	(RB060M-30DD)	Please insert D_SW when improving the efficiency is necessary.
M_LDSW	-	-	-	-	ROHM	RTR030P02FHA	
R_LDSW	-	100	-	kΩ	ROHM	MCR03	
C_LDSW	-	0.47	-	µF	MURATA	GRT21BR71H474KE01	
C_GD	-	33	-	nF	MURATA	GRT155R71H333KE01	
R_LSGATE	-	100	-	kΩ	ROHM	MCR03	
C_VDD	10	10 x 2	47	µF	MURATA	GRT21BC81A106KE01	
L_SWB	-	4.7	-	µH	TDK	LTF5022T-4R7N2R0-H	
C_VCOM	-	-	-	µF	MURATA	-	
C_VGL	0.47	1.0	4.7	µF	MURATA	GRT21BC81E105KE13	
C_DRN	-	0.1	-	µF	MURATA	GRT188R71H104KE13	
D_VGL		-		-	ROHM	RB558WFH	
C_VGH	0.47	2.2	4.7	µF	MURATA	GRT21BC8YA225KE13	
C_CPP1	-	0.1	-	µF	MURATA	GRT188R71H104KE13	
C_VCP	-	1.0	-	µF	MURATA	GRT188C81E105KE13	
C_CPP2	-	0.1	-	µF	MURATA	GRT188R71H104KE13	
R_RE	0.2	2.0	-	kΩ	ROHM	MCR03	
R_NTC1	-	4.7	-	kΩ	ROHM	MCR03	
R_NTC2	-	33	-	kΩ	ROHM	MCR03	
R_NTC3	-	10	-	kΩ	MURATA	NCU18XH103F6SRB	
R_FLT	47	100	200	kΩ	ROHM	MCR03	
R_RST	47	100	200	kΩ	ROHM	MCR03	

*(Note 1)*Please set in consideration of temperature properties and DC bias properties not to become less than the minimum.
Please consider it based on enough evaluations with the actual model.

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Timing Chart3

Start-up Sequence (when operated with LDSW function)

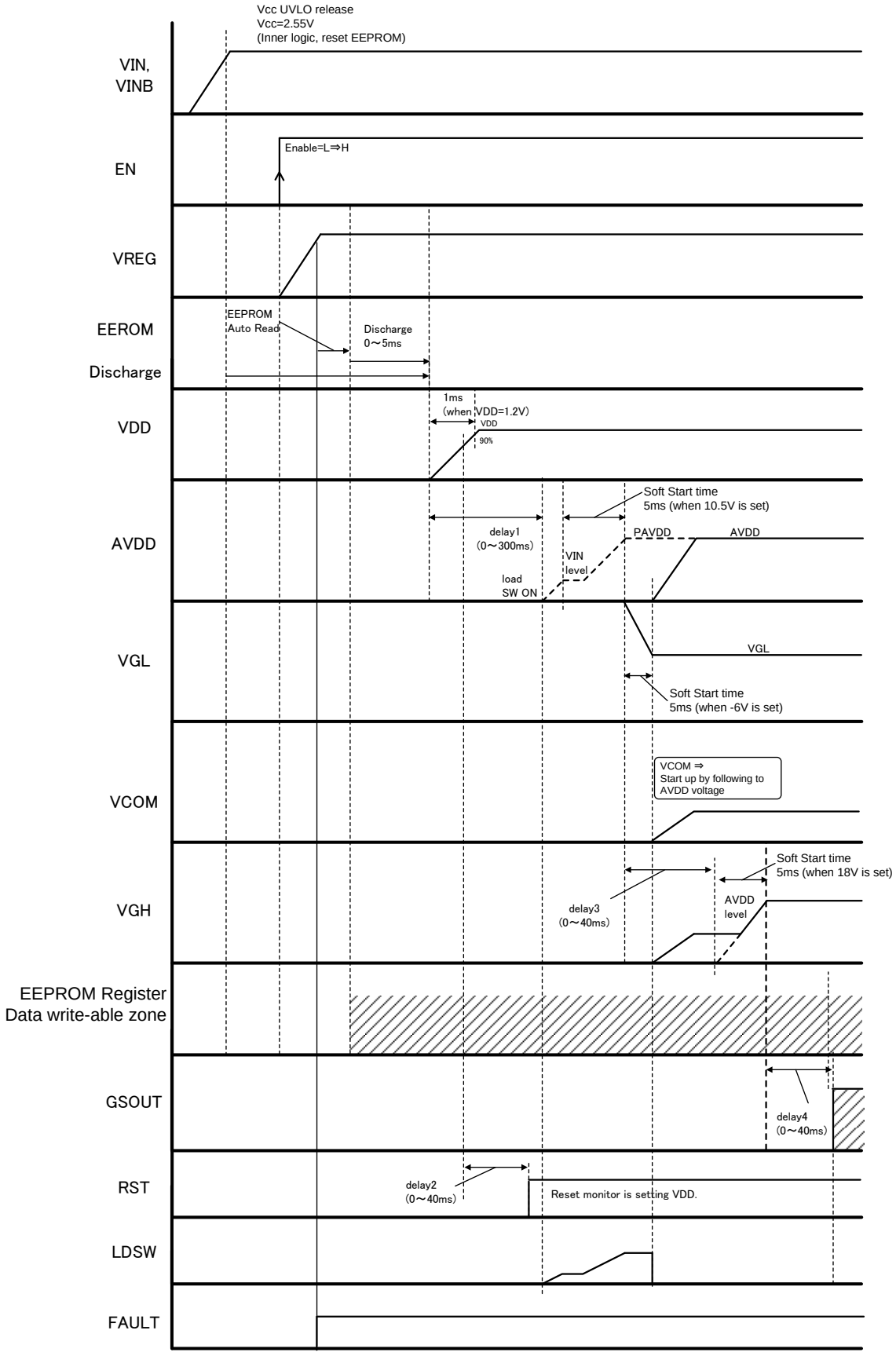

Figure 68. Start-Up Sequence Diagram (when operated with LDSW Function)

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Timing Chart3 - continued

OFF Sequence (when operated with LDSW function)

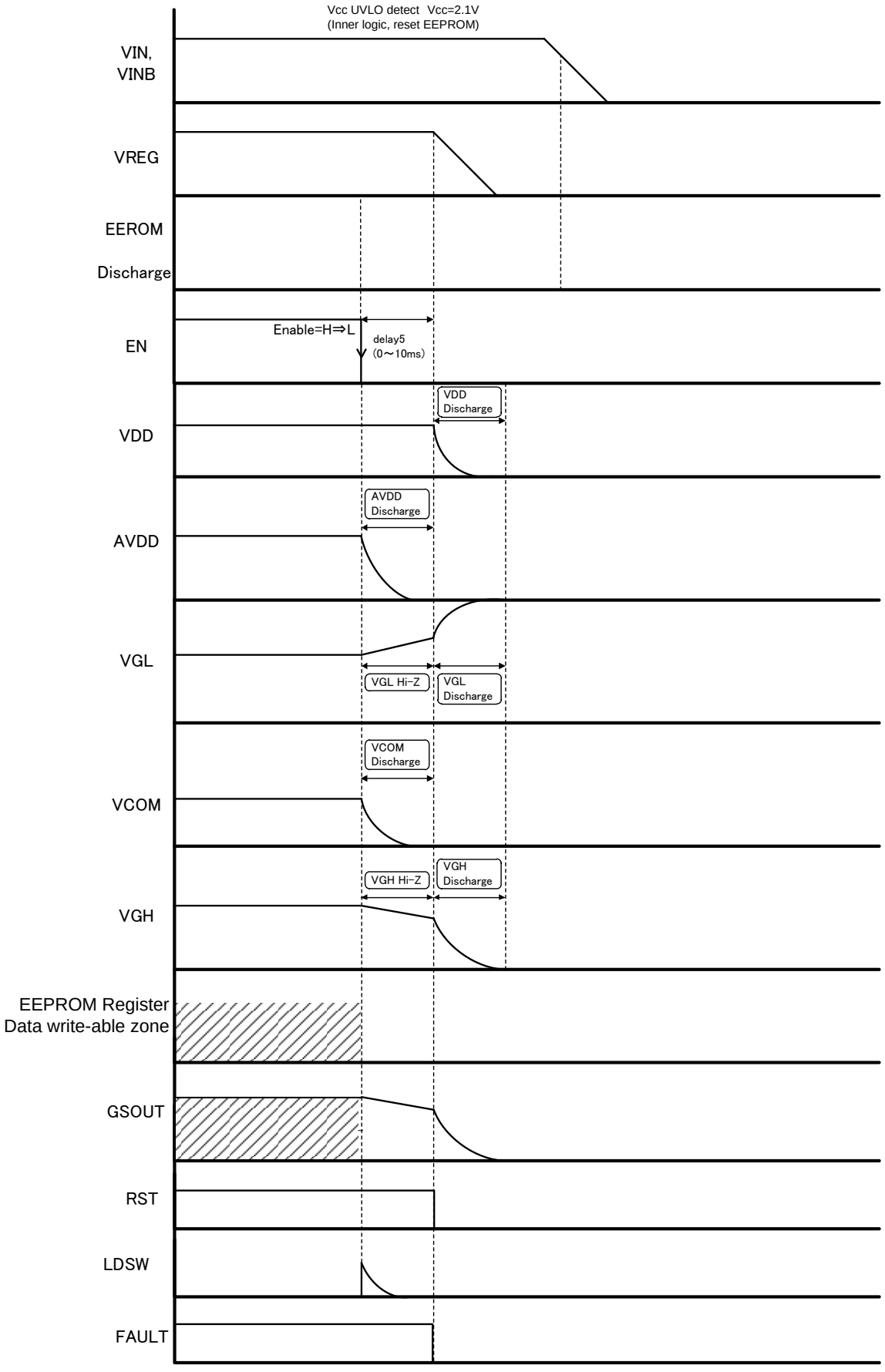

Figure 69. OFF Sequence Diagram (when operated with LDSW Function)

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Serial communication

This IC has two device-address-differential EEPROM installed and data is send or received to/from EEPROM using 2-line serial interface (SCL, SDA). Communication format for data sending or receiving to/from each EEPROM is shown below.

EEPROM I2C Format for DVR (VCOM calibrator)

Write operation	Start	Device address							R/W	ACK	DATA								ACK	STOP
		1	0	0	1	1	1	1	0	0	D6	D5	D4	D3	D2	D1	D0	P	0	
Read operation	Start	Device address							R/W	ACK	DATA								ACK	STOP
		1	0	0	1	1	1	1	1	0	D6	D5	D4	D3	D2	D1	D0	X	1	

When Device Address = 1001111(R/W) is selected, Data is Read or Write EEPROM for DVR(VCOM calibrator).

During Write mode
•When P=1, the sending data is written only to Register.
•When WPN=Low and P=0, the sending data is written only to Register.
•When WPN=High and P=0, the sending data is written both to Register and EEPROM.

During Read mode
The last bit of received data is “Don’t care”.

“D6” is ± select bit: 0 = “+”, 1=”-” from VCOM(HOT) value.
[D5:D0] are voltage band from VCOM(HOT).
The voltage band is calculated; 10mV x [D5:D0],

For example,
[D6:D0,P] = 82h(D6=1, [D5:D0]=1’d, P=0) ••• VCOM = VCOM(HOT) – 1 x 10mV;
[D6:D0,P] = 7Eh(D6=0, [D5:D0]=63’d, P=0) ••• VCOM = VCOM(HOT) + 63 x 10mV;

Sequence of DVR side EEPROM during Read/Write mode is shown in below chart.

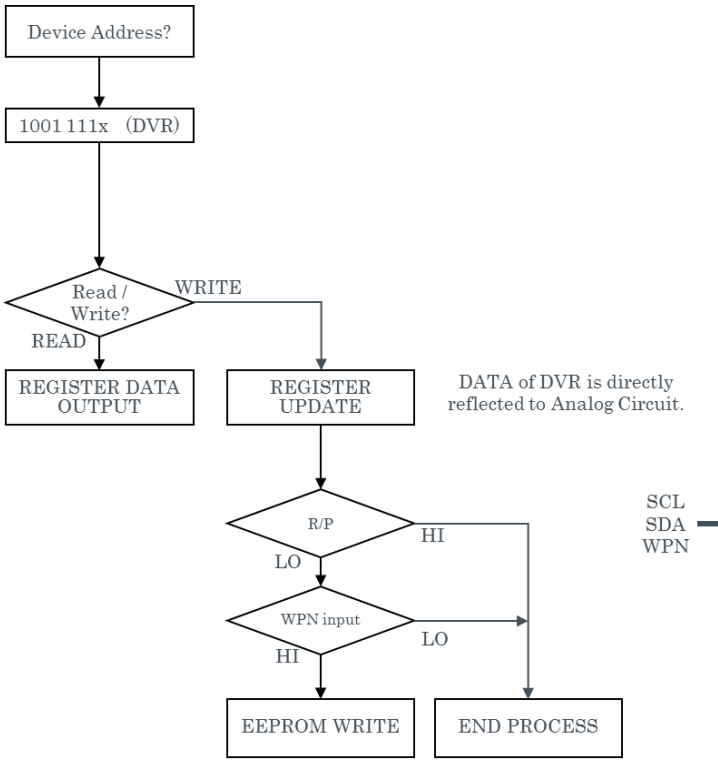

Figure 70

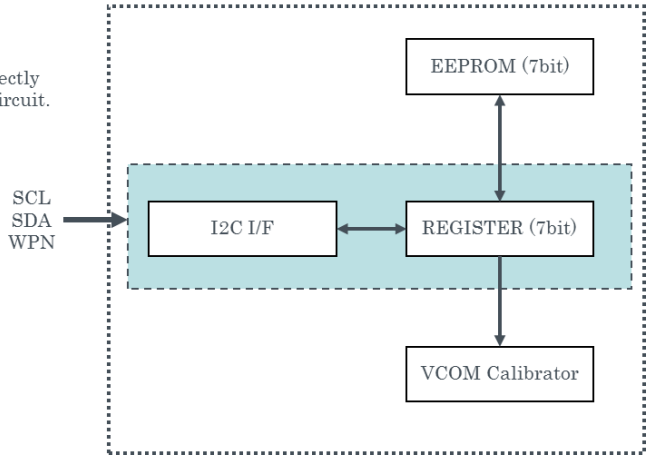

Figure 71

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Serial communication - continued

EEPROM I2C Format for Power Management IC (PMIC)

Write operation	Start	Device address							R/W	ACK	Register Address	ACK	N-bytes Data																			ACK	Stop
		1	0	0	0	0	0	0	0	0	00h ～ 0Dh, 10h, 11h	0																			0	
Read operation	Start	Device address							R/W	ACK	Register Address	ACK	Repeated Start	Device Address								ACK	N-bytes Data									ACK	Stop
		1	0	0	0	0	0	0	0	0	00h ～ 0Dh, 10h, 11h	0		1	0	0	0	0	0	0	1	0									1	

Device Address of BM81810MUV-M is 1000 000x.
Multi write is possible until Register 00h to 0Dh.

	EN	WPN	Start-up(0Ch[7])	PMIC (00h to 0Dh)	Output Function
1	Low	Low	-	-	Shutdown
2	High	Low	-	Register	Active
3	High	High	0*	Register & EEPROM	Shutdown
4	High	High	1	Register & EEPROM	Active

* In the mass production shipment process, please write Start-up (0Ch[7]) to "1" in EEPROM.

The following are the settings if you want to send the Data by I2C.

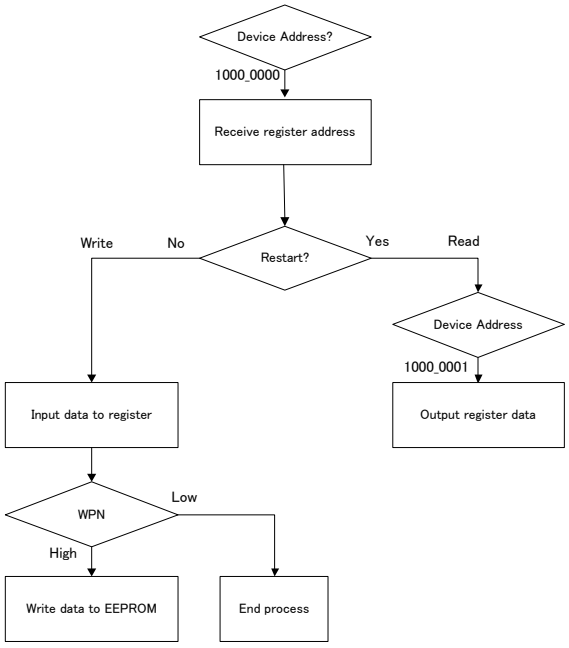

Figure 72

WPN Timing

WPN is normally fixed as Low.
In case of writing to EEPROM, WPN is set to High, and the timing will be as below.
Because the maximum of the auto-read time from EEPROM is 5ms, please between EN signal and I2C input than 5ms.
Also, because the maximum of writing time to EEPROM is 50ms, please between I2C STOP signal and EN falling signal than 50ms.

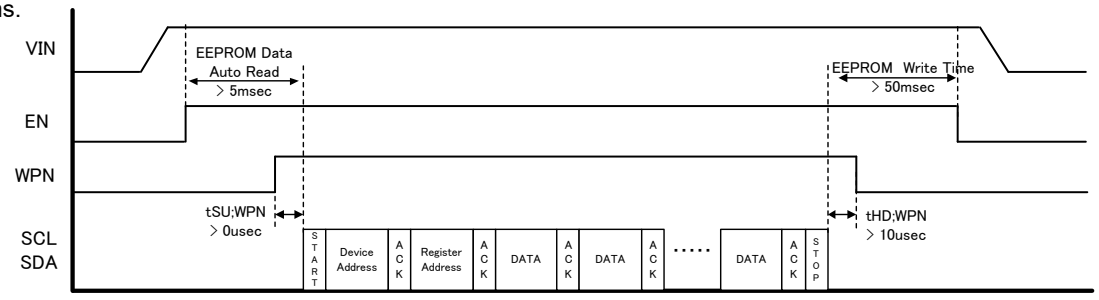

Figure 73

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I2C Timing Diagram

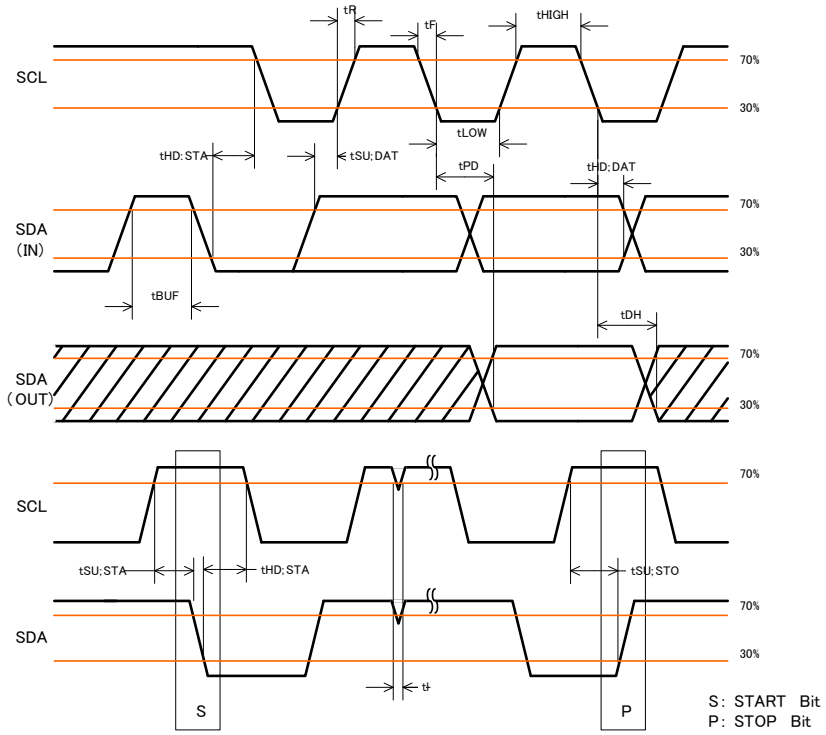

Figure 74. I2C Timing Diagram

Timing standard values

Parameter	Symbol	NORMAL MODE			FAST MODE			Unit
		Min	Typ	Max	Min	Typ	Max	
SCL frequency	fSCL	-	-	100	-	-	400	kHz
SCL high time	tHIGH	4.0	-	-	0.6	-	-	µs
SCL low time	tLOW	4.7	-	-	1.2	-	-	µs
Rise Time	tR	-	-	1.0	-	-	0.3	µs
Fall Time	tF	-	-	0.3	-	-	0.3	µs
Start condition hold time	tHD;STA	4.0	-	-	0.6	-	-	µs
Start condition setup time	tSU;STA	4.7	-	-	0.6	-	-	µs
SDA hold time	tHD;DAT	0	-	-	0	-	-	ns
SDA setup time	tSU;DAT	200	-	-	100	-	-	ns
Acknowledge delay time	tPD	-	-	0.9	-	-	0.9	µs
Acknowledge hold time	tDH	-	0.1	-	-	0.1	-	µs
Stop condition setup time	tSU;STO	4.0	-	-	0.6	-	-	µs
Bus release time	tBUF	4.7	-	-	1.2	-	-	µs
Noise spike width	TI	-	0.1	-	-	0.1	-	µs

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Automatic EEPROM Read Function at Start-up

Upon BM81810MUV-M start-up, a reset signal is generated and each register is initialized.
After VREG activation is finished, data which is stored in the EEPROM is copied to the registers.
The automatic EEPROM read function at start-up is further explained by the flow chart below.

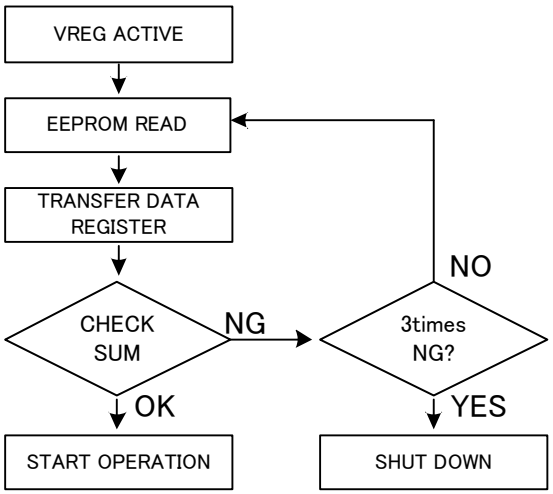

Figure 75. Automatic EEPROM Read Function at Start-up

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EEPROM Parameter Setting

■EEPROM / Main Register Map (device address : 1000000x)

Device Address: 1000000x (PMIC)

Register Address	Bits	Function	Resolution	Comments
00h	8	AVDD Output voltage	0.1V [5.0V to 17.0V]	AVDD Output voltage setting
01h	8	VGH(HOT) Output voltage	0.2V [8.0V to 35.0V]	VGH(HOT) Output voltage setting
02h	8	ΔVGH(COLD) Voltage [6:0]	0.2V [VGH(HOT) + 15V]	
		VGH NTC Enalbe [7]	0:Disable, 1:Enable	
03h	8	VGL Output voltage	0.1V [-14.0V to -4.0V]	VGL Output voltage setting
04h	8	VCOM(HOT) Output voltage	40mV [0.5xAVDD ±4.0V]	VCOM(HOT) Output voltage setting
05h	8	ΔVCOM(COLD) Voltage [6:0]	10mV [VCOM(HOT) - 0.63V]	
		VCOM NTC Enalbe [7]	0:Disable, 1:Enable	
06h	8	VDD Output voltage [5:0]	0.05V [0.9V to 3.4V]	VDD Output voltage setting
		VDD mode select [6]	0 : DC/DC, 1 : LDO	Select VDD operation mode DC/DC or LDO
		VDD Phase [7]	See P.56 page.	select VDD Phase
07h	8	Reset Voltage [4:0]	0.1V [0.6V to 3.3V]	Reset voltage setting
		Reset monitor select [5]	0:VDD, 1:VIN	Select monitor pin of reset function
		GPM input delay [7:6]	00: 0.1usec, 01: 0.5usec, 10: 1.0usec, 11: 1.5usec	GPM input propagation delay time setting
08h	8	Discharge time [2:0]	1msec [0 to 5msec]	Pre-discharge time setting
		Delay1 time [6:3]	[0 to 300msec]	Load switch of AVDD start-up delay time setting
		Function Select [7]	0: PG, 1: LDSW	24pin function select
09h	8	Delay2 time [2:0]	5msec [0 to 30msec, 40msec]	Reset start delay time setting
		DoubleReg [3]	0: Disable, 1: Enable	Double Register Function
		Delay3 time [6:4]	5msec [0 to 30msec, 40msec]	VGL or VGH start-up delay time setting
		DataRef [7]	0: Disable, 1: Enable	Data Refresh Function
0Ah	8	Delay4 time [2:0]	5msec [0 to 30msec, 40msec]	GPM start delay time setting
		AR_Time [3]	0: 0.5sec, 1: 1.0sec	Data Refresh Time
		Delay5 time [6:4]	2msec [0 to 10msec]	VDD stop delay time setting
		VGH Discharge enable [7]	0: Enable, 1: Disable	VGH Discharge function enable
0Bh	8	AVDD Coil[1:0]	See p.49 page.	select AVDD Coil indactance
		AVDD SW Slew Rate [3:2]	See p.48 page.	4step slew rate setting (11:fast → 00:slow)
		AVDD SS time [5:4]	5msec [5msec to 20msec]	AVDD softstart time setting
		AVDD OCP Select [6]	0: 2A, 1: 1A	AVDD OCP min value select
		AVDD COMP [7]	See p.49 page.	AVDD phase compensation setting
0Ch	8	AVDD Frequecy [1:0]	00:2.1MHz, 01:1.05MHz, 10:525KHz, 11:525KHz	Seletc AVDD switching frequency
		VDD Frequecy [3:2]	00:2.1MHz, 01:1.05MHz, 10:525KHz, 11:525KHz	Select VDD switching frequency
		VGH / VGL Frequecy [5:4]	AVDD Freqency (00: x1, 01: --, 10: --, 11: --)	Select VGH and VGL switching frequency. **Choose only "00".**
		VGH mode select [6]	0: x3 mode, 1: x2 or x4 mode	Select VGH charge pump mode
		start-up bit [7]	0:Disable, 1:Enable	

Device Address: 1001111x (VCOM)

Register Address	Bits	Function	Resolution	Comments
-	7	VCOM Calibrator	+/- 0.01V [VCOM +/- 0.63V]	VCOM Calibrator

When Start-up bit(REG0Ch[7]) is ”1”, below Register cannot be modified.

VGH NTC Enable REG02h[7]
VCOM NTC Enable REG05h[7]
VDD mode select REG06h[6]
Function select REG08h[7]
VGH mode select REG0Ch[6]

To change those Register setting, start-up bit(REG0Ch[7]) should be in ”0”.
After changing the register value, set the Start-up bit(REG0Ch[7]) to “1” again to start up with the changed setting.

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Register Map

Device Address : 1000000x (PMIC)

Register Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	AVDD Output Voltage								68h
01h	VGH HOT Output Voltage								59h
02h	VGH NTC Enable	⊿VGH COLD Voltage							83h
03h	VGL Output Voltage								3Bh
04h	VCOM HOT Output Voltage								80h
05h	VCOM NTC Enable	⊿VCOM COLD Votlage							99h
06h	VDD Phase Select	VDD MODE	VDD Output Voltage						20h
07h	GPM Input Delay		Reset Monitor Select	Reset Voltage					04h
08h	Function Select	Delay1 time				Discharge time			09h
09h	Data Refresh	Delay3 time			DoubleReg	Delay2 time			13h
0Ah	VGH Discharge Enable	Delayt5 time			AR_Time	Delay4 time			87h
0Bh	AVDD COMP	AVDD OCP Select	AVDD SS Time		AVDD SW Slew Rate		AVDD Coil Select		3Ch
0Ch	Start-up Bit	VGH mode select	VGH/VGL Frequency		VDD Frequency		AVDD Frequency		05h
0Dh	Check Sum								60h
10h	**AVDD UVP**	**VDD UVP**	**VGH UVP**	**VGL UVP**	**Double Register Error**	**AVDD OCP**	**TSD**	**Check sum Error**	00h

Device Address : 1001111x (VCOM)

Register Address	D6	D5	D4	D3	D2	D1	D0	P	Default
-	VCOM Calibration Voltage							P	80h

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Register Map - continued

Command Table

	Regitser Address																	
	00h	01h	02h		03h	04h	05h		06h			07h			08h			
DATA (HEX)	AVDD Output Voltage [7:0]	VGH HOT Output Voltage [7:0]	VGH NTC Enable [7]	⊿VGH COLD Voltage [6:0]	VGL Output Voltage [7:0]	VCOM HOT Output Voltage [7:0]	VCOM NTC Enable [7]	⊿VCOM COLD Voltage [6:0]	VDD Phase [7]	VDD MODE [6]	VDD Output Voltage [5:0]	GPM Input Delay [7:6]	Reset Monitor Selecet [5]	Reset Voltage [4:0]	Function Select [7]	Delay1 time [6:3]	Discharge time [2:0]
00h				+0.0V		AVDD/2		-0.00V			0.90 V			0.6 V			0 msec
01h				+0.2V		AVDD/2 +0.04V		-0.01V			0.95 V			0.7 V			1 msec
02h				+0.4V		AVDD/2 +0.08V		-0.02V			1.00 V			0.8 V			2 msec
03h				+0.6V		AVDD/2 +0.12V		-0.03V			1.05 V			0.9 V		0 msec	3 msec
04h				+0.8V		AVDD/2 +0.16V		-0.04V			1.10 V			1.0 V			4 msec
05h				+1.0V		AVDD/2 +0.20V		-0.05V			1.15 V			1.1 V			
06h				+1.2V		AVDD/2 +0.24V		-0.06V			1.20 V			1.2 V			5 msec
07h				+1.4V		AVDD/2 +0.28V		-0.07V			1.25 V			1.3 V			
08h				+1.6V		AVDD/2 +0.32V		-0.08V			1.30 V			1.4 V			0 msec
09h				+1.8V		AVDD/2 +0.36V		-0.09V			1.35 V			1.5 V			1 msec
0Ah				+2.0V		AVDD/2 +0.40V		-0.10V			1.40 V			1.6 V			2 msec
0Bh				+2.2V		AVDD/2 +0.44V		-0.11V			1.45 V			1.7 V		5 msec	3 msec
0Ch				+2.4V		AVDD/2 +0.48V		-0.12V			1.50 V			1.8 V			4 msec
0Dh				+2.6V		AVDD/2 +0.52V		-0.13V			1.55 V			1.9 V			
0Eh				+2.8V		AVDD/2 +0.56V		-0.14V			1.60 V			2.0 V			5 msec
0Fh				+3.0V		AVDD/2 +0.60V		-0.15V			1.65 V		VDD	2.1 V			
10h				+3.2V		AVDD/2 +0.64V		-0.16V			1.70 V			2.2 V			0 msec
11h				+3.4V		AVDD/2 +0.68V		-0.17V			1.75 V			2.3 V			1 msec
12h				+3.6V		AVDD/2 +0.72V		-0.18V			1.80 V			2.4 V			2 msec
13h		8.0 V		+3.8V	-4.0 V	AVDD/2 +0.76V		-0.19V			1.85 V			2.5 V			3 msec
14h				+4.0V		AVDD/2 +0.80V		-0.20V			1.90 V			2.6 V		10 msec	4 msec
15h				+4.2V		AVDD/2 +0.84V		-0.21V			1.95 V			2.7 V			
16h				+4.4V		AVDD/2 +0.88V		-0.22V			2.00 V			2.8 V			5 msec
17h				+4.6V		AVDD/2 +0.92V		-0.23V			2.05 V			2.9 V			
18h				+4.8V		AVDD/2 +0.96V		-0.24V			2.10 V			3.0 V			0 msec
19h	5.0 V			+5.0V		AVDD/2 +1.00V		-0.25V			2.15 V			3.1 V			1 msec
1Ah				+5.2V		AVDD/2 +1.04V		-0.26V			2.20 V			3.2 V			2 msec
1Bh				+5.4V		AVDD/2 +1.08V		-0.27V			2.25 V					15 msec	3 msec
1Ch				+5.6V		AVDD/2 +1.12V		-0.28V			2.30 V						4 msec
1Dh				+5.8V		AVDD/2 +1.16V		-0.29V			2.35 V			3.3 V			
1Eh				+6.0V		AVDD/2 +1.20V		-0.30V			2.40 V						5 msec
1Fh				+6.2V		AVDD/2 +1.24V		-0.31V		DC/DC	2.45 V	0.1 usec					
20h				+6.4V		AVDD/2 +1.28V		-0.32V			2.50 V			0.6 V			0 msec
21h				+6.6V		AVDD/2 +1.32V		-0.33V			2.55 V			0.7 V			1 msec
22h				+6.8V		AVDD/2 +1.36V		-0.34V			2.60 V			0.8 V			2 msec
23h				+7.0V		AVDD/2 +1.40V		-0.35V			2.65 V			0.9 V		20 msec	3 msec
24h				+7.2V		AVDD/2 +1.44V		-0.36V			2.70 V			1.0 V			4 msec
25h				+7.4V		AVDD/2 +1.48V		-0.37V			2.75 V			1.1 V			
26h				+7.6V		AVDD/2 +1.52V		-0.38V			2.80 V			1.2 V			5 msec
27h				+7.8V		AVDD/2 +1.56V		-0.39V			2.85 V			1.3 V			
28h		8.2 V		+8.0V	-4.1 V	AVDD/2 +1.60V		-0.40V			2.90 V			1.4 V			0 msec
29h		8.4 V		+8.2V	-4.2 V	AVDD/2 +1.64V		-0.41V			2.95 V			1.5 V			1 msec
2Ah		8.6 V		+8.4V	-4.3 V	AVDD/2 +1.68V		-0.42V			3.00 V			1.6 V			2 msec
2Bh		8.8 V		+8.6V	-4.4 V	AVDD/2 +1.72V		-0.43V			3.05 V			1.7 V		25 msec	3 msec
2Ch		9.0 V		+8.8V	-4.5 V	AVDD/2 +1.76V		-0.44V			3.10 V			1.8 V			4 msec
2Dh		9.2 V		+9.0V	-4.6 V	AVDD/2 +1.80V		-0.45V			3.15 V			1.9 V			
2Eh		9.4 V		+9.2V	-4.7 V	AVDD/2 +1.84V		-0.46V			3.20 V			2.0 V			5 msec
2Fh		9.6 V		+9.4V	-4.8 V	AVDD/2 +1.88V		-0.47V			3.25 V			2.1 V			
30h		9.8 V		+9.6V	-4.9 V	AVDD/2 +1.92V		-0.48V			3.30 V		VIN	2.2 V			0 msec
31h		10.0 V		+9.8V	-5.0 V	AVDD/2 +1.96V		-0.49V			3.35 V			2.3 V			1 msec
32h	5.1 V	10.2 V		+10.0V	-5.1 V	AVDD/2 +2.00V		-0.50V						2.4 V			2 msec
33h	5.2 V	10.4 V		+10.2V	-5.2 V	AVDD/2 +2.04V		-0.51V						2.5 V			3 msec
34h	5.3 V	10.6 V		+10.4V	-5.3 V	AVDD/2 +2.08V		-0.52V						2.6 V		30 msec	4 msec
35h	5.4 V	10.8 V		+10.6V	-5.4 V	AVDD/2 +2.12V		-0.53V						2.7 V			
36h	5.5 V	11.0 V		+10.8V	-5.5 V	AVDD/2 +2.16V		-0.54V						2.8 V			5 msec
37h	5.6 V	11.2 V		+11.0V	-5.6 V	AVDD/2 +2.20V		-0.55V						2.9 V			
38h	5.7 V	11.4 V		+11.2V	-5.7 V	AVDD/2 +2.24V		-0.56V			3.40 V			3.0 V			0 msec
39h	5.8 V	11.6 V		+11.4V	-5.8 V	AVDD/2 +2.28V		-0.57V						3.1 V			1 msec
3Ah	5.9 V	11.8 V		+11.6V	-5.9 V	AVDD/2 +2.32V		-0.58V						3.2 V			2 msec
3Bh	6.0 V	12.0 V		+11.8V	-6.0 V	AVDD/2 +2.36V		-0.59V								35 msec	3 msec
3Ch	6.1 V	12.2 V		+12.0V	-6.1 V	AVDD/2 +2.40V		-0.60V									4 msec
3Dh	6.2 V	12.4 V		+12.2V	-6.2 V	AVDD/2 +2.44V		-0.61V						3.3 V			
3Eh	6.3 V	12.6 V		+12.4V	-6.3 V	AVDD/2 +2.48V		-0.62V									5 msec
3Fh	6.4 V	12.8 V	Disable	+12.6V	-6.4 V	AVDD/2 +2.52V	Disable	-0.63V	VD_Phase Set 1						Disable		
40h	6.5 V	13.0 V		+12.8V	-6.5 V	AVDD/2 +2.56V		-0.64V			0.90 V			0.6 V			0 msec
41h	6.6 V	13.2 V		+13.0V	-6.6 V	AVDD/2 +2.60V		-0.65V			0.95 V			0.7 V			1 msec
42h	6.7 V	13.4 V		+13.2V	-6.7 V	AVDD/2 +2.64V		-0.66V			1.00 V			0.8 V			2 msec
43h	6.8 V	13.6 V		+13.4V	-6.8 V	AVDD/2 +2.68V		-0.67V			1.05 V			0.9 V			3 msec
44h	6.9 V	13.8 V		+13.6V	-6.9 V	AVDD/2 +2.72V		-0.68V			1.10 V			1.0 V		40 msec	4 msec
45h	7.0 V	14.0 V		+13.8V	-7.0 V	AVDD/2 +2.76V		-0.69V			1.15 V			1.1 V			
46h	7.1 V	14.2 V		+14.0V	-7.1 V	AVDD/2 +2.80V		-0.70V			1.20 V			1.2 V			5 msec
47h	7.2 V	14.4 V		+14.2V	-7.2 V	AVDD/2 +2.84V		-0.71V			1.25 V			1.3 V			
48h	7.3 V	14.6 V		+14.4V	-7.3 V	AVDD/2 +2.88V		-0.72V			1.30 V			1.4 V			0 msec
49h	7.4 V	14.8 V		+14.6V	-7.4 V	AVDD/2 +2.92V		-0.73V			1.35 V			1.5 V			1 msec
4Ah	7.5 V	15.0 V		+14.8V	-7.5 V	AVDD/2 +2.96V		-0.74V			1.40 V			1.6 V			2 msec
4Bh	7.6 V	15.2 V			-7.6 V	AVDD/2 +3.00V		-0.75V			1.45 V			1.7 V			3 msec
4Ch	7.7 V	15.4 V			-7.7 V	AVDD/2 +3.04V		-0.76V			1.50 V			1.8 V		60 msec	4 msec
4Dh	7.8 V	15.6 V			-7.8 V	AVDD/2 +3.08V		-0.77V			1.55 V			1.9 V			
4Eh	7.9 V	15.8 V			-7.9 V	AVDD/2 +3.12V		-0.78V			1.60 V			2.0 V			5 msec
4Fh	8.0 V	16.0 V			-8.0 V	AVDD/2 +3.16V		-0.79V			1.65 V			2.1 V			
50h	8.1 V	16.2 V			-8.1 V	AVDD/2 +3.20V		-0.80V			1.70 V		VDD	2.2 V			0 msec
51h	8.2 V	16.4 V			-8.2 V	AVDD/2 +3.24V		-0.81V			1.75 V			2.3 V			1 msec
52h	8.3 V	16.6 V			-8.3 V	AVDD/2 +3.28V		-0.82V			1.80 V			2.4 V			2 msec
53h	8.4 V	16.8 V			-8.4 V	AVDD/2 +3.32V		-0.83V			1.85 V			2.5 V		80 msec	3 msec
54h	8.5 V	17.0 V			-8.5 V	AVDD/2 +3.36V		-0.84V			1.90 V			2.6 V			4 msec
55h	8.6 V	17.2 V			-8.6 V	AVDD/2 +3.40V		-0.85V			1.95 V			2.7 V			
56h	8.7 V	17.4 V			-8.7 V	AVDD/2 +3.44V		-0.86V			2.00 V			2.8 V			5 msec
57h	8.8 V	17.6 V			-8.8 V	AVDD/2 +3.48V		-0.87V			2.05 V			2.9 V			
58h	8.9 V	17.8 V			-8.9 V	AVDD/2 +3.52V		-0.88V			2.10 V			3.0 V			0 msec
59h	9.0 V	18.0 V			-9.0 V	AVDD/2 +3.56V		-0.89V			2.15 V			3.1 V			1 msec
5Ah	9.1 V	18.2 V			-9.1 V	AVDD/2 +3.60V		-0.90V			2.20 V			3.2 V			2 msec
5Bh	9.2 V	18.4 V			-9.2 V	AVDD/2 +3.64V		-0.91V			2.25 V						3 msec
5Ch	9.3 V	18.6 V			-9.3 V	AVDD/2 +3.68V		-0.92V			2.30 V					100 msec	4 msec
5Dh	9.4 V	18.8 V			-9.4 V	AVDD/2 +3.72V		-0.93V			2.35 V			3.3 V			
5Eh	9.5 V	19.0 V			-9.5 V	AVDD/2 +3.76V		-0.94V			2.40 V						5 msec
5Fh	9.6 V	19.2 V			-9.6 V	AVDD/2 +3.80V		-0.95V			2.45 V						
60h	9.7 V	19.4 V			-9.7 V	AVDD/2 +3.84V		-0.96V		LDO	2.50 V	0.5 usec		0.6 V			0 msec
61h	9.8 V	19.6 V			-9.8 V	AVDD/2 +3.88V		-0.97V			2.55 V			0.7 V			1 msec
62h	9.9 V	19.8 V			-9.9 V	AVDD/2 +3.92V		-0.98V			2.60 V			0.8 V			2 msec
63h	10.0 V	20.0 V			-10.0 V	AVDD/2 +3.96V		-0.99V			2.65 V			0.9 V			3 msec
64h	10.1 V	20.2 V			-10.1 V	AVDD/2 +4.00V		-1.00V			2.70 V			1.0 V		**150 msec**	4 msec
65h	10.2 V	20.4 V		+15.0V	-10.2 V	AVDD/2 +4.04V		-1.01V			2.75 V			1.1 V			
66h	10.3 V	20.6 V			-10.3 V	AVDD/2 +4.08V		-1.02V			2.80 V			1.2 V			5 msec
67h	10.4 V	20.8 V			-10.4 V	AVDD/2 +4.12V		-1.03V			2.85 V			1.3 V			
68h	10.5 V	21.0 V			-10.5 V	AVDD/2 +4.16V		-1.04V			2.90 V			1.4 V			0 msec
69h	10.6 V	21.2 V			-10.6 V	AVDD/2 +4.20V		-1.05V			2.95 V			1.5 V			1 msec
6Ah	10.7 V	21.4 V			-10.7 V	AVDD/2 +4.24V		-1.06V			3.00 V			1.6 V			2 msec
6Bh	10.8 V	21.6 V			-10.8 V	AVDD/2 +4.28V		-1.07V			3.05 V			1.7 V		**200 msec**	3 msec
6Ch	10.9 V	21.8 V			-10.9 V	AVDD/2 +4.32V		-1.08V			3.10 V			1.8 V			4 msec
6Dh	11.0 V	22.0 V			-11.0 V	AVDD/2 +4.36V		-1.09V			3.15 V			1.9 V			
6Eh	11.1 V	22.2 V			-11.1 V	AVDD/2 +4.40V		-1.10V			3.20 V			2.0 V			5 msec
6Fh	11.2 V	22.4 V			-11.2 V	AVDD/2 +4.44V		-1.11V			3.25 V		VIN	2.1 V			
70h	11.3 V	22.6 V			-11.3 V	AVDD/2 +4.48V		-1.12V			3.30 V			2.2 V			0 msec
71h	11.4 V	22.8 V			-11.4 V	AVDD/2 +4.52V		-1.13V			3.35 V			2.3 V			1 msec
72h	11.5 V	23.0 V			-11.5 V	AVDD/2 +4.56V		-1.14V						2.4 V			2 msec
73h	11.6 V	23.2 V			-11.6 V	AVDD/2 +4.60V		-1.15V						2.5 V		**250 msec**	3 msec
74h	11.7 V	23.4 V			-11.7 V	AVDD/2 +4.64V		-1.16V						2.6 V			4 msec
75h	11.8 V	23.6 V			-11.8 V	AVDD/2 +4.68V		-1.17V						2.7 V			
76h	11.9 V	23.8 V			-11.9 V	AVDD/2 +4.72V		-1.18V						2.8 V			5 msec
77h	12.0 V	24.0 V			-12.0 V	AVDD/2 +4.76V		-1.19V						2.9 V			
78h	12.1 V	24.2 V			-12.1 V	AVDD/2 +4.80V		-1.20V			3.40 V			3.0 V			0 msec
79h	12.2 V	24.4 V			-12.2 V	AVDD/2 +4.84V		-1.21V						3.1 V			1 msec
7Ah	12.3 V	24.6 V			-12.3 V	AVDD/2 +4.88V		-1.22V						3.2 V			2 msec
7Bh	12.4 V	24.8 V			-12.4 V	AVDD/2 +4.92V		-1.23V								**300 msec**	3 msec
7Ch	12.5 V	25.0 V			-12.5 V	AVDD/2 +4.96V		-1.24V									4 msec
7Dh	12.6 V	25.2 V			-12.6 V	AVDD/2 +5.00V		-1.25V						3.3 V			
7Eh	12.7 V	25.4 V			-12.7 V	AVDD/2 +5.04V		-1.26V									5 msec
7Fh	12.8 V	25.6 V			-12.8 V	AVDD/2 +5.08V		-1.27V									

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Command Table - continued

	Regitser Address																
	00h	01h	02h		03h	04h	05h		06h			07h			08h		
DATA (HEX)	AVDD Output Voltage [7:0]	VGH HOT Output Voltage [7:0]	VGH NTC Enable [7]	⊿VGH COLD Voltage [6:0]	VGL Output Voltage [7:0]	VCOM HOT Output Voltage [7:0]	VCOM NTC Enable [7]	⊿VCOM COLD Voltage [6:0]	VDD Phase [7]	VDD MODE [6]	VDD Output Voltage [5:0]	GPM Input Delay [7:6]	Reset Monitor Selecet [5]	Reset Voltage [4:0]	Function Select [7]	Delay1 time [6:3]	Discharge time [2:0]
80h	12.9 V	25.8 V		+0.0V	-12.9 V	AVDD/2		-0.00V			0.90 V			0.6 V			0 msec
81h	13.0 V	26.0 V		+0.2V	-13.0 V	AVDD/2 -0.04V		-0.01V			0.95 V			0.7 V			1 msec
82h	13.1 V	26.2 V		+0.4V	-13.1 V	AVDD/2 -0.08V		-0.02V			1.00 V			0.8 V			2 msec
83h	13.2 V	26.4 V		+0.6V	-13.2 V	AVDD/2 -0.12V		-0.03V			1.05 V			0.9 V		0 msec	3 msec
84h	13.3 V	26.6 V		+0.8V	-13.3 V	AVDD/2 -0.16V		-0.04V			1.10 V			1.0 V			4 msec
85h	13.4 V	26.8 V		+1.0V	-13.4 V	AVDD/2 -0.20V		-0.05V			1.15 V			1.1 V			
86h	13.5 V	27.0 V		+1.2V	-13.5 V	AVDD/2 -0.24V		-0.06V			1.20 V			1.2 V			5 msec
87h	13.6 V	27.2 V		+1.4V	-13.6 V	AVDD/2 -0.28V		-0.07V			1.25 V			1.3 V			
88h	13.7 V	27.4 V		+1.6V	-13.7 V	AVDD/2 -0.32V		-0.08V			1.30 V			1.4 V			0 msec
89h	13.8 V	27.6 V		+1.8V	-13.8 V	AVDD/2 -0.36V		-0.09V			1.35 V			1.5 V			1 msec
8Ah	13.9 V	27.8 V		+2.0V	-13.9 V	AVDD/2 -0.40V		-0.10V			1.40 V			1.6 V			2 msec
8Bh	14.0 V	28.0 V		+2.2V		AVDD/2 -0.44V		-0.11V			1.45 V			1.7 V		5 msec	3 msec
8Ch	14.1 V	28.2 V		+2.4V		AVDD/2 -0.48V		-0.12V			1.50 V			1.8 V			4 msec
8Dh	14.2 V	28.4 V		+2.6V		AVDD/2 -0.52V		-0.13V			1.55 V			1.9 V			
8Eh	14.3 V	28.6 V		+2.8V		AVDD/2 -0.56V		-0.14V			1.60 V			2.0 V			5 msec
8Fh	14.4 V	28.8 V		+3.0V		AVDD/2 -0.60V		-0.15V			1.65 V		VDD	2.1 V			
90h	14.5 V	29.0 V		+3.2V		AVDD/2 -0.64V		-0.16V			1.70 V			2.2 V			0 msec
91h	14.6 V	29.2 V		+3.4V		AVDD/2 -0.68V		-0.17V			1.75 V			2.3 V			1 msec
92h	14.7 V	29.4 V		+3.6V		AVDD/2 -0.72V		-0.18V			1.80 V			2.4 V			2 msec
93h	14.8 V	29.6 V		+3.8V		AVDD/2 -0.76V		-0.19V			1.85 V			2.5 V		10 msec	3 msec
94h	14.9 V	29.8 V		+4.0V		AVDD/2 -0.80V		-0.20V			1.90 V			2.6 V			4 msec
95h	15.0 V	30.0 V		+4.2V		AVDD/2 -0.84V		-0.21V			1.95 V			2.7 V			
96h	15.1 V	30.2 V		+4.4V		AVDD/2 -0.88V		-0.22V			2.00 V			2.8 V			5 msec
97h	15.2 V	30.4 V		+4.6V		AVDD/2 -0.92V		-0.23V			2.05 V			2.9 V			
98h	15.3 V	30.6 V		+4.8V		AVDD/2 -0.96V		-0.24V			2.10 V			3.0 V			0 msec
99h	15.4 V	30.8 V		+5.0V		AVDD/2 -1.00V		-0.25V			2.15 V			3.1 V			1 msec
9Ah	15.5 V	31.0 V		+5.2V		AVDD/2 -1.04V		-0.26V			2.20 V			3.2 V			2 msec
9Bh	15.6 V	31.2 V		+5.4V		AVDD/2 -1.08V		-0.27V			2.25 V					15 msec	3 msec
9Ch	15.7 V	31.4 V		+5.6V		AVDD/2 -1.12V		-0.28V			2.30 V			3.3 V			4 msec
9Dh	15.8 V	31.6 V		+5.8V		AVDD/2 -1.16V		-0.29V			2.35 V						
9Eh	15.9 V	31.8 V		+6.0V		AVDD/2 -1.20V		-0.30V			2.40 V						5 msec
9Fh	16.0 V	32.0 V		+6.2V		AVDD/2 -1.24V		-0.31V		DC/DC	2.45 V	1.0 usec					
A0h	16.1 V	32.2 V		+6.4V		AVDD/2 -1.28V		-0.32V			2.50 V			0.6 V			0 msec
A1h	16.2 V	32.4 V		+6.6V		AVDD/2 -1.32V		-0.33V			2.55 V			0.7 V			1 msec
A2h	16.3 V	32.6 V		+6.8V		AVDD/2 -1.36V		-0.34V			2.60 V			0.8 V			2 msec
A3h	16.4 V	32.8 V		+7.0V		AVDD/2 -1.40V		-0.35V			2.65 V			0.9 V		20 msec	3 msec
A4h	16.5 V	33.0 V		+7.2V		AVDD/2 -1.44V		-0.36V			2.70 V			1.0 V			4 msec
A5h	16.6 V	33.2 V		+7.4V		AVDD/2 -1.48V		-0.37V			2.75 V			1.1 V			
A6h	16.7 V	33.4 V		+7.6V		AVDD/2 -1.52V		-0.38V			2.80 V			1.2 V			5 msec
A7h	16.8 V	33.6 V		+7.8V		AVDD/2 -1.56V		-0.39V			2.85 V			1.3 V			
A8h	16.9 V	33.8 V		+8.0V		AVDD/2 -1.60V		-0.40V			2.90 V			1.4 V			0 msec
A9h		34.0 V		+8.2V		AVDD/2 -1.64V		-0.41V			2.95 V			1.5 V			1 msec
AAh		34.2 V		+8.4V		AVDD/2 -1.68V		-0.42V			3.00 V			1.6 V			2 msec
ABh		34.4 V		+8.6V		AVDD/2 -1.72V		-0.43V			3.05 V			1.7 V		25 msec	3 msec
ACh		34.6 V		+8.8V		AVDD/2 -1.76V		-0.44V			3.10 V			1.8 V			4 msec
ADh		34.8 V		+9.0V		AVDD/2 -1.80V		-0.45V			3.15 V			1.9 V			
AEh				+9.2V		AVDD/2 -1.84V		-0.46V			3.20 V			2.0 V			5 msec
AFh				+9.4V		AVDD/2 -1.88V		-0.47V			3.25 V		VIN	2.1 V			
B0h				+9.6V		AVDD/2 -1.92V		-0.48V			3.30 V			2.2 V			0 msec
B1h				+9.8V		AVDD/2 -1.96V		-0.49V			3.35 V			2.3 V			1 msec
B2h				+10.0V		AVDD/2 -2.00V		-0.50V						2.4 V			2 msec
B3h				+10.2V		AVDD/2 -2.04V		-0.51V						2.5 V		30 msec	3 msec
B4h				+10.4V		AVDD/2 -2.08V		-0.52V						2.6 V			4 msec
B5h				+10.6V		AVDD/2 -2.12V		-0.53V						2.7 V			
B6h				+10.8V		AVDD/2 -2.16V		-0.54V						2.8 V			5 msec
B7h				+11.0V		AVDD/2 -2.20V		-0.55V						2.9 V			
B8h				+11.2V		AVDD/2 -2.24V		-0.56V			3.40 V			3.0 V			0 msec
B9h				+11.4V		AVDD/2 -2.28V		-0.57V						3.1 V			1 msec
BAh				+11.6V		AVDD/2 -2.32V		-0.58V						3.2 V			2 msec
BBh				+11.8V		AVDD/2 -2.36V		-0.59V								35 msec	3 msec
BCh				+12.0V		AVDD/2 -2.40V		-0.60V									4 msec
BDh				+12.2V		AVDD/2 -2.44V		-0.61V						3.3 V			
BEh				+12.4V		AVDD/2 -2.48V		-0.62V									5 msec
BFh				+12.6V		AVDD/2 -2.52V		-0.63V	**VD_Phase_ Set 2**								
C0h			Enable	+12.8V		AVDD/2 -2.56V	Enable	-0.64V			0.90 V			0.6 V	Enable		0 msec
C1h				+13.0V		AVDD/2 -2.60V		-0.65V			0.95 V			0.7 V			1 msec
C2h				+13.2V		AVDD/2 -2.64V		-0.66V			1.00 V			0.8 V			2 msec
C3h				+13.4V		AVDD/2 -2.68V		-0.67V			1.05 V			0.9 V		40 msec	3 msec
C4h				+13.6V		AVDD/2 -2.72V		-0.68V			1.10 V			1.0 V			4 msec
C5h				+13.8V	-14.0 V	AVDD/2 -2.76V		-0.69V			1.15 V			1.1 V			
C6h				+14.0V		AVDD/2 -2.80V		-0.70V			1.20 V			1.2 V			5 msec
C7h				+14.2V		AVDD/2 -2.84V		-0.71V			1.25 V			1.3 V			
C8h				+14.4V		AVDD/2 -2.88V		-0.72V			1.30 V			1.4 V			0 msec
C9h				+14.6V		AVDD/2 -2.92V		-0.73V			1.35 V			1.5 V			1 msec
CAh				+14.8V		AVDD/2 -2.96V		-0.74V			1.40 V			1.6 V			2 msec
CBh						AVDD/2 -3.00V		-0.75V			1.45 V			1.7 V		60 msec	3 msec
CCh						AVDD/2 -3.04V		-0.76V			1.50 V			1.8 V			4 msec
CDh						AVDD/2 -3.08V		-0.77V			1.55 V			1.9 V			
CEh						AVDD/2 -3.12V		-0.78V			1.60 V			2.0 V			5 msec
CFh						AVDD/2 -3.16V		-0.79V			1.65 V		VDD	2.1 V			
D0h						AVDD/2 -3.20V		-0.80V			1.70 V			2.2 V			0 msec
D1h						AVDD/2 -3.24V		-0.81V			1.75 V			2.3 V			1 msec
D2h						AVDD/2 -3.28V		-0.82V			1.80 V			2.4 V			2 msec
D3h						AVDD/2 -3.32V		-0.83V			1.85 V			2.5 V		80 msec	3 msec
D4h	17.0 V					AVDD/2 -3.36V		-0.84V			1.90 V			2.6 V			4 msec
D5h						AVDD/2 -3.40V		-0.85V			1.95 V			2.7 V			
D6h		35.0 V				AVDD/2 -3.44V		-0.86V			2.00 V			2.8 V			5 msec
D7h						AVDD/2 -3.48V		-0.87V			2.05 V			2.9 V			
D8h						AVDD/2 -3.52V		-0.88V			2.10 V			3.0 V			0 msec
D9h						AVDD/2 -3.56V		-0.89V			2.15 V			3.1 V			1 msec
DAh						AVDD/2 -3.60V		-0.90V			2.20 V			3.2 V			2 msec
DBh						AVDD/2 -3.64V		-0.91V			2.25 V					100 msec	3 msec
DCh						AVDD/2 -3.68V		-0.92V			2.30 V			3.3 V			4 msec
DDh						AVDD/2 -3.72V		-0.93V			2.35 V						
DEh						AVDD/2 -3.76V		-0.94V			2.40 V						5 msec
DFh						AVDD/2 -3.80V		-0.95V			2.45 V						
E0h						AVDD/2 -3.84V		-0.96V		LDO	2.50 V	1.5 usec		0.6 V			0 msec
E1h						AVDD/2 -3.88V		-0.97V			2.55 V			0.7 V			1 msec
E2h						AVDD/2 -3.92V		-0.98V			2.60 V			0.8 V			2 msec
E3h						AVDD/2 -3.96V		-0.99V			2.65 V			0.9 V		**150 msec**	3 msec
E4h						AVDD/2 -4.00V		-1.00V			2.70 V			1.0 V			4 msec
E5h				+15.0V		AVDD/2 -4.04V		-1.01V			2.75 V			1.1 V			
E6h						AVDD/2 -4.08V		-1.02V			2.80 V			1.2 V			5 msec
E7h						AVDD/2 -4.12V		-1.03V			2.85 V			1.3 V			
E8h						AVDD/2 -4.16V		-1.04V			2.90 V			1.4 V			0 msec
E9h						AVDD/2 -4.20V		-1.05V			2.95 V			1.5 V			1 msec
EAh						AVDD/2 -4.24V		-1.06V			3.00 V			1.6 V			2 msec
EBh						AVDD/2 -4.28V		-1.07V			3.05 V			1.7 V		**200 msec**	3 msec
ECh						AVDD/2 -4.32V		-1.08V			3.10 V			1.8 V			4 msec
EDh						AVDD/2 -4.36V		-1.09V			3.15 V			1.9 V			
EEh						AVDD/2 -4.40V		-1.10V			3.20 V			2.0 V			5 msec
EFh						AVDD/2 -4.44V		-1.11V			3.25 V		VIN	2.1 V			
F0h						AVDD/2 -4.48V		-1.12V			3.30 V			2.2 V			0 msec
F1h						AVDD/2 -4.52V		-1.13V			3.35 V			2.3 V			1 msec
F2h						AVDD/2 -4.56V		-1.14V						2.4 V			2 msec
F3h						AVDD/2 -4.60V		-1.15V						2.5 V		**250 msec**	3 msec
F4h						AVDD/2 -4.64V		-1.16V						2.6 V			4 msec
F5h						AVDD/2 -4.68V		-1.17V						2.7 V			
F6h						AVDD/2 -4.72V		-1.18V						2.8 V			5 msec
F7h						AVDD/2 -4.76V		-1.19V						2.9 V			
F8h						AVDD/2 -4.80V		-1.20V			3.40 V			3.0 V			0 msec
F9h						AVDD/2 -4.84V		-1.21V						3.1 V			1 msec
FAh						AVDD/2 -4.88V		-1.22V						3.2 V			2 msec
FBh						AVDD/2 -4.92V		-1.23V								**300 msec**	3 msec
FCh						AVDD/2 -4.96V		-1.24V									4 msec
FDh						AVDD/2 -5.00V		-1.25V						3.3 V			
FEh						AVDD/2 -5.04V		-1.26V									5 msec
FFh						AVDD/2 -5.08V		-1.27V									

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Command Table - continued

	Regitser Address																		
	09h				0Ah				0Bh					0Ch					0Dh
DATA (HEX)	DataRef [7]	Delay3 time [6:4]	DoubleReg [3]	Delay2 time [2:0]	VGH Discharge Enable [7]	Delay5 time [6:4]	AR_Time [3]	Delay4 time [2:0]	AVDD COMP [7]	AVDD OCP Select [6]	AVDD SS time [5:4]	AVDD SW Slew Rate [3:2]	AVDD COIL [1:0]	Start-up Bit [7]	VGH mode select [6]	VGH/VGL Frequency [5:4]	VDD Frequency [3:2]	AVDD Frequency [1:0]	Check Sum [7:0]
00h	Disable	0 msec	Disable	0 msec	Enable	0 msec	0.5 sec	0 msec	AV_COMP_Set 1	2.0 A	5 msec	Slow2	AVC_Set1	Disable	x3 mode	2.1MHz	2.1MHz	2.1MHz	
01h				5 msec				5 msec					AVC_Set2			1.05MHz		1.05MHz	
02h				10 msec				10 msec					AVC_Set3			525KHz		525KHz	
03h				15 msec				15 msec					AVC_Set4						
04h				20 msec				20 msec				Slow1	AVC_Set1			2.1MHz	1.05MHz	2.1MHz	
05h				25 msec				25 msec					AVC_Set2			1.05MHz		1.05MHz	
06h				30 msec				30 msec					AVC_Set3			525KHz		525KHz	
07h				40 msec				40 msec					AVC_Set4						
08h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			2.1MHz	525KHz	2.1MHz	
09h				5 msec				5 msec					AVC_Set2			1.05MHz		1.05MHz	
0Ah				10 msec				10 msec					AVC_Set3			525KHz		525KHz	
0Bh				15 msec				15 msec					AVC_Set4						
0Ch				20 msec				20 msec				Fast2	AVC_Set1			2.1MHz		2.1MHz	
0Dh				25 msec				25 msec					AVC_Set2			1.05MHz		1.05MHz	
0Eh				30 msec				30 msec					AVC_Set3			525KHz		525KHz	
0Fh				40 msec				40 msec					AVC_Set4						
10h		5 msec	Disable	0 msec		2 msec	0.5 sec	0 msec			10 msec	Slow2	AVC_Set1			1.05MHz	2.1MHz	2.1MHz	
11h				5 msec				5 msec					AVC_Set2			525KHz		1.05MHz	
12h				10 msec				10 msec					AVC_Set3			256KHz		525KHz	
13h				15 msec				15 msec					AVC_Set4						
14h				20 msec				20 msec				Slow1	AVC_Set1			1.05MHz	1.05MHz	2.1MHz	
15h				25 msec				25 msec					AVC_Set2			525KHz		1.05MHz	
16h				30 msec				30 msec					AVC_Set3			256KHz		525KHz	
17h				40 msec				40 msec					AVC_Set4						
18h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			1.05MHz	525KHz	2.1MHz	
19h				5 msec				5 msec					AVC_Set2			525KHz		1.05MHz	
1Ah				10 msec				10 msec					AVC_Set3			256KHz		525KHz	
1Bh				15 msec				15 msec					AVC_Set4						
1Ch				20 msec				20 msec				Fast2	AVC_Set1			1.05MHz		2.1MHz	
1Dh				25 msec				25 msec					AVC_Set2			525KHz		1.05MHz	
1Eh				30 msec				30 msec					AVC_Set3			256KHz		525KHz	
1Fh				40 msec				40 msec					AVC_Set4						
20h		10 msec	Disable	0 msec		4 msec	0.5 sec	0 msec			15 msec	Slow2	AVC_Set1			525KHz	2.1MHz	2.1MHz	
21h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
22h				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
23h				15 msec				15 msec					AVC_Set4						
24h				20 msec				20 msec				Slow1	AVC_Set1			525KHz	1.05MHz	2.1MHz	
25h				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
26h				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
27h				40 msec				40 msec					AVC_Set4						
28h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			525KHz	525KHz	2.1MHz	
29h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
2Ah				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
2Bh				15 msec				15 msec					AVC_Set4						
2Ch				20 msec				20 msec				Fast2	AVC_Set1			525KHz		2.1MHz	
2Dh				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
2Eh				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
2Fh				40 msec				40 msec					AVC_Set4						
30h		15 msec	Disable	0 msec		6 msec	0.5 sec	0 msec			20 msec	Slow2	AVC_Set1			525KHz	2.1MHz	2.1MHz	
31h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
32h				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
33h				15 msec				15 msec					AVC_Set4						
34h				20 msec				20 msec				Slow1	AVC_Set1			525KHz	1.05MHz	2.1MHz	
35h				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
36h				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
37h				40 msec				40 msec					AVC_Set4						
38h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			525KHz	525KHz	2.1MHz	
39h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
3Ah				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
3Bh				15 msec				15 msec					AVC_Set4						
3Ch				20 msec				20 msec				Fast2	AVC_Set1			525KHz		2.1MHz	
3Dh				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
3Eh				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
3Fh				40 msec				40 msec					AVC_Set4						
40h		20 msec	Disable	0 msec		8 msec	0.5 sec	0 msec		1.0 A	5 msec	Slow2	AVC_Set1			2.1MHz	2.1MHz	2.1MHz	
41h				5 msec				5 msec					AVC_Set2			1.05MHz		1.05MHz	
42h				10 msec				10 msec					AVC_Set3			525KHz		525KHz	
43h				15 msec				15 msec					AVC_Set4						
44h				20 msec				20 msec				Slow1	AVC_Set1			2.1MHz	1.05MHz	2.1MHz	
45h				25 msec				25 msec					AVC_Set2			1.05MHz		1.05MHz	
46h				30 msec				30 msec					AVC_Set3			525KHz		525KHz	
47h				40 msec				40 msec					AVC_Set4						
48h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			2.1MHz	525KHz	2.1MHz	
49h				5 msec				5 msec					AVC_Set2			1.05MHz		1.05MHz	
4Ah				10 msec				10 msec					AVC_Set3			525KHz		525KHz	
4Bh				15 msec				15 msec					AVC_Set4						
4Ch				20 msec				20 msec				Fast2	AVC_Set1			2.1MHz		2.1MHz	
4Dh				25 msec				25 msec					AVC_Set2			1.05MHz		1.05MHz	
4Eh				30 msec				30 msec					AVC_Set3			525KHz		525KHz	
4Fh				40 msec				40 msec					AVC_Set4						
50h		25 msec	Disable	0 msec		10 msec	0.5 sec	0 msec			10 msec	Slow2	AVC_Set1			1.05MHz	525KHz	2.1MHz	
51h				5 msec				5 msec					AVC_Set2			525KHz		1.05MHz	
52h				10 msec				10 msec					AVC_Set3			256KHz		525KHz	
53h				15 msec				15 msec					AVC_Set4						
54h				20 msec				20 msec				Slow1	AVC_Set1			1.05MHz	1.05MHz	2.1MHz	
55h				25 msec				25 msec					AVC_Set2			525KHz		1.05MHz	
56h				30 msec				30 msec					AVC_Set3			256KHz		525KHz	
57h				40 msec				40 msec					AVC_Set4						
58h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			1.05MHz	2.1MHz	2.1MHz	
59h				5 msec				5 msec					AVC_Set2			525KHz		1.05MHz	
5Ah				10 msec				10 msec					AVC_Set3			256KHz		525KHz	
5Bh				15 msec				15 msec					AVC_Set4						
5Ch				20 msec				20 msec				Fast2	AVC_Set1			1.05MHz		2.1MHz	
5Dh				25 msec				25 msec					AVC_Set2			525KHz		1.05MHz	
5Eh				30 msec				30 msec					AVC_Set3			256KHz		525KHz	
5Fh				40 msec				40 msec					AVC_Set4						
60h		30 msec	Disable	0 msec		10 msec	0.5 sec	0 msec			15 msec	Slow2	AVC_Set1		x2 mode	525KHz	525KHz	2.1MHz	
61h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
62h				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
63h				15 msec				15 msec					AVC_Set4						
64h				20 msec				20 msec				Slow1	AVC_Set1			525KHz	1.05MHz	2.1MHz	
65h				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
66h				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
67h				40 msec				40 msec					AVC_Set4						
68h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			525KHz	2.1MHz	2.1MHz	
69h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
6Ah				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
6Bh				15 msec				15 msec					AVC_Set4						
6Ch				20 msec				20 msec				Fast2	AVC_Set1			525KHz		2.1MHz	
6Dh				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
6Eh				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
6Fh				40 msec				40 msec					AVC_Set4						
70h		40 msec	Disable	0 msec			0.5 sec	0 msec			20 msec	Slow2	AVC_Set1			525KHz	525KHz	2.1MHz	
71h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
72h				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
73h				15 msec				15 msec					AVC_Set4						
74h				20 msec				20 msec				Slow1	AVC_Set1			525KHz	1.05MHz	2.1MHz	
75h				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
76h				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
77h				40 msec				40 msec					AVC_Set4						
78h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			525KHz	2.1MHz	2.1MHz	
79h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
7Ah				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
7Bh				15 msec				15 msec					AVC_Set4						
7Ch				20 msec				20 msec				Fast2	AVC_Set1			525KHz		2.1MHz	
7Dh				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
7Eh				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
7Fh				40 msec				40 msec					AVC_Set4						

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Command Table – continued

	Regitser Address																		
	09h				0Ah				0Bh					0Ch					0Dh
DATA (HEX)	DataRef [7]	Delay3 time [6:4]	DoubleReg [3]	Delay2 time [2:0]	VGH Discharge Enable [7]	Delay5 time [6:4]	AR_Time [3]	Delay4 time [2:0]	AVDD COMP [7]	AVDD OCP Select [6]	AVDD SS time [5:4]	AVDD SW Slew Rate [3:2]	AVDD COIL [1:0]	Start-up Bit [7]	VGH mode select [6]	VGH/VGL Frequency [5:4]	VDD Frequency [3:2]	AVDD Frequency [1:0]	Check Sum [7:0]
80h	Enable	0 msec	Disable	0 msec	Disable	0 msec	0.5 sec	0 msec	AV_COMP_Set 2	2.0 A	5 msec	Slow2	AVC_Set1	Enable	x3 mode	2.1MHz	2.1MHz	2.1MHz	
81h				5 msec				5 msec					AVC_Set2			1.05MHz		1.05MHz	
82h				10 msec				10 msec					AVC_Set3			525KHz		525KHz	
83h				15 msec				15 msec					AVC_Set4						
84h				20 msec				20 msec				Slow1	AVC_Set1			2.1MHz	1.05MHz	2.1MHz	
85h				25 msec				25 msec					AVC_Set2			1.05MHz		1.05MHz	
86h				30 msec				30 msec					AVC_Set3			525KHz		525KHz	
87h				40 msec				40 msec					AVC_Set4						
88h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			2.1MHz	525KHz	2.1MHz	
89h				5 msec				5 msec					AVC_Set2			1.05MHz		1.05MHz	
8Ah				10 msec				10 msec					AVC_Set3			525KHz		525KHz	
8Bh				15 msec				15 msec					AVC_Set4						
8Ch				20 msec				20 msec				Fast2	AVC_Set1			2.1MHz		2.1MHz	
8Dh				25 msec				25 msec					AVC_Set2			1.05MHz		1.05MHz	
8Eh				30 msec				30 msec					AVC_Set3			525KHz		525KHz	
8Fh				40 msec				40 msec					AVC_Set4						
90h		5 msec	Disable	0 msec		2 msec	0.5 sec	0 msec			10 msec	Slow2	AVC_Set1			1.05MHz	2.1MHz	2.1MHz	
91h				5 msec				5 msec					AVC_Set2			525KHz		1.05MHz	
92h				10 msec				10 msec					AVC_Set3			256KHz		525KHz	
93h				15 msec				15 msec					AVC_Set4						
94h				20 msec				20 msec				Slow1	AVC_Set1			1.05MHz	1.05MHz	2.1MHz	
95h				25 msec				25 msec					AVC_Set2			525KHz		1.05MHz	
96h				30 msec				30 msec					AVC_Set3			256KHz		525KHz	
97h				40 msec				40 msec					AVC_Set4						
98h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			1.05MHz	525KHz	2.1MHz	
99h				5 msec				5 msec					AVC_Set2			525KHz		1.05MHz	
9Ah				10 msec				10 msec					AVC_Set3			256KHz		525KHz	
9Bh				15 msec				15 msec					AVC_Set4						
9Ch				20 msec				20 msec				Fast2	AVC_Set1			1.05MHz		2.1MHz	
9Dh				25 msec				25 msec					AVC_Set2			525KHz		1.05MHz	
9Eh				30 msec				30 msec					AVC_Set3			256KHz		525KHz	
9Fh				40 msec				40 msec					AVC_Set4						
A0h		10 msec	Disable	0 msec		4 msec	0.5 sec	0 msec			15 msec	Slow2	AVC_Set1			525KHz	2.1MHz	2.1MHz	
A1h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
A2h				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
A3h				15 msec				15 msec					AVC_Set4						
A4h				20 msec				20 msec				Slow1	AVC_Set1			525KHz	1.05MHz	2.1MHz	
A5h				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
A6h				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
A7h				40 msec				40 msec					AVC_Set4						
A8h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			525KHz	525KHz	2.1MHz	
A9h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
AAh				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
ABh				15 msec				15 msec					AVC_Set4						
ACh				20 msec				20 msec				Fast2	AVC_Set1			525KHz		2.1MHz	
ADh				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
AEh				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
AFh				40 msec				40 msec					AVC_Set4						
B0h		15 msec	Disable	0 msec		6 msec	0.5 sec	0 msec			20 msec	Slow2	AVC_Set1			525KHz	2.1MHz	2.1MHz	
B1h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
B2h				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
B3h				15 msec				15 msec					AVC_Set4						
B4h				20 msec				20 msec				Slow1	AVC_Set1			525KHz	1.05MHz	2.1MHz	
B5h				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
B6h				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
B7h				40 msec				40 msec					AVC_Set4						
B8h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			525KHz	525KHz	2.1MHz	
B9h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
BAh				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
BBh				15 msec				15 msec					AVC_Set4						
BCh				20 msec				20 msec				Fast2	AVC_Set1			525KHz		2.1MHz	
BDh				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
BEh				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
BFh				40 msec				40 msec					AVC_Set4						
C0h		20 msec	Disable	0 msec		8 msec	0.5 sec	0 msec		1.0 A	5 msec	Slow2	AVC_Set1			2.1MHz	2.1MHz	2.1MHz	
C1h				5 msec				5 msec					AVC_Set2			1.05MHz		1.05MHz	
C2h				10 msec				10 msec					AVC_Set3			525KHz		525KHz	
C3h				15 msec				15 msec					AVC_Set4						
C4h				20 msec				20 msec				Slow1	AVC_Set1			2.1MHz	1.05MHz	2.1MHz	
C5h				25 msec				25 msec					AVC_Set2			1.05MHz		1.05MHz	
C6h				30 msec				30 msec					AVC_Set3			525KHz		525KHz	
C7h				40 msec				40 msec					AVC_Set4						
C8h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			2.1MHz	525KHz	2.1MHz	
C9h				5 msec				5 msec					AVC_Set2			1.05MHz		1.05MHz	
CAh				10 msec				10 msec					AVC_Set3			525KHz		525KHz	
CBh				15 msec				15 msec					AVC_Set4						
CCh				20 msec				20 msec				Fast2	AVC_Set1			2.1MHz		2.1MHz	
CDh				25 msec				25 msec					AVC_Set2			1.05MHz		1.05MHz	
CEh				30 msec				30 msec					AVC_Set3			525KHz		525KHz	
CFh				40 msec				40 msec					AVC_Set4						
D0h		25 msec	Disable	0 msec		10 msec	0.5 sec	0 msec			10 msec	Slow2	AVC_Set1			1.05MHz	2.1MHz	2.1MHz	
D1h				5 msec				5 msec					AVC_Set2			525KHz		1.05MHz	
D2h				10 msec				10 msec					AVC_Set3			256KHz		525KHz	
D3h				15 msec				15 msec					AVC_Set4						
D4h				20 msec				20 msec				Slow1	AVC_Set1			1.05MHz	1.05MHz	2.1MHz	
D5h				25 msec				25 msec					AVC_Set2			525KHz		1.05MHz	
D6h				30 msec				30 msec					AVC_Set3			256KHz		525KHz	
D7h				40 msec				40 msec					AVC_Set4						
D8h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			1.05MHz	525KHz	2.1MHz	
D9h				5 msec				5 msec					AVC_Set2			525KHz		1.05MHz	
DAh				10 msec				10 msec					AVC_Set3			256KHz		525KHz	
DBh				15 msec				15 msec					AVC_Set4						
DCh				20 msec				20 msec				Fast2	AVC_Set1			1.05MHz		2.1MHz	
DDh				25 msec				25 msec					AVC_Set2			525KHz		1.05MHz	
DEh				30 msec				30 msec					AVC_Set3			256KHz		525KHz	
DFh				40 msec				40 msec					AVC_Set4						
E0h		30 msec	Disable	0 msec		10 msec	0.5 sec	0 msec			15 msec	Slow2	AVC_Set1			525KHz	2.1MHz	2.1MHz	
E1h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
E2h				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
E3h				15 msec				15 msec					AVC_Set4						
E4h				20 msec				20 msec				Slow1	AVC_Set1			525KHz	1.05MHz	2.1MHz	
E5h				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
E6h				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
E7h				40 msec				40 msec					AVC_Set4						
E8h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			525KHz	525KHz	2.1MHz	
E9h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
EAh				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
EBh				15 msec				15 msec					AVC_Set4						
ECh				20 msec				20 msec				Fast2	AVC_Set1			525KHz		2.1MHz	
EDh				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
EEh				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
EFh				40 msec				40 msec					AVC_Set4						
F0h		40 msec	Disable	0 msec			0.5 sec	0 msec			20 msec	Slow2	AVC_Set1			525KHz	2.1MHz	2.1MHz	
F1h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
F2h				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
F3h				15 msec				15 msec					AVC_Set4						
F4h				20 msec				20 msec				Slow1	AVC_Set1			525KHz	1.05MHz	2.1MHz	
F5h				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
F6h				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
F7h				40 msec				40 msec					AVC_Set4						
F8h			Enable	0 msec			1.0 sec	0 msec				Fast1	AVC_Set1			525KHz	525KHz	2.1MHz	
F9h				5 msec				5 msec					AVC_Set2			256KHz		1.05MHz	
FAh				10 msec				10 msec					AVC_Set3			128KHz		525KHz	
FBh				15 msec				15 msec					AVC_Set4						
FCh				20 msec				20 msec				Fast2	AVC_Set1			525KHz		2.1MHz	
FDh				25 msec				25 msec					AVC_Set2			256KHz		1.05MHz	
FEh				30 msec				30 msec					AVC_Set3			128KHz		525KHz	
FFh				40 msec				40 msec					AVC_Set4						

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Check Sum

Check Sum which has been adopted in BM81810MUV-M is shown below.
You will calculate the Check Sum that the sum of the data, including the Check Sum(CHK7 to CHK0) is 00h.

Register	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
00h	A7	A6	A5	A4	A3	A2	A1	A0
01h	B7	B6	B5	B4	B3	B2	B1	B0
02h	C7	C6	C5	C4	C3	C2	C1	C0
03h	D7	D6	D5	D4	D3	D2	D1	D0
04h	E7	E6	E5	E4	E3	E2	E1	E0
05h	F7	F6	F5	F4	F3	F2	F1	F0
06h	G7	G6	G5	G4	G3	G2	G1	G0
07h	H7	H6	H5	H4	H3	H2	H1	H0
08h	I7	I6	I5	I4	I3	I2	I1	I0
09h	J7	J6	J5	J4	J3	J2	J1	J0
0Ah	K7	K6	K5	K4	K3	K2	K1	K0
0Bh	L7	L6	L5	L4	L3	L2	L1	L0
0Ch	M7	M6	M5	M4	M3	M2	M1	M0
0Dh	CHK7	CHK6	CHK5	CHK4	CHK3	CHK2	CHK1	CHK0

[A7:A0] + [B7:B0] + [C7:C0] + [D7:D0] + [E7:E0] + [F7:F0] + [G7:G0] + [H7:H0] + [I7:I0] + [J7:J0] + [K7:K0] + [L7:L0] + [M7:M0] + [CHK7:CHK0] = 00h

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Soft Start Time

BM81810MUV-M has soft start function on AVDD, VGH, VGL and VDD.
Time of the soft start is up to the output voltage reaches the typ Value.
The output voltage typ Value of each block is shown in the following table.

BLOCK	Soft Start Output Voltage Typ Value	Soft Start Time
AVDD	10.5 V	Set Register
VGH	18.0 V	5 msec
VGL	-6.0 V	5 msec
VDD	1.2 V	1 msec

The time setting Soft Start of AVDD is shown in the table below.

Bit		AVDD Soft Start Time
0	0	5 msec
0	1	10 msec
1	0	15 msec
1	1	20 msec

The soft-start time of VGH and VGL are 5msec.
The soft-start time of VDD is 1msec.

The soft-start setting an example of AVDD and VGH are shown in the figure below.

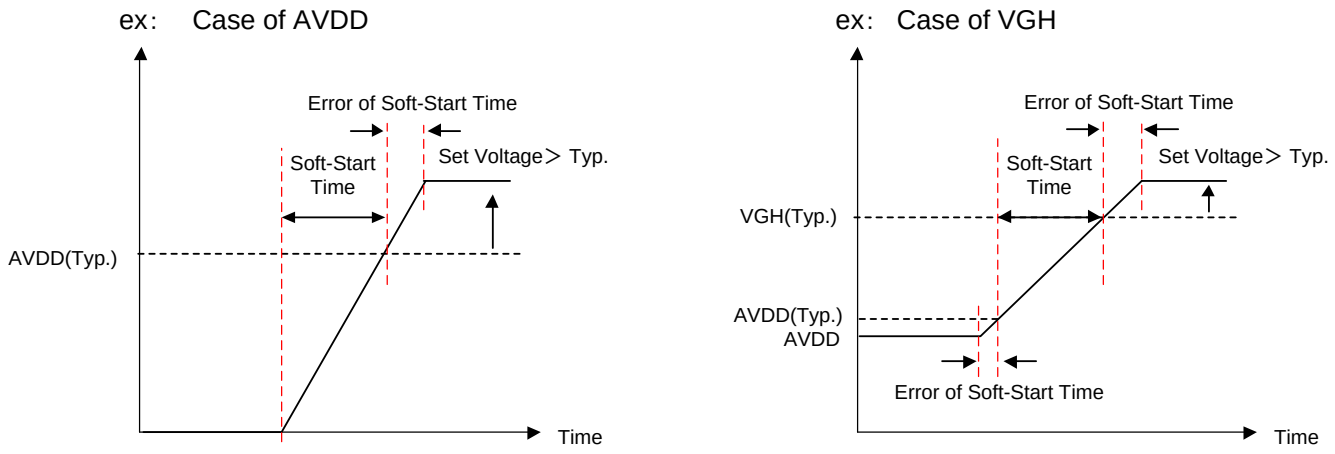

Figure 76. Soft-Start Time

If you change the setting voltage from typ values, occurs error in the soft-start time.

•The setting voltage > Typ Value ••• Soft-start will be more slow.
•The setting voltage < Typ Value ••• Soft-start will be more faster.

No error of soft-start is occurred for change of frequency.

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Block Diagram

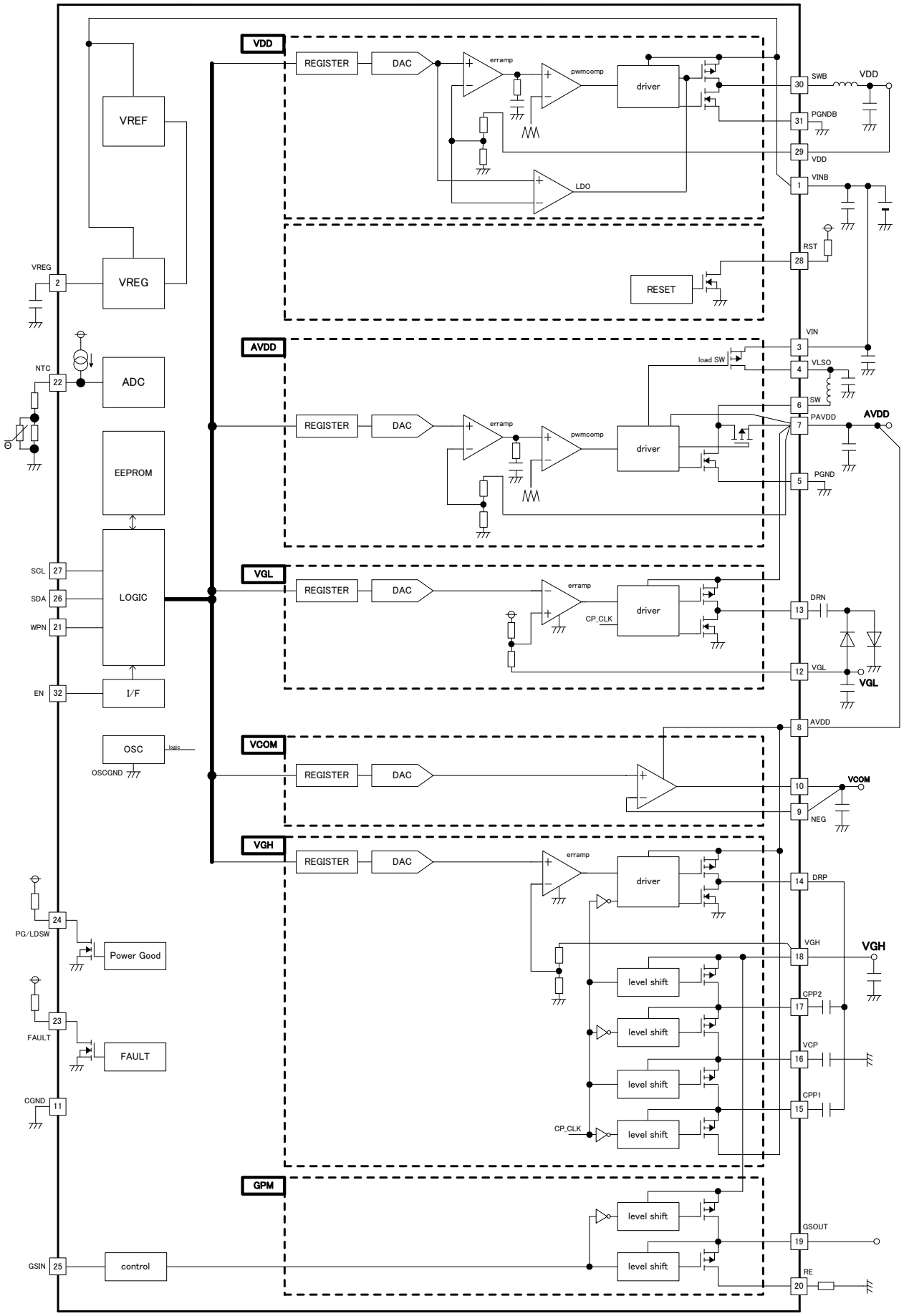

Figure 77. Block Diagram

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AVDD Block Function

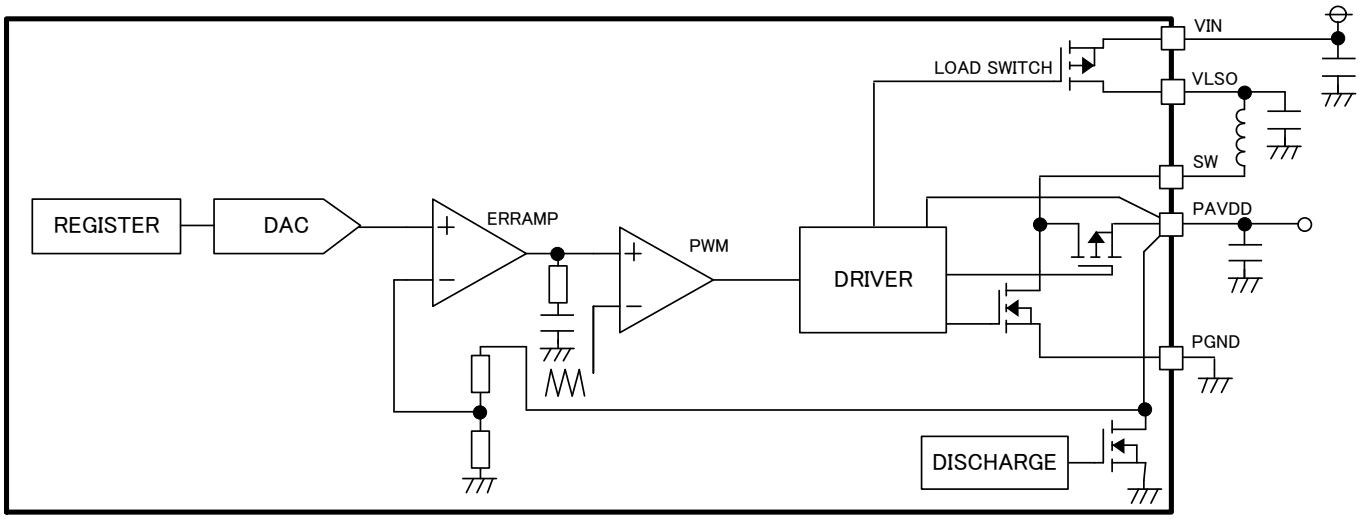

Figure 78. AVDD Block Diagram

AVDD Block (Boost DC / DC) can set the following functions by EEPROM.

1. AVDD Voltage (Register Address 00h [7:0])
   AVDD voltage can be set in 0.1V step from 5.0V to 17.0V.

2. SW Switching Frequency (Register Address 0Ch [1:0])
   The switching frequency can be set at 525KHz, 1.05MHz or 2.1MHz.

3. Soft Start Time (Register Address 0Bh [5:4])
   Soft Start Time of AVDD can be set in 5msec step from 5msec to 20msec.

4. SW Switching Slew Rate (Register Address 0Bh [3:2])
   SW pin switching Slew Rate can be controlled by the register setting.
   11'b is the fastest slew rate setting, 00'b is the slowest slew rate setting.

   The slew rate by each setting is as follows.
   Slew Rate changes by the external part and load electric current conditions such as a coil or the diode, but adjustment is possible on a true set condition because Slew Rate changes by Slew Rate setting change like Figure.79.
   The EMI properties are improved by slowing a slew rate, but please do enough evaluations after a slew rate change because efficiency becomes the tendency to decrease.

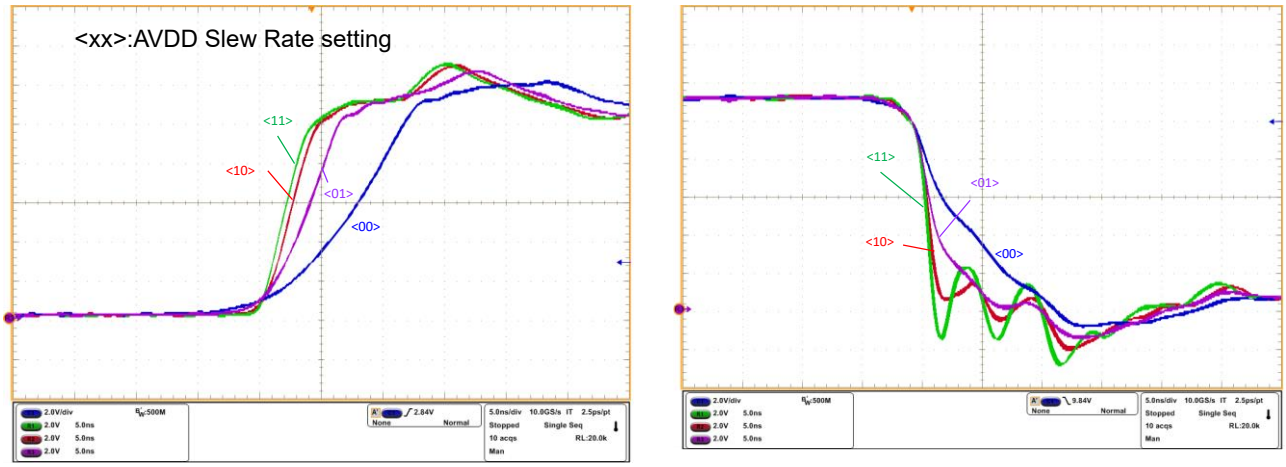

Figure 79. AVDD Switching Slew Rate
(VIN=3.3V, AVDD=10.5V, Freq=2.1MHz, L=4.7µH, IAVDD=100mA)

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AVDD Block Function - continued

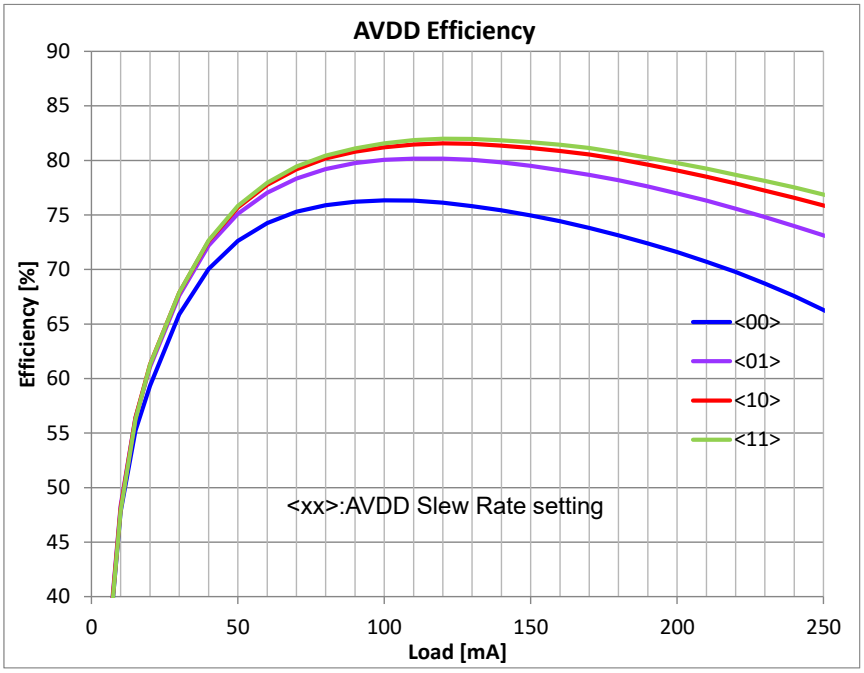

Figure 80. AVDD Efficiency
(dependent on Slew Rate)
(VIN=3.3V, AVDD=10.5V, Freq=2.1MHz, L=4.7µH, IAVDD=100mA)

5. OCP Detect Level (Register Address 0Bh [6])
   SW pin Over Current Protection detection level can be set at 1.0A(Min) or 2.0A(Min).

6. COMP Adjust (Register Address 0B [7])
   Phase Margin can be adjusted.

   0'b: AV_COMP_SET1
   1'b: AV_COMP_SET2

7. COIL Adjust (Register Address 0Bh [1:0])
   You can adjust the settings to match the coil constant to be used.

   00'b:AV_COIL_SET1
   01'b:AV_COIL_SET2
   10'b:AV_COIL_SET3
   11'b:AV_COIL_SET4

Please set the setting of COIL Adjust by frequency setting (fs) and a coil to use.

f_{OSC}[kHz]	Coil[µH]	Coil Adjust 0Bh[1:0]	Comp Adjust 0Bh[7]
525	4.7	00'b	0'b
525	10	11'b	0'b
1050	4.7	00'b	0'b
1050	10	11'b	0'b
2100	4.7	00'b	0'b
2100	10	11'b	0'b

*Please become more than 10µF/25V product (GRT31CC81E106KE01) x3 with AVDD output capacitor at the time of the use with a coil of 10µH.

In addition, COMP Adjust coordinates phase constant of the ERRAMP output and is effective to shift to the zero point 25% low frequency side to produce by the ERRAMP output by making Comp Adjust 1'b and is effective in reducing ringing at the time of the load response by the responsiveness adjustment with the actual machine.

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AVDD Block Function – continued

About the phase characteristic, please consider it based on enough evaluations with the actual model.

(1) Setting the Output L Constant (Boost Converter)

The coil to use for output is decided by the rating current I_{LR} and input current maximum value I_{INMAX} of the coil.

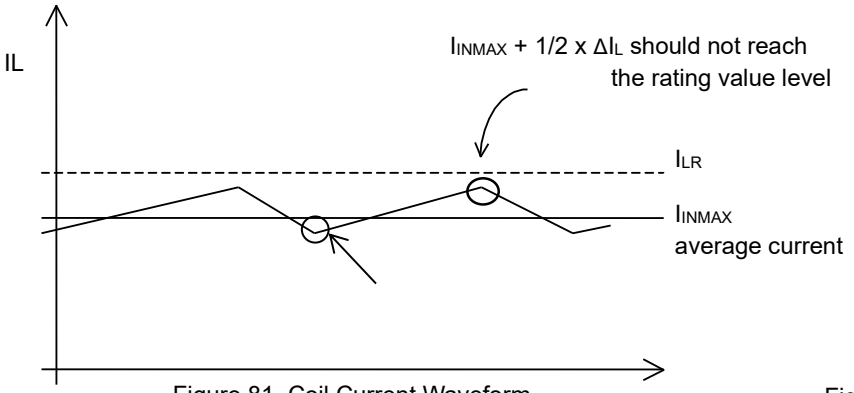

Figure 81. Coil Current Waveform

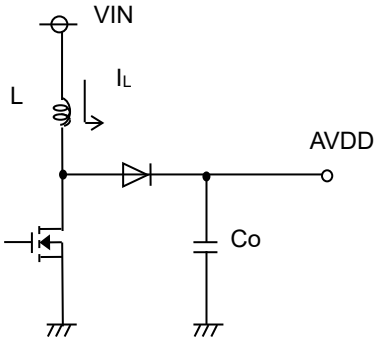

Figure 82. Output Application Circuit Diagram

Adjust so that $I_{INMAX}+\Delta I_L$ does not reach the rating current value I_{LR}. ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} VIN \times \frac{AVDD - VIN}{AVDD} \times \frac{1}{f} \quad [A]$$

Here, f is the switching frequency.

Set with sufficient margin because the coil value may have the dispersion of ±30%. If the coil current exceeds the rating current I_{LR} of the coil, it may damage the IC internal element.

BM81810MUV-M uses the current mode DC/DC converter control and has the optimized design at the coil value. A coil inductance (L) of 4.7 µH to 10 µH is recommended from viewpoints of electric power efficiency, response, and stability.

(2) Output Capacity Settings

For the capacitor to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} allowance value and the drop voltage allowance value at the time of sudden load change. Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{fCo} \times \frac{VIN}{AVDD} \times \left(I_{LMAX} - \frac{\Delta I_L}{2}\right) \quad [V]$$

Here, f is the switching frequency and R_{ESR} is ESR of output capacitor.

Perform setting so that the voltage is within the allowable ripple voltage range.

For the drop voltage during sudden load change; V_{DR}, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{Co} \times 10\,\mu s \quad [V]$$

However, 10 µs is the rough calculation value of the DC/DC response speed. Please set the capacitance considering the sufficient margin so that these two values are within the standard value range.

(3) Selecting the Input Capacitor

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the input side. For the reason, the low ESR capacitor is recommended as an input capacitor which has the value more than 10 µF and less than 100 mΩ. If a capacitor out of this range is selected, the excessive ripple voltage is superposed on the input voltage, accordingly it may cause the malfunction of IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform the margin check using the actual product.

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VGH Block Function

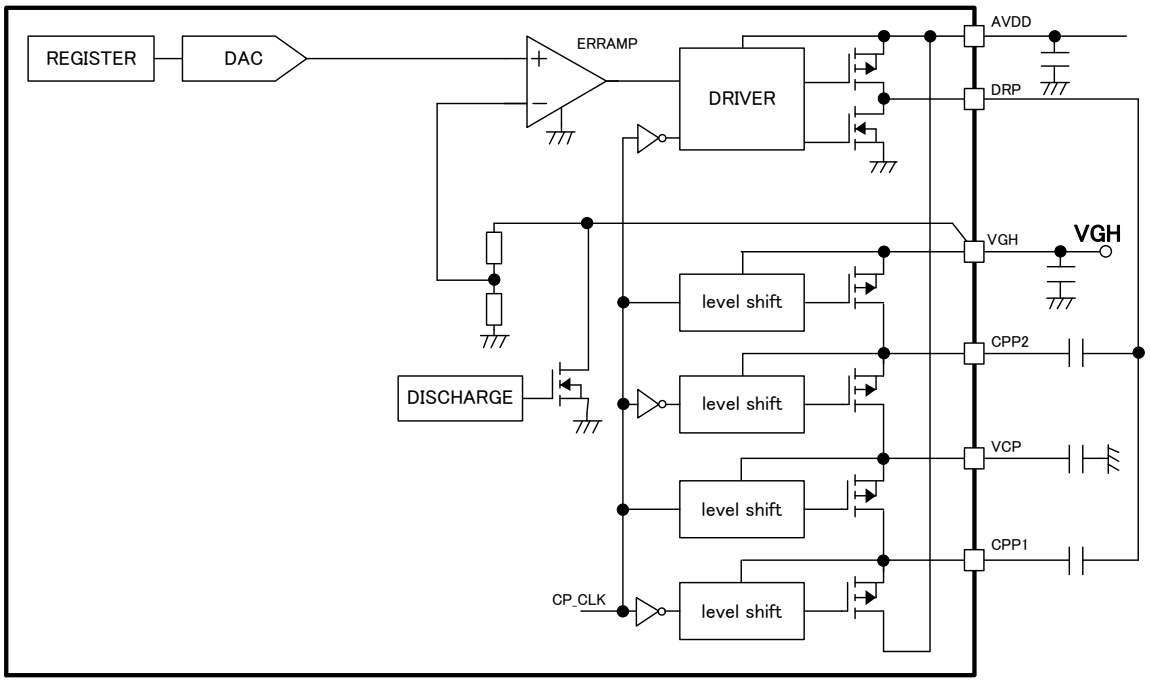

Figure 83. VGH Block Diagram

VGH Block (Positive Charge Pump) can set below functions by EEPROM.

1. VGH (HOT) Voltage (Register Address 01h [7:0])
   VGH (HOT) voltage can be set in 0.2V step from 8.0V to 35.0V.

2. DRP Switching Frequency (Register Address 0Ch [5:4])
   Switching frequency can be set at AVDD frequency x1, x1/2, or x1/4.

3. VGH (COLD) Voltage (Register Address 02h [6:0])
   To set VGH (COLD) voltage can have the VGH voltage relates to NTC Pin voltage, when NTC Function is used.
   VGH (COLD) voltage range can be set in 0.2V step from VGH (HOT) + 0V to VGH (HOT) + 15.0V.
   Refer “NTC Block Function” for the detail description of NTC Function.

4. VGH Mode Select (Register Address 0Ch [6])
   Boost Stage of Positive Charge Pump can be set by x2, x3, or x4.
   x2, x3 can be formed with internal element by EEPROM setting.
   x4 can be formed by connecting with external Diode.
   Since this function switch needs to change the application construction,
   input writing signal by I2C cannot perform Register writing.
   To write this Register setting, start-up bit(REG0Ch[7]) should be ”0”.

   The VGH voltage output range with the AVDD voltage is related, and may take UVP without being able to output the VGH voltage of the setting when do not choose appropriate constitution.
   Please choose appropriate constitution referring after the following pages.

5. VGH Discharge enable (Register Address 0Ah [7])
   When OFF sequence, VGH pin Discharge function can be Enable/Disable.
   This function is to confirm when IC starts to operate. If read-and-write is performed after IC starts, the first time OFF sequence will not be reflected.

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VGH Block Function - continued

Application Example for VGH (3rd Stage Positive Charge Pump)

Depending on the circuit construction, output voltage range of Charge Pump can be limited.

Besides, increasing VGH negative current can lower the possible output voltage.
Please consider the actual application need to select appropriate circuit construction.

Below Figure shows the circuit construction of 3rd Stage Positive Charge Pump.
Under this circuit, the possible setting range of VGH output voltage is (AVDD + 2) V to (AVDD x 3 - 2) V.
(When VGH negative current is 0mA)

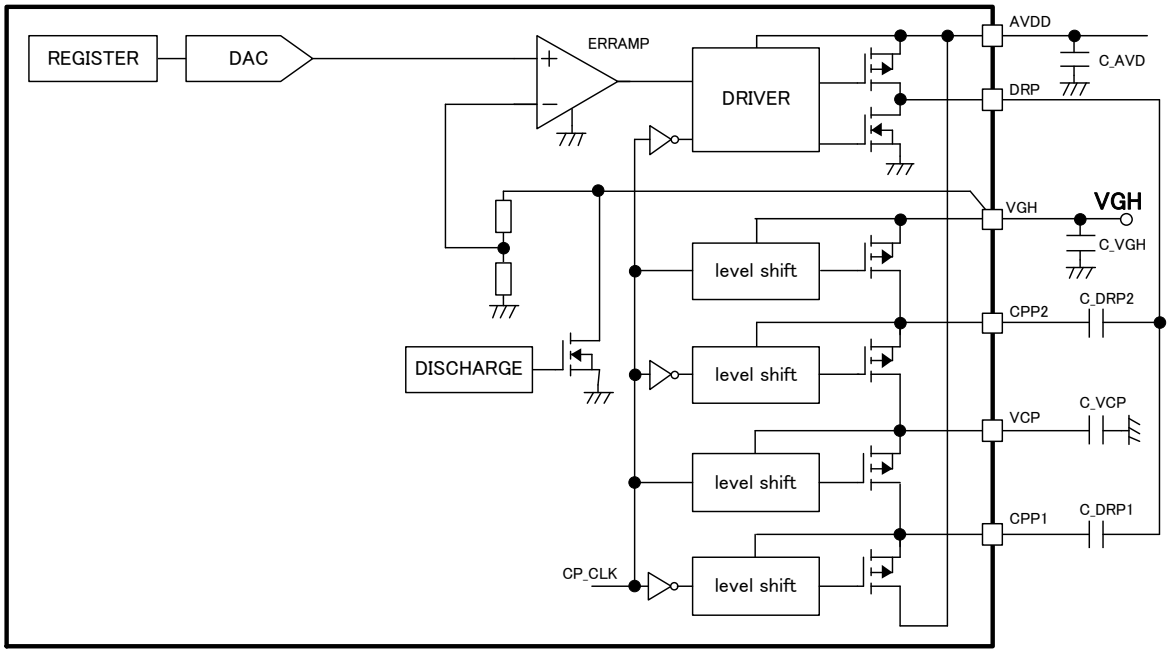

Figure 84. 3rd Stage Positive Charge Pump

Application Example for VGH (2nd Stage Positive Charge Pump)

Below Figure shows the circuit construction of 2nd Stage Positive Charge Pump.
Under this circuit, the possible setting range of VGH output voltage is (AVDD + 1) V to (AVDD x 2-1) V
(When VGH negative current is 0mA)

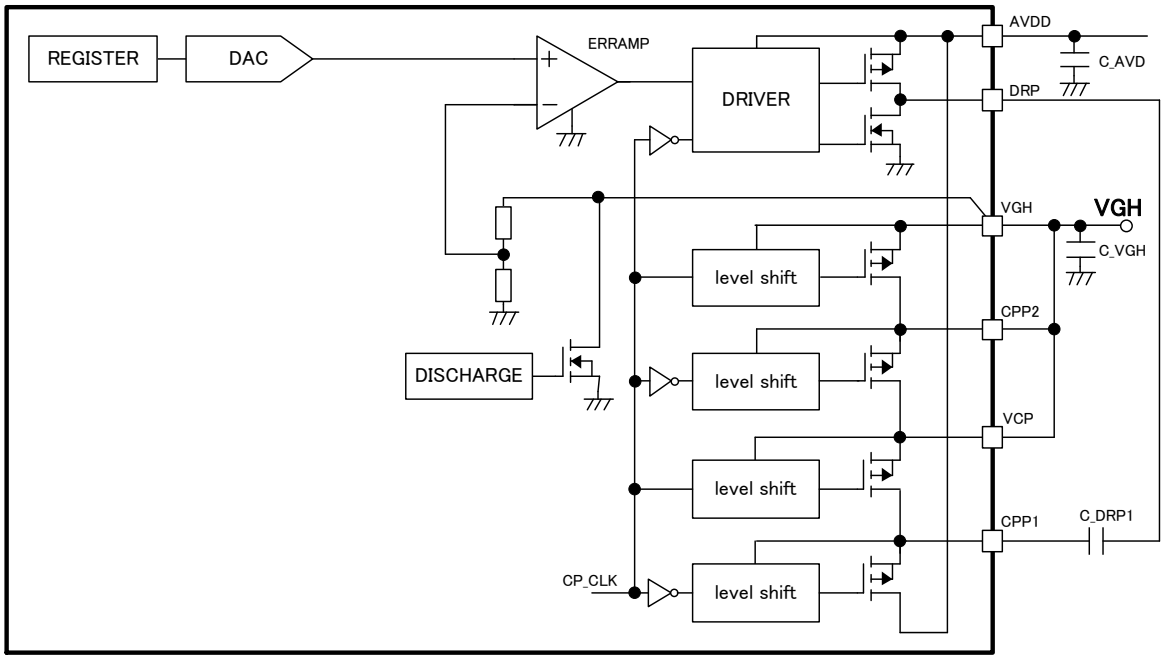

Figure 85. 2nd Stage Positive Charge Pump

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VGH Block Function - continued

Application Example for VGH (4th Stage Positive Charge Pump)

Below Figure shows the circuit construction of 4th Stage Positive Charge Pump.
Under this circuit, the possible setting range of VGH output voltage is (AVDD + 3) V to (AVDD x 4 - 3) V
(When VGH negative current is 0mA)

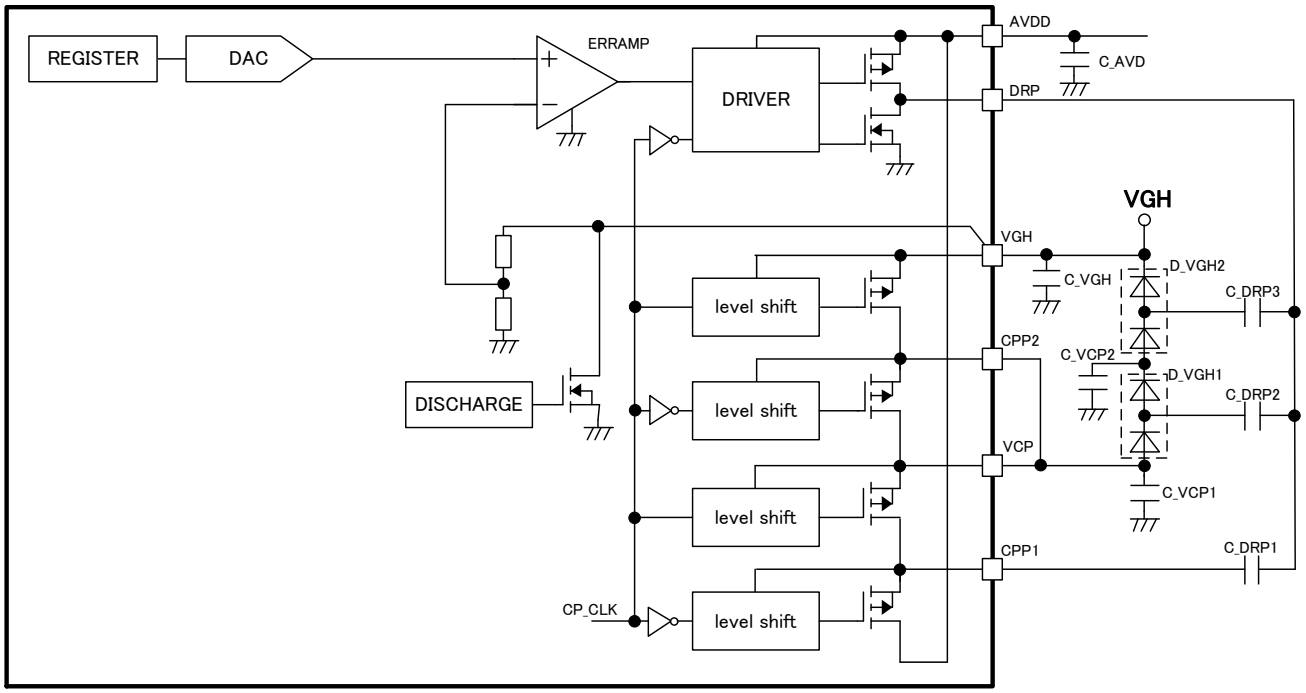

Figure 86. 4th Stage Positive Charge Pump

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VGL Block Function

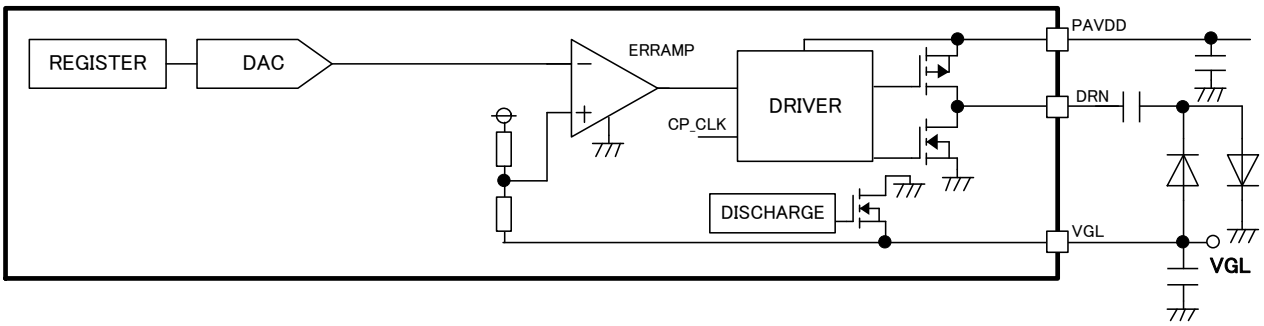

Figure 87. VGL Block Diagram

VGL Block (Negative Charge Pump) can set below functions by EEPROM.

1. VGL Voltage (Register Address 03h [7:0])
   VGL voltage can be set by 0.1V step from -4.0V to -14.0V.

2. DRN Switching Frequency (Register Address 0Ch [5:4])
   Switching frequency can set AVDD frequency x1, x1/2, or x1/4.

Application Example for VGL (1st Stage Negative Charge Pump)

Below Figure shows the circuit construction of 1st Stage Negative Charge Pump.
Under this circuit, the possible setting range of VGL output voltage is -4 V to -(AVDD – 2Vf) V
(When VGL positive current is 0mA)

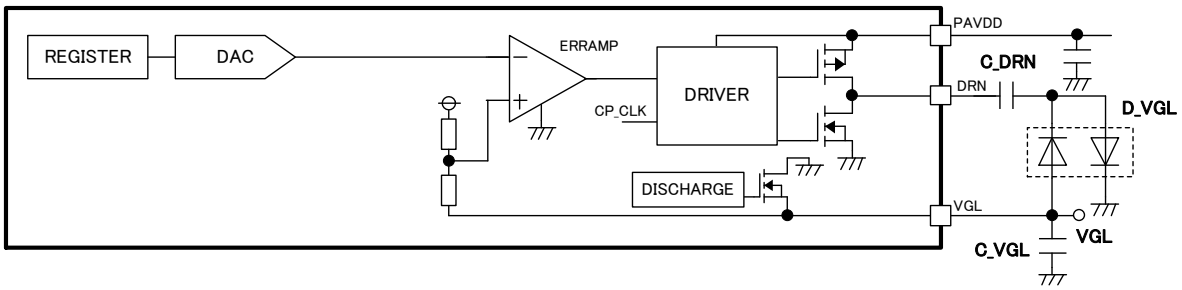

Figure 88. 1st Stage Negative Charge Pump

Application Example for VGL (2nd Stage Negative Charge Pump)

Below Figure shows the circuit construction of 2nd Stage Negative Charge Pump.
Under this circuit, the possible setting range of VGL output voltage is -4 V to -(AVDDx2 – 4Vf) V
(When VGL positive current is 0mA)

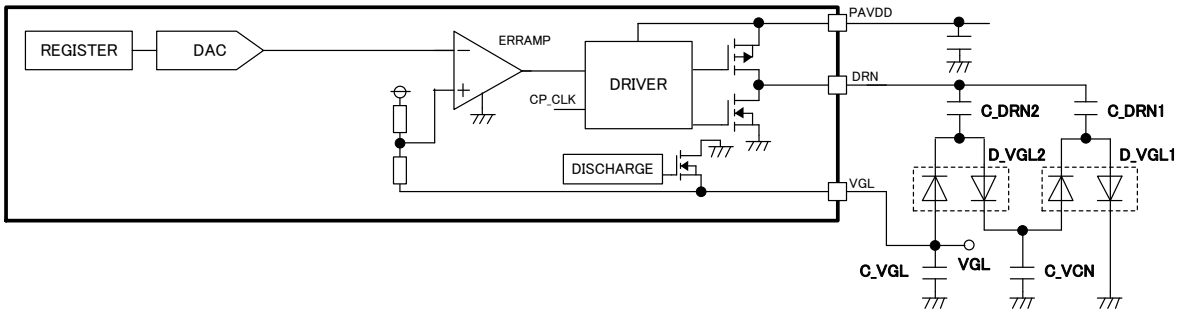

Figure 89. 2nd Stage Negative Charge Pump

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VCOM Block Function

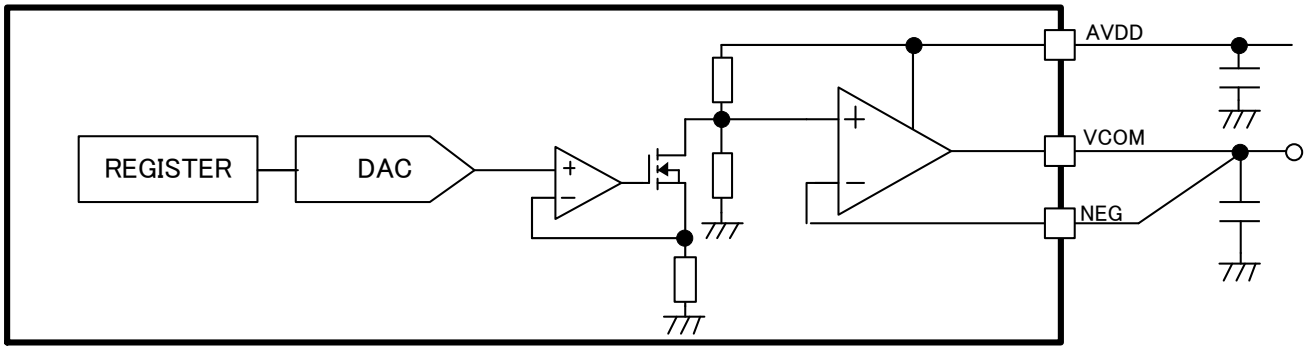


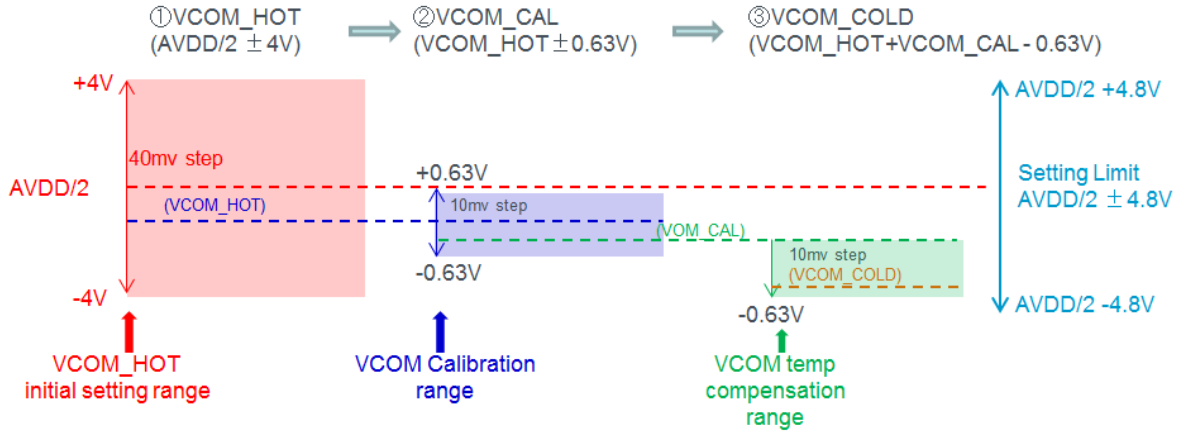
Figure 90. VCOM Block Diagram

VCOM Block (VCOM Calibrator) can set below functions by EEPROM.

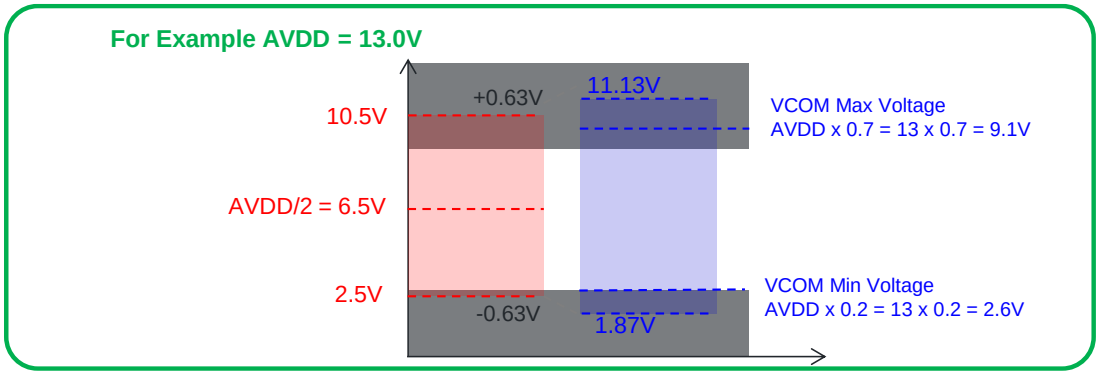
1. VCOM (HOT) Voltage (Register Address 04h [7:0])
   VCOM (HOT) voltage can be set by 40mV step from AVDD/2 +/- 0.0V to 4.0V.

2. VCOM (CAL) Voltage (Device Address 1001111x)
   VCOM (CAL) voltage is the function to make minor adjustment of VCOM (HOT) voltage value.
   VCOM (HOT) can be set by 10mV step from +/- 0.0V to 0.63V.
   Refer Page 19, “EEPROM I2C Format for DVR (VCOM calibrator)” for VCOM (CAL) voltage setting.

3. VCOM (COLD) Voltage (Register Address 05h [6:0])
   To set VCOM (COLD) voltage can have the VCOM voltage relates to NTC Pin voltage, when NTC Function is used.
   VCOM (COLD) voltage range can be set by 10mV step from VCOM (CAL)–0V to VCOM (CAL)+0.63V.
   Refer “NTC Block Function” for the detail description of NTC Function.



However, VCOM output voltage setting range is AVDD x0.7 to AVDD x0.2 or AVDD/2+4.8V to AVDD/2-4.8V.



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VDD Block Function

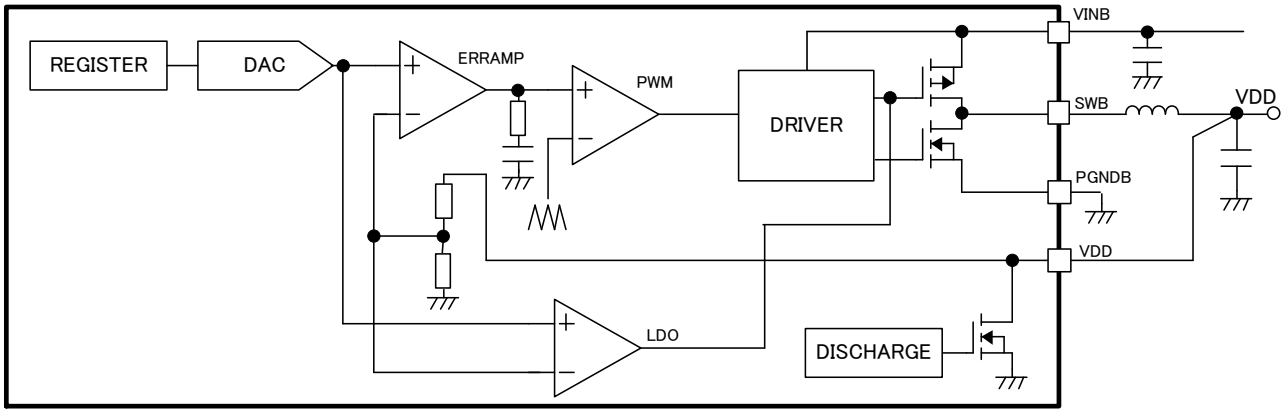

Figure 91. VDD Block Diagram

VDD Block (Buck DC/DC) can set below functions by EEPROM.

1. VDD Voltage (Register Address 06h [5:0])
   VDD voltage can be set by 0.05V step from 0.9V to 3.4V.

2. SWB Switching Frequency (Register Address 0Ch [3:2])
   Switching frequency can be set at 525KHz, 1.05MHz, or 2.1MHz.

3. VDD Phase Adjust (Register Address 06h [7])
   Phase Margin can be adjusted.

   0’b : VD_Phase_Set1
   1’b : VD_Phase_Set2

VIN[V]	VDD[V]	VDD Phase Adjust
5	0.9 to 1.25	1'b
	1.3 to	0'b
3.3	0.9 to	0'b

Set VDD Phase Adjust 1’b when On-duty < 25%.

4. VDD Mode Select (Register Address 06h [6])
   VDD Block can be switched to DC/DC or LDO Mode.
   Since this function switch needs to change the application construction,
   input writing signal by I2C cannot perform Register writing.
   To write this Register setting, start-up bit(REG0Ch[7]) should be ”0”.

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VDD Block Function – continued

Application Example for VDD (Buck DC/DC)

VDD application can select Buck DC/DC or LDO by “VDD Mode Select” of EEPROM setting.
When VDD Mode is selected at ”0”, Buck DC/DC operates.
Below figure shows example of Buck DC/DC application circuit.

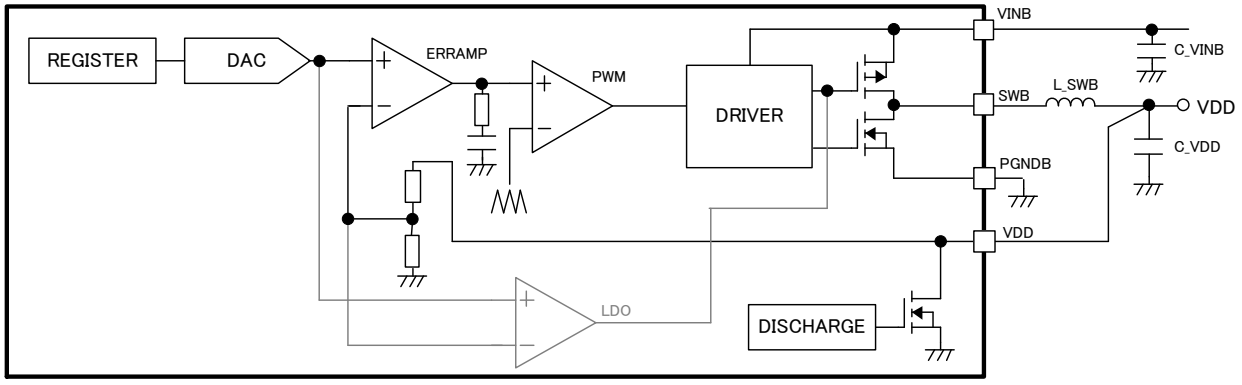

Figure 92. VDD Block Diagram(Buck DC/DC)

Application Example for VDD (LDO)

When VDD Mode is selected at ”1”, LDO operates.
Below figure shows example of LDO application circuit.

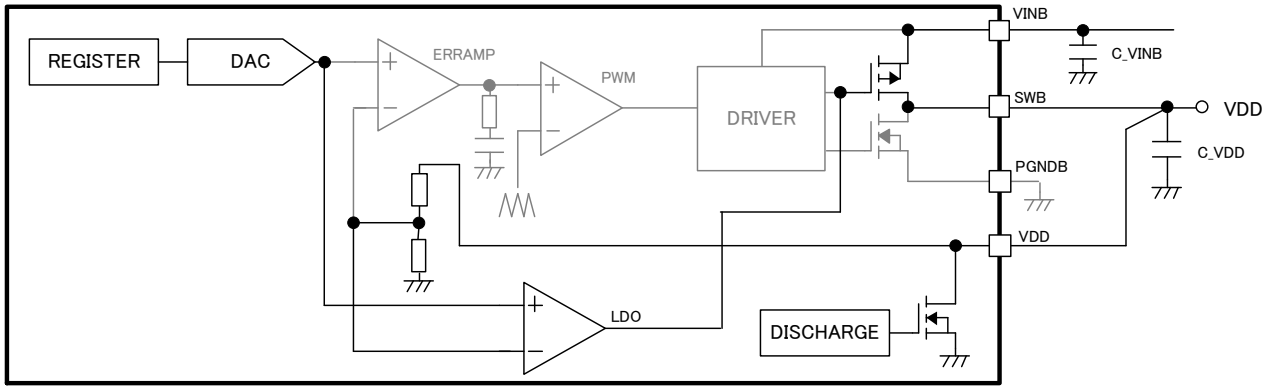

Figure 93. VDD Block Diagram(LDO)

C_VDD in LDO mode, please use 1.0µF to 10µF.

In addition, when VDD function is not used, please set in VDD LDO mode, and, please connect capacitor more than 1.0µF.

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GPM Block Function

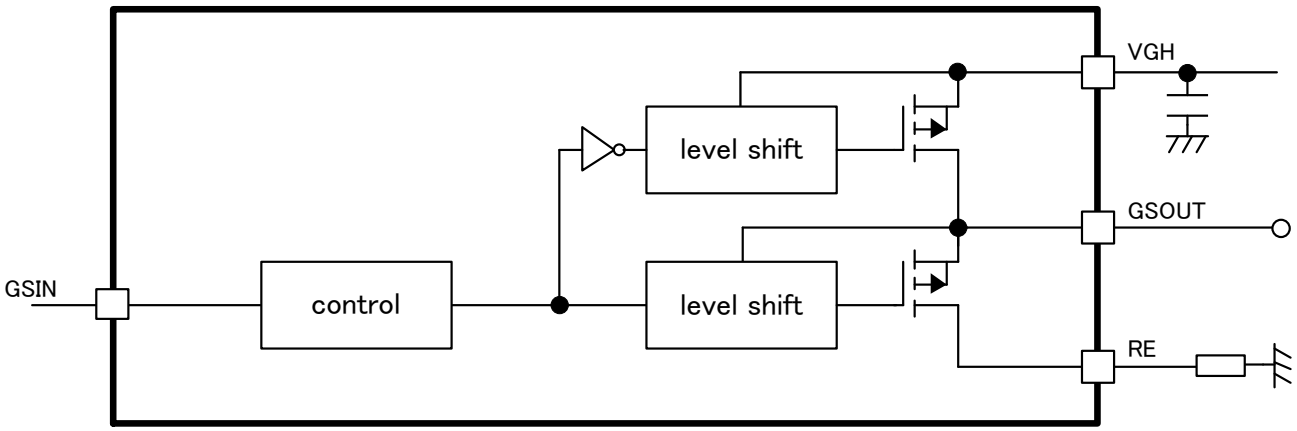

Figure 94. GPM Block Diagram

GPM Block (Gate Pulse Modulation) can set below functions by EEPROM.

1. Input Delay Time (Register Address 07h [7:6])
   Falling timing of input signal can be set at 0.1µsec, 0.5µsec, 1.0µsec, or 1.5µsec.

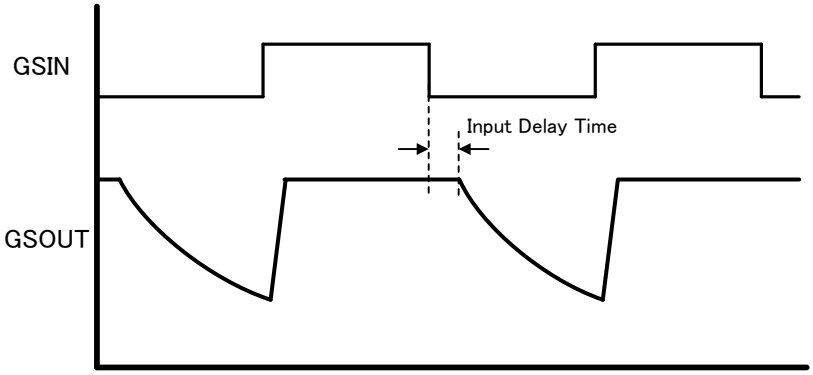

Figure 95. GPM Input Delay Time

Pin connection when GPM is not used

When GPM function is not used, connect GSIN pin to VIN.
Connect RE pin to resistance (2.0kohm).
GSOUT pin should be OPEN.

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RESET Block Function

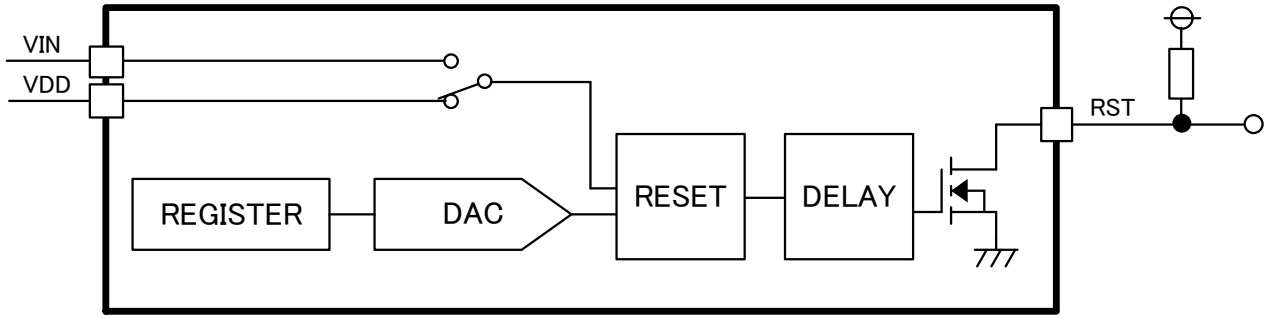

Figure 96. RESET Block Diagram

RESET Block can set below functions by EEPROM.

1. RESET Detect Voltage (Register Address 07h [4:0])
   RESET detection voltage can be set by 0.1V step from 0.6V to 3.3V.

2. RESET Monitor Select (Register Address 07h [5])
   RESET detection pin can select from VDD and VIN.

3. Delay2 Time (Register Address 09h [2:0])
   RESET detection time can be set from 0msec to 40msec.

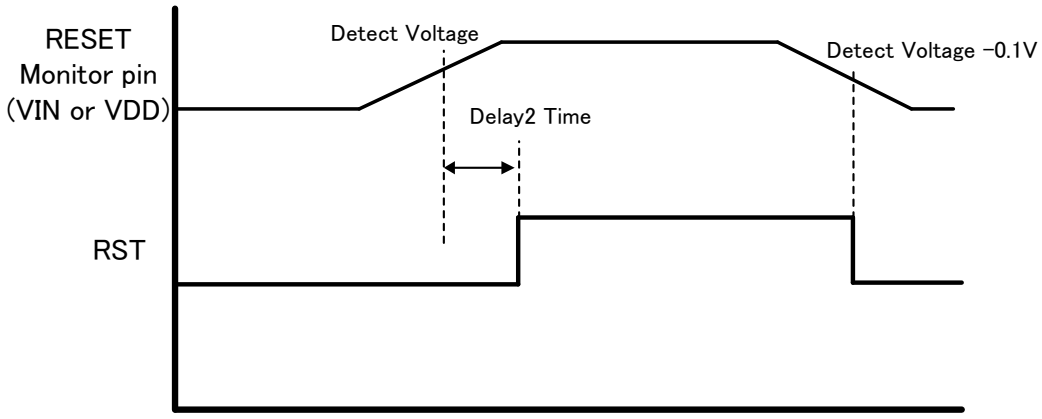

Figure 97. RESET Function

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PG/LDSW Block Function

PG/LDSW Block can switch PG (Power Good) and LDSW (Load Switch) function by EEPROM.

Case of PG Function,
When GPM Block becomes workable, PG pin will change from High to Low to recognize as all boost sequence is completed.

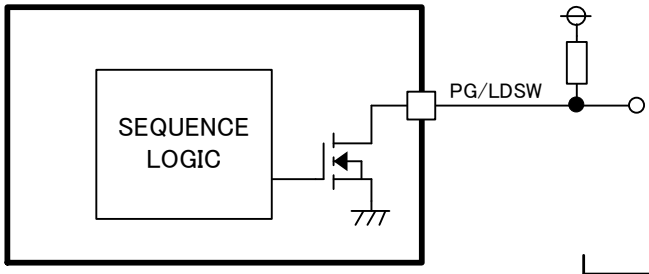


Figure 98. PG/LDSW Block Diagram

Case of LDSW Function,
This function is used when VGL voltage output is prior to AVDD voltage output.
With below application construction, "Timing Chart 3" sequence can be realized.

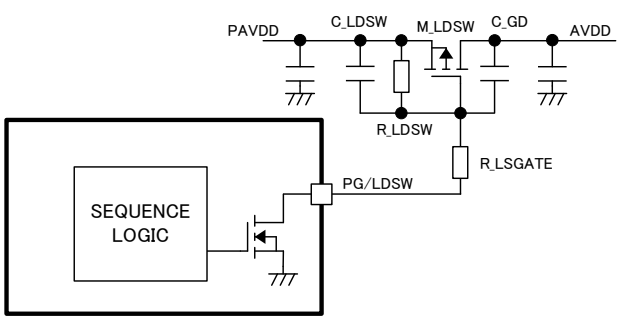
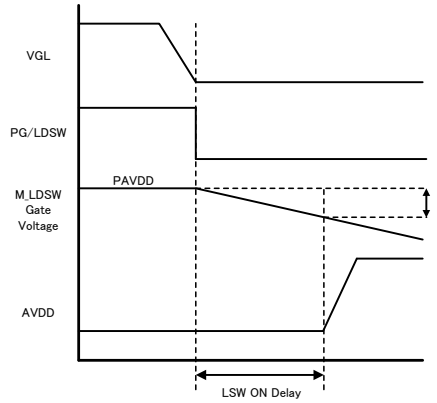


Figure 99. LDSW Function



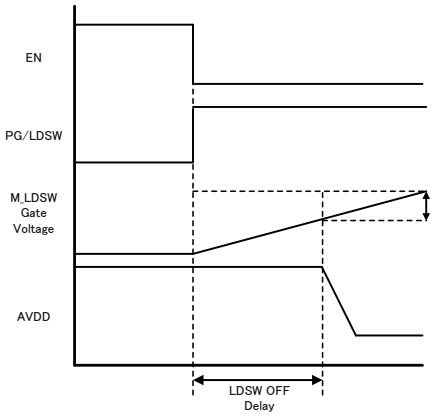


Figure 100. LDSW Delay Time

LDSW on delay can be set by the formula below.

$$LDSW\ ON\ Delay = -C_{LDSW} \times \left(\frac{R_{LSGATE} \times R_{LDSW}}{R_{LSGATE} + R_{LDSW}}\right) \ln\left(1 - \frac{R_{LSGATE} + R_{LDSW}}{R_{LDSW}} \times \frac{Vth}{AVDD}\right)\ [sec]$$

LDSW off delay can be set by the formula below.

$$LDSW\ OFF\ Delay = -C_LDSW \times R_LDSW \times \ln\left(\frac{R_{LSGATE} + R_{LDSW}}{R_{LDSW}} \times \frac{Vth}{AVDD}\right)[sec]$$

where:
AVDD is AVDD setting voltage.
Vth is M_LDSW gate threshold voltage

When using the LDSW function, set the delay3 time to be longer than or equal to the sum of the maximum value including the variation of the load switch ON delay time and VGL soft start time. If the delay3 time setting is short, UVP is applied at startup.

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NTC Block Function

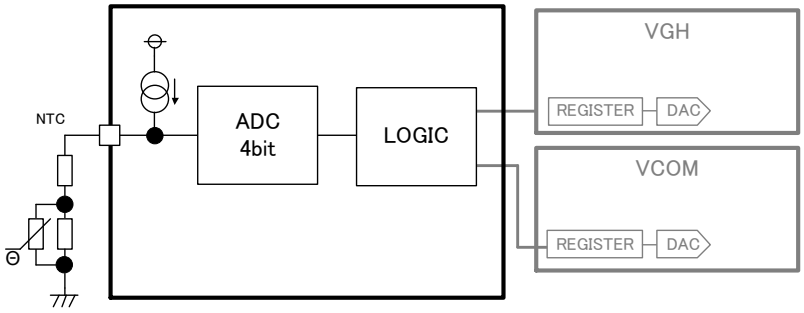


Figure 101. NTC Block Diagram

NTC Block is the function to adjust VGH, VCOM voltage depending on NTC pin voltage.
NTC pin will output 40μA (Typ) current.
Connecting thermistor element can perform temperature adjustment function.

Below functions can be set by EEPROM.

1. VGH NTC Enable (Register Address 02h [7])
   VGH Block NTC Function can be changed to Enable or Disable.

2. VCOM NTC Enable (Register Address 05h [7])
   VCOM Block NTC Function can be changed to Enable or Disable.

Pin connection when NTC is not used.

When NTC function is not used, connect NTC pin to OPEN.

EN Block Function

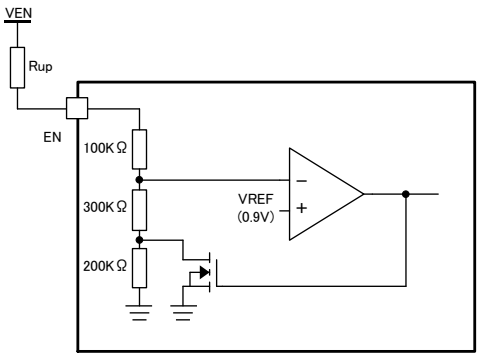
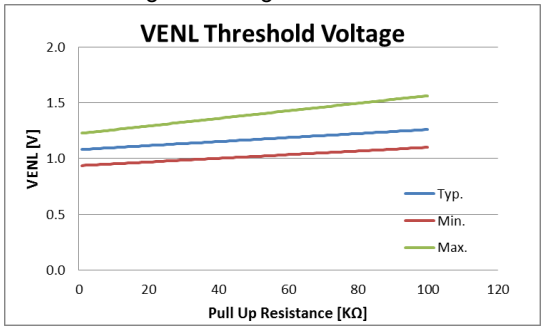


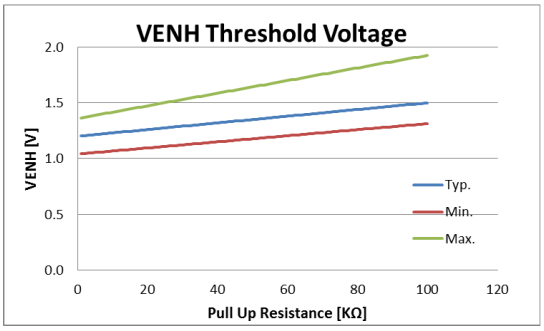
Figure 102. EN Block Diagram

When inserting resistor to EN terminal, EN threshold voltage is decided by resistance division with internal resistor.

Threshold Voltage calculation;
EN threshold voltage high typical (VENH) = 0.9/300x (400+Rup) [V]
EN threshold voltage low typical (VENL) = 0.9/500x (600+Rup) [V]

The EN threshold voltage including unevenness is as follows;





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VGH and VCOM temperature compensation

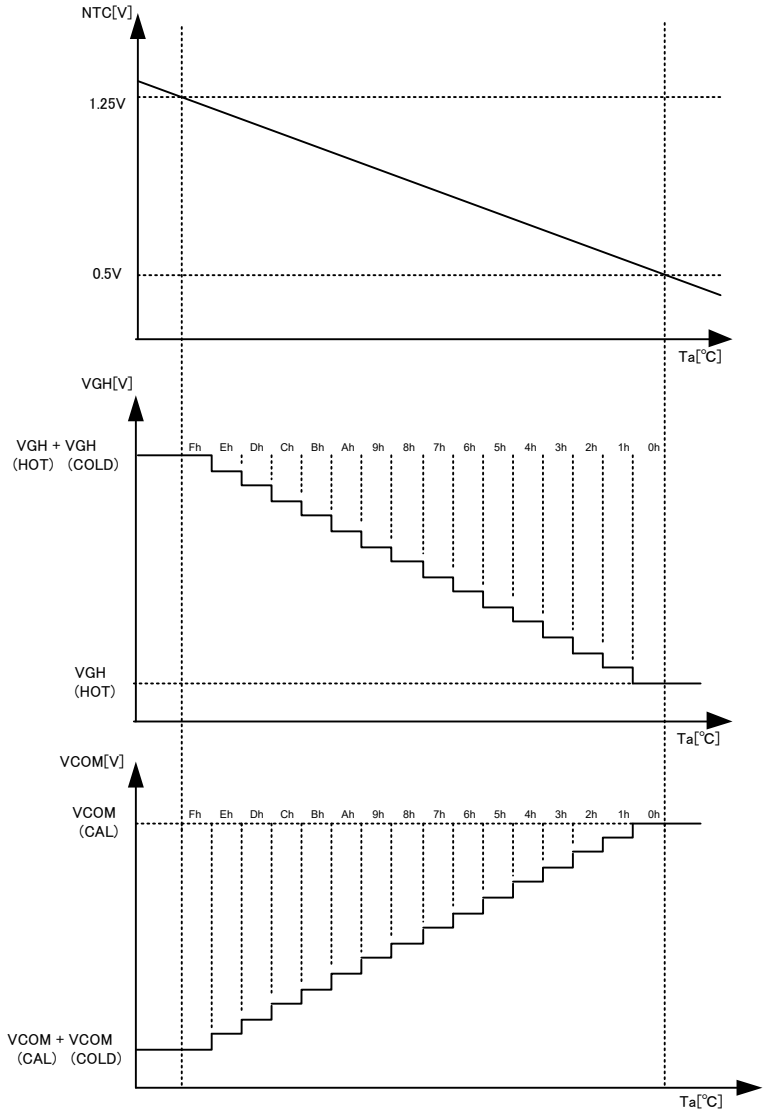

Figure 103. NTC Function

NTC Function can adjust VGH, VCOM voltage depending on NTC voltage (VNTC).
4 bit ADC is used to detect NTC voltage.

When NTC pin voltage VNTC ≤ 0.5V, NTC function will judge as HOT setting.
In this case, VGH and VCOM output voltage can be calculated by below formula.

VGH = VGH (HOT)
VCOM = VCOM (CAL)

When NTC pin voltage VNTC ≥ 1.25V, NTC function will judge as COLD setting.

VGH = VGH (HOT) + ΔVGH (COLD)
VCOM = VCOM (CAL) – ΔVCOM (COLD)

When NTC pin voltage is 0.5V < VNTC < 1.25V, VGH and VCOM can be estimated by below formula.

$$VGH = \frac{\Delta VGH(COLD)}{\mathbf{15}} * \left(ROUNDUP\left(\frac{VNTC - 0.5V}{0.047V}\right) - \mathbf{1}\right) + VGH(HOT)\ [\mathrm{V}]$$

$$VCOM = VCOM(CAL) - \frac{\Delta \mathrm{VCOM}(COLD)}{\mathbf{15}} * \left(ROUNDUP\left(\frac{VNTC - 0.5V}{0.047V}\right) - \mathbf{1}\right)\ [V]$$

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FAULT Block Function

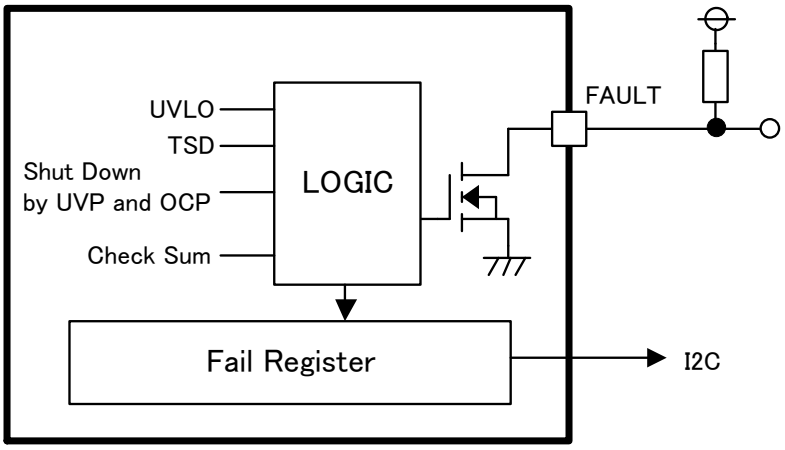

Figure 104. FAULT Block Diagram

FAULT Function is to inform IC situation to outside.
When the operation is normal, FAULT pin will be High.
When the operation is abnormal, FAULT pin will be Low.

Below are the conditions to have FAULT pin to Low.
I. Detect UVLO
II. Start TSD
III. Shutdown by UVP or OCP
IV. Check Sum NG

Fail Register Function

When FAULT PIN is Low, it is possible to confirm which protection circuit is activating by reading Data from Fail Register.

Fail Register will reflect the protection detected circuit at the moment of FAULT=Low
Register Address of Fail Register is 10h.

Register Address	D7	D6	D5	D4	D3	D2	D1	D0
10h	AVDD UVP	VDD UVP	VGH UVP	VGL UVP	Double Register Error	AVDD OCP	TSD	Check sum Error

Fail Register does not have EEPROM writing function.
When VIN UVLO is detected, the data will be deleted.

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Protection function explanation of POWER MANAGEMENT block

I. UNDER VOLTAGE LOCK OUT (UVLO)
The BM81810MUV-M has UVLO function for VIN and a circuit miss-operation during in under UVLO voltage operation is prevented. If VIN below UVLO voltage, it shuts down VDD, AVDD, VGH, VGL, GPM, VCOM and RESET.

II. THERMAL SHUTDOWN (TSD)
The BM81810MUV-M incorporates a Thermal Shut Down (TSD) function. If IC temperature exceeds 175°C (TYP), it shuts down VDD, AVDD, VGH, VGL, GPM, VCOM and RESET.

III. UNDER VOLTAGE PROTECTION (UVP)
This block has Under Voltage Protection (UVP) function for VDD, AVDD, VGH and VGL output.
When detecting UVP, inner Counter will be activated, and after 5ms passed, it shuts down VDD, AVDD, VGH, VGL, GPM, and VCOM. (It also shuts down RESET when RESET monitors VDD voltage.)

IV. OVER VOLTAGE PROTECTION (OVP)
This block has Over Voltage Protection (OVP) function for AVDD output.
When detecting OVP, output voltage rising is limited by forcing Switching turn off. If output voltage falls, Switching is restarted.

V. OVER CURRENT PROTECTION (OCP)
This block has Over Current Protection (OCP) function for VDD and AVDD.
When detecting OCP, it controls Switching and limits generating over current in FET.

BLOCK	Protective Function	Working Condition	Action	Protective removal
VDD	Over current Protection (Buck DCDC mode)	ISWB > 1.0 A (Min)	Control switching pulse duty to not over current limit	ISWB < 1.0 A (Min)
	Over current Protection (LDO mode)	ISWB > 0.3 A (Min)	Control LDO to not over current limit.	ISWB < 0.3 A (Min)
	Under Voltage Protection	Detect : VDD<Target value x 0.8 Release : VDD>Target value x 0.9	IC shutdown if UVP status maintains during 5msec	IC restart
AVDD	Over Voltage Protection	AVDD > (Target value x 1.1)	Switching STOP	AVDD < (Target Value x 1.05)
	Over current Protection	ISW > 1.0 A (Min) or 2.0 A (Min)	Control switching pulse duty to not over current limit	ISW < 1.0 A (Min) or 2.0 A (Min)
			IC shutdown if OCP status maintains during 5msec	IC restart
	Under Voltage Protection	Detect : AVDD<Target value x 0.8 Release : AVDD>Target value x 0.9	IC shutdown if UVP status maintains during 5msec	IC restart
VGH	Under Voltage Protection	Detect : VGH<Target value x 0.8 Release : VGH>Target value x 0.9	IC shutdown if UVP status maintains during 5msec	IC restart
VGL	Under Voltage Protection	Detect : VGL>Target value x 0.8 Release : VGL<Target value x 0.85	IC shutdown if UVP status maintains during 5msec	IC restart
General	Under Voltage Lockout	VIN < 2.0V (Min)	IC shutdown	VIN > 2.55V (Typ)
	Thermal shutdown	Tj > 175°C (Typ)	IC shutdown	Tj < 150°C (Typ)

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Double Register

BM81810MUV-M can perform various setting by Register.

If these settings are changed without intension, to avoid application abnormal operation, certain specific Register has error detection function.

Below shows the Register with anomaly detection function.

Register Address	D7	D6	D5	D4	D3	D2	D1	D0
00h	AVDD Output Voltage							
01h	VGH HOT Output Voltage							
02h	VGH NTC Enable	⊿VGH COLD Voltage						
03h	VGL Output Voltage							
04h	VCOM HOT Output Voltage							
05h	VCOM NTC Enable	VCOM COLD Votlage						
06h	VDD Phase	VDD MODE	VDD Output Voltage					
07h	GPM Input Delay		Reset Monitor Select	Reset Voltage				
08h	Function Select	Delay1 time				Discharge time		
09h	Data Refresh	Delay3 time			DoubleReg	Delay2 time		
0Ah	VGH Discharge Enable	Delayt5 time			AR_Time	Delay4 time		
0Bh	AVDD COMP	AVDD OCP Select	AVDD SS Time		AVDD SW Slew Rate		AVDD COIL	
0Ch	Start-up Bit	VGH mode select	VGH/VGL Frequency		VDD Frequency		AVDD Frequency	
0Dh	Check Sum							
10h	AVDD UVP	VDD UVP	VGH UVP	VGL UVP	Double Register Error	AVDD OCP	TSD	Check sum Error

Double Register correspond BIT

Data Refresh

Data Refresh is the Function to read Data from EEPROM periodically.
If Register setting is suddenly changed without intension, Data Refresh function can read Data from EEPROM to recover to the normal Data.

Data Refresh performs at certain cycle period.
The time of period can be set by Register at 0.5sec or 1.0sec.

In the case of WPN=Low, Double Register Function and Data Refresh Function can be set by Register as Enable or Disable.
Below table shows the function by each combination.

In the case of WPN=High, Double Register Function and Data Refresh Function are Disable.

WPN	Data Refresh	Double Register	Data Refresh Operation	Double Register Check
Low	0 : Disable	0 : Disable	Disable	Disable （Keep working even logic abnormality happens）
Low	0 : Disable	1 : Enable	Disable	Enable （First shutdown once logic abnormality detects. After Fault to be low for 1msec, then re-start）
Low	1 : Enable	0 : Disable	Enable （Data Refresh at set period）	Disable （Keep working even logic abnormality happens）
Low	1 : Enable	1 : Enable	Enable （Data Refresh at set period）	Enable (Perform Data Refresh once logic abnormality detects)
High	-	-	Disable	Disable （Keep working even logic abnormality happens）

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PCB Layout Guide

GND Wiring Pattern

The high current GND (PGND) should be wired thick. To reduce line impedance, the GND lines must be as short and thick as possible and uses few via. Therefore design at PCB board four layers or above is recommended. (Please use the middle layer as GND shielding and directly connect each GND.) In the case of two layers or less at PCB board designs, please enough confirm with the actual model about the heat and the noise with care to a GND wiring.

Switching-Line Wiring Pattern

The wiring from switching line (SW pin) of DC/DC converter to inductor and diode must be as short and thick as possible. If a wiring is long, ringing by switching increases, and the voltage over the resistance of this IC might be generated. Please note that switching line does not vary PCB layer.
Switching line and wiring easily affected by noise such as feedback line must be placed separately.
Switching noise spread may cause the lack of operation stability. In case the multi-layer PCB board, please note that a switching line and a line easily affected by noise or the external components are not adjacent between layers.
Drawing GND shield line between switching line and these lines easily affected by noise is recommended if these lines are placed close.

Power Supply Voltage Line Wiring Pattern

For power supply voltage (VIN, VINB, VLSO, PAVDD, AVDD, VGH), place smooth capacitor nearby IC pin.
Please note that smooth capacitor does not vary PCB layer.

The figure 105 shows an application circuit on the basis of the basic PCB layout pattern guideline mentioned above.

- Bold line: High current line
- Blue line(two dots and dashed line): Wiring easily affected by noise
- Red line (dashed line): Noise source line such as switching line.
- Place smooth capacitor nearby IC pin
- D_SW locates it near SW terminal / PAVDD terminal of BM81810MUV-M, and a current loop of SW terminal ••• SBD ••• PAVDD, please become as short as possible.

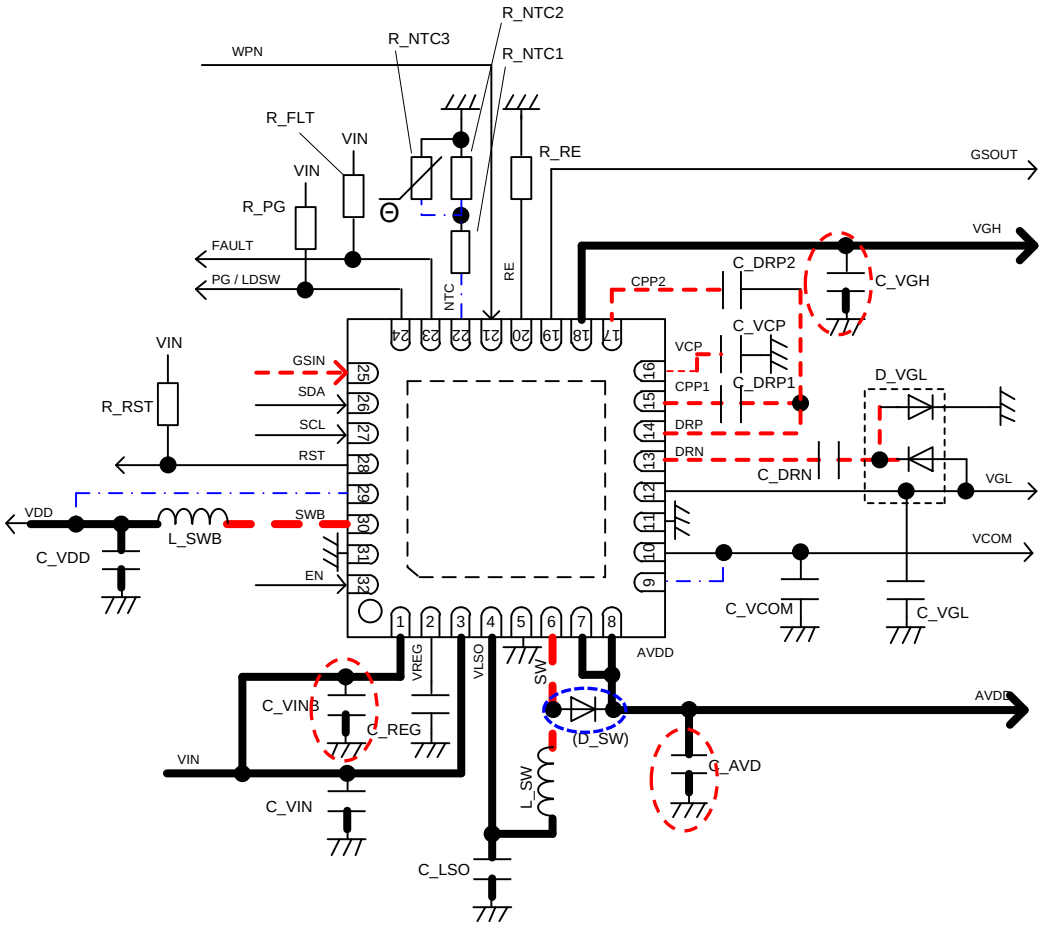

Figure 105. PCB Layout Indications

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EMC Layout Guide

Introduce the plan that can design on the PCB as EMC measures.

Measures by the board pattern
- •Wire AVDD line briefly thickly. (1)
- •Wire the current loop of Boost DC/DC briefly thickly. (2)

Measures by the external component
- •Insert a common mode filter or a beads coil in the AVDD line and form the EMC filter. (3)
- •Place output capacitor and small capacitor (10pF - 1,000pF) in parallel. (4)
- •Insert the snubber circuit in SW pin. (Assumed the efficiency becomes worse) (5)

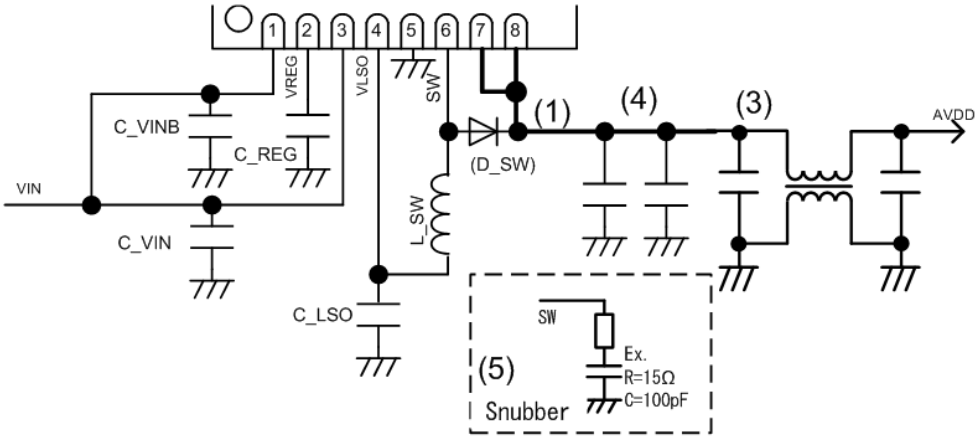

Figure 106. EMI Circuit 1

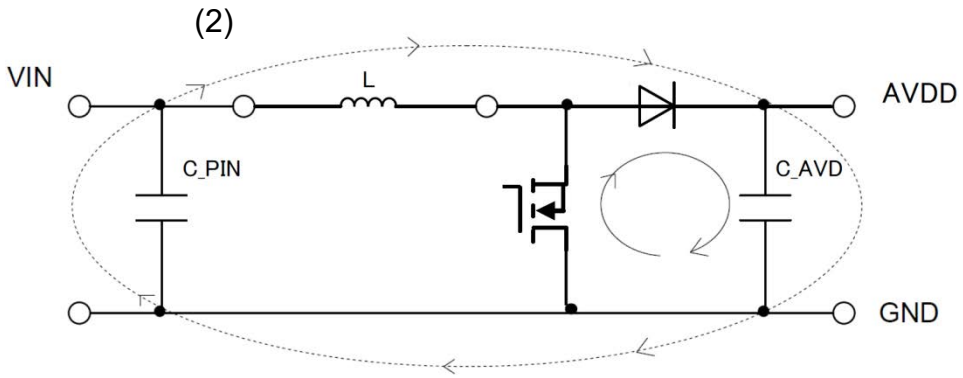

Figure 107. EMI Circuit 2

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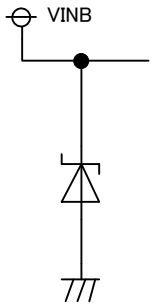
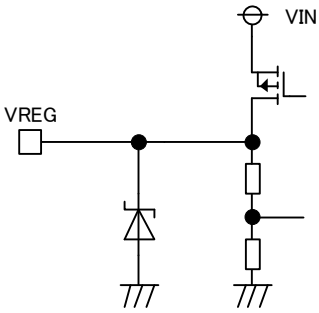
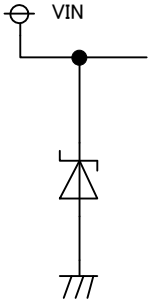
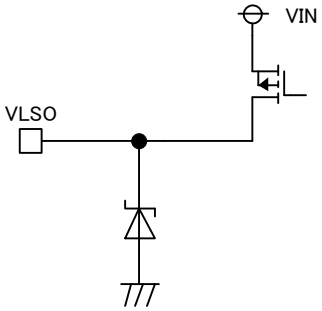
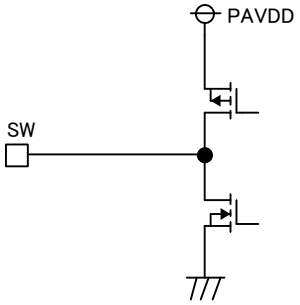
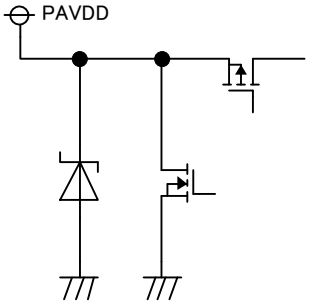
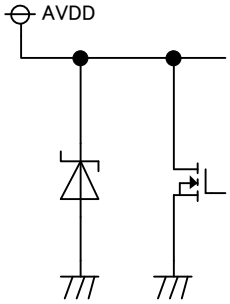
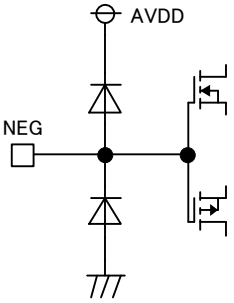
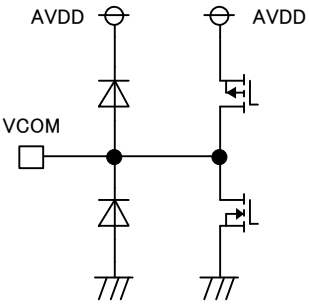
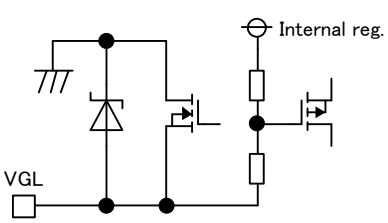
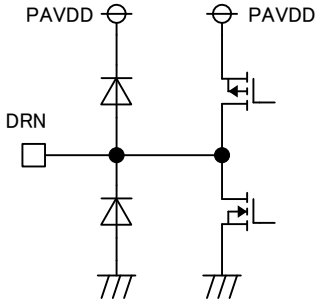
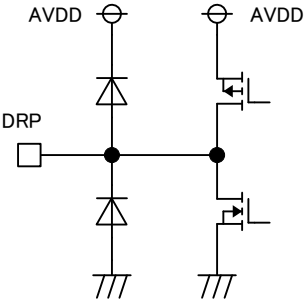
I/O Equivalence Circuit

1. VINB	2. VREG	3. VIN
		
4. VLSO	**6. SW**	**7. PAVDD**
		
8. AVDD	**9. NEG**	**10. VCOM**
		
12. VGL	**13. DRN**	**14. DRP**
		

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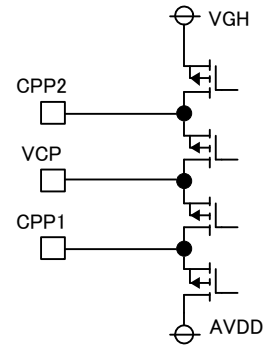
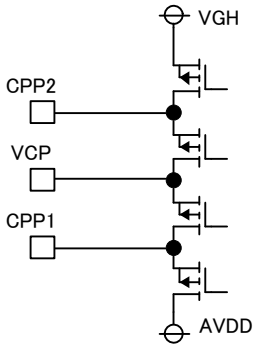
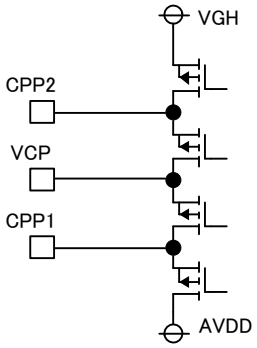
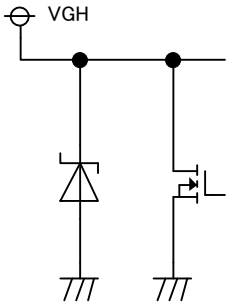
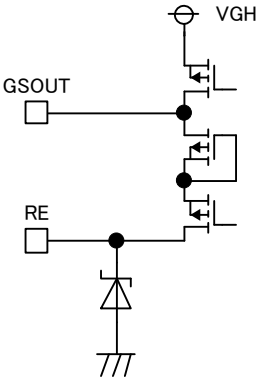
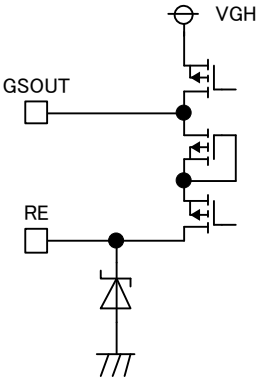
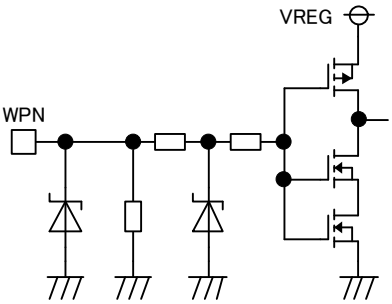
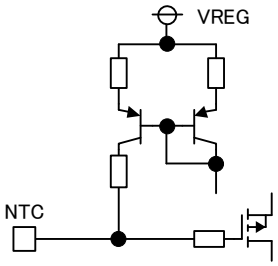
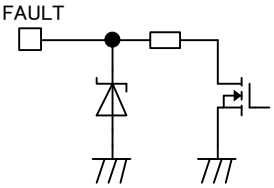
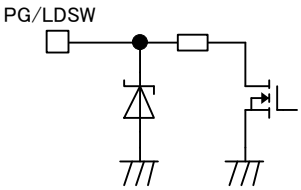
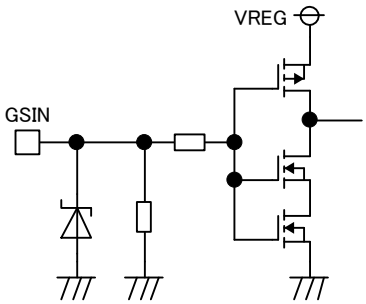
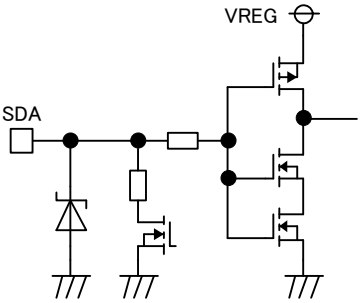
I/O Equivalence Circuit - continued

15. CPP1	16. VCP	17. CPP2
		
18. VGH	**19. GSOUT**	**20. RE**
		
21. WPN	**22. NTC**	**23. FAULT**
		
24. PG/LDSW	**25. GSIN**	**26. SDA**
		

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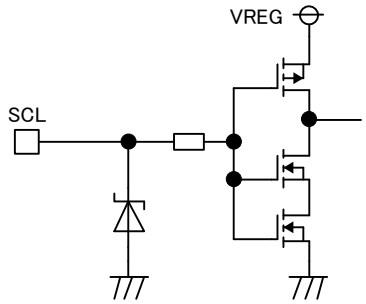
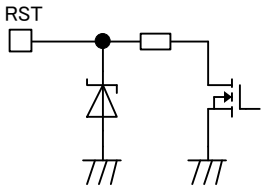
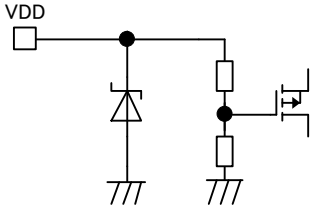
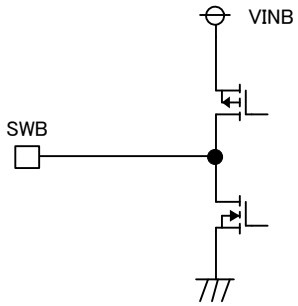
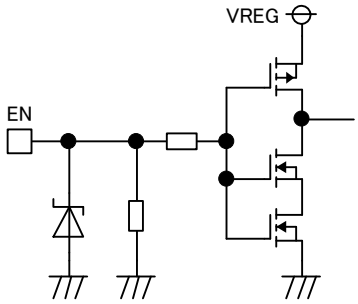
I/O Equivalence Circuit - continued

27. SCL	28. RST	29. VDD
		
30. SWB	**32. EN**	
		

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Operation Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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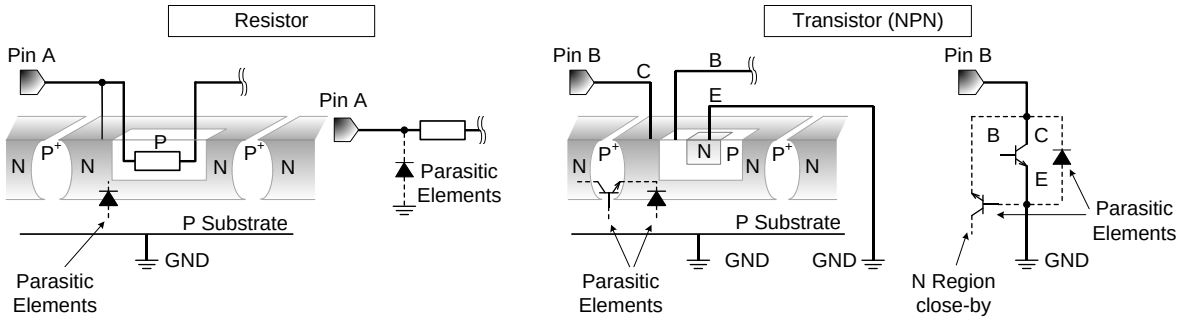
Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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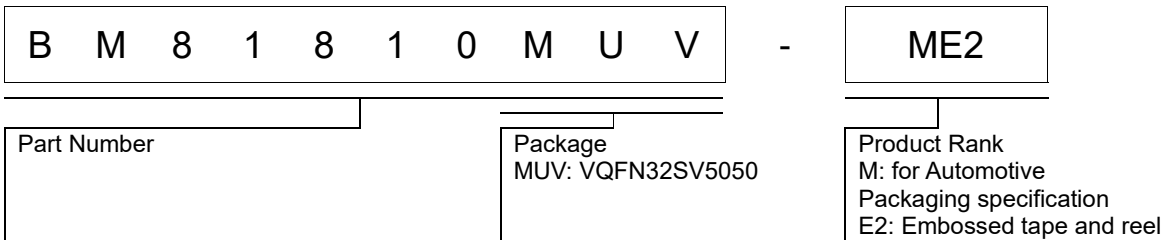
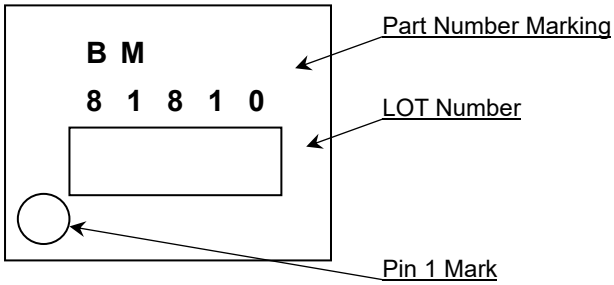
Ordering Information



Marking Diagram

VQFN32SV5050(TOP VIEW)



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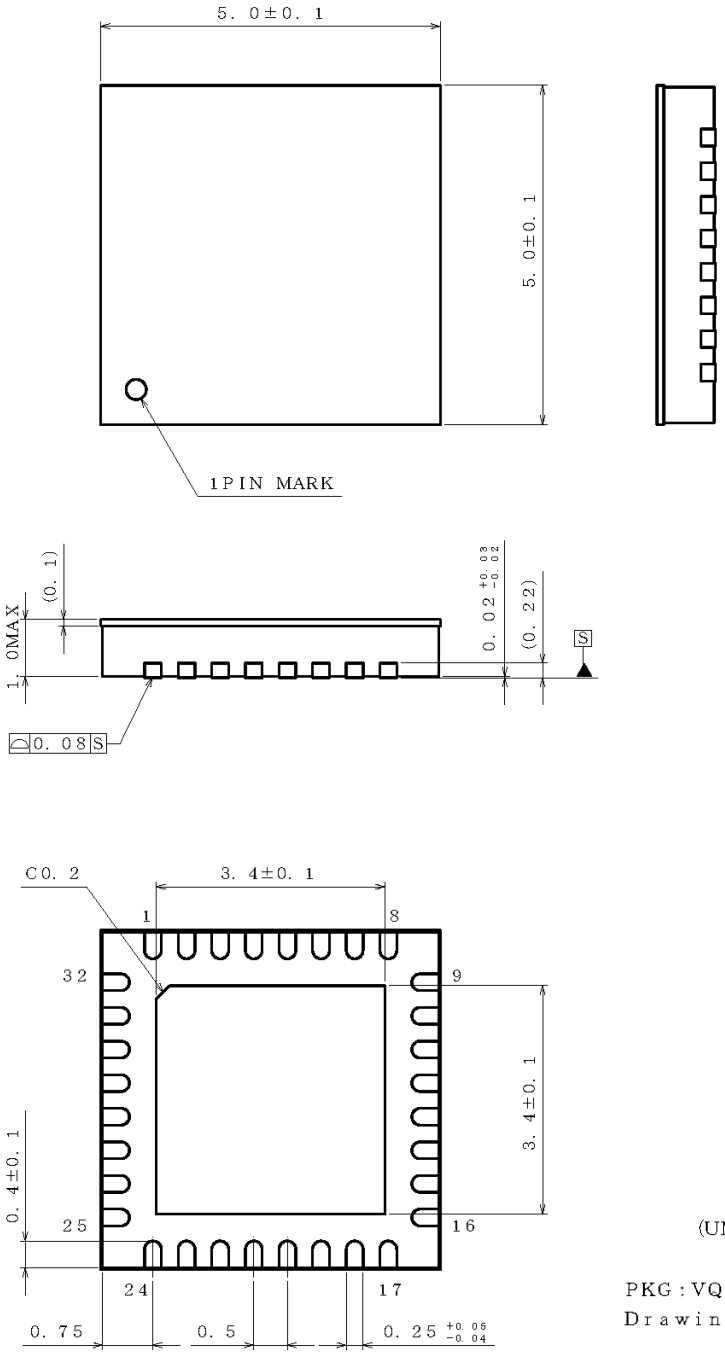
Physical Dimension, Tape and Reel Information

Package Name	VQFN32SV5050

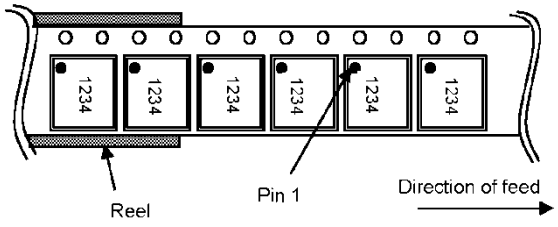


(UNIT : mm)

PKG : VQFN32SV5050
Drawing No. EX385-5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
25.July.2016	001	New Release
10.Jan.2019	002	AVDD Current Limit (1A setting) Limit Maximum 3.0A -> 2.5A (P.6)
		Remove WPN pin from input tolerant. (P.1)
		Describe the package name in detail. (P.1)
		Change absolute maximum ratings value of WPN pin. (P.4)
		Add C_GD to application circuit when using LDSW mode.(P.31, P32)
		Correct some minor typographical errors.
9.Dec.2020	003	Updated packages and part numbers. P.75-2, P.75-3

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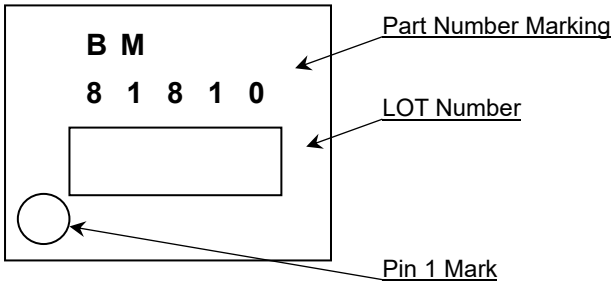
Ordering Information

B M 8 1 8 1 0 M U V	-	MZE2

- Part Number
- Package
  MUV: VQFN32SV050A
- Product Rank
  M: for Automotive
  Production site
  Z: Added
  Packaging specification
  E2: Embossed tape and reel

Marking Diagram

VQFN32SV050A(TOP VIEW)



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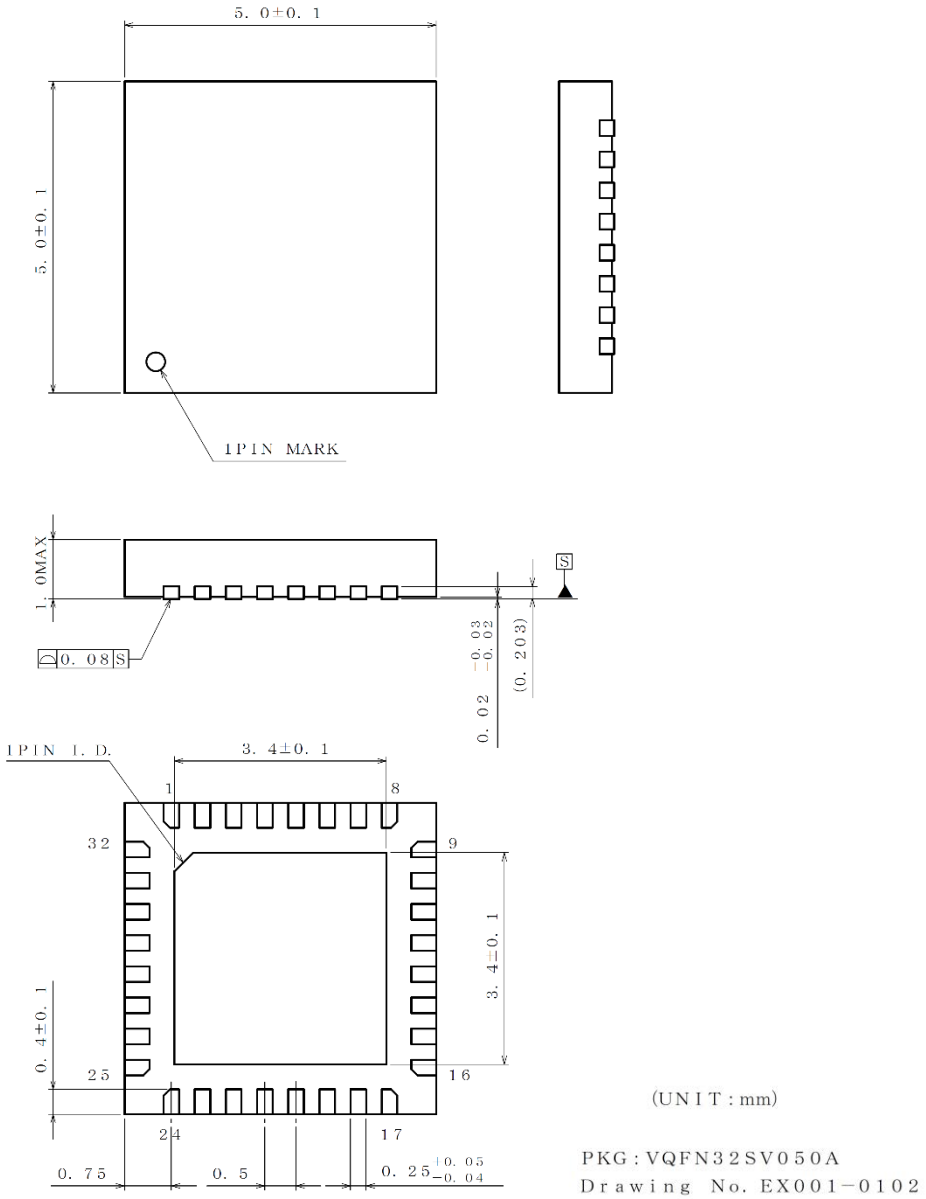
Physical Dimension, Tape and Reel Information

Package Name	VQFN32SV050A



(UNIT : mm)

PKG : VQFN32SV050A
Drawing No. EX001−0102

< Tape and Reel Information >

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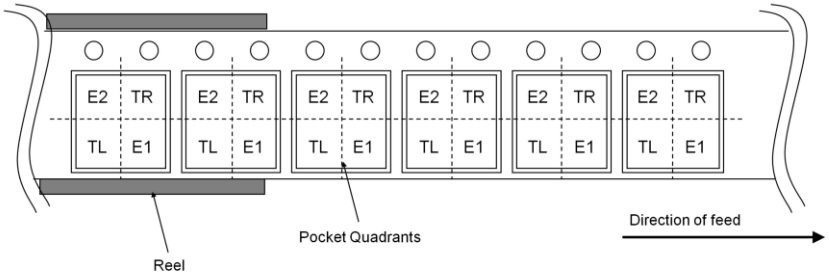
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



E2 : PIN1 is placed to the top left corner.
TR : PIN1 is placed to the top right corner.
TL : PIN1 is placed to the lower left.
E1 : PIN1 is placed to the lower right.

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Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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