THE DATASHEET OF

BQ24188YFFT

bq24188 2A, 30V, Host-Controlled Single-Input, Single Cell Switchmode Li-Ion Battery Charger with Power Path Management and USB-OTG Support

1 Features

- Charge Time Optimizer (Enhanced CC/CV Transition) for Faster Charging
- Integrated FETs for Up to 2A Charge Rate at 5% Accuracy and 93% Peak Efficiency
- Boost Capability to Supply 5V at 1A at IN for USB OTG Supply
- Integrated 17mΩ Power Path MOSFET and optional BGATE control to Maximize Battery Life and Instantly Startup From a Deeply Discharged Battery or No Battery
- 30V Input Rating with Over-Voltage Protection Supports 5V USB2.0/3.0 and 12V USB Power Delivery
- Small Solution Size In a 2.4mm x 2.4mm 36-ball WCSP or 4mm x 4mm QFN-24 Package
  - Total Charging Solution Can be 50mm^2 or less with WCSP
- Safe and Accurate Battery Management Functions Programmed Using I^{2}C Interface
  - Charge Voltage, Current, Termination Threshold, Input Current Limit, V_{IN_DPM} Threshold
  - Voltage-based, JEITA Compatible NTC Monitoring Input
  - Thermal Regulation Protection for Input Current Control
  - Thermal Shutdown and Protection

2 Applications

- Smartphone and Tablets
- Handheld Products
- Power Banks and External Battery Packs
- Small Power Tools
- Portable Media Players and Gaming

3 Description

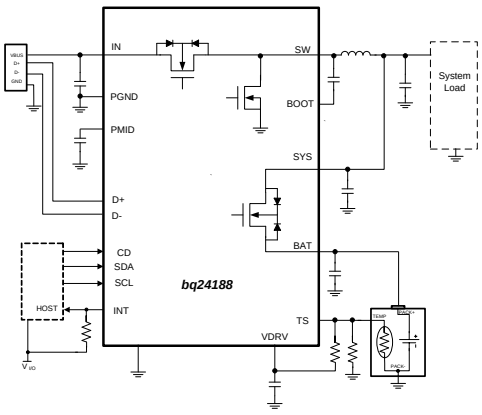
The bq24188 is a highly integrated single cell Li-Ion battery charger and system power path management device that supports operation from either a USB port or wall adapter supply. The power path feature allows the bq24188 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The power path also permits the battery to supplement the system current requirements when the adapter cannot. Many features are programmable using the I2C interface. To support USB OTG applications, the bq24188 is configurable to boost the battery voltage to 5V and supply up to 1A at the input. The battery is charged with three phases: precharge, constant current and constant voltage. Thermal regulation prevents the die temperature from exceeding 125°C. Additionally, a JEITA compatible battery pack thermistor monitoring input (TS) is included to prevent the battery from charging outside of its safe temperature range.

Device Information(1)

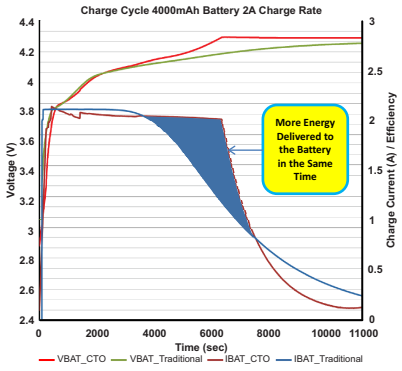
PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24188	DSBGA (36)	2.40 mm × 2.40 mm
bq24188	QFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Application Schematic



Charge Time Optimizer Effect



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5 Revision History

Changes from Original (December 2014) to Revision A **Page**

- Changed minimum capacitance for DRV pin from 1 µF to 2.2 µF ... 4
- Changed absolute max voltage for DRV, SYS from 5.0 V to 5.5 V ... 5
- Added specifications to Electrical Characteristics table pertaining to RGE package. ... 6
- Added separate lines for I_{INLIM} current for YFF and RGE packages. ... 8
- Changed V_{DO_DRV} spec MAX voltage from "500 mV" to "450 mV" ... 8
- Added footnote to the Electrical Characteristics table for the $I_{LIM(DISCH)}$ specification: "Continuous and periodic pulse currents from BAT to SYS are limited by output current specifications in the Absolute Max Ratings table" ... 10
- Changed the DRV bypass capacitor in the Typical Application circuit diagrams from 1 µF to 2.2 µF ... 36

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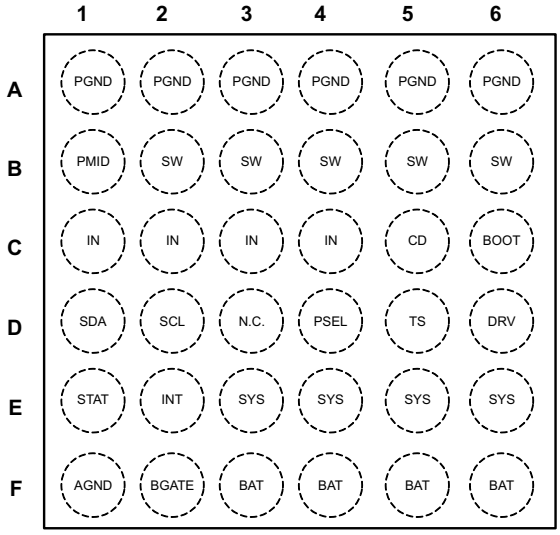
6 Device Comparison Table

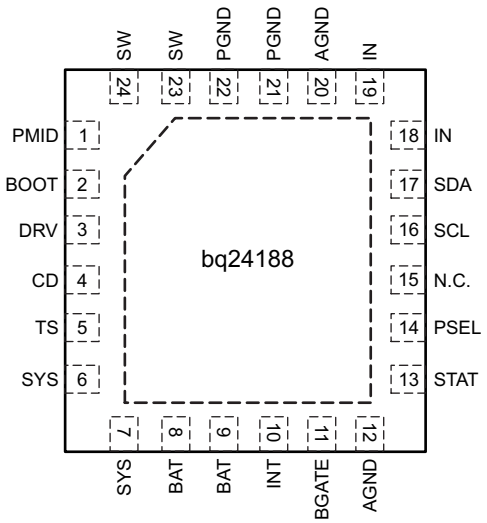
PART NUMBER	OVP	$\overline{CE}$ BIT DEFAULT	D+/D– DETECTION	TIMERS (SAFETY and WATCHDOG)	NTC MONITORING	OTG BOOST	I2C ADDRESS
bq242188	14	1 (Charge Disabled)	NO	YES	JEITA	YES	6B

7 Pin Configuration and Functions

36-Ball 2,4mm x 2,4mm WCSP (YFF)
bq24188 Top View



24-Terminal 4mm × 4mm QFN (RGE)
bq24188 Top View



Pin Functions

PIN NAME	PIN NUMBER bq24188		I/O	DESCRIPTION
	YFF	RGE		
AGND	F1	12, 20		Analog Ground. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
BAT	F3-F6	8, 9	I/O	Battery Connection. Connect to the positive terminal of the battery. Bypass BAT to GND with at least 1µF of ceramic capacitance. See Application section for additional details.
BGATE	F2	11	O	External Discharge MOSFET Gate Connection. BGATE drives an external P-Channel MOSFET to provide a very low resistance discharge path. Connect BGATE to the gate of the external MOSFET. BGATE is low during high impedance mode or when no input is connected. If no external FET is required, leave BGATE disconnected. Do not connect BGATE to GND.
BOOT	C6	2	I	High Side MOSFET Gate Driver Supply. Connect 0.033µF of ceramic capacitance (voltage rating > 10V) from BOOT to SW to supply the gate drive for the high side MOSFET.
CD	C5	4	I	IC Hardware Disable Input. Drive CD high to place the bq24188 in high-z mode. Drive CD low for normal operation. CD is pulled low internally with 100kΩ
D+	–	–	I	D+ and D– Connections for USB Input Adapter Detection. When a source is initially connected to the input during DEFAULT mode, and a short is detected between D+ and D–, the input current limit is set to 1.5A. If a short is not detected, the USB100 mode is selected.
D–	–	–	I	
DRV	D6	3	O	Gate Drive Supply. DRV is the bias supply for the gate drive of the internal MOSFETs. Bypass DRV to PGND with at least a 10-V or higher rated, +/-10%, X5R or better 2.2 µF ceramic capacitor. DRV may be used to drive external loads up to 10mA. DRV is active whenever the input is connected and $V_{IN} > V_{UVLO}$ and $V_{IN} > (V_{BAT} + V_{SLP})$.
IN	C1-C4	18, 19	I	DC Input Power Supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to PGND with at least a 4.7µF of ceramic capacitance.
INT	E2	10	O	Status Output. INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete, disabled or the charger is in high impedance mode. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. INT is enabled /disabled using the EN_STAT bit in the control register. Connect INT to a logic rail through a 100kΩ resistor to communicate with the host processor.
PGND	A1-A6	21,22	–	Ground terminal. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
PMID	B1	1	I	High Side Bypass Connection. Connect at least 1µF of ceramic capacitance from PMID to PGND as close to the PMID and PGND terminals as possible.
PSEL	D4	14	I	Hardware Input Current Limit. In DEFAULT mode, PSEL selects the input current limit. Drive PSEL high to select USB100, drive PSEL low to select 1.5A mode.
SCL	D2	16	I	I^2C Interface Clock. Connect SCL to the logic rail through a 10kΩ resistor. Do not leave floating.
SDA	D1	17	I/O	I^2C Interface Data. Connect SDA to the logic rail through a 10kΩ resistor.
STAT	E1	13	O	Status Output. STAT is an open-drain output that signals charging status and fault interrupts. STAT pulls low during charging. STAT is high impedance when charging is complete, disabled or the charger is high impedance mode. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. STAT is enabled /disabled using the EN_STAT bit in the control register. Connect STAT to a logic rail using an LED for visual indication or through a 100kΩ resistor to communicate with the host processor.
SW	B2-B6	23, 24	O	Inductor Connection. Connect to the switched side of the external inductor. The inductance must be between 1.5µH and 2.2µH.
SYS	E3-E6	6, 7	I	System Voltage Sense and Charger FET Connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with at least 10µF of ceramic capacitance. The SYS rail must have at least 20µF of total capacitance for stable operation. See Application section for additional details.
TS	D5	5	I	Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from DRV to GND. The NTC is connected from TS to GND. The TS function provides 4 thresholds for JEITA compatibility. TS faults are reported by the I^2C interface. Pull TS high to V_{DRV} to disable the TS function if unused. See the *NTC Monitor* section for more details on operation and selecting the resistor values.
Thermal PAD	–	–	–	There is an internal electrical connection between the exposed thermal pad and the PGND terminal of the device. The thermal pad must be connected to the same potential as the PGND terminal on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. PGND terminal must be connected to ground at all times.

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8 Specifications

8.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Terminal Voltage Range (with respect to PGND)	IN	–1.3	30	V
	BOOT, PMID	–0.3	30	
	SW	–0.7	20	
	BAT, BGATE, CD, INT, PSEL, SDA, SCL, STAT, TS	–0.3	5.0	
	DRV, SYS	–0.3	5.5	
BOOT to SW		–0.3	5	V
Output Current (Continuous)	SW		4.5	A
	SYS, BAT (charging/ discharging)		3.5	
Output Current (<20ms pulse, <10% duty cycle)	BAT (discharging)		6	A
Input Current (Continuous)			2.75	A
Output Sink Current	STAT, INT		10	mA
Operating free-air temperature range		–40	85	°C
Junction temperature, T_J		–40	125	
Storage Temperature, T_{stg}			300	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	IN voltage range	4.2		28(1)	V
	IN operating voltage range (bq24188)	4.2		13.2	
I_{IN}	Input current, IN input			2.5	A
I_{SW}	Output Current from SW, DC			2	A
I_{BAT}, I_{SYS}	Charging			2	A
	Discharging, using internal battery FET			3	
T_J	Operating junction temperature range	0		125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW terminals. A *tight* layout minimizes switching noise.

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8.4 Thermal Information

THERMAL METRIC(1)		bq24188		UNIT
		YFF (36 PINS)	RGE (24 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.8	32.6	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	0.5	30.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	10	3.3	
ψ_{JT}	Junction-to-top characterization parameter	2.6	0.4	
ψ_{JB}	Junction-to-board characterization parameter	9.9	9.3	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Circuit of Figure 7, $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT} + V_{SLP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{IN}	Supply current for control	$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT} + V_{SLP}$ PWM switching		15		mA
		YFF Package: $V_{UVLO} < V_{IN} < V_{OVP}$ and $_{VIN} > V_{BAT} + V_{SLP}$ PWM NOT switching			6.5	
		RGE Package: $V_{UVLO} < V_{IN} < V_{OVP}$ and $_{VIN} > V_{BAT} + V_{SLP}$ PWM NOT switching			6.65	
		0°C< T_J < 85°C, V_{IN} = 5V, High-Z Mode			250	µA
I_{BAT_HIZ}	Battery discharge current in High Impedance mode, (BAT, SW, SYS)	0°C< T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = 5V, SCL, SDA = 0V or 1.8V, High-Z Mode			15	µA
		YFF Package: 0°C< T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = 0V, SCL, SDA = 0V or 1.8V			77	
		RGE Package: 0°C< T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = 0V, SCL, SDA = 0V or 1.8V			80	
POWER-PATH MANAGEMENT						
$V_{SYSREG(LO)}$	System Regulation Voltage	$V_{BAT} < V_{MINSYS}$	V_{MINSYS} + 80mV	V_{MINSYS} + 100mV	V_{MINSYS} + 120mV	V
$V_{SYSREG(HI)}$	System Regulation Voltage	Battery FET turned off, no charging, V_{BAT} > 3.5V	V_{BATREG} +1.4%	V_{BATREG} +1.6%	V_{BATREG} +1.77%	V
V_{MINSYS}	Minimum System Voltage Regulation Threshold	$V_{BAT} + V_{DO(SYS_BAT)} < 3.5V$	3.44	3.5	3.55	V
$t_{DGL(MINSYS_CMP)}$	Deglitch time, VMINSYS comparator rising			8		ms
V_{BSUP1}	Enter supplement mode threshold	$V_{BAT} > V_{BUVLO}$		V_{BAT} – 20mV		V
V_{BSUP2}	Exit supplement mode threshold	$V_{BAT} > V_{BUVLO}$		V_{BAT} – 5mV		V
$I_{LIM(DISCH)}$	Current Limit, Discharge or Supplement Mode(1)	$V_{LIM(BGATE)} = V_{BAT} – V_{SYS}$	6	9		A
$t_{DGL(SC1)}$	Deglitch Time, OUT Short Circuit during Discharge or Supplement Mode	Measured from I_{BAT} = 7A to FET off		250		µs
$t_{REC(SC1)}$	Recovery time, OUT Short Circuit during Discharge or Supplement Mode			2		s
	Battery Range for BGATE Operation		2.5		4.5	V

(1) Continuous and periodic pulse currents from BAT to SYS are limited by output current specifications in the *Absolute Maximum Ratings* table.

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Electrical Characteristics (continued)

Circuit of Figure 7, $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+ V_{SLP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BATTERY CHARGER							
$R_{ON(BAT-SYS)}$	Internal battery charger MOSFET on-resistance	Measured from BAT to SYS, V_{BAT} = 4.2V, High-Z mode	YFF		17	25	mΩ
			RGE		32	47	
V_{BATREG}	Charge Voltage	Operating in voltage regulation, Programmable Range		3.5		4.44	V
	RGE Package Voltage Regulation Accuracy	T_J = 0°C to 50°C		-0.5%		0.5%	
	RGE Package Voltage Regulation Accuracy	T_J = 0°C to 85°C		-0.7%		0.7%	
	YFF Package Voltage Regulation Accuracy	T_J = 0°C to 85°C		-0.75%		0.75%	
	RGE and YFF Package Voltage Regulation Accuracy	T_J = 0°C to 125°C		-1.0%		1.0%	
	YFF Package Voltage Regulation Accuracy	T_J = 25°C		-29.2		28.1	mV
	YFF Package Voltage Regulation Accuracy	T_J = 0°C to 85°C		-32.0		29.3	
	YFF Package Voltage Regulation Accuracy	T_J = 0°C to 125°C		-40.2		29.3	
I_{CHARGE}	Fast Charge Current Range	$V_{BATSHRT} \le V_{BAT} < V_{BAT(REG)}$		500		2000	mA
	Fast Charge Current Accuracy	500 mA ≤ I_{CHARGE} ≤ 1A		–10%		10%	
		I_{CHARGE} > 1000 mA		–5%		5%	
$V_{BATSHRT}$	Battery short circuit threshold			1.9	2	2.1	V
$V_{BATSHRT_HYS}$	Hysteresis for $V_{BATSHRT}$	Battery voltage falling			100		mV
	Deglitch time for battery short to fastcharge transition	V_{BAT} rising or falling			1		ms
$I_{BATSHRT}$	Battery short circuit charge current	$V_{BAT} < V_{BATSHRT}$		33.5	50	66.5	mA
I_{TERM}	Termination charge current	I_{TERM} ≤ 50 mA		–30%		30%	
		50 mA < $_{ITERM}$ < 200 mA		–15%		15%	
		I_{TERM} ≥ 200 mA		–15%		10%	
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL}=100ns			32		ms
V_{RCH}	Recharge threshold voltage	Below V_{BATREG}		100	120	150	mV
$t_{DGL(RCH)}$	Deglitch time	V_{BAT} falling below V_{RCH}, t_{FALL}=100ns			32		ms
$V_{DET(SRC1)}$	Battery detection voltage threshold (TE = 1)	During current source (Turn $I_{BATSHRT\ off}$)			V_{RCH}		V
$V_{DET(SRC2)}$		During current source (Turn $I_{BATSHRT\ on}$)			V_{RCH} – 200mV		V
$V_{DET(SNK)}$		During current sink			$V_{BATSHRT}$		V
I_{DETECT}	Battery detection current before charge done (sink current)	Termination enabled (TE = 1)			7		mA
$t_{DETECT(SRC)}$	Battery detection time (sourcing current)	Termination enabled (TE = 1)			2		s
$t_{DETECT(SNK)}$	Battery detection time (sinking current)	Termination enabled (TE = 1)			250		ms

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Electrical Characteristics (continued)

Circuit of Figure 7, $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+ V_{SLP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENT LIMITING							
I_{INLIM}	Input current limiting threshold	USB charge mode, V_{IN} = 5V, Current pulled from SW	I_{INLIM}=USB100	90	95	100	mA
			I_{INLIM}=USB500	450	475	500	
			I_{INLIM}=USB150	125	140	150	
			I_{INLIM}=USB900	800	850	900	
			I_{INLIM}=1.5A	1425	1500	1575	
			I_{INLIM}=2A, YFF Package	1850	2000	2150	
			I_{INLIM}=2A, RGE Package	1850	2000	2200	
			I_{INLIM}=2.5A, YFF Package	2300	2500	2700	
			I_{INLIM}=2.5A, RGE Package	2225	2500	2825	
V_{IN_DPM}	Input based DPM threshold range	Charge mode, programmable via I^2C		4.2		11.6	V
	V_{IN_DPM} threshold Accuracy			–3%		3%	
V_{DRV} BIAS REGULATOR							
V_{DRV}	Internal bias regulator voltage	V_{IN}>5V		4.3	4.8	5.3	V
I_{DRV}	DRV Output Current			0		10	mA
V_{DO_DRV}	DRV Dropout Voltage ($V_{IN\ –\ VDRV}$)	I_{IN} = 1A, V_{IN} = 4.2V, I_{DRV} = 10mA				450	mV
STATUS OUTPUT (STAT, INT)							
V_{OL}	Low-level output saturation voltage	I_O = 10 mA, sink current				0.4	V
I_{IH}	High-level leakage current	V_{STAT} = V_{INT} = 5V				1	µA
INPUT PINS (CD, PSEL)							
V_{IL}	Input low threshold					0.4	V
V_{IH}	Input high threshold			1.4			V
$R_{PULLDOWN}$	CD pull-down resistance	CD Only			100		kΩ
	Deglitch for CD and PSEL	CD or PSEL rising/falling			100		µs

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Electrical Characteristics (continued)

Circuit of Figure 7, $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+ V_{SLP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION						
V_{UVLO}	IC active threshold voltage	V_{IN} rising	3.2	3.3	3.4	V
V_{UVLO_HYS}	IC active hysteresis	V_{IN} falling from above V_{UVLO}		300		mV
$V_{BATUVLO}$	Battery Undervoltage Lockout threshold	V_{BAT} falling, 100mV Hysteresis		2.4	2.6	V
V_{SLP}	Sleep-mode entry threshold, V_{IN}-V_{BAT}	2.0 V < V_{BAT} < V_{BATREG}, V_{IN} falling	0	40	120	mV
$t_{DGL(BAT)}$	Deglitch time, BAT above $V_{BATUVLO}$ before SYS starts to rise			1.2		ms
V_{SLP_HYS}	Sleep-mode exit hysteresis	V_{IN} rising above V_{SLP}	40	100	190	mV
$t_{DGL(VSLP)}$	Deglitch time for supply rising above V_{SLP}+V_{SLP_HYS}	Rising voltage, 2-mV over drive, t_{RISE}=100ns		30		ms
V_{OVP}	Input supply OVP threshold voltage	N rising, 100mV hysteresis	13.6	14	14.4	V
V_{BATGD}	Good Battery Monitor Threshold	V_{IN} Rising	3.51	3.7	3.89	V
$t_{DGL(BUCK_OVP)}$	Deglitch time, VIN OVP in Buck Mode	IN falling below V_{OVP}		30		ms
V_{BOVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{OREG} to turn off charger during charge	1.03 × V_{BATREG}	1.05 × V_{BATREG}	1.07 × V_{BATREG}	V
V_{BOVP_HYS}	V_{BOVP} hysteresis	Lower limit for V_{BAT} falling from above V_{BOVP}		1		% of V_{BATREG}
$t_{DGL(BOVP)}$	BOVP Deglitch	Battery entering/exiting BOVP		8		ms
$I_{CbCLIMIT}$	Cycle-by-cycle current limit	V_{SYS} shorted	4.1	4.5	4.9	A
T_{SHTDWN}	Thermal trip			150		°C
	Thermal hysteresis			10		°C
T_{REG}	Thermal regulation threshold	Input current begins to cut off		125		°C
	Safety Timer Accuracy		–20%		20%	
PWM						
R_{DSON_Q1}	Internal top MOSFET on-resistance	YFF Package: Measured from IN to SW		75	120	mΩ
		RGE Package: Measured from IN to SW		80	135	mΩ
R_{DSON_Q2}	Internal bottom N-channel MOSFET on-resistance	YFF Package: Measured from SW to PGND		75	115	mΩ
		RGE Package: Measured from SW to PGND		80	135	mΩ
f_{OSC}	Oscillator frequency		1.35	1.5	1.65	MHz
D_{MAX}	Maximum duty cycle			95		%
D_{MIN}	Minimum duty cycle		0			
BATTERY-PACK NTC MONITOR (1)						
V_{HOT}	High temperature threshold	V_{TS} falling, 2% V_{DRV} Hysteresis	27.3	30	32.6	%V_{DRV}
V_{WARM}	Warm temperature threshold	V_{TS} falling, 2% V_{DRV} Hysteresis	36.0	38.3	41.2	%V_{DRV}
V_{COOL}	Cool temperature threshold	V_{TS} rising, 2% V_{DRV} Hysteresis	54.7	56.4	58.1	%V_{DRV}
V_{COLD}	Low temperature threshold	V_{TS} rising, 2% V_{DRV} Hysteresis	58.2	60	61.8	%V_{DRV}
TSOFF	TS Disable threshold	V_{TS} rising, 4% V_{DRV} Hysteresis	80		85	%V_{DRV}
$t_{DGL(TS)}$	Deglitch time on TS change	Applies to V_{HOT}, V_{WARM}, V_{COOL} and V_{COLD}		50		ms
I²C COMPATIBLE INTERFACE						
V_{IH}	Input low threshold level	$V_{PULL-UP}$=1.8V, SDA and SCL	1.3			V
V_{IL}	Input low threshold level	$V_{PULL-UP}$=1.8V, SDA and SCL			0.4	V
V_{OL}	Output low threshold level	IL=5mA, sink current			0.4	V
I_{BIAS}	High-Level leakage current	$V_{PULL-UP}$=1.8V, SDA and SCL			1	µA
$t_{WATCHDOG}$			30	50		s
$t_{I2CRESET}$				700		ms

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Electrical Characteristics (continued)

Circuit of Figure 7, $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT} + V_{SLP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OTG BOOST SUPPLY							
I_{QBAT_BOOST}	Quiescent current during boost mode (BAT pin)	3.3V<V_{BAT}<4.5V, no switching				100	µA
	Battery voltage range for specified boost operation	VBAT falling		3.3		4.5	V
V_{IN_BOOST}	Boost output voltage (to pin VBUS)	3.3V<V_{BAT}<4.5V over line and load		4.95	5.05	5.2	V
I_{BO}	Maximum output current for boost	3.3V<V_{BAT}<4.5V	BOOST_ILIM = 1	1000			mA
			BOOST_ILIM = 0	500			
I_{BLIMIT}	Cycle by cycle current limit for boost (measured at low-side FET)	3.3V<V_{BAT}<4.5V	BOOST_ILIM = 1		4		A
			BOOST_ILIM = 0		2		
$V_{BOOSTOVP}$	Over voltage protection threshold for boost (IN pin)	Signals fault and exits boost mode		5.8	6	6.2	V
$t_{DGL(BOOST_OVP)}$	Deglitch Time, VIN OVP in Boost Mode				170		µs
$V_{BURST(ENT)}$	Upper V_{IN} voltage threshold to enter burst mode (stop switching)			5.1	5.2	5.3	V
$V_{BURST(EXIT)}$	Lower V_{BUS} voltage threshold to exit burst mode (start switching)			4.9	5	5.1	V

8.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency		1.35	1.5	1.65	Mhz
D_{MAX}	Maximum duty cycle			95%		
D_{MIN}	Minimum duty cycle		0%			

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8.7 Typical Characteristics

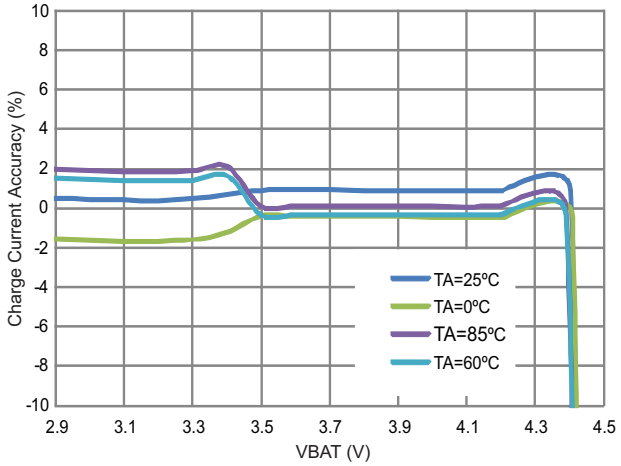

Figure 1. Charge Current vs Battery Voltage

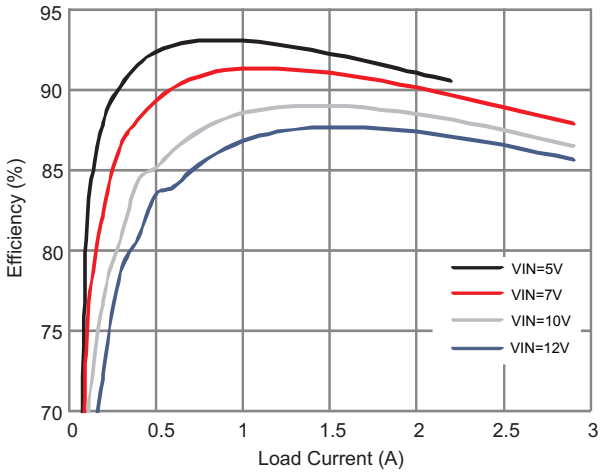

Figure 2. Efficiency vs Output Current

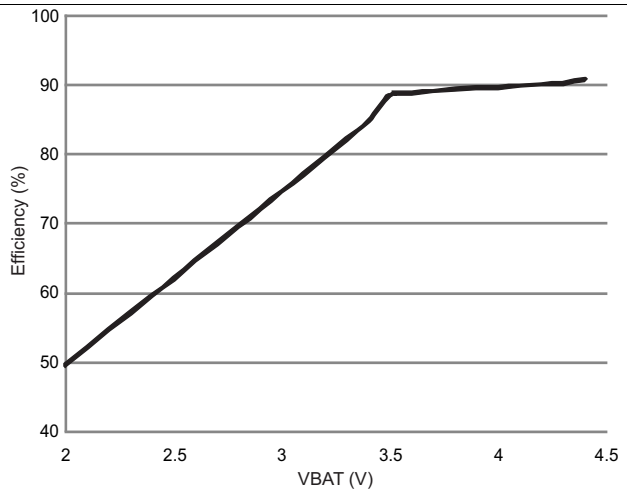

Figure 3. Efficiency vs Battery Voltage

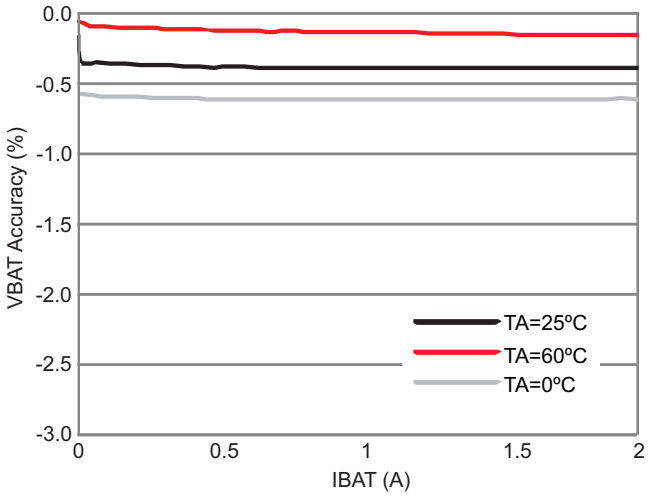

Figure 4. VBAT Accuracy vs IBAT – 4.2V Setting

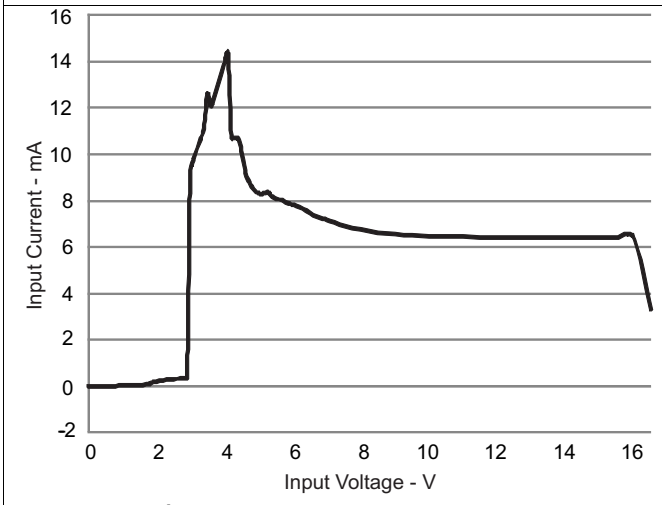

Figure 5. Input IQ - No Battery, No System

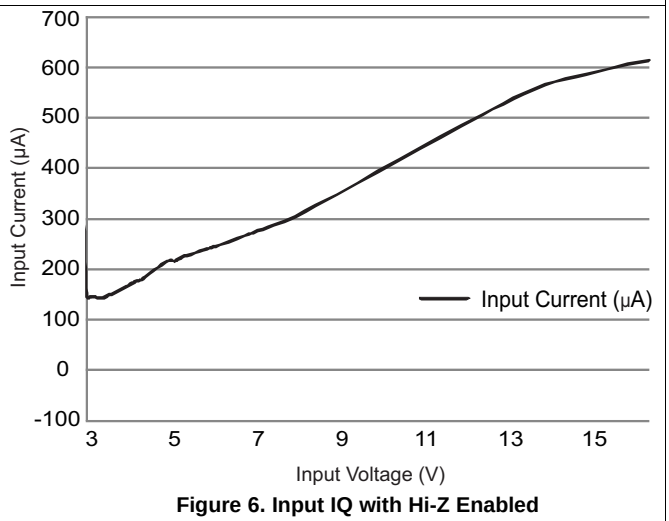

Figure 6. Input IQ with Hi-Z Enabled

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9 Detailed Description

9.1 Overview

The bq24188 is a highly integrated single cell Li-Ion battery charger and system power path management device targeted for space-limited, portable applications with high capacity batteries. The single cell charger has a single input that supports operation from either a USB port or wall adapter supply for a versatile solution.

The power path management feature allows the bq24188 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit or the adapter cannot support the required load, causing the adapter voltage to fall (V_{IN_DPM}). This allows for proper charge termination and timer operation. The system voltage is regulated to the battery voltage but will not drop below 3.5V (V_{MINSYS}). This minimum system voltage support enables the system to run with a defective or absent battery pack and enables instant system turn-on even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. The power-path feature coupled with V_{IN}-DPM, enables the use of many adapters with no hardware change. The charge parameters are programmable using the I2C interface. To Support USB OTG applications, the bq24188 is configurable to boost the battery voltage to 5V at the input. In this mode, the bq24188 supplies up to 1A and operates with battery voltages down to 3.3V.

The battery is charged using a standard Li-Ion charge profile with three phases: precharge, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the input current to prevent the junction temperature from rising above 125°C. Additionally, a voltage-based, JEITA compatible battery pack thermistor monitoring input (TS) is included that monitors battery temperature and automatically changes charge parameters to prevent the battery from charging outside of its safe temperature range.

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9.2 Functional Block Diagram

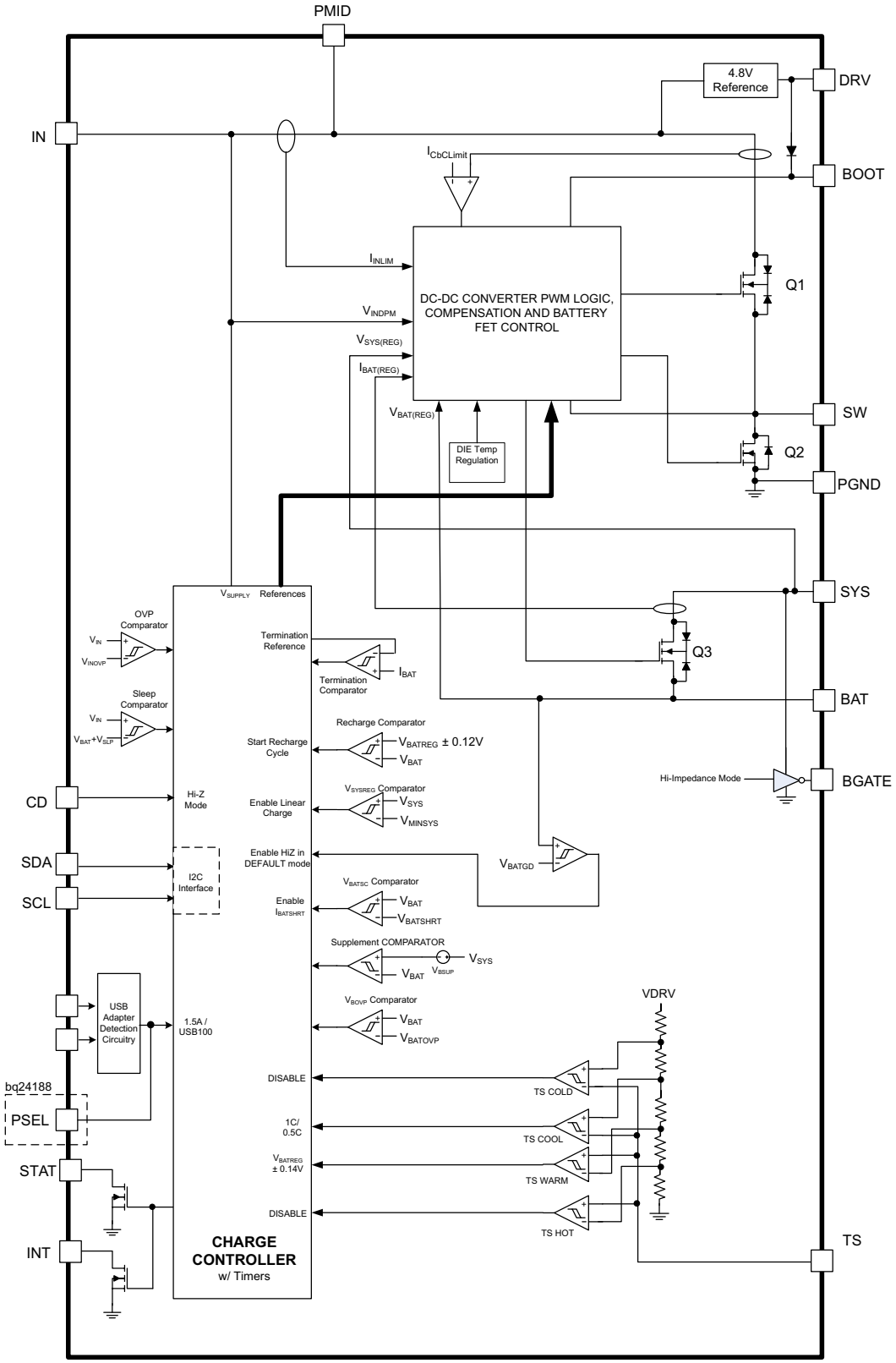

Figure 7. Block Diagram in Charging Mode

Functional Block Diagram (continued)

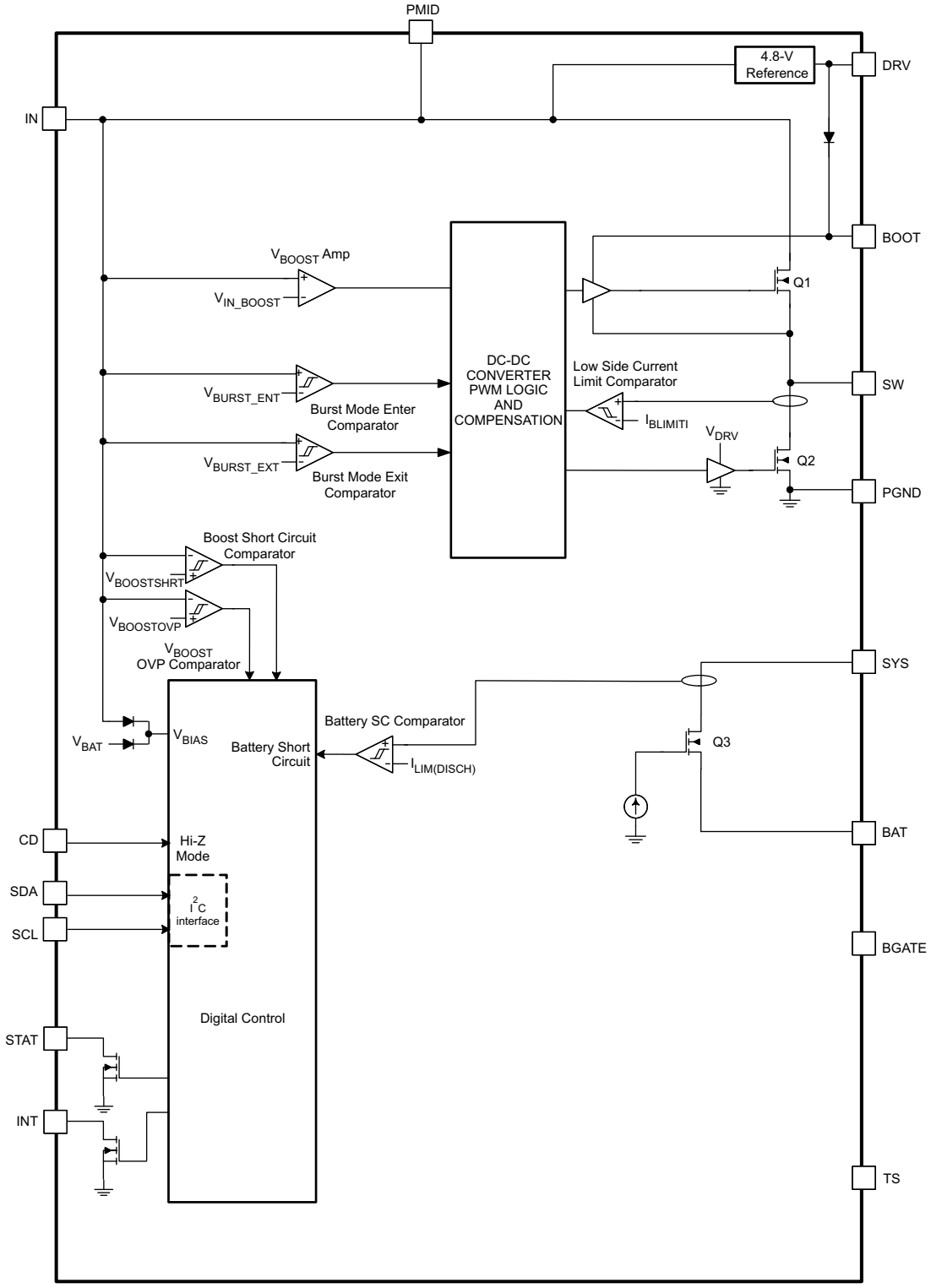

Figure 8. Block Diagram in Boost Mode

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9.3 Feature Description

The bq24188 is a highly integrated single cell Li-Ion battery charger and system power path management device that supports operation from either a USB port or wall adapter supply. The power path feature allows the bq24188 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The power path also permits the battery to supplement the system current requirements when the adapter cannot. Many features are programmable using the I2C interface. To support USB OTG applications, the bq24188 is configurable to boost the battery voltage to 5V and supply up to 1A at the input. The battery is charged with three phases: precharge, constant current and constant voltage. Thermal regulation prevents the die temperature from exceeding 125°C. Additionally, a JEITA compatible battery pack thermistor monitoring input (TS) is included to prevent the battery from charging outside of its safe temperature range

The Device Functional Modes section explains these features in detail.

9.4 Device Functional Modes

9.4.1 High Impedance Mode

High Impedance mode (Hi-Z mode) is the low quiescent current state for the bq24188. During Hi-Z mode, the buck converter is off, and the battery FET and BGATE are on. SYS is powered by BAT. The bq24188 is in Hi-Z mode when $V_{IN} < V_{UVLO}$, the HZ_MODE bit in the I^2C is '1' or the CD terminal is driven high. Hi-Z mode resets the safety timer.

The bq24188 contains a CD input that is used to disable the IC and place the bq24188 into high-impedance mode. Drive CD low to enable the bq24188 and enter normal operation. Drive CD high to disable charge and place the bq24188 into high-impedance mode. CD is internally pulled down to PGND with a 100kΩ resistor. When exiting Hi-Z mode, charging resumes in approximately 110ms.

9.4.2 Battery Only Connected

When the battery is connected with no input source, the battery FET is turned on. After the battery rises above $V_{BATUVLO}$ and the deglitch time, $t_{DGL(BAT)}$, the SYS output starts to rise. In this mode, the current is not regulated; however, there is a short circuit current limit. If the short circuit limit ($I_{LIM(DISCHG)}$) is reached for the deglitch time ($t_{DGL(SC)}$), the battery FET is turned off for the recovery time ($t_{REC(SC)}$). After the recovery time, the battery FET is turned on to test and see if the short has been removed. If it has not, the FET turns off and the process repeats until the short is removed. This process protects the internal FET from over current. If an external FET is used for discharge, the body diode prevents the load on SYS from being disconnected from the battery and $t_{DGL(BAT)}$ is not applicable.

9.4.3 Input Connected

9.4.3.1 Input Voltage Protection in Charge Mode

9.4.3.1.1 Sleep Mode

The bq24188 enters the low-power sleep mode if the voltage on V_{IN} falls below sleep-mode entry threshold, $V_{BAT}+V_{SLP}$, and V_{IN} is higher than the undervoltage lockout threshold, V_{UVLO}. In sleep mode, the input is isolated from the battery. This feature prevents draining the battery during the absence of V_{IN}. When $V_{IN} < V_{BAT}+ V_{SLP}$, the bq24188 turns off the PWM converter, turns the battery FET and BGATE on, sends a single 128µs pulse on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. Once $V_{IN} > V_{BAT}+ V_{SLP}$, the STATx bits are cleared and the device initiates a new charge cycle. The FAULT_x bits are not cleared until they are read in the I^2C and the sleep condition no longer exists.

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Device Functional Modes (continued)

9.4.3.1.2 Input Voltage Based Dynamic Power Management (V_{IN}-DPM)

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage deceases. Once the supply drops to V_{IN_DPM} (default 4.2V), the charge current limit is reduced to prevent the further drop of the supply. When the IC enters this mode, the charge current is lower than the set value and the DPM_STATUS bit is set. This feature ensures IC compatibility with adapters with different current capabilities without a hardware change. Figure 9 shows the V_{IN}-DPM behavior to a current limited source. In this figure the input source has a 2A current limit and the device is charging at 1A. A 2.5A load transient then occurs on V_{SYS} causing the adapter to hit its current limit and collapse, while V_{SYS} goes from $V_{SYSREG(LO)}$ to V_{MINSYS}. If the 2X timer is set, the safety timer is extended while V_{IN}-DPM is active. Additionally, termination is disabled.

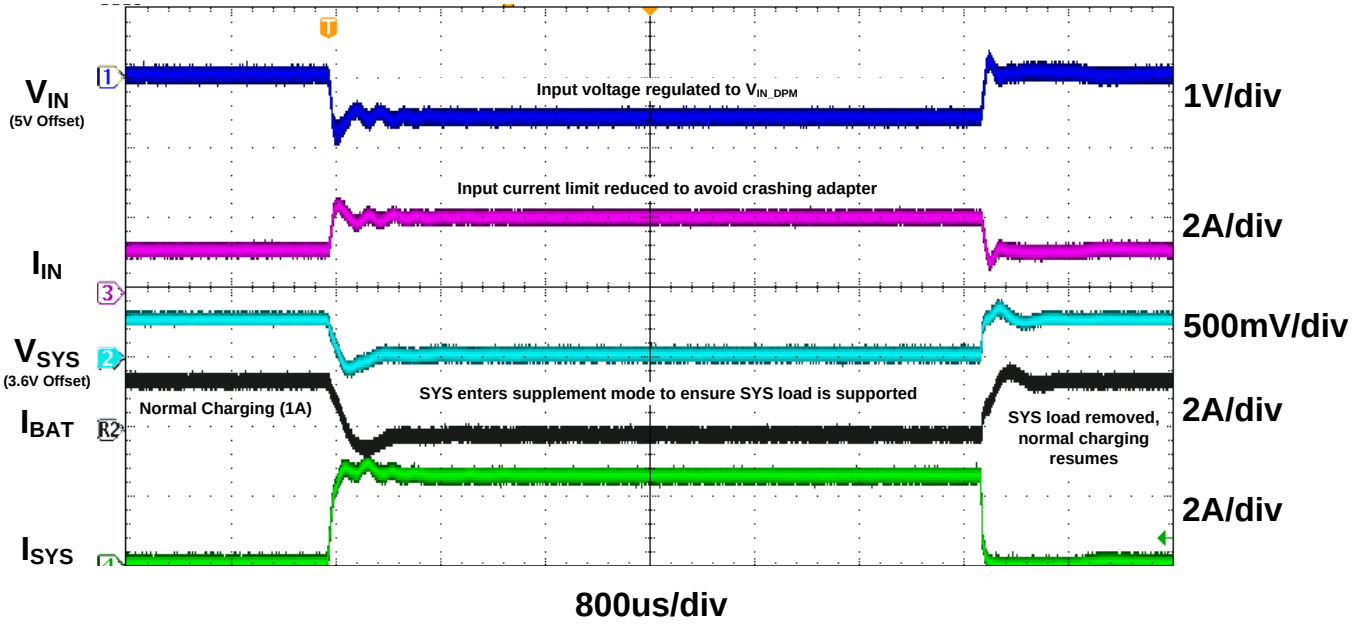

Figure 9. bq24188 V_{IN}-DPM

9.4.3.1.3 Input Over-Voltage Protection

The built-in input over-voltage protection protects the bq24188 and downstream components connected to SYS and/or BAT against damage from overvoltage on the input supply (Voltage from V_{IN} to PGND). When $V_{IN} > V_{OVP}$, the bq24188 turns off the PWM converter immediately. After the deglitch time $t_{DGL(BUCK_OVP)}$, an OVP fault is determined to exist. During the OVP fault, the bq24188 turns the battery FET and BGATE on, sends a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits are updated in the I^2C. Once the OVP fault is removed, the STATx bits are cleared and the device returns to normal operation. The FAULT_x bits are not cleared until they are read in the I^2C after the OVP condition no longer exists.

The OVP threshold for the bq24188 is set to 14V to enable operation from 12V sources.

9.4.3.2 Charge Profile

When a valid input source is connected ($V_{IN} > V_{UVLO}$ and $V_{BAT} + V_{SLP} < V_{IN} < V_{OVP}$), the $\overline{CE}$ bit in the control register determines whether a charge cycle is initiated. By default, the bq24188 does not enable the charge cycle when a valid input source is connected ($\overline{CE}$ = 1 by default). When the $\overline{CE}$ bit is 1 and a valid input source is connected, the battery FET is turned off and the SYS output is regulated to VSYSREG(HI). A charge cycle is initiated when the $\overline{CE}$ bit is written to a 0.

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Device Functional Modes (continued)

The bq24188 supports a precision Li-Ion or Li-Polymer charging system for single-cell applications. Charging is done through the internal battery MOSFET. There are 6 loops that influence the charge current; constant current loop (CC), constant voltage loop (CV), thermal regulation loop, minimum system voltage loop (MINSYS), input current limit and V_{IN}-DPM. During the charging process, all six loops are enabled and the one that is dominant takes control. The minimum system output feature regulates the system voltage to $V_{SYSREG(LO)}$, so that startup is enabled even for a missing or deeply discharged battery. Figure 10 shows a typical charge profile including the minimum system output voltage feature.

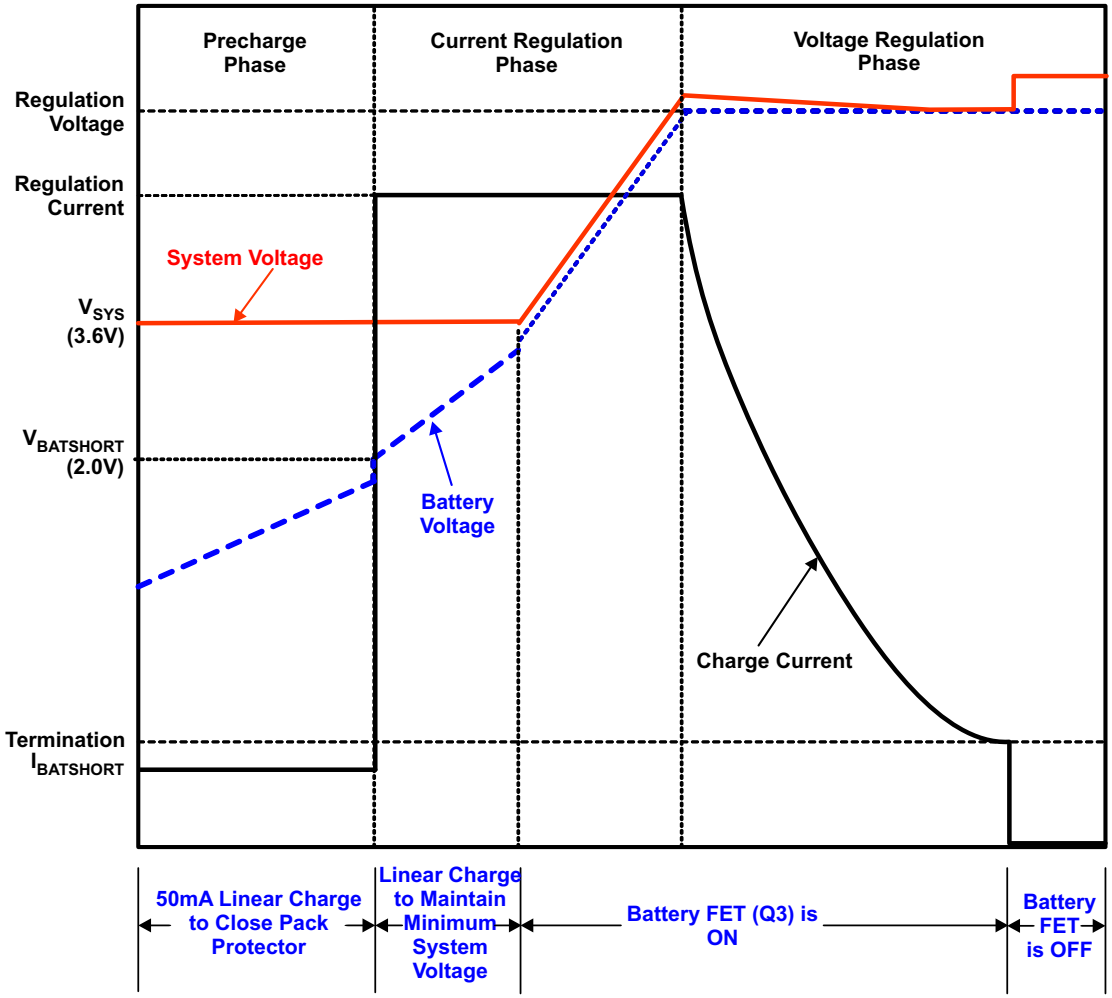

Figure 10. Typical Charging Profile of bq24188 with Termination Enabled

9.4.4 Battery Charging Process

When the battery is deeply discharged or shorted, the bq24188 applies a $I_{BATSHRT}$ current to close the battery protector switch and bring the battery voltage up to acceptable charging levels. During this time, the battery FET is off and the system output is regulated to $V_{SYSREG(LO)}$. Once the battery rises above $V_{BATSHRT}$, the charge current is regulated to the value set in the I^2C register. The battery FET is linearly regulated to maintain the system voltage at $V_{SYSREG(LO)}$. Under normal conditions, the time spent in this region is a very short percentage of the total charging time, so the linear regulation of the charge current does not affect the overall charging efficiency for very long. If the die temperature does heat up, the thermal regulation loop reduces the input current to maintain a die temperature at 125°C. If the current limit for the SYS output is reached (limited by the input

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Device Functional Modes (continued)

current limit, V_{IN}-DPM, or 100% duty cycle), the SYS output drops to the V_{MINSYS} output voltage. When this happens, the charge current is reduced to ensure the system is supplied with all the current that is needed while maintaining the minimum system voltage. If the charge current is reduced to 0mA, pulling further current from SYS causes the output to fall to the battery voltage and enter supplement mode (see the “Dynamic Power Path Management” section for more details).

Once the battery is charged enough that the system voltage rises above $V_{SYSREG(LO)}$ (approximately 3.5V), the battery FET is turned on fully and the battery is charged with the full programmed charge current set by the I^2C interface, I_{CHARGE}. The charge current is regulated to I_{CHARGE} until the voltage between BAT and PGND reaches the regulation voltage. The voltage between BAT and PGND is regulated to V_{BATREG} (CV mode) while the charge current naturally tapers down as shown in Figure 10. During CV mode, the SYS output remains connected to the battery. The impedance of the battery FET is increased to 4x of the fully on value when IBAT falls below ~350mA to provide increased accuracy during termination. This will show a small rise in the SYS voltage when the R_{DSON} increases below ~350mA.

When termination is enabled (TE bit is '1'), the bq24188 monitors the charging current during the CV mode. Once the charge current tapers down to the termination threshold, I_{TERM}, and the battery voltage is above the recharge threshold, the bq24188 terminates charge, turns off the battery charging FET and enters battery detection (see Battery Detection section for more details). The system output is regulated to the $V_{SYSREG(HI)}$ and supports the full current available from the input. The battery supplement mode is available to supply any SYS load that cannot be supported by the input source (see the “Dynamic Power Path Management” section for more details). The termination current level is programmable. To disable the charge current termination, the host sets the charge termination bit (TE) of charge control register to 0. Refer to I^2C section for details. When termination is disabled, V_{BAT} is continuously regulated to V_{BATREG}. Termination is also disabled when any loop is active other than CC or CV. This includes V_{INDPM}, input current limit, or thermal regulation. Termination is also disabled during TS warm/cool conditions and when the LOW_CHG bit is set to '1'.

A charge cycle is initiated when one of the following conditions is detected:

1. The battery voltage falls below the V_{BATREG}-V_{RCH} threshold.
2. IN Power-on reset (POR)
3. CE bit toggle or RESET bit is set (Host controlled)
4. CD terminal is toggled

9.4.5 Charge Time Optimizer

The CC to CV transition is enhanced in the bq24188 architecture. The "knee" between CC and CV is sharp. This enables the charger to remain in CC mode as long as possible before beginning to taper the charge current (CV mode). This provides a decrease in charge time as compared to older topologies.

9.4.6 Battery Detection

When termination conditions are met, a battery detection cycle is started. During battery detection, I_{DETECT} is pulled from V_{BAT} for $t_{DETECT(SNK)}$ to verify there is a battery. If the battery voltage remains above $V_{DET(SINK)}$ for the full duration of $t_{DETECT(SNK)}$, a battery is determined to present and the IC enters “Charge Done”. If V_{BAT} falls below $V_{DET(SINK)}$, a “Battery Not Present” fault is signaled, the charge parameters are reset (V_{BATREG}, I_{CHARGE} and I_{TERM}) and battery detection continues. The next cycle of battery detection, the bq24188 turns on $I_{BATSHRT}$ for $t_{DETECT(SRC)}$. If V_{BAT} rises to $V_{DET(SRC1)}$, the current source is turned off and a “No Battery” condition is registered. In order to keep VBAT high enough to close the battery protector, the current source turns on if V_{BAT} falls to $V_{DET(SRC2)}$. The source cycle continues for $t_{DETECT(SRC)}$. After $t_{DETECT(SRC)}$, the battery detection continues through another current sink cycle. Battery detection continues until charge is disabled, the bq24188 enters high-z mode or a battery is detected. Once a battery is detected, the fault status clears and a new charge cycle begins. With no battery connected, the BAT output will transition from VRCH to PGND with a high period of $t_{DETECT(SRC)}$ and a low period of $t_{DETECT(SNK)}$. See Figure 29 in the *Application Curves* section. Battery detection is not performed when termination is disabled.

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Device Functional Modes (continued)

9.4.7 Battery Overvoltage Protection (BOVP)

If the battery is ever above the battery OVP threshold (V_{BOVP}), the battery OVP circuit shuts the PWM converter off and the battery FET is turned on to discharge the battery to safe operating levels. A battery OVP most commonly occurs when the bq24188 returns to DEFAULT mode after a watchdog timer expiration or RESET bit written to '1'. In this condition, the V_{BATREG} is reset and may be below the battery voltage. Other conditions may be when the input is initially plugged in before I^2C communication is established or TS WARM conditions or when writing the V_{BATREG} to less than the battery voltage. The battery OVP condition is cleared when the battery voltage falls below the hysteresis of V_{BOVP} either by the battery discharging or writing the V_{BATREG} to a higher value. When a battery OVP event exists for $t_{DGL(BOVP)}$, the bq24188 turns the battery FET and BGATE on, sends a single 128µs pulse on the STAT / INT outputs and the STATx and FAULT_x bits are updated in the I^2C. Once the BOVP fault is removed, the STATx bits are cleared and the device returns to normal operation. The FAULT_x bits are not cleared until they are read in the I^2C after the BOVP condition no longer exists.

9.4.8 Dynamic Power Path Management

The bq24188 features a SYS output that powers the external system load connected to the battery. This output is active whenever a valid source is connected to IN or BAT. When $V_{SYS} > V_{SYSREG(LO)}$, the SYS output is connected to V_{BAT}. If the battery voltage falls to V_{MINSYS}, V_{SYS} is regulated to the $V_{SYSREG(LO)}$ threshold to maintain the system output even with a deeply discharged or absent battery. In this mode, the SYS output voltage is regulated by the buck converter and the battery FET is linearly regulated to regulate the charge current into the battery. The current from the supply is shared between charging the battery and powering the system load at SYS. The dynamic power path management (DPPM) circuitry of the bq24188 monitors the current limits continuously and if the SYS voltage falls to the V_{MINSYS} threshold, it adjusts charge current to maintain the minimum system voltage and supply the load on SYS. If the charge current is reduced to zero and the load increases further, the bq24188 enters battery supplement mode. During supplement mode, the battery FET is turned on and $V_{BAT} = V_{SYS}$ while the battery supplements the system load.

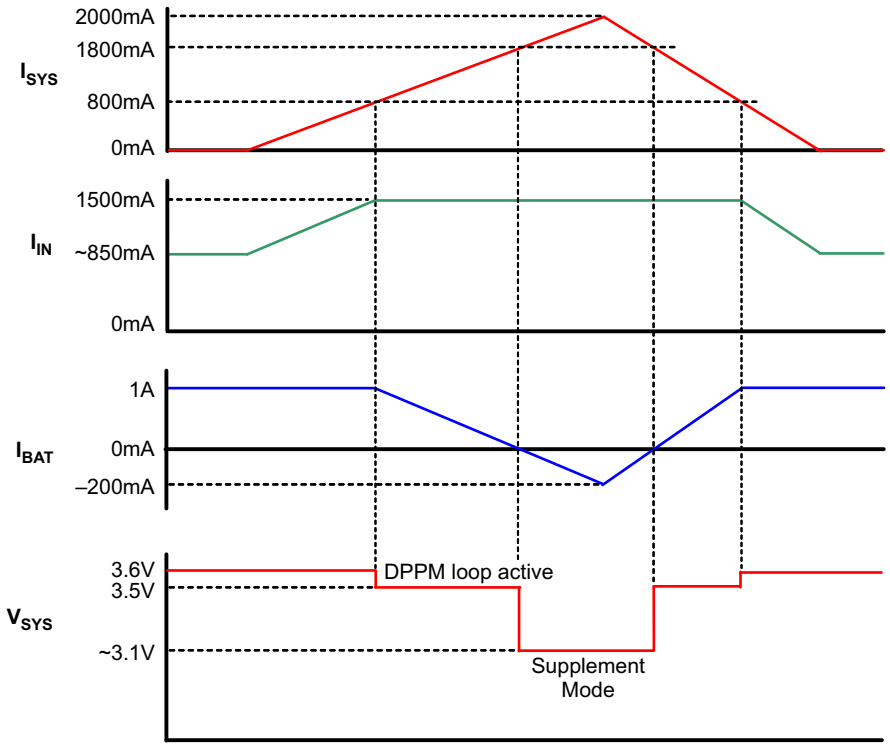

Figure 11. Example DPPM Response (V_{Supply}=5V, V_{BAT} = 3.1V, 1.5A Input Current Limit)

Device Functional Modes (continued)

9.4.9 Battery Discharge FET (BGATE)

The bq24188 contains a MOSFET driver to drive an external discharge FET between the battery and the system output. This external FET provides a low impedance path for supplying the system from the battery. Connect BGATE to the gate of the external discharge P-channel MOSFET. BGATE is on (low) under the following conditions:

1. No input supply connected.
2. HZ_MODE = 1
3. CD terminal = 1

9.4.10 DEFAULT Mode

DEFAULT mode is used when I2C communication is not available. DEFAULT mode is entered in the following situations:

1. When the charger is enabled and $V_{BAT}<V_{BATGD}$ before I^2C communication is established
2. When the watchdog timer expires without a reset from the I^2C interface
3. The RESET bit is written in the I^2C register

In DEFAULT mode, the I^2C registers are reset to the default values. The 2 minute safety timer is reset and starts when DEFAULT mode is entered if a charge cycle is underway. The default value for V_{BATREG} is 3.6V for the BQ24188 , and the default value for I_{CHARGE} is 1A. For the bq24188, the input current limit in DEFAULT mode is set by PSEL. (See *Power Source Selector Input* section) DEFAULT mode is exited by writing to the I^2C interface. Note that if termination is enabled and charging has terminated, a new charge cycle is NOT initiated when entering DEFAULT mode.

9.4.11 Good Battery Monitor

The bq24188 contains a good battery monitor circuit that places the bq24188 into high-z mode if the battery voltage is above the V_{BATGD} threshold while in DEFAULT mode. This function is used to enable compliance to the battery charging standard that prevents charging from an un-enumerated USB host while the battery is above the good battery threshold. If the bq24188 is in HOST mode, it is assumed that USB host has been enumerated and the good battery circuit has no effect on charging. Any write to the i2c places the bq24188 in HOST mode and clears the high-impedance mode condition. The HZ_MODE bit is not updated during this condition.

9.4.12 Power Source Selector Input

The bq24188 contains a PSEL input that is used to program the input current limit during DEFAULT mode. Drive PSEL high to indicate a USB source is connected to the input and program the 100mA current limit for IN. Drive PSEL low to indicate that an AC Adapter is connected to the input. When PSEL is low, the IC starts up with a 1.5A input current limit. Once an I^2C write is done and the device is in HOST mode, the PSEL has no effect on the input current limit until the watchdog timer expires and returns the bq24188 to DEFAULT mode.

9.4.13 Safety Timer and Watchdog Timer in Charge Mode

At the beginning of charging process, the bq24188 starts the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, the IC enters suspend mode where charging is disabled. When a safety timer fault occurs, a single 128µs pulse is sent on the $\overline{\text{STAT}}$ and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I2C. The $\overline{\text{CE}}$ bit, Hi-Z mode, or power must be toggled in order to clear the safety timer fault. The safety timer duration is selectable using the TMR_X bits in the Safety Timer Register/ NTC Monitor register. When the safety timer is active, changing the safety timer duration resets the safety timer. The bq24188 also contains a 2X_TIMER bit that enables the 2x timer function to prevent premature safety timer expiration when the charge current is reduced by a load on SYS or a NTC condition. When 2X_TIMER is enabled, the timer runs at half speed when any loop is active other than CC or CV. This includes V_{INDPM}, input current limit, or thermal regulation. The timer also runs at half speed during TS warm/cool conditions and when the LOW_CHG bit is set to '1'.

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Device Functional Modes (continued)

In addition to the safety timer, the bq24188 contains a 30-second ($t_{WATCHDOG}$) watchdog timer that monitors the host through the I^2C interface. Once a write is performed on the I^2C interface, a watchdog timer is started. The watchdog timer is reset by the host using the I^2C interface. This is done by writing a "1" to the reset bit (TMR_RST) in the control register. The TMR_RST bit is automatically set to "0" when the watchdog timer is reset. This process must continue as long as the input is connected in order to maintain the register contents. If the watchdog timer expires, the IC enters DEFAULT mode where the default register values are loaded, the safety timer restarts at 2 minutes once charging continues. The I^2C may be accessed again to reinitialize the desired values and restart the watchdog timer. The watchdog timer flow chart is shown in Figure 12.

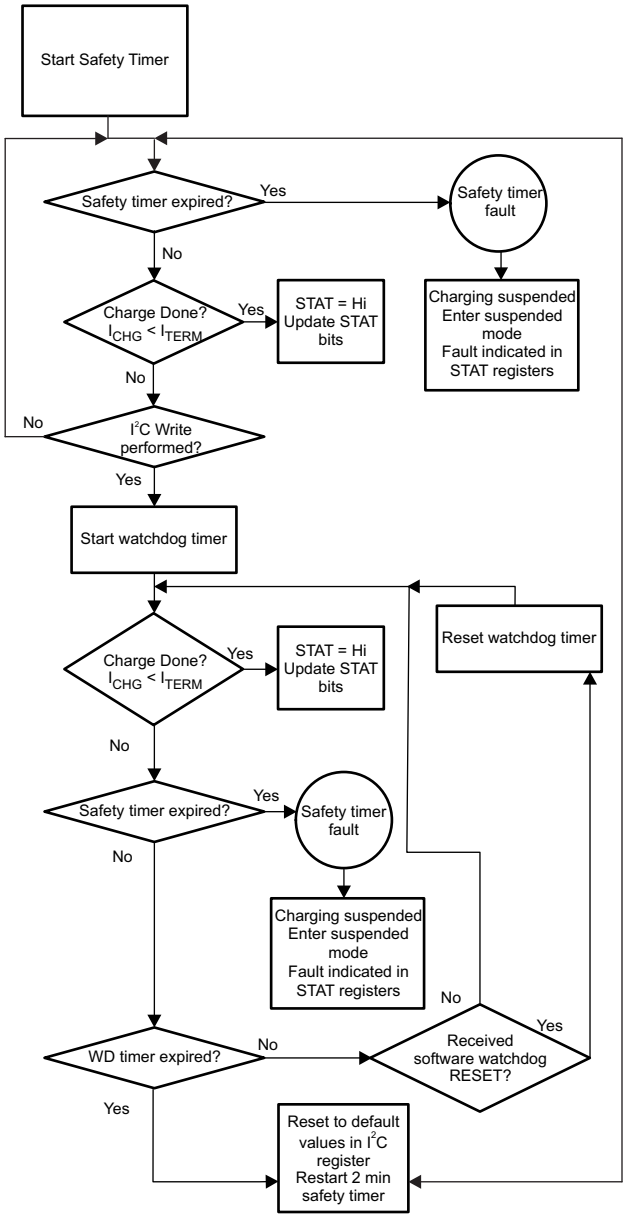

Figure 12. The Watchdog Timer Flow Chart for bq24188

Device Functional Modes (continued)

9.4.14 LDO Output (DRV)

The bq24188 contains a linear regulator (DRV) that is used to supply the internal MOSFET drivers and other circuitry. Additionally, DRV supplies up to 10mA external loads to power the STAT LED or the USB transceiver circuitry. The maximum value of the DRV output is 5.3V so it ideal to protect voltage sensitive USB circuits. The LDO is on whenever a supply is connected to the input of the bq24188 . The DRV is disabled under the following conditions:

1. V_{SUPPLY} < UVLO
2. V_{SUPPLY} < V_{BAT} + V_{SLP}
3. Thermal Shutdown

9.4.15 External NTC Monitoring (TS)

The I^2C interface allows the user to easily implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. Additionally, the bq24188 provides a flexible, voltage based TS input for monitoring the battery pack NTC thermistor. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. The JEITA specification is shown in Figure 13.

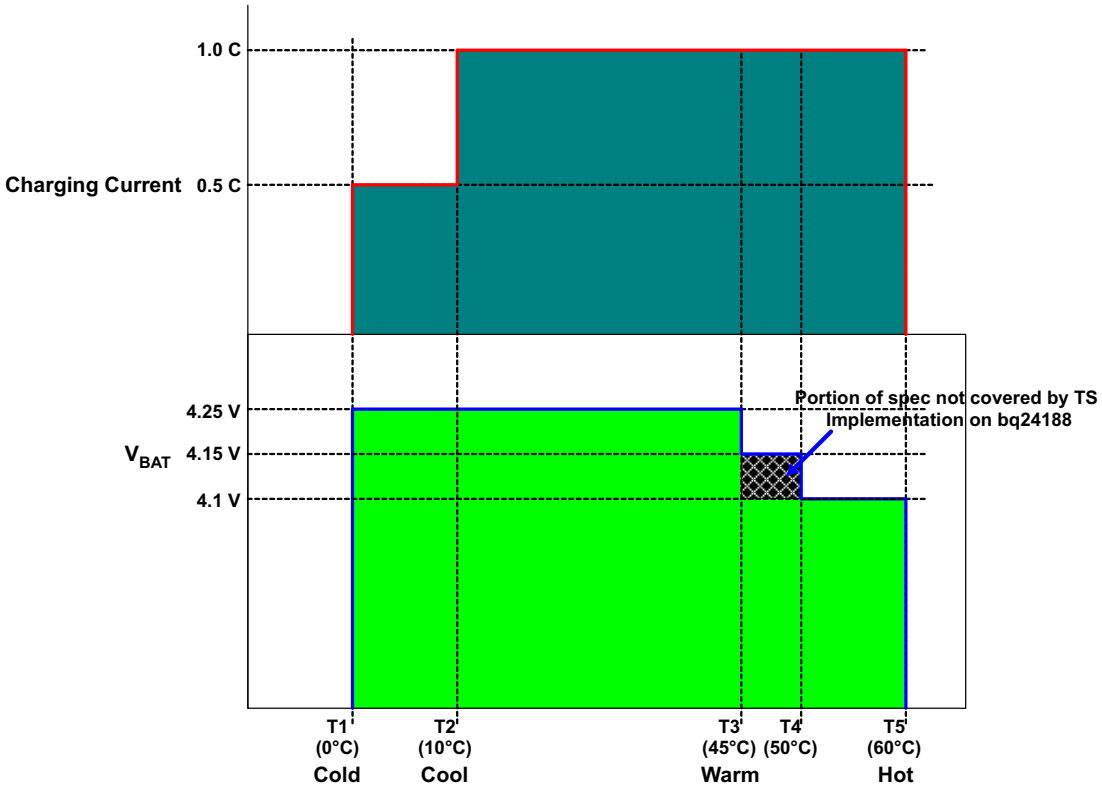

Figure 13. Charge Current During TS Conditions

To satisfy the JEITA requirements, four temperature thresholds are monitored; the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < T_{NTC} < 10°C), the warm battery threshold (45°C < T_{NTC} < 60°C) and the hot battery threshold (T_{NTC} > 60°C). These temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds in the EC table. Charging is suspended and timers are suspended when V_{TS} < V_{HOT} or V_{TS} > V_{COLD}. When V_{COOL} < V_{TS} < V_{COLD}, the charging current is reduced to half of the programmed charge current. When V_{HOT} < V_{TS} < V_{WARM}, the battery regulation voltage is reduced by 140mV from the programmed regulation threshold. The TS function is disabled by connecting TS directly to DRV (V_{TS} > V_{TSOFF}).

The TS function is voltage based for maximum flexibility. Connect a resistor divider from DRV to GND with TS connected to the center tap to set the threshold. The connections are shown in Figure 14. The resistor values are calculated using the following equations:

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Device Functional Modes (continued)

$$RLO = \frac{V_{DRV} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{DRV}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{DRV}}{V_{COLD}} - 1\right]} \quad (1)$$

$$RHI = \frac{\frac{V_{DRV}}{V_{COLD}} - 1}{\frac{1}{RLO} + \frac{1}{RCOLD}} \quad (2)$$

Where:

$V_{COLD} = 0.60 \times V_{DRV}$

$V_{HOT} = 0.30 \times V_{DRV}$

$$RCOOL = \frac{RLO \times RHI \times 0.564}{RLO - RLO \times 0.564 - RHI \times 0.564} \quad (3)$$

$$RWARM = \frac{RLO \times RHI \times 0.383}{RLO - RLO \times 0.383 - RHI \times 0.383} \quad (4)$$

Where RHOT is the NTC resistance at the hot temperature and RCOLD is the NTC resistance at cold temperature.

The WARM and COOL thresholds are not independently programmable. The COOL and WARM NTC resistances for a selected resistor divider are calculated using Equation 3 and Equation 4.

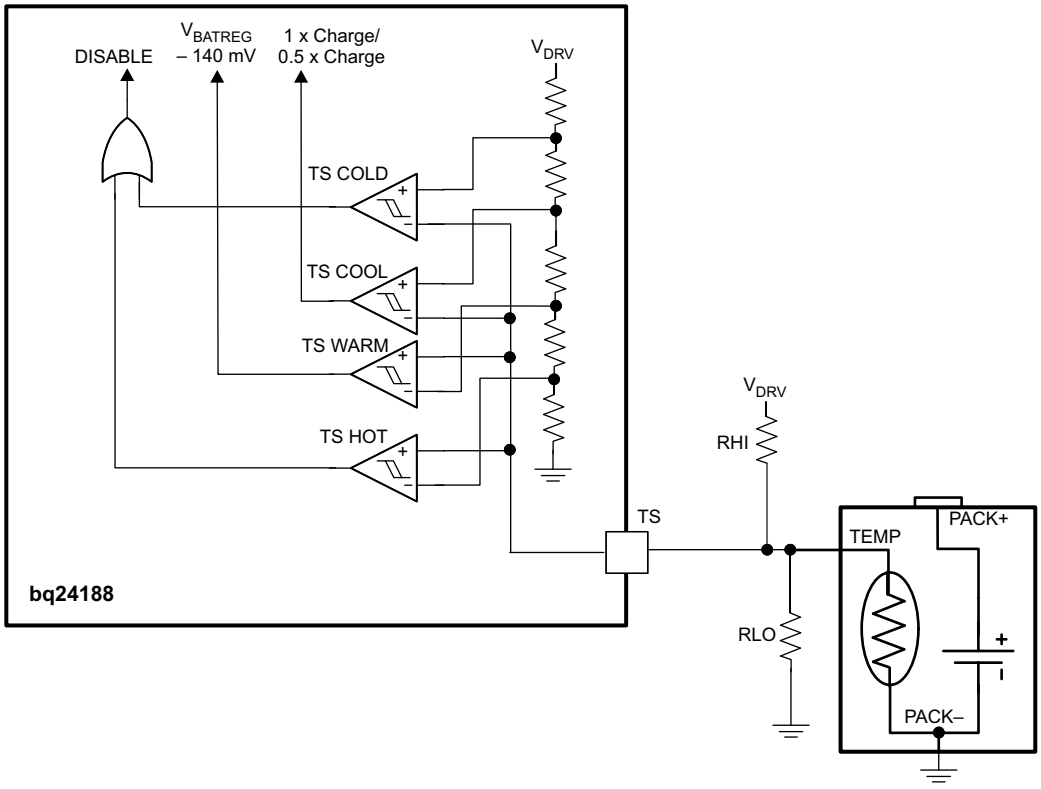

Figure 14. TS Circuit

Device Functional Modes (continued)

9.4.16 Thermal Regulation and Protection

During the charging process, to prevent overheating in the chip, bq24188 monitors the junction temperature, T_J, of the die and reduces the input current once T_J reaches the thermal regulation threshold, T_{REG}. The input current is reduced to zero when the junction temperature increases about 10°C above T_{REG}. Once the input current is reduced to 0, the system current is reduced while the battery supplements the load to supply the system. When the input current is completely reduced to 0 and T_J > 125°C, this is may cause a thermal shutdown of the bq24188 if the die temperature rises too high. At any state, if T_J exceeds T_{SHTDWN}, bq24188 stops charging and disables the buck converter. During thermal shutdown mode, PWM is turned off, all timers are suspended, and a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. The charge cycle resumes when T_J falls below T_{SHTDWN} by approximately 10°C.

9.4.17 Charge Status Outputs (STAT, INT)

The STAT/INT output is used to indicate operation conditions for bq24188. STAT/INT is pulled low during charging when EN_STAT bit in the control register is set to “1”. When charge is complete or disabled, STAT/INT is high impedance. When a fault occurs, a 128-µs pulse (interrupt) is sent out to notify the host. The status of STAT/INT during different operation conditions is summarized in Table 1. STAT/INT drives an LED for visual indication or can be connected to the logic rail for host communication. The EN_STAT bit in the control register is used to enable/disable the charge status for STAT/INT. The interrupt pulses are unaffected by EN_STAT and will always be shown.

Table 1. STAT Terminal Summary

CHARGE STATE	STAT and INT BEHAVIOR
Charge in progress and EN_STAT=1	Low
Other normal conditions	High-Impedance
Charge mode faults: Timer faults, sleep mode, VIN over voltage, VIN < UVLO or Sleep mode, BOVP, thermal shutdown, No Battery and Battery Temperature faults	128-µs pulse, then High Impedance

9.4.18 Boost Mode Operation

In HOST mode, when the operation mode bit (BOOST_EN) in the control register is set to 1, bq24188 operates in boost mode and delivers 5V to IN to supply USB OTG devices connected to the USB connector. Boost operation can start with VBAT between 3.45V to 4.5V, and will maintain boost output until VBAT falls to 3.3V. IN supplies up to 1A to power these devices. It is not recommended to operate boost mode when the battery voltage is less than 3.3V. Proper operation is not ensured.

9.4.18.1 Chip Disable Input During Boost Mode (CD)

The bq24188 contains a CD input that is used to disable the IC and place the bq24188 into high-impedance mode. CD must be low to enter boost mode. Driving CD high during boost mode places the bq24188 into high-z mode and resets the BOOST_EN bit in the I^2C. When CD is high, the buck converter is off, and the battery FET and BGATE are turned on. CD is internally pulled down to GND with a 100kΩ resistor.

9.4.18.2 PWM Controller in Boost Mode

Similar to charge mode operation, in boost mode the IC switches at 1.5MHz to regulate the voltage at IN to 5V. The voltage control loop is internally compensated to provide enough phase margin for stable operation with the full battery voltage range and up to 1A.

In boost mode, the cycle-by-cycle current limit is set to 4A or 2A (depending on the I^2C setting) to provide protection against short circuit conditions. If the cycle-by-cycle current limit is active for 8ms, an overload condition is detected and the device exits boost mode, and signals an over-current fault. Additionally, discharge current limit ($I_{LIM(DISCHG)}$) is active to protect the battery from overload. Synchronous operation and burst mode are used to maximize efficiency over the full load range.

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The bq24188 will not enter boost mode unless the IN voltage is less than the UVLO. When the boost function is enabled, the bq24188 enters a linear mode to bring IN up to the battery voltage. Once V_{IN} > (V_{BAT} – 1V), the bq24188 begins switching and regulates IN up to 5V. If V_{IN} does not rise to within 1V of V_{BAT} within 8ms, an over-current event is detected and boost mode is exited and a boost mode over-current event is announced, the BOOST_EN bit is reset to '0' and the STAT_x and FAULT_x bits in the Status/ Control register are updated.

9.4.18.3 Burst Mode during Light Load

In boost mode, the IC operates using burst mode to improve light load efficiency and reduce power loss. During boost mode, the PWM converter is turned off when the device reaches minimum duty cycle and the output voltage rises to $V_{BURST(ENT)}$ threshold. This corresponds to approximately a 75mA inductor current. The converter then restarts when V_{IN} falls to $V_{BURST(EXT)}$. See Figure 37 in the Typical Operating Characteristics for an example waveform.

9.4.18.4 Watchdog Timer in Boost Mode

During boost mode, the watchdog timer is active. The watchdog timer works the same as in charge mode. Write a "1" to the TMR_RST reset bit in the control register. If the watchdog timer expires, the IC resets the EN_BOOST bit to 0, signals the fault pulse on the STAT and INT terminals. The FAULT_x bits read "Low Supply Fault" as this is a higher priority fault than the WD timer.

9.4.18.5 STAT/ INT During Boost Mode

During boost mode, the STAT and INT outputs are high impedance. Under fault conditions, a 128µs pulse is sent out to notify the host of the error condition.

9.4.18.6 Protection in Boost Mode

9.4.18.6.1 Output Over-Voltage Protection

The bq24188 contains integrated over-voltage protection on the IN terminal. During boost mode, if an over-voltage condition is detected (V_{IN} > $V_{BOOSTOVP}$), after deglitch $t_{DGL(BOOST_OVP)}$, the IC turns off the PWM converter, resets EN_BOOST bit to 0, sets fault status bits and sends out a fault pulse on STAT and INT. The converter does not restart when VIN drops to the normal level until the EN_BOOST bit is reset to 1.

9.4.18.6.2 Output Over-Current Protection

The bq24188 contains over current protection to prevent the device and battery damage when IN is overloaded. When an over-current condition occurs, the cycle-by-cycle current limit limits the current from the battery to the load. If the overload condition lasts for 8ms, the overload fault is detected. When an overload condition is detected, the bq24188 turns off the PWM converter, resets EN_BOOST bit to 0, sets the fault status bits and sends out the fault pulse on STAT and INT. The boost operation starts only after the fault is cleared and the EN_BOOST bit is reset to 1 using the I^2C.

9.4.18.6.3 Battery Voltage Protection

During boost mode, when the battery voltage is below the minimum battery voltage threshold, $V_{BATUVLO}$, the IC turns off the PWM converter, resets EN_BOOST bit to 0, sets fault status bits and sends out a fault pulse on STAT and INT. Once the battery voltage returns to the acceptable level, the boost starts only after the EN_BOOST bit is set to 1. Proper operation below 3.3V down to the $V_{BATUVLO}$is not specified.

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9.5 Programming

9.5.1 Serial Interface Description

The bq24188 uses an I^2C compatible interface to program charge parameters. I^2C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor, see I^2C-Bus Specification, Version 5, October 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O terminals, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The bq24188 device works as a slave and supports the following data transfer modes, as defined in the I^2C Bus™ Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. The I^2C circuitry is powered from IN when a supply is connected. If the IN supply is not connected, the I^2C circuitry is powered from the battery through BAT. The battery voltage must stay above $V_{BATUVLO}$ with no input connected in order to maintain proper operation.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The device only supports 7-bit addressing. The device 7-bit address is defined as '1101011' (0x6Bh).

To avoid I^2C hang-ups, a timer ($t_{I2CRESET}$) runs during I2C transactions. If the transaction takes longer than $t_{I2CRESET}$, any additional commands are ignored and the I2C engine is reset. The timeout is reset with START and repeated START conditions and stops when a valid STOP condition is sent.

9.5.2 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 15. All I^2C -compatible devices should recognize a start condition.

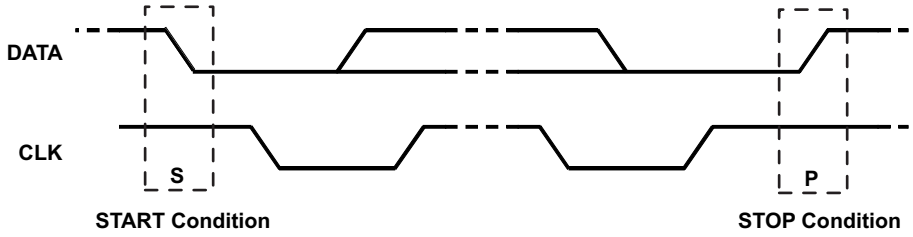

Figure 15. START and STOP Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 16). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 17) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

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Programming (continued)

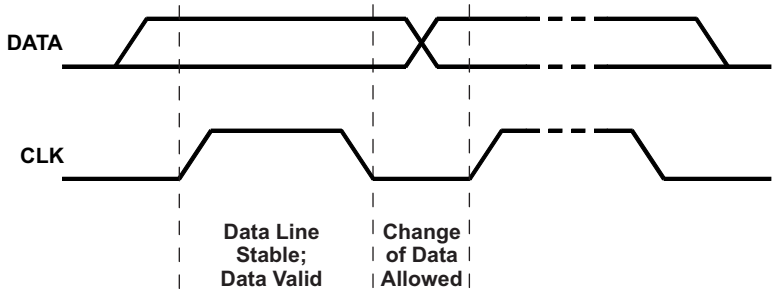

Figure 16. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 0) or receive data from the slave (R/W bit 1. In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 15). This releases the bus and stops the communication link with the addressed slave. All I2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs to send a STOP condition to prevent the slave I2C logic from remaining in a incorrect state. Attempting to read data from register addresses not listed in this section will result in 0xFFh being read out.

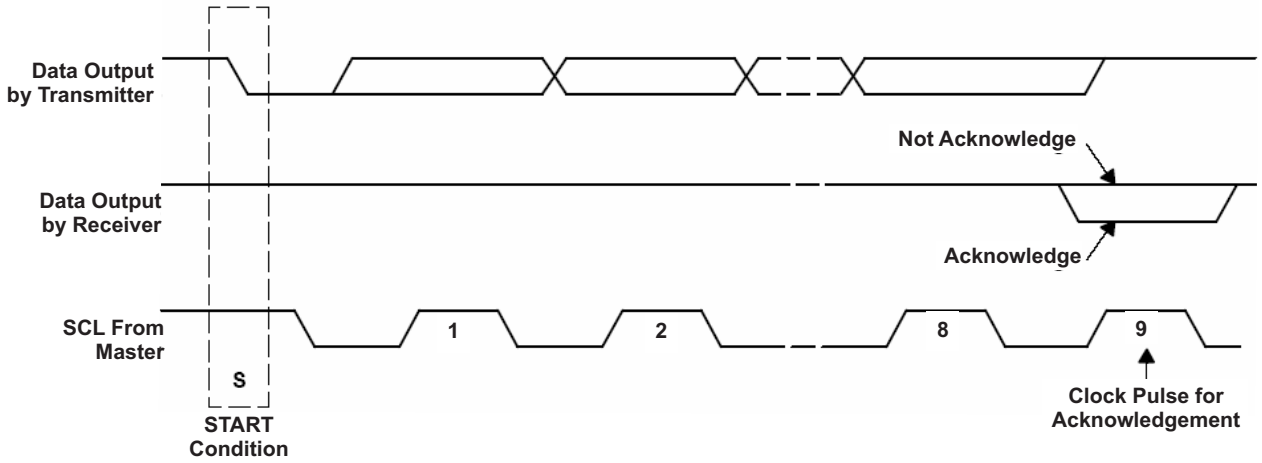

Figure 17. Acknowledge on the I2C Bus

Programming (continued)

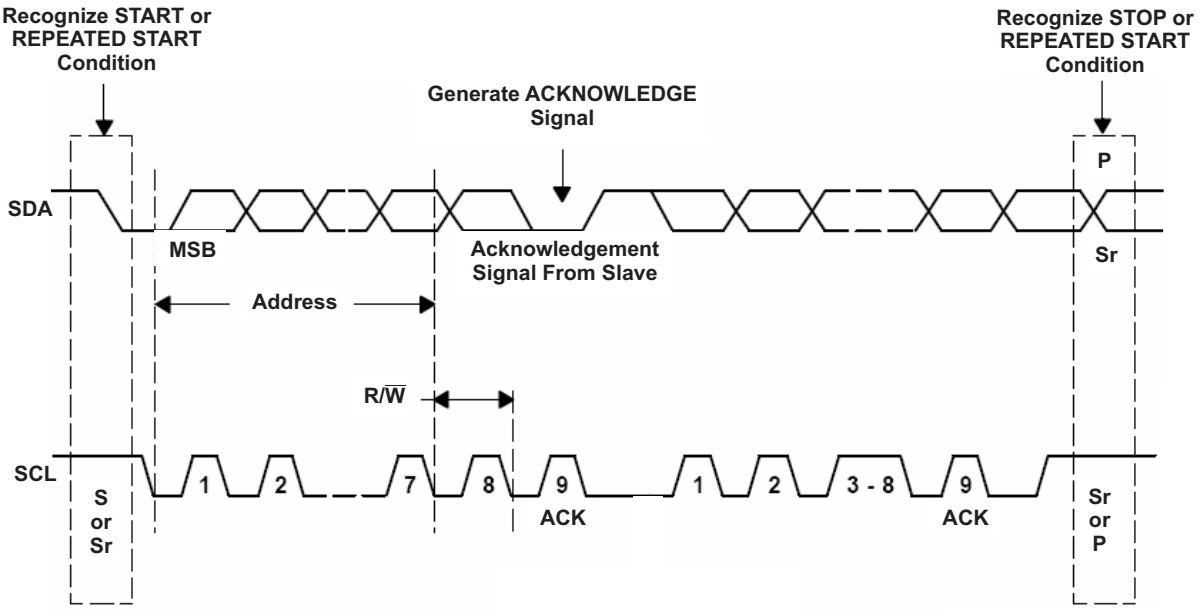

Figure 18. Bus Protocol

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9.6 Register Descriptions

9.6.1 Status/Control Register (READ/WRITE)

Memory location: 00, Reset state: 00xx 0xxx

Figure 19. Status/Control Register

B7(MSB)	B6	B5	B4	B3	B2	B1	B0(LSB)
0	0	X	X	0	X	X	X
R/W	R/W	R	R	R/W	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

BIT	FEILD(1) (2)	TYPE	DESCRIPTION
B7(MSB)	TMR_RST	R/W	Write: TMR_RST function, write “1” to reset the watchdog timer (auto clear) Read: Always 0
B6	EN_BOOST	R/W	0-Charger Mode 1-Boost Mode (default 0)
B5	STAT_1	R	00-Ready 01-Charge in progress 10-Charge done 11-Fault
B4	STAT_0	R	
B3	EN_SHIPMODE	R/W	0-Normal Operation 1-Ship Mode Enabled (default 0)
B2	FAULT_2	R	000-Normal 001-VIN > VOVP or Boost Mode OVP 010- Low Supply connected (VIN<VUVLO or VIN<VSLP) or Boost Mode Overcurrent 011- Thermal Shutdown 100-Battery Temperature Fault 101- Timer Fault (watchdog or safety timer) 110-Battery OVP 111-No Battery connected
B1	FAULT_1	R	
B0(LSB)	FAULT_0	R	

(1) STAT_x bits show current status. These bits change based on the current condition. When a status change occurs, a single 128us pulse on the STAT and INT outputs occur and the STATx and FAULT_x bits of the status registers are updated in the I^2C. Once the fault is removed, the STATx bits are updated to show the current status.

(2) FAULT_x bits show faults. If a fault occurs, these bits announce the fault and do not clear until read. If more than one fault occurs only the highest priority fault is shown, ranked from 1 to 8 in the order shown in the table. When a fault occurs, a single 128µs pulse on the STAT and INT outputs occur and the STATx and FAULT_x bits of the status registers are updated in the I^2C. The FAULT_x bits are not cleared until they are read in the I^2C and the fault condition no longer exists.

EN_BOOST Bit (Operation Mode)

The EN_BOOST bit selects the operation mode for the bq24188 . Write a “1” to enable boost mode and regulate IN to 5V to supply OTG peripherals. See the *Boost Mode Operation* section for more details.

EN_SHIPMODE Bit

Writing the EN_SHIPMODE bit to a “1” latches off the IC, battery FET and BGATE until a high to low transition on UVLO occurs. This means that if EN_SHIPMODE is written to a “1” while the input is connected, it must first be removed and then replaced before the battery FET turns on. This allows the end product with no load on the battery and the end user will enable the device by plugging it into the adapter. The EN_SHIPMODE bit can be cleared using the I^2C interface as well.

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9.6.2 Control Register (READ/WRITE)

Memory location: 01, Reset state: 1xxx 1100

Figure 20. Control Register

B7(MSB)	B6	B5	B4	B3	B2	B1	B0(LSB)
1	X	X	X	1	1	0	.0
W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

BIT	FIELD	TYPE	DESCRIPTION
B7(MSB)	RESET	W	Write: 1-Reset all registers to default values 0-No effect Read: always get “1”
B6	IN_LIMIT_2	R/W	000-USB2.0 host with 100mA current limit 001-USB3.0 host with 150mA current limit 010 – USB2.0 host with 500mA current limit 011 – USB3.0 host/charger with 900mA current limit 100 – Charger with 1500mA current limit 101—Charger with 1950mA current limit 110 – Charger with 2500mA current limit 111- Charger with 2000mA current limit (default 000 (1))
B5	IN_LIMIT_1	R/W	
B4	IN_LIMIT _0	R/W	
B3	EN_STAT	R/W	0-Disable STAT function (STAT only shows faults) 1-Enable STAT function (default 1)
B2	TE	R/W	0-Disable charge current termination 1-Enable charge current termination (default 1)
B1	$\overline{CE}$	R/W	0-Charger enabled 1-Charger is disabled (default 0)
B0(LSB)	HZ_MODE	R/W	0-Not high impedance mode 1-High impedance mode (default 0)

(1) When in DEFAULT mode, PSEL determines the default input current limit.

RESET Bit

The RESET bit in the control register (0x01h) is used to reset all the charge parameters. Write “1” to RESET bit to reset all the registers to default values and place the bq24188 into DEFAULT mode and turn off the watchdog timer. The RESET bit is automatically cleared to zero once the bq24188 enters DEFAULT mode.

$\overline{CE}$ Bit (Charge Enable)

The $\overline{CE}$ bit is used to disable or enable the charge process. A low logic level (0) on this bit enables the charge and a high logic level (1) disables the charge. When charge is disabled, the SYS output regulates to $V_{SYS(REG)}$ and battery is disconnected from the SYS. Supplement mode is available if the system load demands cannot be met by the supply.

HZ_MODE Bit (High Impedance Mode Enable)

The HZ_MODE bit is used to disable or enable the high impedance mode. A low logic level (0) on this bit enables the IC and a high logic level (1) puts the IC in a low quiescent current state called high impedance mode. When in high impedance mode, the converter is off and the battery FET and BGATE are on. The load on SYS is supplied by the battery. BGATE is low (external FET turned on) while in high impedance mode.

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9.6.3 Control/Battery Voltage Register (READ/WRITE)

Memory location: 02, Reset state: 0001 0100

Figure 21. Control/Battery Voltage Register

B7(MSB)	B6	B5	B4	B3	B2	B1	B0(LSB)
1	0	0	0	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

BIT	FIELD	TYPE	DESCRIPTION
B7(MSB)	V_{BREG5}	R/W	Battery Regulation Voltage: 640mV (default 0)
B6	V_{BREG4}	R/W	Battery Regulation Voltage: 320mV (default 0)
B5	V_{BREG3}	R/W	Battery Regulation Voltage: 160mV (default 0)
B4	V_{BREG2}	R/W	Battery Regulation Voltage: 80mV (default 1)
B3	V_{BREG1}	R/W	Battery Regulation Voltage: 40mV (default 0)
B2	V_{BREG0}	R/W	Battery Regulation Voltage: 20mV (default 1)
B1	MOD_FREQ1	R/W	Modify Switching Frequency Target – 00 – No Change to Nominal Frequency Target 01 – +10% Change to Nominal Frequency 10 – -10% Change to Nominal Frequency 11 – NA (default 00)
B0(LSB)	MOD_FREQ0	R/W	

V_{BREG} Bits (Battery Regulation Threshold setting)

Use V_{BREG} bits to set the battery regulation threshold. The VBATREG is calculated using the following equation:

$$V_{BATREG} = 3.5\ V + V_{BREG}CODE \times 20\ mV$$

The charge voltage range is 3.5V to 4.44V with the offset of 3.5V and step of 20mV. The default setting is 3.6V. If a value greater than 4.44V is written, the setting goes to 4.44V. It is recommended to set V_{BATREG} above V_{MINSYS}.

MOD_FREQx Bits (Frequency Modification)

The MOD_FREQx bits are used to change the switching frequency by ±10%. This is used for applications where the 1.5MHz switching frequency noise interferes with other device operation. The frequency may be modified by ±10% of the nominal frequency.

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9.6.4 Vender/Part/Revision Register (READ only)

Memory location: 03, Reset state: 0100 0110

Figure 22. Vender/Part/Revision Register

B7(MSB)	B6	B5	B4	B3	B2	B1	B0(LSB)
0	1	0	0	0	1	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

BIT	FIELD	TYPE	DESCRIPTION
B7(MSB)	Vendor2	R	Vender Code: bit 2 (default 0)
B6	Vendor1	R	Vender Code: bit 1 (default 1)
B5	Vendor0	R	Vender Code: bit 0 (default 0)
B4	PN1	R	For I^2C Address 6Bh: 00
B3	PN0	R	
B2	NA	R	NA
B1	NA	R	NA
B0(LSB)	NA	R	NA

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9.6.5 Battery Termination/Fast Charge Current Register (READ/WRITE)

Memory location: 04, Reset state: 0010 1010

Figure 23. Battery Termination/Fast Charge Current Register

B7(MSB)	B6	B5	B4	B3	B2	B1	B0(LSB)
0	0	1	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

BIT	FIELD	TYPE	DESCRIPTION
B7(MSB)	I_{CHRG4}	R/W	Charge current 1600mA – (default 0)
B6	I_{CHRG3}	R/W	Charge current: 800mA — (default 0)
B5	I_{CHRG2}	R/W	Charge current: 400mA —(default 1)
B4	I_{CHRG1}	R/W	Charge current: 200mA — (default 0)
B3	I_{CHRG0}	R/W	Charge current: 100mA (default 1)
B2	I_{TERM2}	R/W	Termination current sense: 200mA (default 0)
B1	I_{TERM1}	R/W	Termination current sense voltage: 100mA (default 1)
B0(LSB)	I_{TERM0}	R/W	Termination current sense voltage: 50mA (default 0)

I_{CHRG} Bits (Charge Current Regulation Threshold setting)

Use I_{CHRG} bits to set the charge current regulation threshold. The charge current is programmable from 500mA to 2A in 100mA steps. The default is 1A. The I_{CHARGE} is calculated using the following equation:

$$I_{CHARGE} = 500\ mA + I_{CHRG}CODE \times 100\ mA$$

Any Operation above 2A is not specified.

I_{TERM} Bits (Charge Current Termination Threshold setting)

Use I_{TERM} bits to set the charge current termination threshold. The termination threshold is programmable from 50mA to 300mA in 50mA steps. The default is 150mA. The I_{TERM} is calculated using the following equation:

$$I_{TERM} = 50\ mA + I_{TERM}CODE \times 50\ mA$$

Any setting programmed above 300mA selects the 300mA setting.

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9.6.6 V_{IN-DPM} Voltage/ MINSYS Status Register

Memory location: 05, Reset state: xx00 x000

Figure 24. V_{IN-DPM} Voltage/ MINSYS Status Register

B7(MSB)	B6	B5	B4	B3	B2	B1	B0(LSB)
X	X	0	0	X	0	0	0
R	R	R/W	R/W	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

BIT	FIELD	TYPE	DESCRIPTION
B7(MSB)	MINSYS_STATUS	R	0 – Minimum System Voltage mode is not active 1 – Minimum System Voltage mode is active (low battery
B6	VINDPM_STATUS	R	0 – VIN-DPM mode is not active 1 – VIN-DPM mode is active
B5	LOW_CHG	R/W	0 – Normal charge current set by 04h 1 – Low charge current setting 300mA (default 0)
B4	NA	R	NA
B3	CD_STATUS	R	0 – CD low, IC enabled 1 – CD high, IC disabled
B2	V_{INDPM2}	R/W	Input V_{IN-DPM} voltage: V_{DPMOFF} + 8% (default 0)
B1	V_{INDPM1}	R/W	Input V_{IN-DPM} voltage: V_{DPMOFF} + 4% (default 0)
B0(LSB)	V_{INDPM0}	R/W	Input V_{IN-DPM} voltage: V_{DPMOFF} + 2% (default 0)

- V_{IN-DPM} voltage offset is programmable using the VINDPM_OFF bit (bit 0 of register 0x06) and default V_{IN-DPM} threshold is 4.2V.

LOW_CHG Bit (Low Charge Mode Enable)

The LOW_CHG bit is used to reduce the charge current to a minimum current. This feature is used by systems where battery NTC is monitored by the host and requires a reduced charge current setting or by systems that need a “preconditioning” current for low battery voltages. Write a “1” to this bit to charge at 300mA. Write a “0” to this bit to charge at the programmed charge current.

V_{INDPM} Bits (V_{INDPM} Threshold setting)

Use V_{INDPM} bits to set the V_{INDPM} regulation threshold. The V_{INDPM} threshold is calculated using the following equation:

$$V_{INDPM} = V_{INDPM_OFF} + V_{INDPM}CODE \times 2\% \times V_{INDPM_OFF}$$

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9.6.7 Safety Timer/ NTC Monitor Register (READ/WRITE)

Memory location: 06, Reset state: 1001 1xx0

Figure 25. Safety Timer/ NTC Monitor Register

B7(MSB)	B6	B5	B4	B3	B2	B1	B0(LSB)
1	0	0	1	1	X	X	0
R/W	R/W	R/W	R/W	R/W	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

BIT	FIELD	TYPE	DESCRIPTION
B7(MSB)	2XTMR_EN	R/W	0 – Timer not slowed at any time 1 – Timer slowed by 2x when in thermal regulation, V_{IN_DPM} or input current limit (default 1)
B6	TMR_1	R/W	Safety Timer Time Limit – 00 – 1.25 minute fast charge 01 – 6 hour fast charge 10 – 9 hour fast charge 11 – Disable safety timers (default 00)
B5	TMR_2	R/W	
B4	BOOST_ILIM	R/W	0 – 500mA 1 – 1A (Default 1)
B3	TS_EN	R/W	0 – TS function disabled 1 – TS function enabled (default 1)
B2	TS_FAULT1	R	TS Fault Mode: 00 – Normal, No TS fault 01 – TS temp < T_{COLD} or TS temp > T_{HOT}(Charging suspended) 10 – T_{COOL} > TS temp > T_{COLD} (Charge current reduced by half) 11 – T_{WARM} < TS temp < T_{HOT} (Charge voltage reduced by 100mV)
B1	TS_FAULT0	R	
B0(LSB)	VINDPM_OFF	R/W	0 – 4.2V 1 – 10.1V (Default 0)

BOOST_ILIM Bit (Boost current limit setting)

The BOOST_ILIM bit programs the cycle by cycle current limit threshold for boost operation. The 1 A setting sets the low side cycle by cycle current limit to 4 A (typ). This ensures that at least 1 A can be supplied from the boost converter over the entire battery range. The 500 mA setting sets the current limit to 2 A (typ) to ensure at least 500 mA available from the boost converter. See the *Output Over-Current Protection* section for more details.

VINDPM_OFF Bit (V_{INDPM} offset setting)

The VINDPM_OFF bit programs the offset for the VINDPM function. The 4.2 V setting is intended to work with a standard 5V output adapter. The 10.1 V setting supports 12 V adapters and the 12 V output for the new USB Power Delivery specification (USB PD).

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10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The bq24188EVM evaluation module (EVM) is a complete charger module for evaluating the bq24188. The application curves were taken using the bq24188. See *Related Documentation* .

10.2 Typical Applications

10.2.1 bq24188 Typical Application

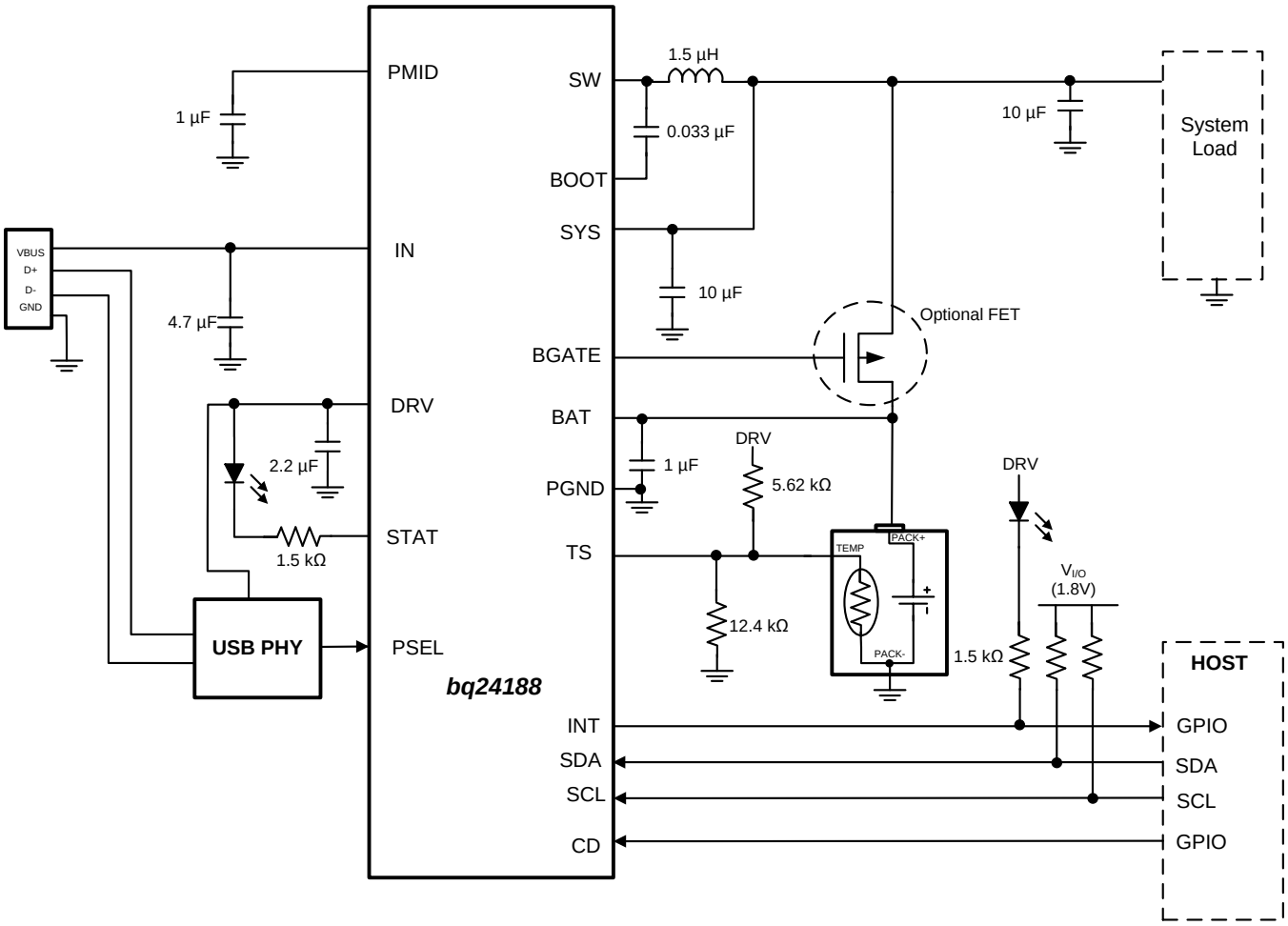

Figure 26. bq24188 Typical Application Circuit

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Typical Applications (continued)

10.2.1.1 Design Requirements

Table 2. Design Requirements

DESIGN PARAMATER	EXAMPLE VALUE
Input Voltage Range	4.75 V to 5.25 V nominal, withstand 28 V
Input Current Limit	1500 mA
Input DPM Threshold	4.25 V
Fast Charge Current	2000 mA
Battery Charge Voltage	4.2 V
Termination Current	50 mA

10.2.1.2 Detailed Design Procedure

The parameters are configurable using the EVM software.

The typical application circuit shows the minimum capacitance requirements for each pin. Options for sizing the inductor outside the 1.5 µH recommended value and additional SYS pin capacitance are explained in the next section. The resistors on STAT and INT are sized per each LED's current requirements. The TS resistor divider for configuring the TS function to work with the battery's specific thermistor can be computed from Equation 1 and Equation 2. The external battery FET is optional.

10.2.2 bq24188 Typical Application – External Discharge FET

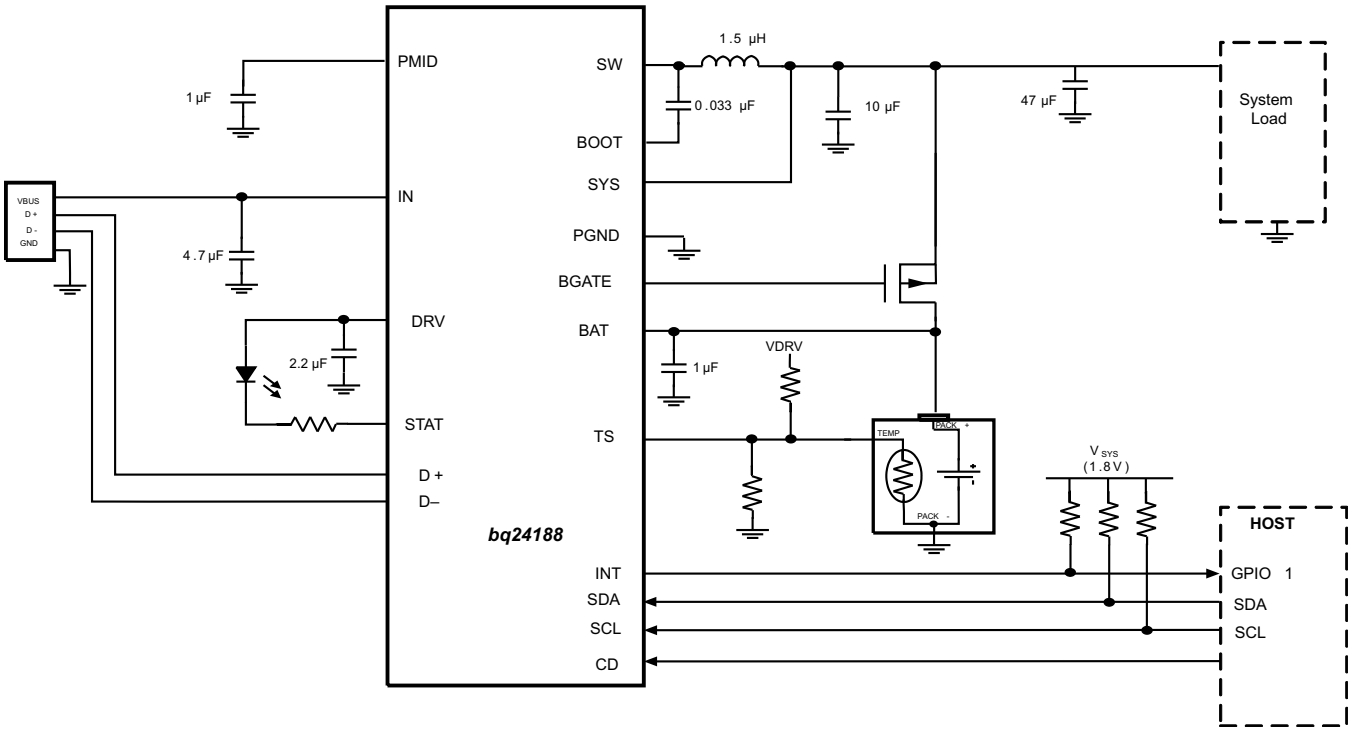

Figure 27. bq24188 Typical Application Circuit

10.2.3 Output Inductor and Capacitor Selection Guidelines

When selecting an inductor, several attributes must be examined to find the right part for the application. First, the inductance value should be selected. The bq24188 is designed to work with 1.5 µH to 2.2 µH inductors. The chosen value will have an effect on efficiency and package size. Due to the smaller current ripple, some efficiency gain is reached using the 2.2 µH inductor, however, due to the physical size of the inductor, this may not be a viable option. The 1.5 µH inductor provides a good tradeoff between size and efficiency.

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Once the inductance has been selected, the peak current must be calculated in order to choose the current rating of the inductor. Use Equation 5 to calculate the peak current.

$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{\%_{RIPPPLE}}{2}\right) \quad (5)$$

The inductor selected must have a saturation current rating greater than or equal to the calculated I_{PEAK}. Due to the high currents possible with the bq24188, a thermal analysis must also be done for the inductor. Many inductors have 40°C temperature rise rating. This is the DC current that will cause a 40°C temperature rise above the ambient temperature in the inductor. For this analysis, the typical load current may be used adjusted for the duty cycle of the load transients. For example, if the application requires a 1.5A DC load with peaks at 2.5A 20% of the time, a Δ40°C temperature rise current must be greater than 1.7A:

$I_{TEMPRISE} = I_{LOAD} + D \times (I_{PEAK} - I_{LOAD}) = 1.5\ A + 0.2 \times (2.5\ A - 1.5\ A) = 1.7\ A$

The internal loop compensation of the bq24188 is designed to be stable with 10 µF to 150 µF of local capacitance but requires at least 20 µF total capacitance on the SYS rail (10 µF local + ≥ 10 µF distributed). The capacitance on the SYS rail can be higher than 150 µF if distributed amongst the rail. To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 10 µF and 47 µF is recommended for local bypass to SYS. If greater than 100 µF effective capacitance is on the SYS rail, place at least 10 µF bypass on the BAT terminal. Pay special attention to the DC bias characteristics of ceramic capacitors. For small case sizes, the capacitance can be derated as high as 70% at workable voltages. All capacitances specified in this datasheet are effective capacitance, not capacitor value.

10.2.4 Application Curves

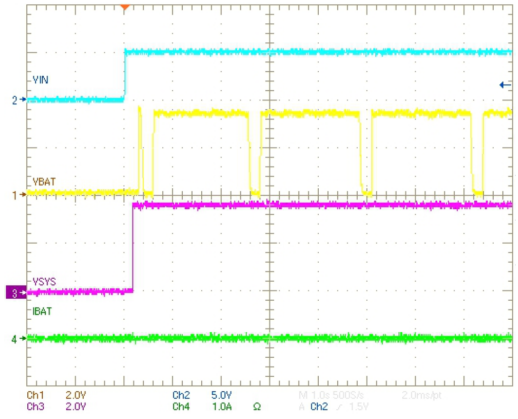
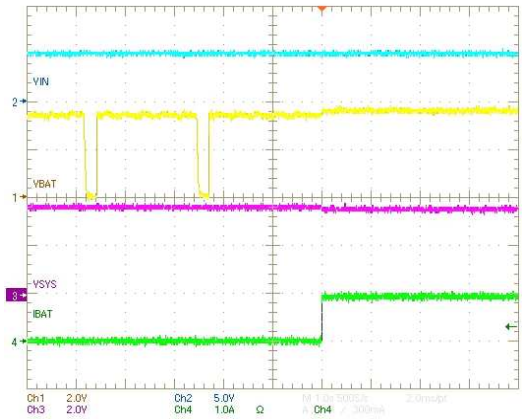


Figure 28. Startup With No Battery



VBAT = 3.8V VIN = 5V
VREG = 4.2V ICHG = 0.5V

Figure 29. Battery Detection

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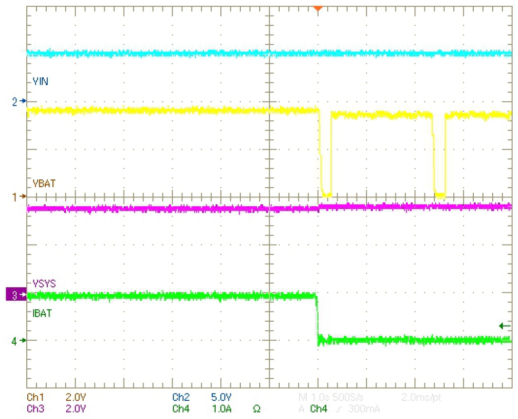


Figure 30. Battery Removal

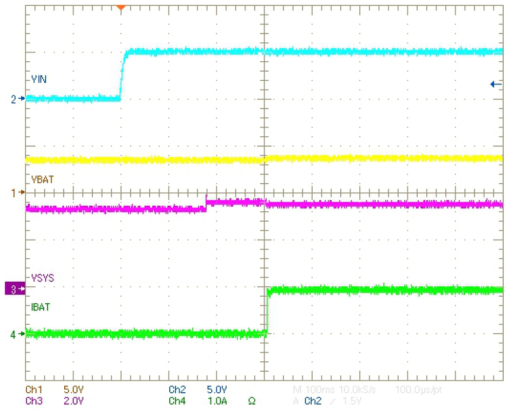


Figure 31. Default Start-Up - bq24188 (D+/D– Shorted)

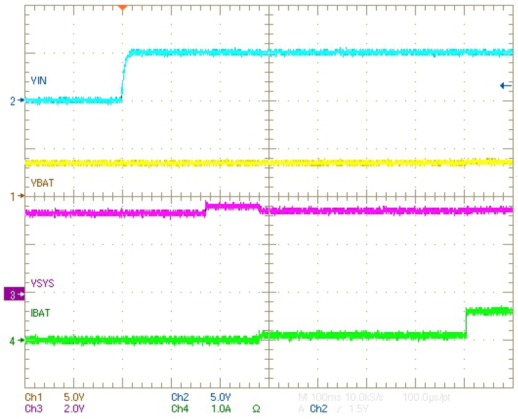
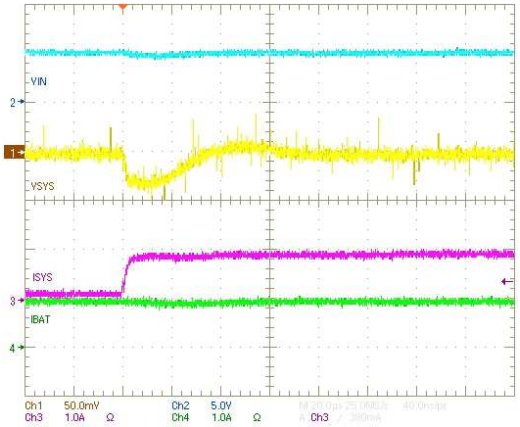
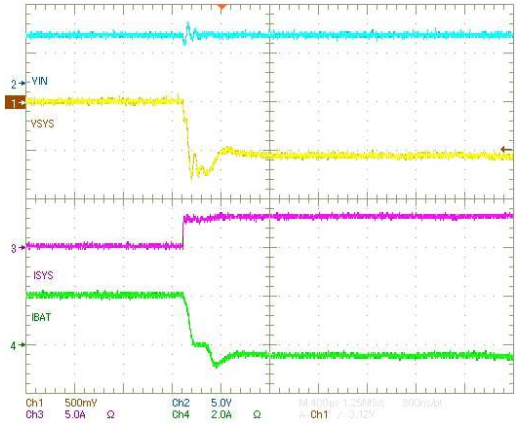


Figure 32. Default Start-Up - bq24188 (D+/D– Not Shorted)



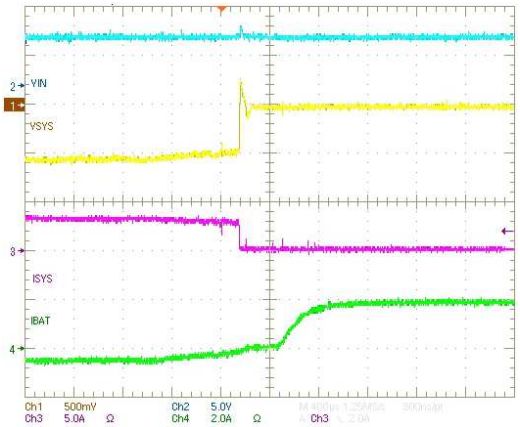
VBATREG = 3.6V VIN = 5.5V
VSYS = 3.68V Step from 100mA to 3.3A

Figure 33. VSYS Transient Without Supplement Mode



VBATREG = 3.6V VIN = 5V
VBAT = 3.4V Step from 100mA to 3.3A

Figure 34. VSYS Transient With Supplement Mode



VBATREG = 3.6V VIN = 5V
VBAT = 3.4V Step from 100mA to 3.3A

Figure 35. VSYS Transient With Supplement Mode

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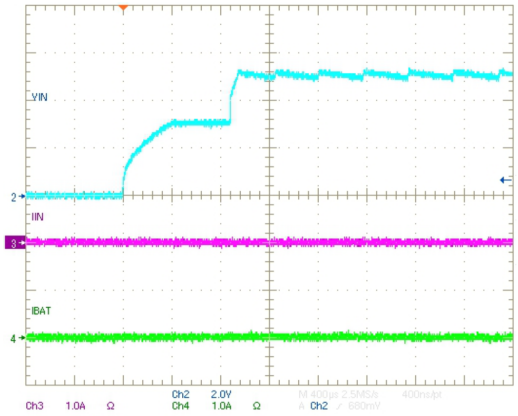


Figure 36. Boost Startup No Load

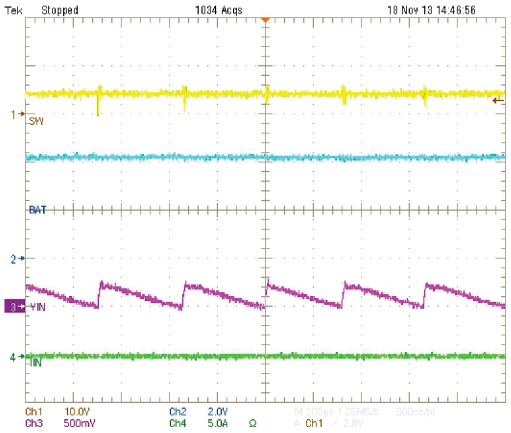


Figure 37. Boost Burst Mode During Light Load

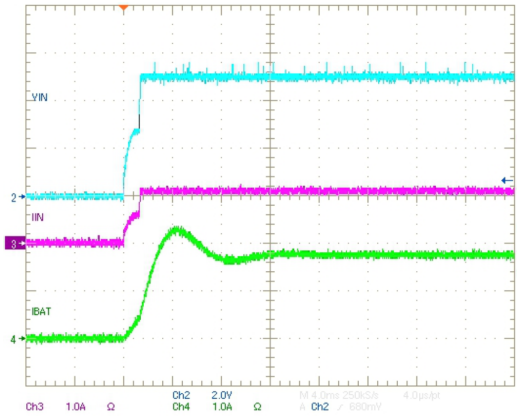


Figure 38. Boost Startup 1A Load

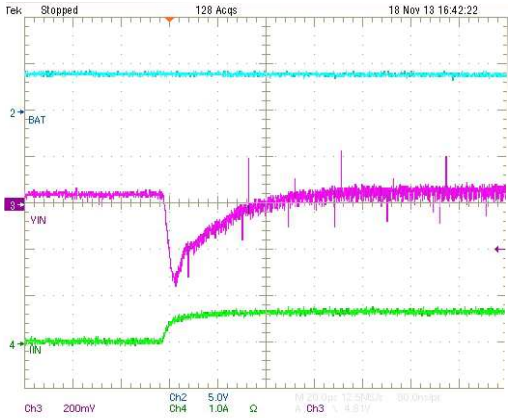


Figure 39. Boost Transient Response

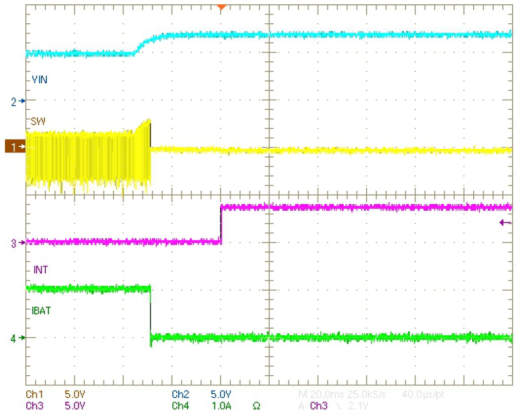
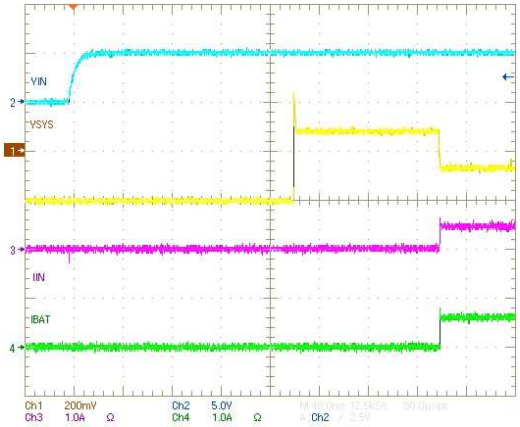


Figure 40. Input OVP Event with INT



VBAT = 3.6V VBATREG = 4.2V
ICHG = 2A ILIM = 0.5A
ISYS = 0A VDPM = 4.36V

Figure 41. Startup, 4.2V

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11 Power Supply Recommendations

11.1 Requirements for SYS Output

In order to provide an output voltage on SYS, the bq24188 requires either a power supply between 4.2 V and 6.0 V input on all versions, 4.2 and 14 V on bq24188 with at least 100 mA current rating connected to IN; or, a single-cell Li-Ion battery with voltage > VBATUVLO connected to BAT. The source current rating needs to be at least 2.5 A in order for the buck converter of the charger to provide maximum output power to SYS.

11.2 Requirements for Charging

In order for charging to occur the source voltage measured at the IN terminals of the IC, factoring in cable/trace losses from the source, must be greater than the VINDPM threshold, but less than the maximum values shown above. The current rating of the source must be higher than the buck converter needs to provide the load on SYS. For charging at a desired charge current of I_{CHRG}, V_{IN} x I_{IN} x η > V_{SYS} x ($_{ISYS}$+ I_{CHRG}) where η is the efficiency estimate from Figure 2 or Figure 3 and VSYS = VBAT when VBAT charges above VMINSYS. The charger limits I_{IN} to the current limit setting of that input. With ISYS = 0 A, the charger consumes maximum power at the end of CC mode, when the voltage at the BAT terminal is near VBATREG but ICHRG has not started to taper off toward ITERM.

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12 Layout

12.1 Layout Guidelines

The following provides some guidelines:

- Place 1µF input capacitor as close to PMID terminal and PGND terminal as possible to make high frequency current loop area as small as possible.
- Connect the GND of the PMID and IN caps as close as possible.
- Place 4.7µF input capacitor as close to IN terminal and PGND terminal as possible to make high frequency current loop area as small as possible.
- The local bypass capacitor from SYS to GND should be connected between the SYS terminal and PGND of the IC. The intent is to minimize the current path loop area from the SW terminal through the LC filter and back to the PGND terminal.
- Place all decoupling capacitors close to their respective IC terminal and as close as to PGND as possible. Do not place components such that routing interrupts power stage currents. All small control signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias. Two vias per capacitor for power-stage capacitors and one via per capacitor for small-signal components. It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results.
- The high-current charge paths into IN, BAT, SYS and from the SW terminals must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND terminals should be connected to the ground plane to return current through the internal low-side FET.
- For high-current applications, the balls for the power paths should be connected to as much copper in the board as possible. This allows better thermal performance as the board pulls heat away from the IC.

12.2 Layout Example

It is important to pay special attention to the PCB layout. Figure 42 provides a sample layout for the high current paths of the bq24188YFF. Figure 43 provides a sample layout for the high current paths of the bq24188RGE.

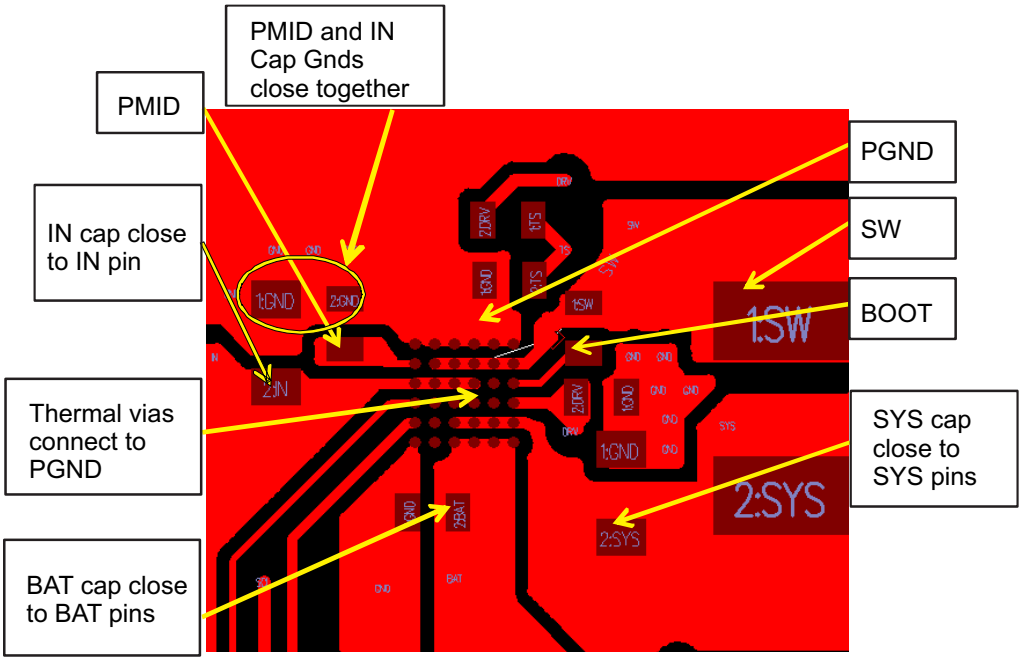

Figure 42. Recommended bq24188 PCB Layout for WCSP Package

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Layout Example (continued)

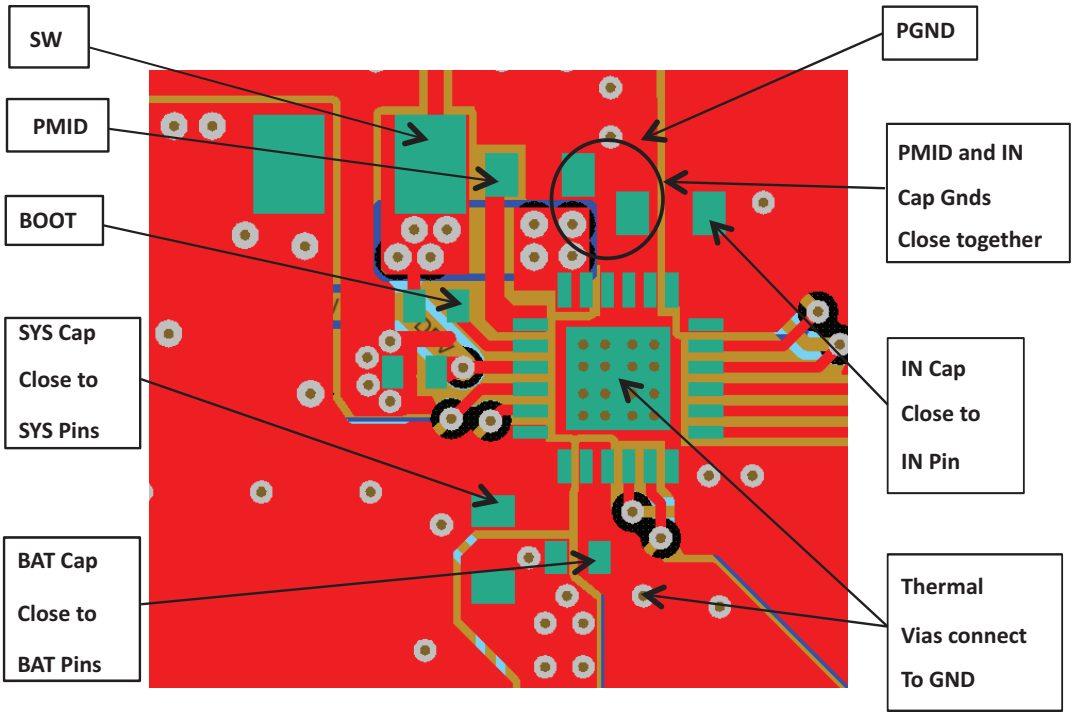

Figure 43. Recommended bq24188 PCB Layout for QFN Package

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

User's Guide for WCSP Packaged bq24260, bq24261 and bq24262A 3-A Battery Charger Evaluation Module, SLUUAB0.

User's Guide for QFN Packaged bq24260, bq24261, and bq24262 3-A Battery Charger Evaluation Module, SLUUAV8.

3A, Host-Controlled Single-Input, Single Cell Switchmode Li-Ion Battery Charger Evaluation Module, http://www.ti.com/tool/bq24261evm-611.

Host-Controlled Single-Input, Single Cell Switchmode Li-Ion Battery Charger Evaluation Module, http://www.ti.com/tool/bq24261evm-079.

EVM Software, SLUC519

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24188YFFR	ACTIVE	DSBGA	YFF	36	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24188	Samples
BQ24188YFFT	ACTIVE	DSBGA	YFF	36	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24188	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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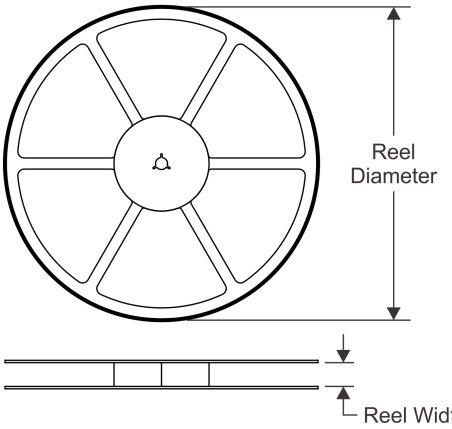
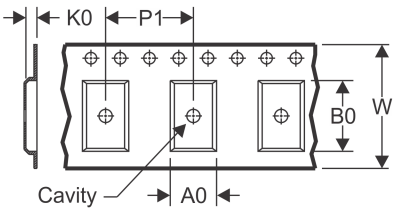
TAPE AND REEL INFORMATION

REEL DIMENSIONS

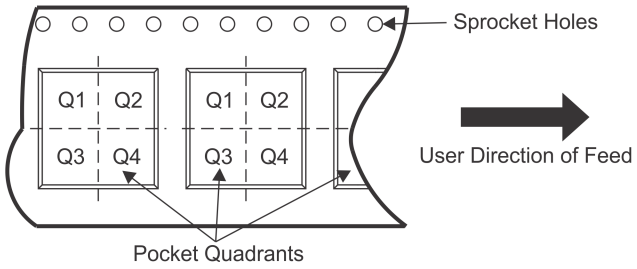


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

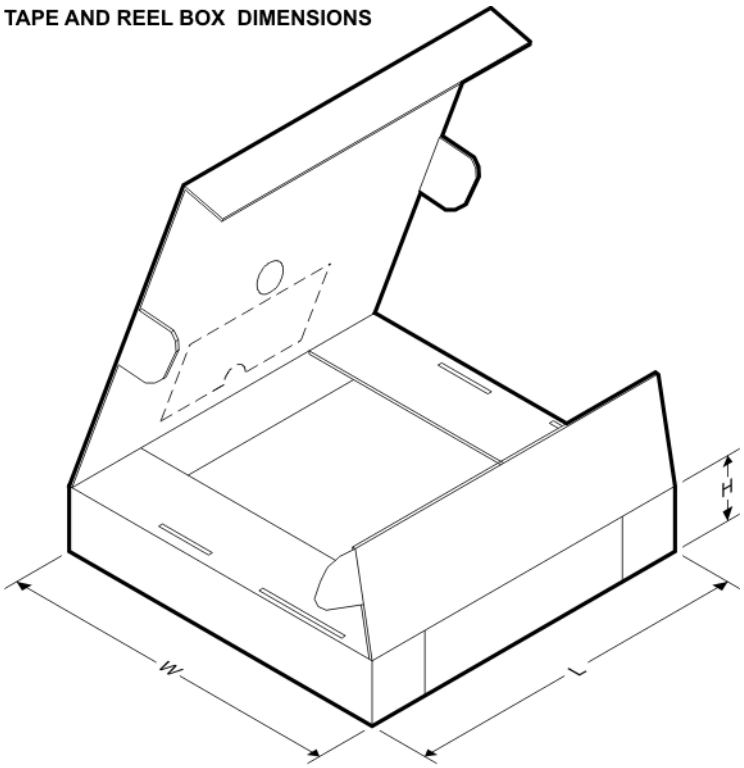
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24188YFFR	DSBGA	YFF	36	3000	180.0	8.4	2.54	2.54	0.76	4.0	8.0	Q1
BQ24188YFFT	DSBGA	YFF	36	250	180.0	8.4	2.54	2.54	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

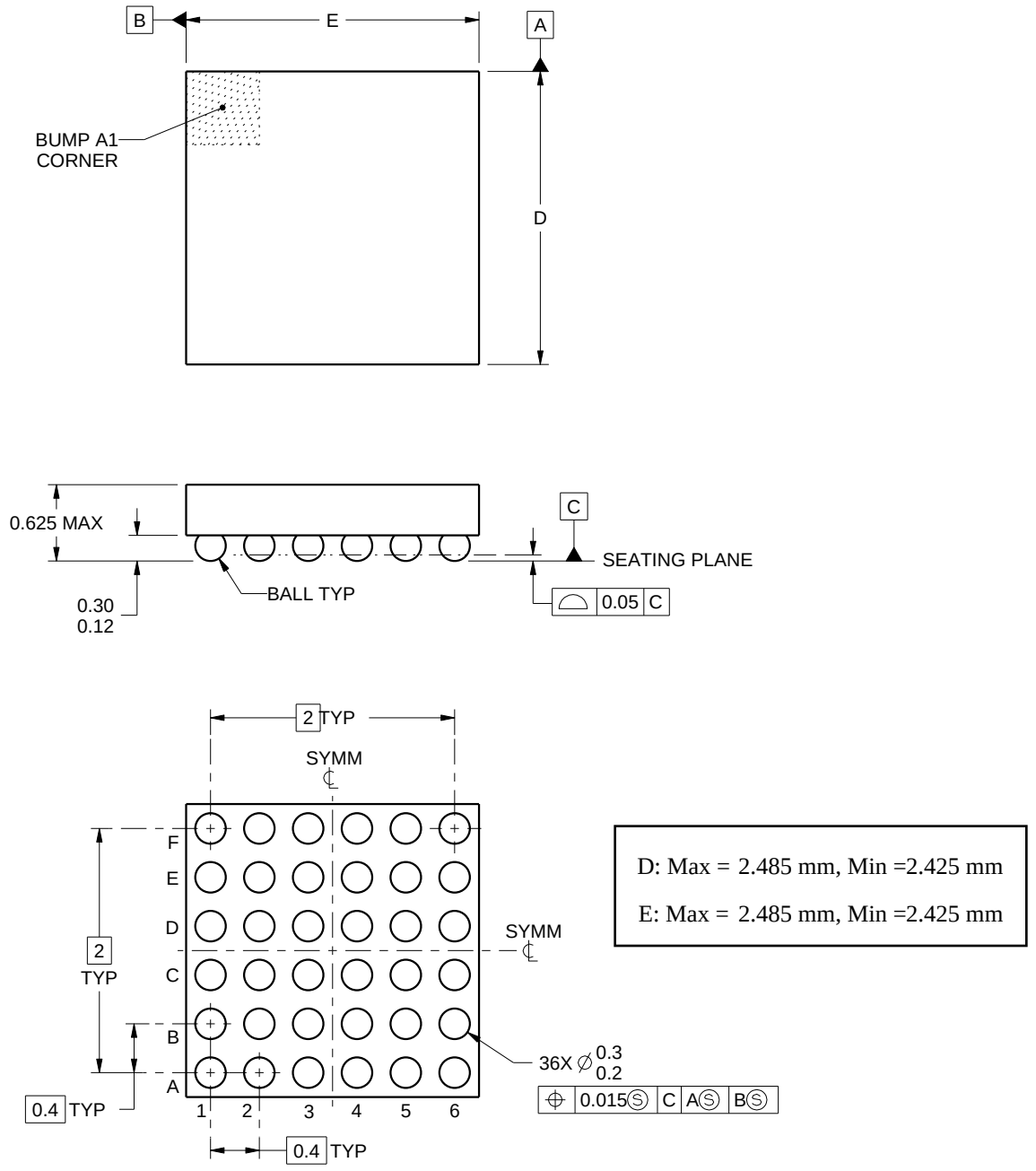
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24188YFFR	DSBGA	YFF	36	3000	182.0	182.0	20.0
BQ24188YFFT	DSBGA	YFF	36	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0036

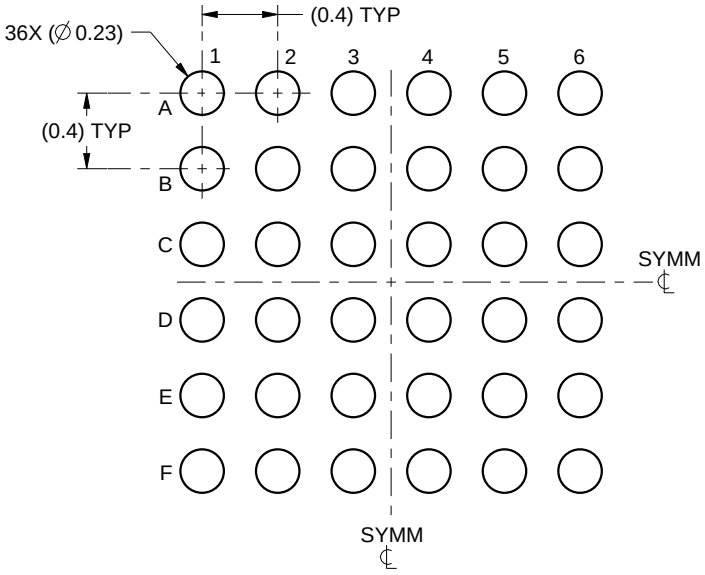
DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

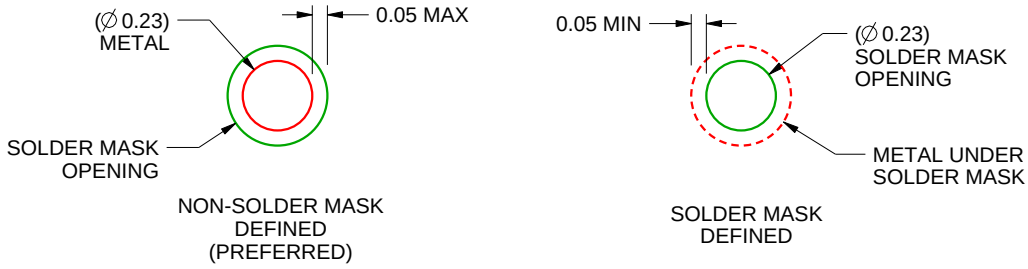


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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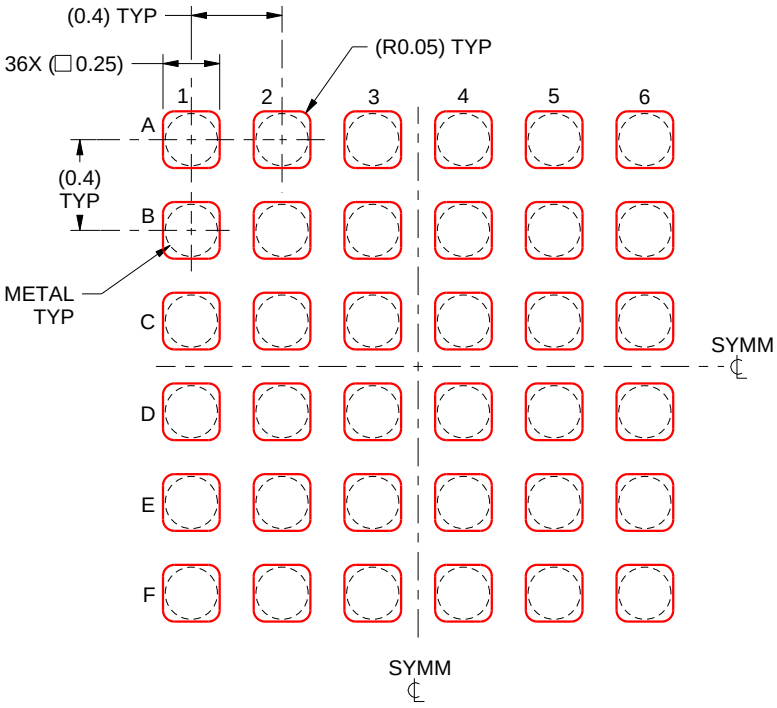
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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