

## Power Management LSI Series for Automotive Body Control

# LDO Regulator



## BD3940FP, BD3941FP/HFP/T

### ●Description

BD394□FP Series regulators feature a high 36 V breakdown voltage and are compatible with onboard vehicle microcontrollers. They offer an output current of 500 mA while limiting dark current to 30  $\mu$ A (TYP). The series supports the use of ceramic capacitors as output phase compensation capacitors. Since the ICs use P-channel DMOS output transistors, increased loads do not result in increased total supply current. BD394□FP Series is ideal for lowering current consumption and costs in battery direct-coupled systems.

### ●Features

- 1) Super-low dark current: 30  $\mu$ A (Typ.)
- 2) Low-saturation voltage type P-channel DMOS output transistors  
Output on resistance: 1.6  $\Omega$  (Typ.)
- 3) High precision output voltage: 5 V  $\pm$ 2% (Ta = 25°C) / I<sub>omax</sub> = 500 mA
- 4) Low-ESR ceramic capacitors can be used as output capacitors
- 5) V<sub>cc</sub> power supply voltage = 36 V / Peak power supply voltage = 50 V (tr  $\geq$  1 ms, tH  $\leq$  200 ms)
- 6) Built-in over current protection circuit and thermal shutdown circuit
- 7) TO252-3/HRP-5/TO220FP-3 package

### ●Applications

Vehicle equipment, car stereos, satellite navigation systems, etc.

### ●Product line

Model	BD3940FP	BD3941FP/HFP/T
Output voltage	3.3 V	5.0 V

### ●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Power supply voltage	V <sub>cc</sub>	36 <sup>*1</sup>	V
Output current	I <sub>o</sub>	500	mA
Power dissipation	P <sub>d</sub>	1.2 <sup>*2</sup>	W
		1.6 <sup>*3</sup>	
		2.0 <sup>*4</sup>	
Operating temperature range	T <sub>opr</sub>	-40 to +125	°C
Storage temperature range	T <sub>stg</sub>	-55 to +150	°C
Peak power supply voltage	V <sub>cc Peak</sub>	50 <sup>*5</sup>	V
Maximum junction temperature	T <sub>jmax</sub>	150	°C

\* 1Not to exceed P<sub>d</sub>.

\*2 For TO252-3, reduced by 9.6 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm  $\times$  70 mm  $\times$  1.6 mm).

\*3 Reduced by 12.8 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm  $\times$  70 mm  $\times$  1.6 mm).

\*4 For TO220FP-3, reduced by 16.0 mW/°C over 25°C.

\*5 Application time 200 ms or shorter. (tr  $\geq$  1 ms)

●Recommended operating conditions (Ta = 25°C)

Parameter		Symbol	Min.	Max.	Unit
Input voltage	BD3940FP/HFP	Vcc	4.5	25.0	V
	BD3941FP/HFP/T	Vcc	6.2	25.0	V
Output current		Io	—	500	mA

●Electrical characteristics (Unless otherwise specified, Ta = 25°C; Vcc = 13.2 V; Io = 200 mA)

Parameter	Symbol	Limit			Unit	Conditions	
		Min.	Typ.	Max.			
Bias current 1	Ib1	—	30	40	μA	Io = 0 mA	
Bias current 2	Ib2	—	30	—	μA	Io = 200 mA	
Output voltage	BD3940FP	Vo	3.234	3.300	3.366	V	
	BD3941FP/HFP/T	Vo	4.900	5.000	5.100	V	
Output current	Io	500	—	—	mA		
Minimum I/O voltage difference	BD3940FP	ΔVd	—	0.45	0.65	V	Vcc = 3.135 V, Io = 100 mA
	BD3941FP/HFP/T						Vcc = 4.75 V, Io = 200 mA
Ripple rejection	R.R.	45	55	—	dB	f = 120 Hz, ein = 1 Vrms, Io = 100 mA	
Input stability	BD3940FP	Reg.I	—	10	30	mV	Vcc = 4.5 V → 25 V
	BD3941FP/HFP/T						Vcc = 6.2 V → 25 V
Load stability	Reg.L	—	20	60	mV	Io = 0 mA → 200 mA	

●Electrical characteristics (Unless otherwise specified, Ta = -40°C to +125°C; Vcc = 13.2 V; Io = 200 mA)

Parameter	Symbol	Limit			Unit	Conditions	
		Min.	Typ.	Max.			
Bias current 1	Ib1	—	30	40	μA	Io = 0 mA	
Bias current 2	Ib2	—	30	—	μA	Io = 200 mA	
Output voltage	BD3940FP	Vo	3.168	3.300	3.366	V	
	BD3941FP/HFP/T	Vo	4.800	5.000	5.100	V	
Output current	Io	500	—	—	mA		
Minimum I/O voltage difference	BD3940FP	ΔVd	—	—	0.9	V	Vcc = 3.135 V, Io = 100 mA
	BD3941FP/HFP/T						Vcc = 4.75 V, Io = 200 mA
Ripple rejection	R.R.	45	55	—	dB	f = 120 Hz, ein = 1 Vrms, Io = 100 mA	
Input stability	BD3940FP	Reg. I	—	10	45	mV	Vcc = 4.5 V → 25 V
	BD3941FP/HFP/T						Vcc = 6.2 V → 25 V
Load stability	Reg.L	—	20	60	mV	Io = 0 mA → 200 mA	

Note: This IC is not designed to be radiation-resistant.

Note: All characteristics are measured with 0.33 μF and 0.1 μF capacitors connected to input and output pins, respectively.

Because measurements (pulse measurements) were taken when Ta ≈ Tj, data other than the output voltage/temperature coefficient does not include fluctuations due to temperature variations.

●Reference data (Unless otherwise specified,  $T_a = 25^\circ\text{C}$ )

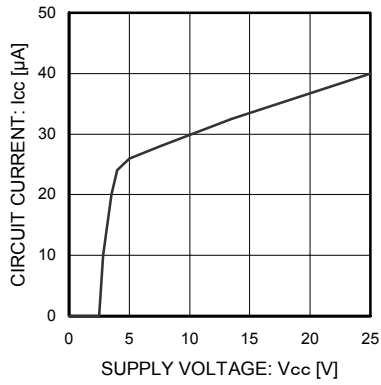


Fig. 1 Total Supply Current

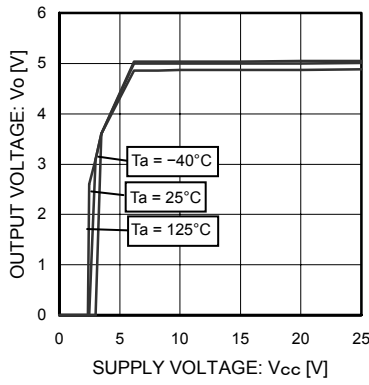


Fig. 2 Output Voltage vs Power Supply Voltage

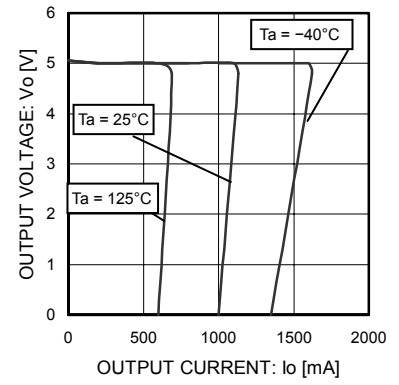


Fig. 3 Output Voltage vs Load

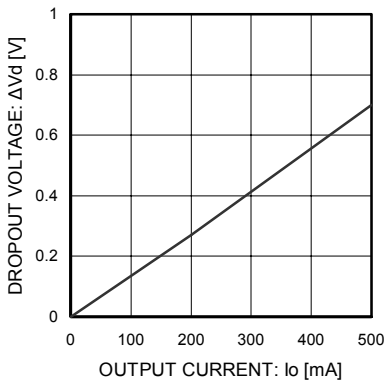


Fig. 4 I/O Voltage Difference

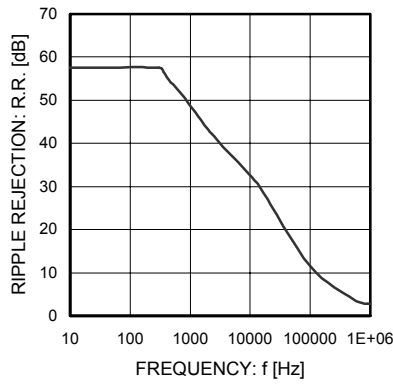


Fig. 5 Ripple Rejection

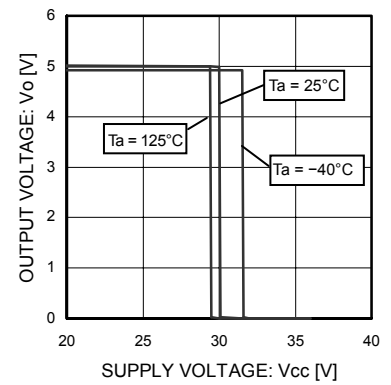


Fig. 6 Overvoltage Protection

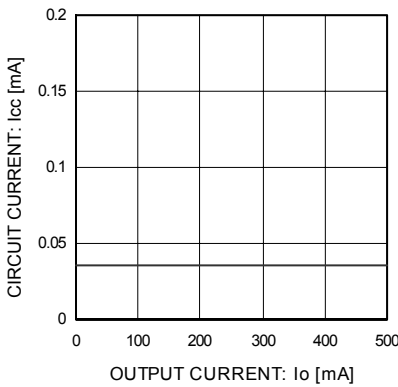


Fig. 7 Total Supply Current Classified by Load

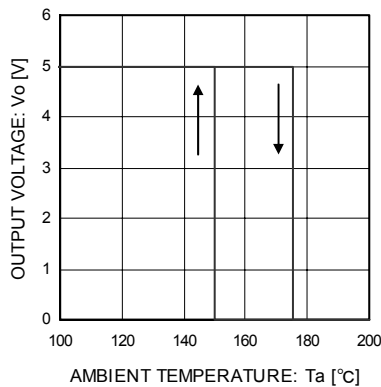


Fig. 8 Thermal Shutdown Circuit

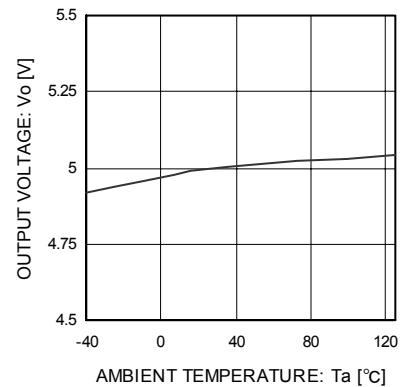


Fig. 9 Output Voltage vs Temperature

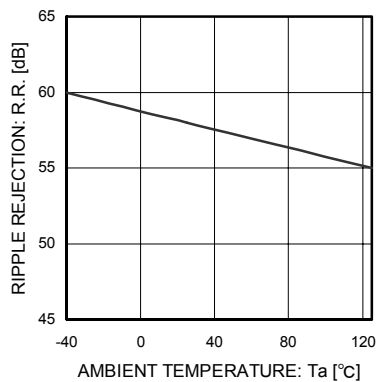


Fig. 10 Ripple Rejection vs Temperature

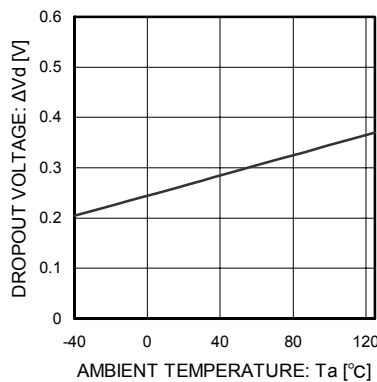


Fig. 11 Min. I/O Voltage Differential vs Temperature

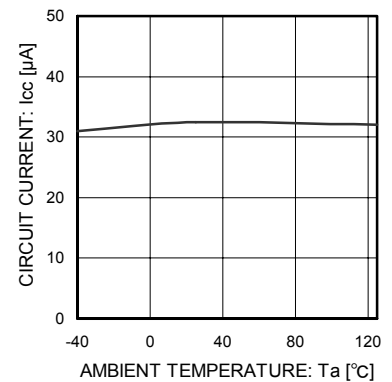


Fig. 12 Total Supply Current vs Temperature

●Block diagram

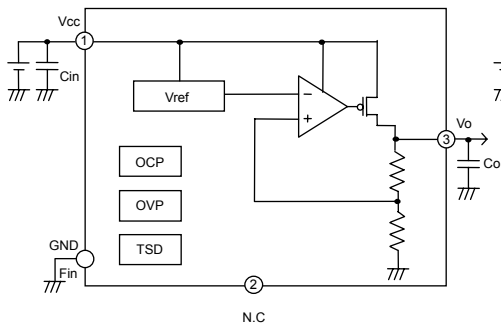


Fig.13 TO252-3

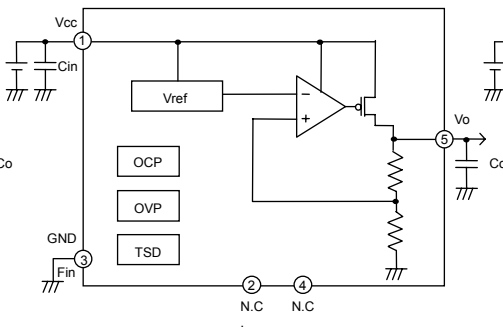


Fig.14 HRP5

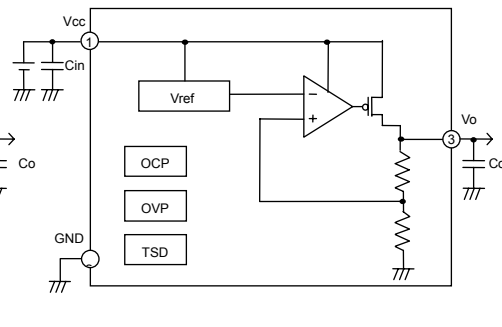


Fig.15 TO220FP-3

Cin : 0.33  $\mu$ F to 1000  $\mu$ F

Co : 0.1  $\mu$ F to 1000  $\mu$ F

●Pin assignments

- TO252-3

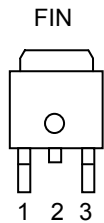


Fig.16

Pin No.	Pin No.	Function
1	Vcc	Power supply pin
2	N.C.	NC pin
3	Vo	Voltage output pin
Fin	GND	Ground pin

- HRP5

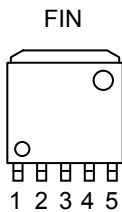


Fig.17

Pin No.	Pin No.	Function
1	Vcc	Power supply pin
2	N.C.	NC pin
3	GND	Ground pin
4	N.C.	NC pin
5	Vo	Voltage output pin
Fin	GND	Ground pin

- TO220FP-3

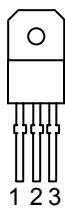


Fig.18

Pin No.	Pin No.	Function
1	Vcc	Power supply pin
2	GND	Ground pin
3	Vo	Voltage output pin

●Thermal design

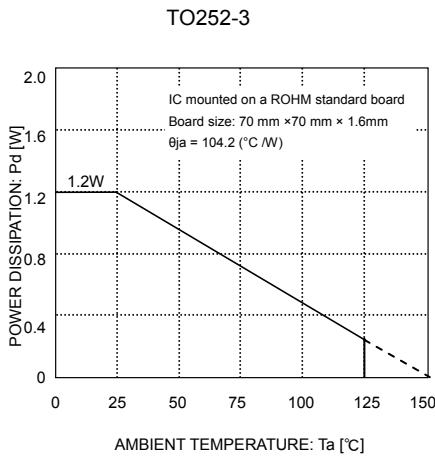


Fig.19

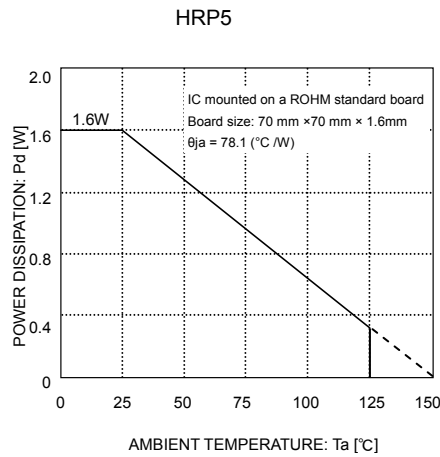


Fig.20

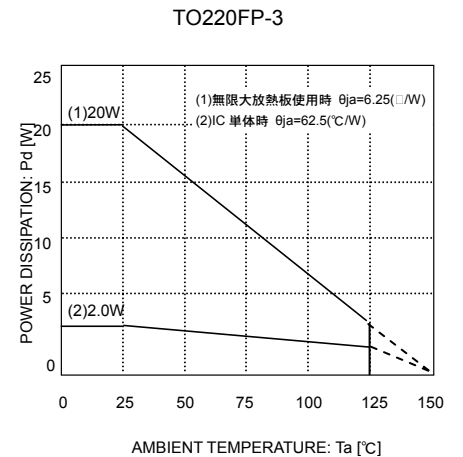


Fig.21

Refer to the dissipation reduction illustrated in Figs. 19 to 21 when using the IC in an environment where  $T_a \geq 25^\circ\text{C}$ . The characteristics of the IC are greatly influenced by the operating temperature. If the temperature exceeds the maximum junction temperature  $T_{jmax}$ , the elements of the IC may be damaged. It is necessary to give sufficient consideration to the heat of the IC in view of two points, i.e., the protection of the IC from instantaneous damage and the maintenance of the reliability of the IC in long-time operation.

In order to protect the IC from thermal destruction, the operating temperature of the IC must not exceed the maximum junction temperature  $T_{jmax}$ . Fig. 19 illustrates the power dissipation/power reduction for the TO252 package. Operate the IC within the power dissipation  $P_d$ . The following method is used to calculate the power consumption  $P_c$  (W).

$$P_c = (V_{cc} - V_o) \times I_o + V_{cc} \times I_{cc}$$

$$\text{Power dissipation } P_d \leq P_c$$

$V_{cc}$ : Input voltage  
 $V_o$ : Output voltage  
 $I_o$ : Load current  
 $I_{cc}$ : Total supply current

The load current  $I_o$  is obtained to operate the IC within the power dissipation.

$$I_o \leq \frac{P_d - V_{cc} \times I_{cc}}{V_{cc} - V_o} \quad (\text{Refer to } I_{cc} \text{ in Fig.12})$$

The maximum load current  $I_{omax}$  for the applied voltage  $V_{cc}$  can be calculated during the thermal design process.

Calculation example

Example)  $V_{cc} = 12 \text{ V}$  and  $V_o = 5.0 \text{ V}$  at  $T_a = 85^\circ\text{C}$ , BD3941FP

$$I_o \leq \frac{0.624 - 12 \times I_{cc}}{12 - 5}$$

$$I_o \leq 89 \text{ mA} \quad (I_{cc} = 30 \mu\text{A})$$

$\theta_{ja} = 104.2^\circ\text{C/W} \rightarrow -9.6 \text{ mAW}/^\circ\text{C}$   
 $25^\circ\text{C} = 1.2 \text{ W} \rightarrow 85^\circ\text{C} = 0.624 \text{ W}$

Make a thermal calculation in consideration of the above equations so that the whole operating temperature range will be within the power dissipation. The power consumption  $P_c$  of the IC, in the event of shorting (i.e., if the  $V_o$  and GND pins are shorted), will be obtained from the following equation:

$$P_c = V_{cc} \times (I_{cc} + I_{short}) \quad I_{short}: \text{Short current}$$

●External settings for pins and precautions

1)  $V_{cc}$  pin

Insert capacitors with a capacitance of  $0.33 \mu\text{F}$  to  $1,000 \mu\text{F}$  between the  $V_{cc}$  and GND pins. The capacitance varies with the application. Be sure to design the capacitance with a sufficient margin.

2) Capacitors for stopping oscillation at output pins

Capacitors for stopping oscillation must be placed between each output pin and the GND pin. Use a capacitor within a capacitance range between  $1 \mu\text{F}$  and  $1,000 \mu\text{F}$ . A ceramic capacitor with low ESR values, from  $0.001 \Omega$  to  $100$ , can be used. Unstable input voltage and load fluctuations can affect output voltages. Output capacitor capacitance values should be determined for actual application.

● **Operation Notes**

- 1) Absolute maximum ratings  
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
- 2) GND voltage  
The potential of GND pin must be minimum potential in all operating conditions.
- 3) Thermal design  
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
- 4) Inter-pin shorts and mounting errors  
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.
- 5) Actions in strong electromagnetic field  
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
- 6) Testing on application boards  
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

- 7) Regarding input pin of the IC  
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:  
When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.  
When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.  
Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

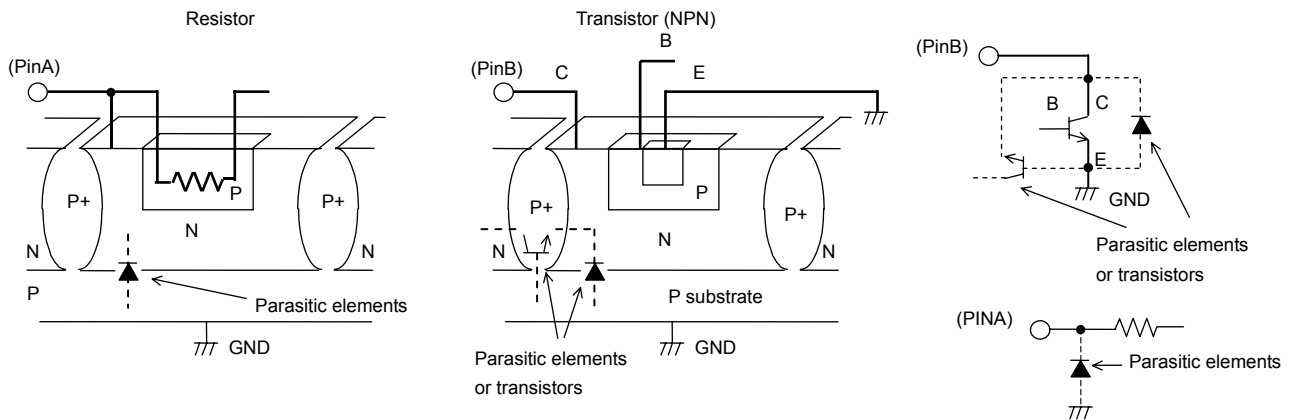


Fig.22 Example of a Simple Monolithic IC Architecture

- 8) Ground Wiring Pattern  
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

- 9) Applications or inspection processes with modes where the potentials of the Vcc pin and other pins may be reversed from their normal states may cause damage to the IC's internal circuitry or elements.  
 Use an output pin capacitance of 1,000  $\mu$ F or lower in case Vcc is shorted with the GND pin while the external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with Vcc or bypass diodes between Vcc and each pin.

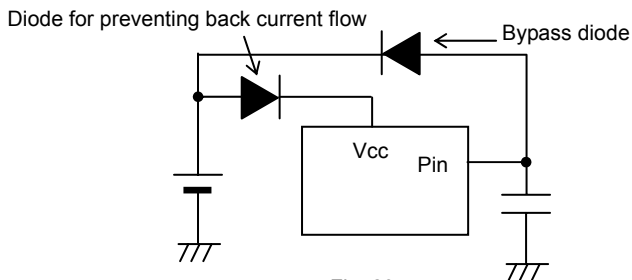
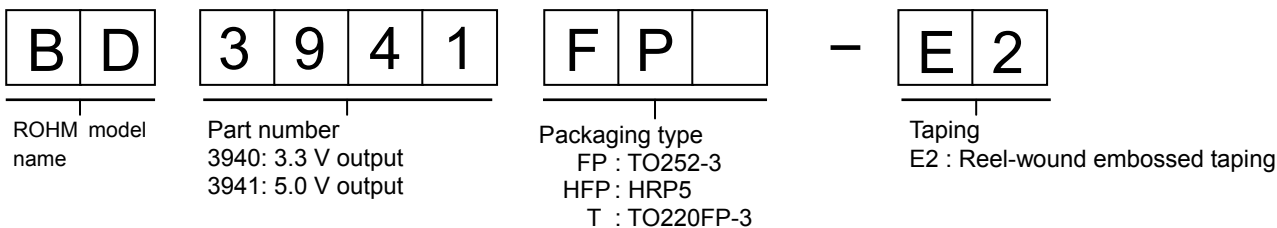


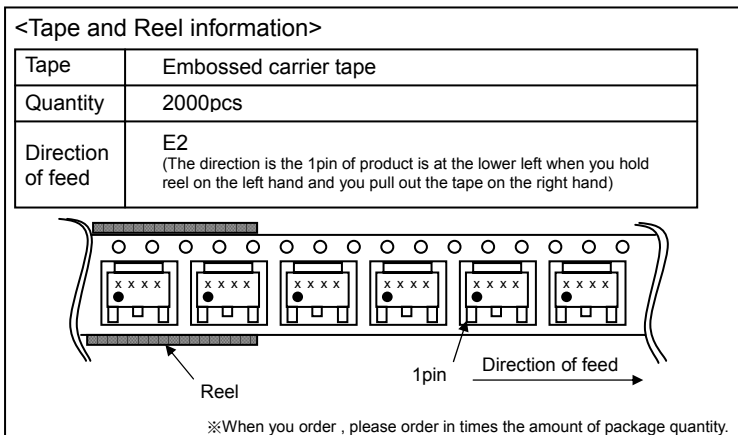
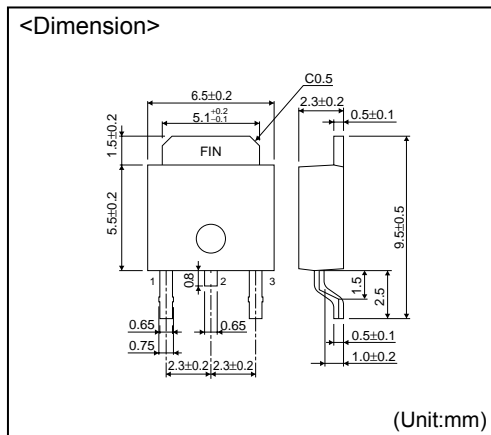
Fig. 23

- 10) Thermal shutdown circuit (TSD)  
 This IC incorporates a built-in thermal shutdown circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's temperature  $T_j$  will trigger the thermal shutdown circuit to turn off all output power elements. The circuit will automatically reset once the chip's temperature  $T_j$  drops. Operation of the thermal shutdown circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the thermal shutdown circuit. (See Fig. 8)
- 11) Overcurrent protection circuit (OCP)  
 The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. However, while this protection circuit is effective in preventing damage due to sudden and unexpected accidents, it is not compatible with continuous operation or use during transitional periods. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures. (See Fig. 3.)
- 12) Overvoltage protection circuit (OVP)  
 Overvoltage protection is designed to turn off all output when the voltage differential between the VCC and GND pins exceeds approximately 30 V (typ.). Use caution when determining the power supply voltage range to use. (See Fig. 6)

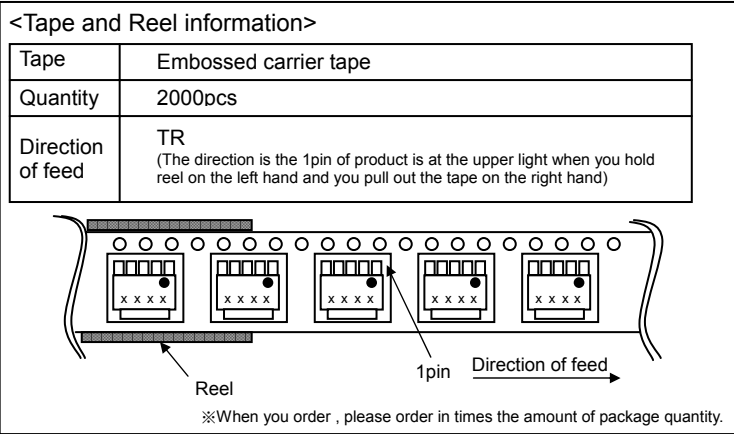
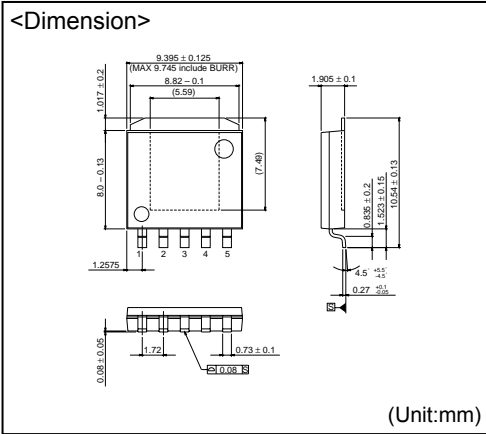
●Selecting a model name when ordering



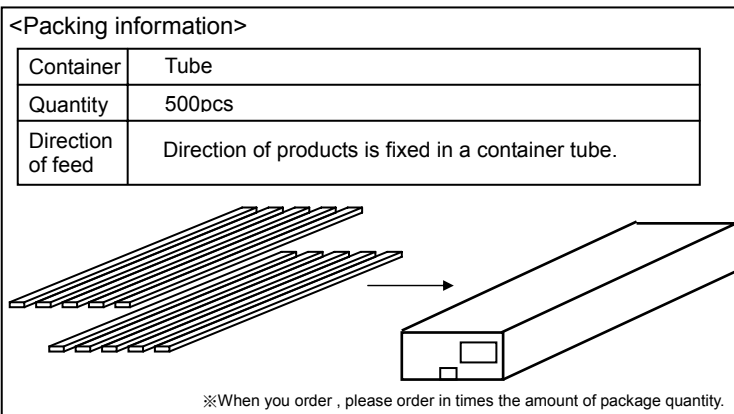
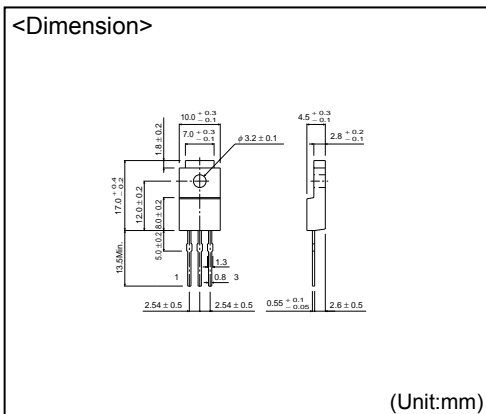
TO252-3



## HRP5



## TO220FP-3



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