



**THE DATASHEET OF
DMP4010SK3-13**



Product Summary

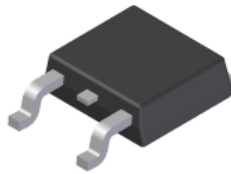
BV_{DSS}	$R_{DS(ON)}$ Max	I_D $T_C = +25^\circ C$
-40V	9.9m Ω @ $V_{GS} = -10V$	-50A
	14m Ω @ $V_{GS} = -4.5V$	-45A

Description

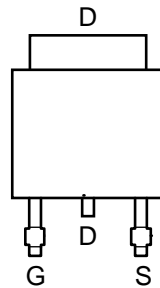
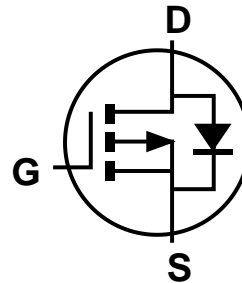
This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- DC-DC Converters
- Power Management Functions
- Backlighting

TO252


Top View


 Top View
Pin-Out


Equivalent Circuit

Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low On-Resistance
- Fast Switching Speed
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

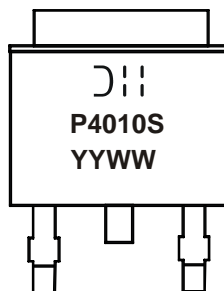
- Case: TO252
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin Finish Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 $\text{\textcircled{E}}$
- Weight: 0.33 grams (Approximate)

Ordering Information (Note 4)

Part Number	Case	Packaging
DMP4010SK3-13	TO252	2,500/Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



D = Manufacturer's Marking
 P4010S = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Year (ex: 15 = 2015)
 WW = Week (01 to 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-40	V
Gate-Source Voltage			V_{GSS}	± 25	V
Continuous Drain Current (Note 6) $V_{GS} = -10\text{V}$	Steady State	$T_C = +25^\circ\text{C}$ $T_C = +70^\circ\text{C}$	I_D	-50 -40	A
	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	-15 -12	A
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)			I_{DM}	-100	A
Maximum Body Diode Forward Current (Note 6)			I_S	-5.5	A
Avalanche Current, L = 1mH (Note 7)			I_{AS}	-22	A
Avalanche Energy, L = 1mH (Note 7)			E_{AS}	260	mJ

Thermal Characteristics

Characteristic			Symbol	Value	Unit
Total Power Dissipation (Note 5)			P_D	1.7	W
Thermal Resistance, Junction to Ambient (Note 5)		Steady State	$R_{\theta JA}$	73	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)			P_D	3.3	W
Thermal Resistance, Junction to Ambient (Note 6)		Steady State	$R_{\theta JA}$	38	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case			$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Operating and Storage Temperature Range			T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -40\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.5	-2	-2.5	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	7.5	9.9	m Ω	$V_{GS} = -10\text{V}, I_D = -9.8\text{A}$
		—	10.5	14		$V_{GS} = -4.5\text{V}, I_D = -9.8\text{A}$
Diode Forward Voltage	V_{SD}	—	-0.7	-1	V	$V_{GS} = 0\text{V}, I_S = -1\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{ISS}	—	4,234	—	pF	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{OSS}	—	1,036	—		
Reverse Transfer Capacitance	C_{RSS}	—	526	—		
Gate Resistance	R_g	—	7.8	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = -4.5\text{V}$)	Q_g	—	42.7	—	nC	$V_{DS} = -20\text{V},$ $I_D = -9.8\text{A}$
Total Gate Charge ($V_{GS} = -10\text{V}$)	Q_g	—	91	—		
Gate-Source Charge	Q_{GS}	—	14.2	—		
Gate-Drain Charge	Q_{GD}	—	13.5	—		
Turn-On Delay Time	$t_{D(ON)}$	—	13.2	—	ns	$V_{GS} = -10\text{V}, V_{DD} = -20\text{V},$ $R_G = 6\Omega, I_D = -1\text{A}$
Turn-On Rise Time	t_R	—	10	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	303	—		
Turn-Off Fall Time	t_F	—	138	—		
Reverse Recovery Time	t_{RR}	—	26	—	ns	$I_F = -9.8\text{A}, di/dt = -100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{RR}	—	20	—	nC	$I_F = -9.8\text{A}, di/dt = -100\text{A}/\mu\text{s}$

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

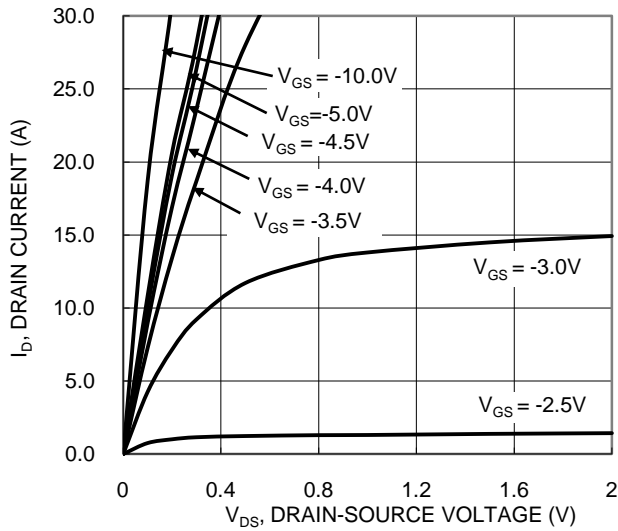


Figure 1. Typical Output Characteristic

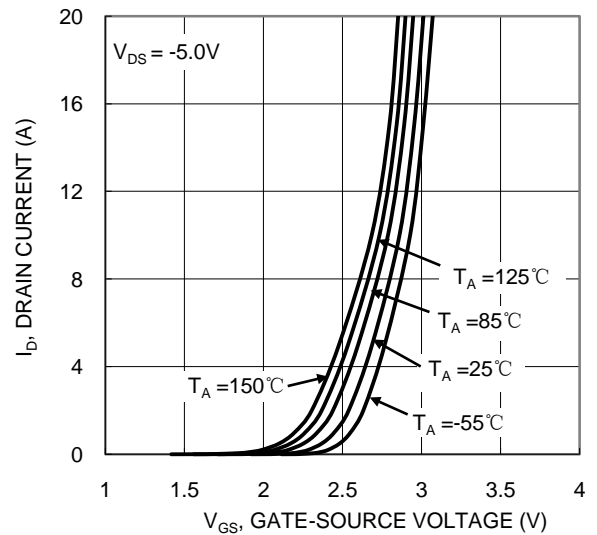


Figure 2. Typical Transfer Characteristic

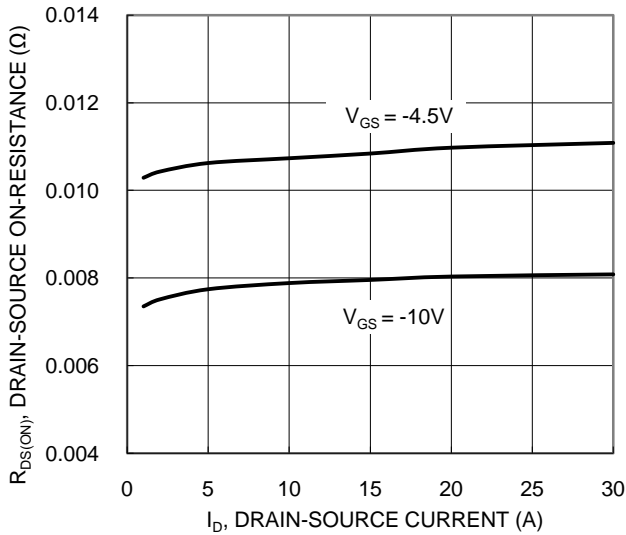


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

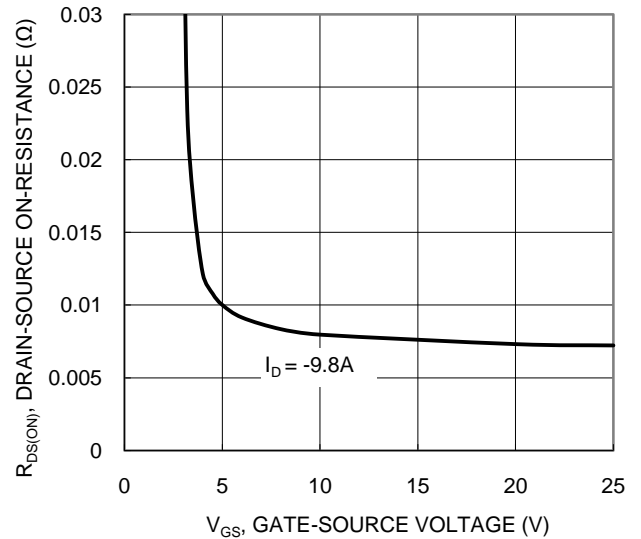


Figure 4. Typical Transfer Characteristic

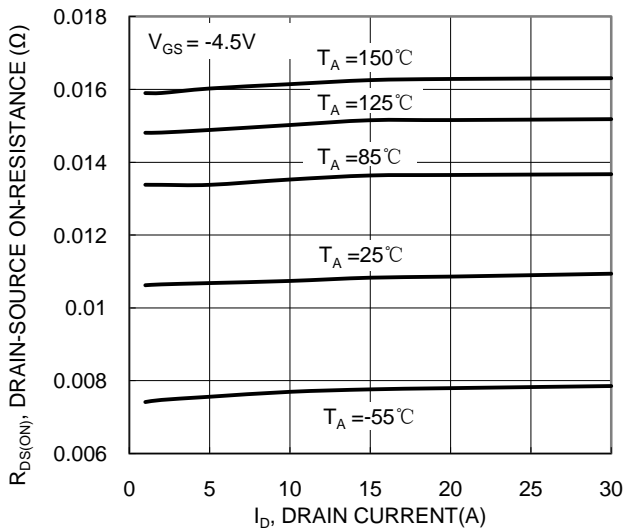


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

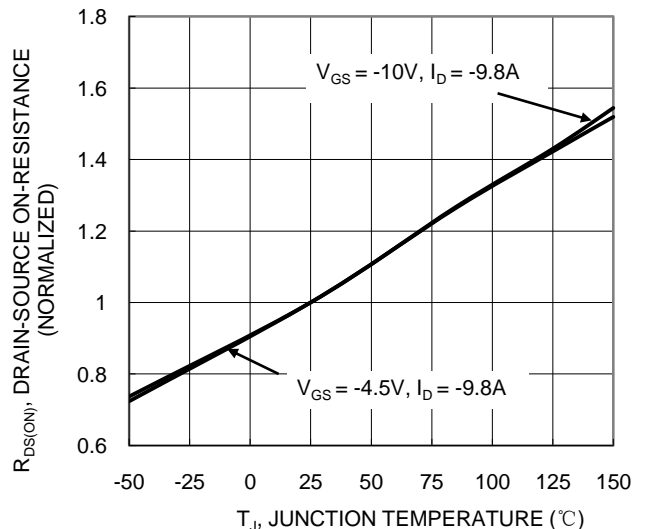


Figure 6. On-Resistance Variation with Temperature

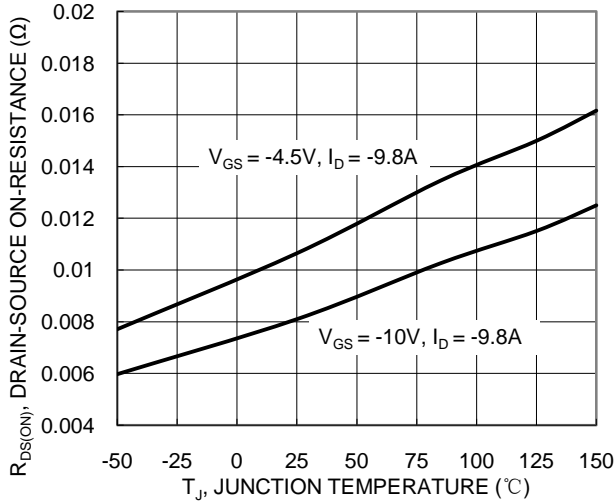


Figure 7. On-Resistance Variation with Temperature

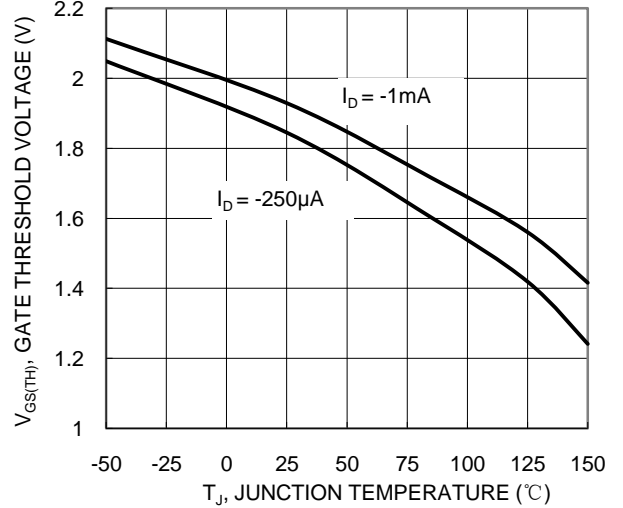


Figure 8. Gate Threshold Variation vs. Junction Temperature

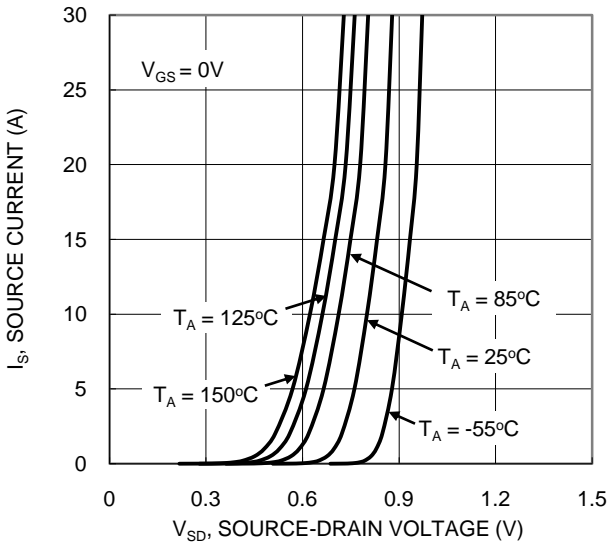


Figure 9. Diode Forward Voltage vs. Current

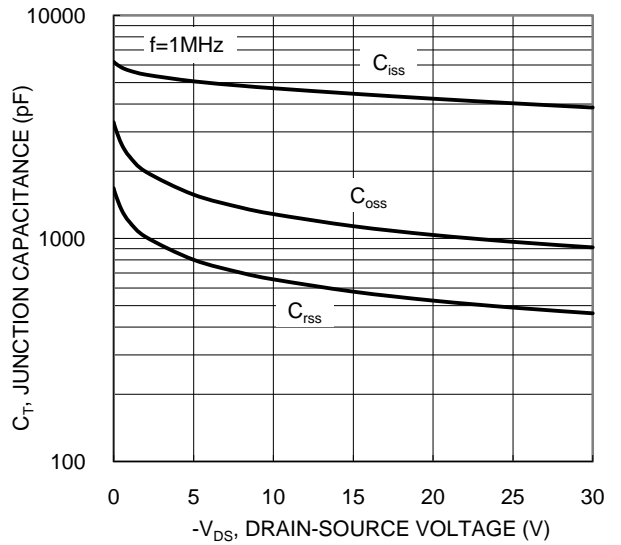


Figure 10. Typical Junction Capacitance

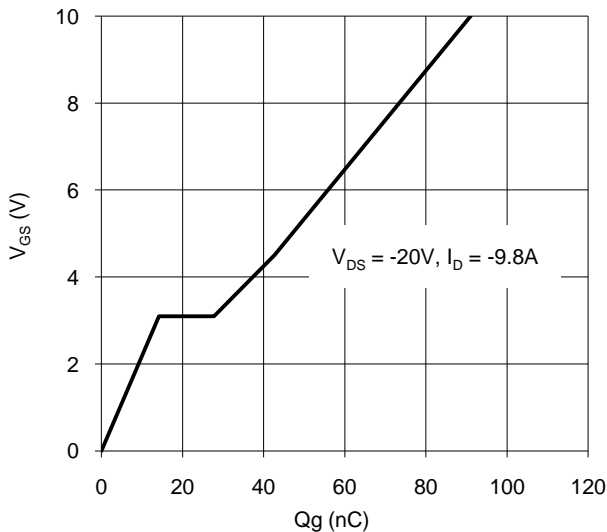


Figure 11. Gate Charge

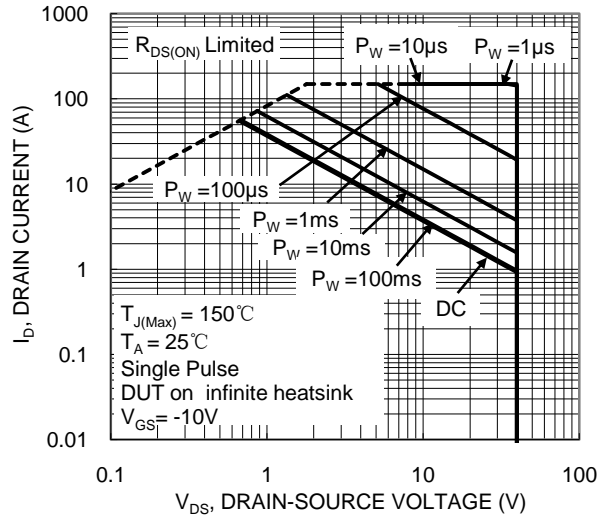


Figure 12. SOA, Safe Operation Area

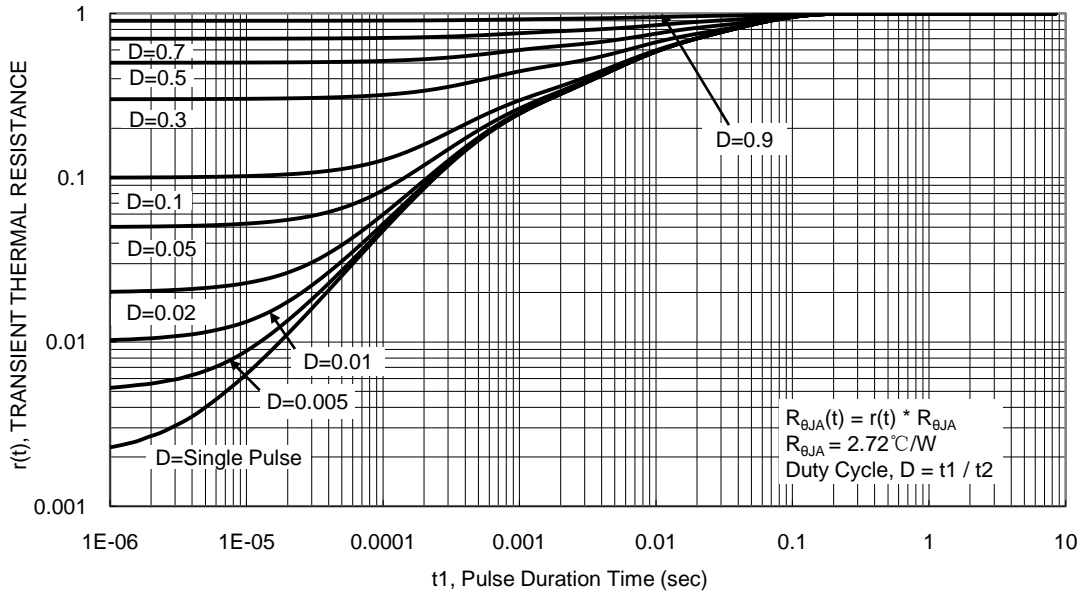


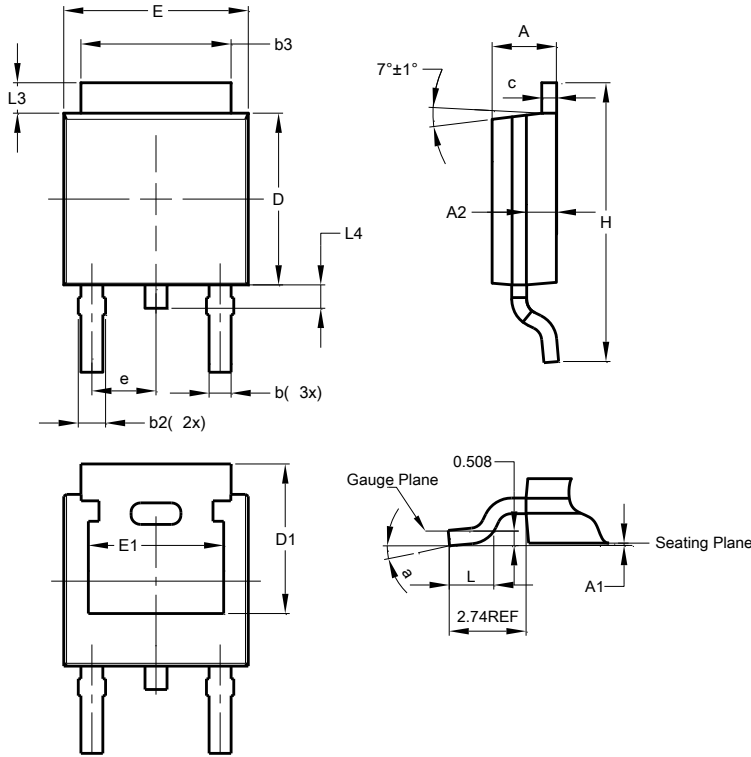
Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.

NEW PRODUCT

TO252 (DPAK)

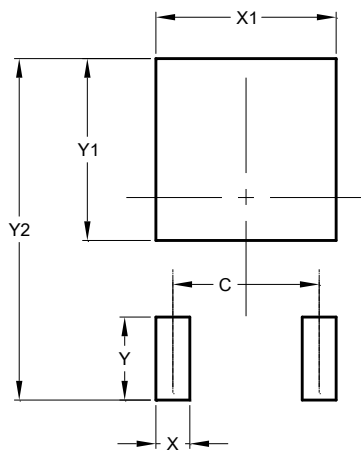


TO252 (DPAK)			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	—	—
e	—	—	2.286
E	6.45	6.70	6.58
E1	4.32	—	—
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	—
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

TO252 (DPAK)



Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700

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