



**THE DATASHEET OF
EFM32PG1B200F256GM48-C0**



EFM32 Pearl Gecko Family

EFM32PG1 Data Sheet



The EFM32 Pearl Gecko MCUs are the world's most energy-friendly microcontrollers.

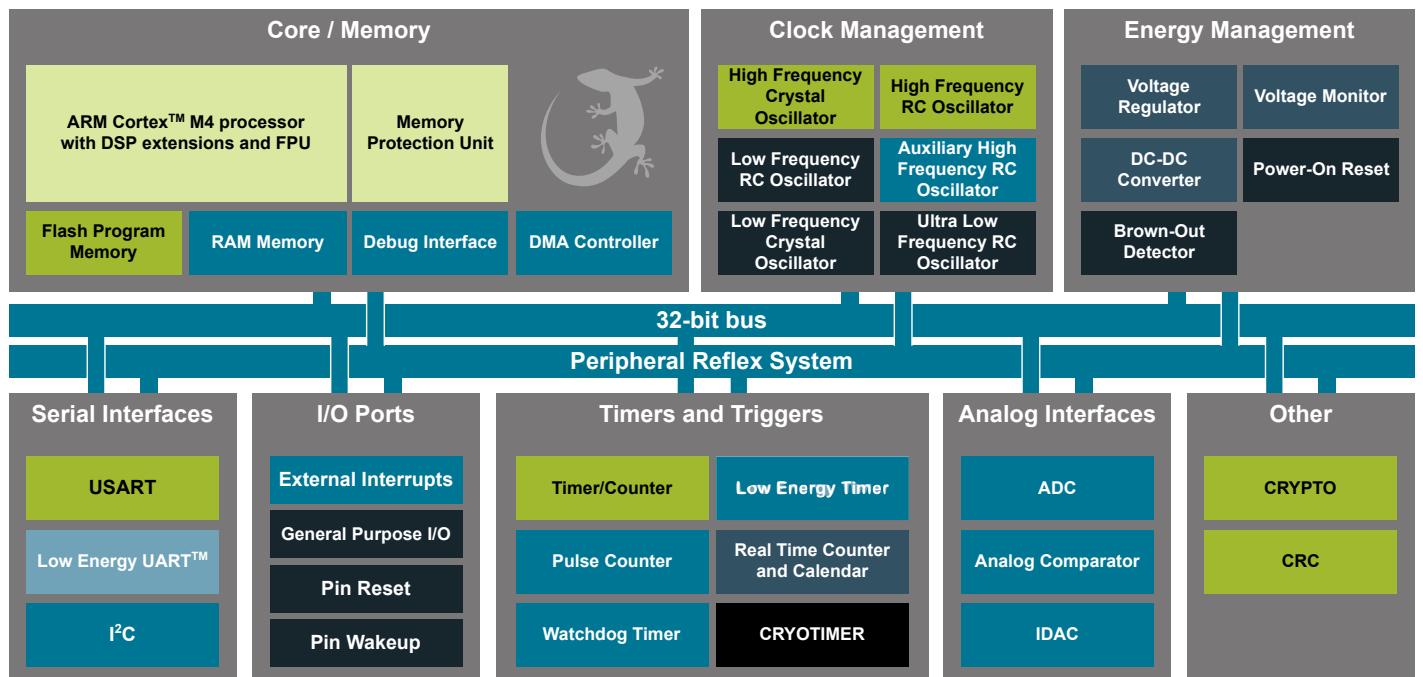
EFM32PG1 features a powerful 32-bit ARM® Cortex®-M4 and a wide selection of peripherals, including a unique cryptographic hardware engine supporting AES, ECC, and SHA. These features, combined with ultra-low current active mode and short wake-up time from energy-saving modes, make EFM32PG1 microcontrollers well suited for any battery-powered application, as well as other systems requiring high performance and low-energy consumption.

Example applications:

- IoT devices and sensors
- Health and fitness
- Smart accessories
- Home automation and security
- Industrial and factory automation

ENERGY FRIENDLY FEATURES

- ARM Cortex-M4 at 40 MHz
- Ultra low energy operation:
 - 2.1 μ A EM3 Stop current (CRYOTIMER running with state/RAM retention)
 - 2.5 μ A EM2 DeepSleep current (RTCC running with state and RAM retention)
 - 63 μ A/MHz in Energy Mode 0 (EM0)
- Hardware cryptographic engine supports AES, ECC, and SHA
- Integrated dc-dc converter
- CRYOTIMER operates down to EM4
- 5 V tolerant I/O



Lowest power mode with peripheral operational:



1. Feature List

The EFM32PG1 highlighted features are listed below.

- **ARM Cortex-M4 CPU platform**
 - High performance 32-bit processor @ up to 40 MHz
 - DSP instruction support and Floating Point Unit
 - Memory Protection Unit
 - Wake-up Interrupt Controller
- **Flexible Energy Management System**
 - 63 μ A/MHz in Energy Mode 0 (EM0)
 - 2.5 μ A EM2 DeepSleep current (RTCC running with state and RAM retention)
 - 0.58 μ A EM4H Hibernate Mode (128 byte RAM retention)
- **Up to 256 kB flash program memory**
- **32 kB RAM data memory**
- **Up to 32 General Purpose I/O Pins**
 - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - Asynchronous external interrupts
 - Output state retention and wake-up from Shutoff Mode
- **Hardware Cryptography**
 - AES 128/256-bit keys
 - ECC B/K163, B/K233, P192, P224, P256
 - SHA-1 and SHA-2 (SHA-224 and SHA-256)
- **Timers/Counters**
 - 2 \times 16-bit Timer/Counter
 - 3 + 4 Compare/Capture/PWM channels
 - 1 \times 32-bit Real Time Counter and Calendar
 - 1 \times 32-bit Ultra Low Energy CRYOTIMER for periodic wake-up from any Energy Mode
 - 16-bit Low Energy Timer for waveform generation
 - 16-bit Pulse Counter with asynchronous operation
 - Watchdog Timer with dedicated RC oscillator
- **8 Channel DMA Controller**
- **12 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Communication Interfaces**
 - 2 \times Universal Synchronous/Asynchronous Receiver/ Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
 - Triple buffered full/half-duplex operation with flow control
 - Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - I²C Interface with SMBus support
 - Address recognition in EM3 Stop Mode
- **Ultra Low-Power Precision Analog Peripherals**
 - 12-bit 1 Msamples/s Analog to Digital Converter
 - 2 \times Analog Comparator
 - Digital to Analog Current Converter
 - Up to 32 pins connected to analog channels (APORT) shared between Analog Comparators, ADC, and IDAC
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
 - 2-pin Serial Wire Debug interface
 - 1-pin Serial Wire Viewer
 - JTAG (programming only)
- **Wide Operating Range**
 - 1.85 V to 3.8 V single power supply
 - Integrated dc-dc, down to 1.8 V output with up to 200 mA load current for system
 - Standard (-40 °C to 85 °C T_{AMB}) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
 - 7 mm \times 7 mm QFN48
 - 5 mm \times 5 mm QFN32
- **Pre-Programmed UART Bootloader**
- **Full Software Support**
 - CMSIS register definitions
 - Low-power Hardware Abstraction Layer (HAL)
 - Portable software components
 - Third-party middleware
 - Free and available example code

2. Ordering Information

| Ordering Code | Flash (kB) | RAM (kB) | DC-DC Converter | GPIO | Package | Temp Range |
|-------------------------|------------|----------|-----------------|------|---------|-------------|
| EFM32PG1B200F256GM48-C0 | 256 | 32 | Yes | 32 | QFN48 | -40 to +85 |
| EFM32PG1B200F256IM48-C0 | 256 | 32 | Yes | 32 | QFN48 | -40 to +125 |
| EFM32PG1B200F128GM48-C0 | 128 | 32 | Yes | 32 | QFN48 | -40 to +85 |
| EFM32PG1B200F256GM32-C0 | 256 | 32 | Yes | 20 | QFN32 | -40 to +85 |
| EFM32PG1B200F256IM32-C0 | 256 | 32 | Yes | 20 | QFN32 | -40 to +125 |
| EFM32PG1B200F128GM32-C0 | 128 | 32 | Yes | 20 | QFN32 | -40 to +85 |
| EFM32PG1B100F256GM32-C0 | 256 | 32 | No | 24 | QFN32 | -40 to +85 |
| EFM32PG1B100F256IM32-C0 | 256 | 32 | No | 24 | QFN32 | -40 to +125 |
| EFM32PG1B100F128GM32-C0 | 128 | 32 | No | 24 | QFN32 | -40 to +85 |

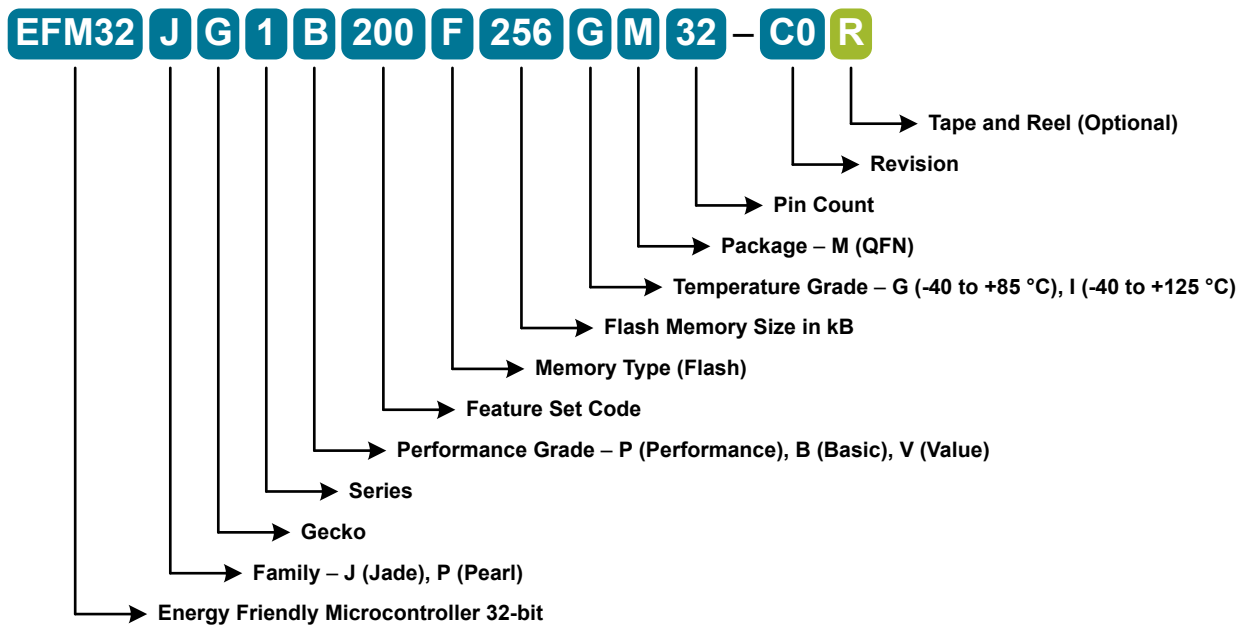


Figure 2.1. OPN Decoder

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3. System Overview

3.1 Introduction

The EFM32PG1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the EFM32PG1 Reference Manual.

A block diagram of the EFM32PG1 family is shown in [Figure 3.1 Detailed EFM32PG1 Block Diagram on page 7](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

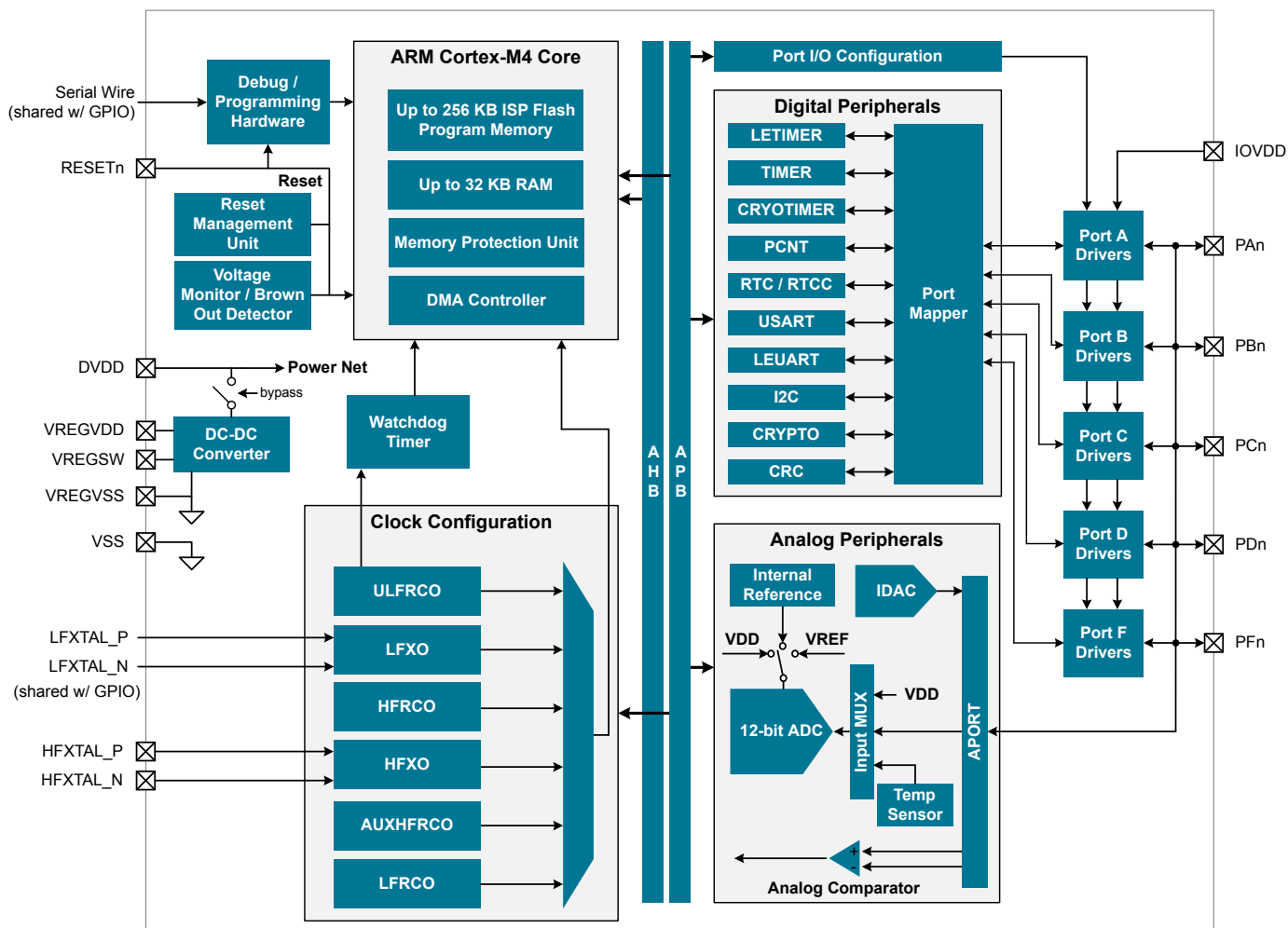


Figure 3.1. Detailed EFM32PG1 Block Diagram

3.2 Power

The EFM32PG1 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated dc-dc buck regulator can be utilized to further reduce the current consumption. The dc-dc regulator requires one external inductor and one external capacitor.

AVDD and VREGVDD need to be 1.85 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the dc-dc to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.3 General Purpose Input/Output (GPIO)

EFM32PG1 has up to 32 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32PG1. Individual enabling and disabling of clocks to all peripherals is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32PG1 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.5.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.5.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The peripheral may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O interface. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.6.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.3 Inter-Integrated Circuit Interface (I²C)

The I²C interface enables communication between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C peripheral allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.6.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripherals without software involvement. Peripherals producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals, which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7 Security Features

3.7.1 General Purpose Cyclic Redundancy Check (GPCRC)

The GPCRC block implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFM32PG1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO peripheral allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog peripherals on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Digital to Analog Current Converter (IDAC)

The IDAC can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μA and 64 μA with several ranges consisting of various step sizes.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32PG1. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- DSP instruction support and Floating Point Unit
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 256 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all peripherals
- 2-pin Serial-Wire debug interface

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.10.4 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the [Documentation] area.

3.11 Memory Map

The EFM32PG1 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

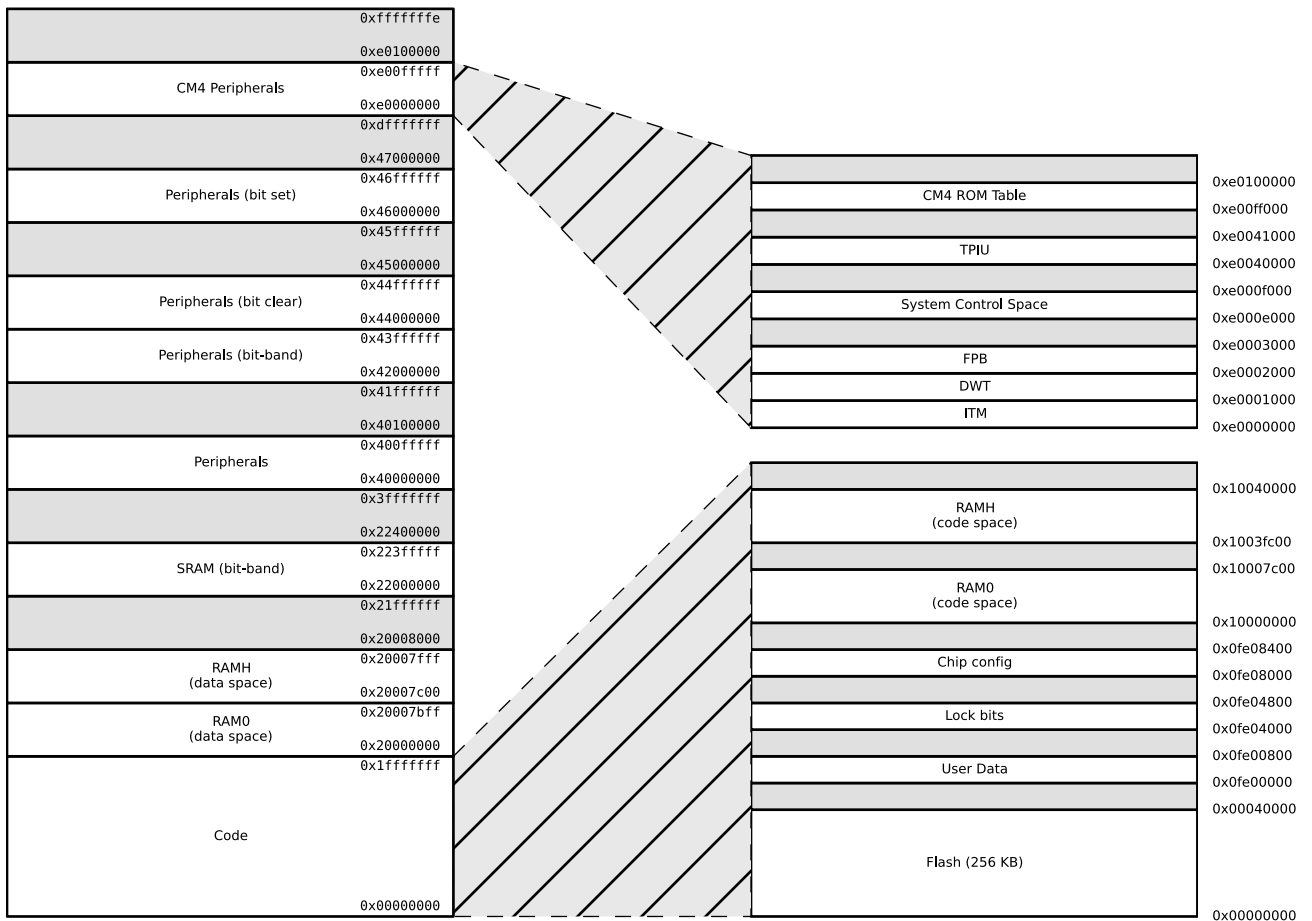


Figure 3.2. EFM32PG1 Memory Map — Core Peripherals and Code Space

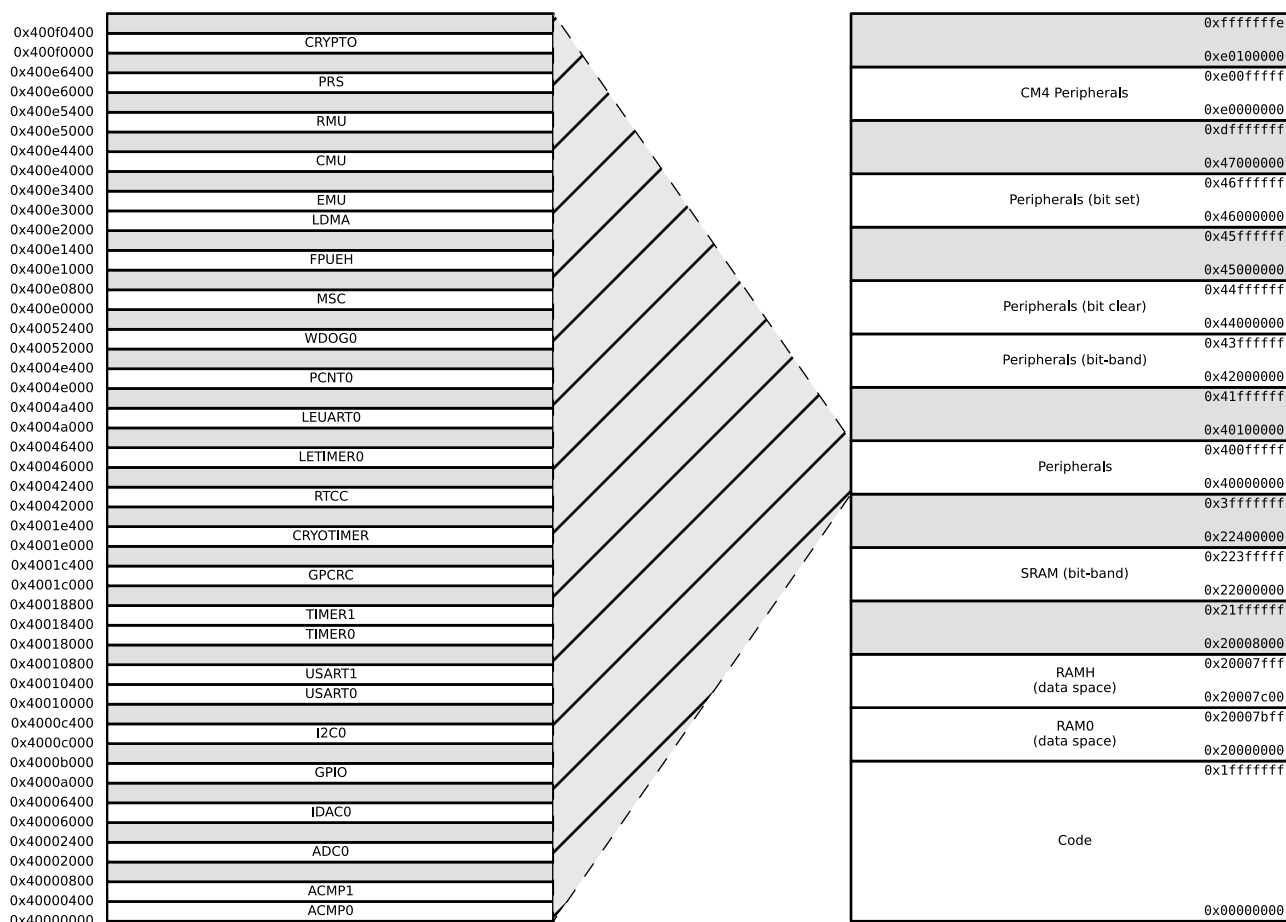


Figure 3.3. EFM32PG1 Memory Map — Peripherals

3.12 Configuration Summary

The features of the EFM32PG1 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.1. Configuration Summary

| Module | Configuration | Pin Connections |
|--------|-------------------------------|---------------------------------|
| USART0 | IrDA SmartCard | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | I ² S SmartCard | US1_TX, US1_RX, US1_CLK, US1_CS |
| TIMER0 | with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | | TIM1_CC[3:0] |

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{AMB}=25\text{ }^{\circ}\text{C}$ and $V_{DD}=3.3\text{ V}$, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to [Table 4.2 General Operating Conditions on page 15](#) for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.1. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------|----------------|------|-----|--------------------------|--------------------|
| Storage temperature range | T_{STG} | | -50 | — | 150 | $^{\circ}\text{C}$ |
| External main supply voltage | V_{DDMAX} | | 0 | — | 3.8 | V |
| External main supply voltage ramp rate | $V_{DDRAMPMAX}$ | | — | — | 1 | V / μs |
| Voltage on any 5V tolerant GPIO pin ¹ | V_{DIGPIN} | | -0.3 | — | Min of 5.25 and IOVDD +2 | V |
| Voltage on non-5V tolerant GPIO pins | | | -0.3 | — | IOVDD+0.3 | V |
| Voltage on HFXO pins | $V_{HFXOPIN}$ | | -0.3 | — | 1.4 | V |
| Total current into VDD power lines (source) | I_{VDDMAX} | | — | — | 200 | mA |
| Total current into VSS ground lines (sink) | I_{VSSMAX} | | — | — | 200 | mA |
| Current per I/O pin (sink) | I_{IOMAX} | | — | — | 50 | mA |
| Current per I/O pin (source) | | | — | — | 50 | mA |
| Current for all I/O pins (sink) | $I_{IOALLMAX}$ | | — | — | 200 | mA |
| Current for all I/O pins (source) | | | — | — | 200 | mA |
| Voltage difference between AVDD and VREGVDD | ΔV_{DD} | | — | — | 0.3 | V |
| Junction Temperature for -G grade devices | T_J | | -40 | — | 105 | $^{\circ}\text{C}$ |
| Junction Temperature for -I grade devices | | | -40 | — | 125 | $^{\circ}\text{C}$ |

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be the highest voltage in the system
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|---|------|-----|----------------------|------|
| Operating temperature range | T _{OP} | -G temperature grade, Ambient Temperature | -40 | 25 | 85 | °C |
| | | -I temperature grade, Junction Temperature | -40 | 25 | 125 | °C |
| AVDD Supply voltage ¹ | V _{AVDD} | | 1.85 | 3.3 | 3.8 | V |
| VREGVDD Operating supply voltage ^{1 2} | V _{VREGVDD} | DCDC in regulation | 2.4 | 3.3 | 3.8 | V |
| | | DCDC in bypass, 50mA load | 1.85 | 3.3 | 3.8 | V |
| | | DCDC not in use. DVDD externally shorted to VREGVDD | 1.85 | 3.3 | 3.8 | V |
| VREGVDD Current | I _{VREGVDD} | DCDC in bypass, T _{amb} ≤ 85 °C | — | — | 200 | mA |
| | | DCDC in bypass, T _{amb} > 85 °C | — | — | 100 | mA |
| DVDD Operating supply voltage | V _{DVDD} | | 1.62 | — | V _{VREGVDD} | V |
| IOVDD Operating supply voltage | V _{IOVDD} | | 1.62 | — | V _{VREGVDD} | V |
| Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD) | dV _{DD} | | — | — | 0.1 | V |
| HFCLK frequency | f _{CORE} | 0 wait-states (MODE = WS0) ³ | — | — | 26 | MHz |
| | | 1 wait-states (MODE = WS1) ³ | — | — | 40 | MHz |

Note:

1. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
2. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as V_{DVDD_min} + I_{LOAD} * R_{BYP_max}
3. In MSC_READCTRL register

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------|---------------------|--|-----|------|-----|------|
| Thermal Resistance | THETA _{JA} | QFN32 Package, 2-Layer PCB, Air velocity = 0 m/s | — | 79 | — | °C/W |
| | | QFN32 Package, 2-Layer PCB, Air velocity = 1 m/s | — | 62.2 | — | °C/W |
| | | QFN32 Package, 2-Layer PCB, Air velocity = 2 m/s | — | 54.1 | — | °C/W |
| | | QFN32 Package, 4-Layer PCB, Air velocity = 0 m/s | — | 32 | — | °C/W |
| | | QFN32 Package, 4-Layer PCB, Air velocity = 1 m/s | — | 28.1 | — | °C/W |
| | | QFN32 Package, 4-Layer PCB, Air velocity = 2 m/s | — | 26.9 | — | °C/W |
| | | QFN48 Package, 2-Layer PCB, Air velocity = 0 m/s | — | 64.5 | — | °C/W |
| | | QFN48 Package, 2-Layer PCB, Air velocity = 1 m/s | — | 51.6 | — | °C/W |
| | | QFN48 Package, 2-Layer PCB, Air velocity = 2 m/s | — | 47.7 | — | °C/W |
| | | QFN48 Package, 4-Layer PCB, Air velocity = 0 m/s | — | 26.2 | — | °C/W |
| | | QFN48 Package, 4-Layer PCB, Air velocity = 1 m/s | — | 23.1 | — | °C/W |
| | | QFN48 Package, 4-Layer PCB, Air velocity = 2 m/s | — | 22.1 | — | °C/W |

4.1.4 DC-DC Converter

Test conditions: $L_{DCDC}=4.7\ \mu\text{H}$ (Murata LQH3NPN4R7MM0L), $C_{DCDC}=1.0\ \mu\text{F}$ (Murata GRM188R71A105KA61D), $V_{DCDC_I}=3.3\ \text{V}$, $V_{DCDC_O}=1.8\ \text{V}$, $I_{DCDC_LOAD}=50\ \text{mA}$, Heavy Drive configuration, $F_{DCDC_LN}=7\ \text{MHz}$, unless otherwise indicated.

Table 4.4. DC-DC Converter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------|---|------|-----|--------------------|------|
| Input voltage range | V_{DCDC_I} | Bypass mode, $I_{DCDC_LOAD} = 50\ \text{mA}$ | 1.85 | — | $V_{VREGVDD_MAX}$ | V |
| | | Low noise (LN) mode, 1.8 V output, $I_{DCDC_LOAD} = 100\ \text{mA}$, or Low power (LP) mode, 1.8 V output, $I_{DCDC_LOAD} = 10\ \text{mA}$ | 2.4 | — | $V_{VREGVDD_MAX}$ | V |
| | | Low noise (LN) mode, 1.8 V output, $I_{DCDC_LOAD} = 200\ \text{mA}$ | 2.6 | — | $V_{VREGVDD_MAX}$ | V |
| Output voltage programmable range ¹ | V_{DCDC_O} | | 1.8 | — | $V_{VREGVDD}$ | V |
| Regulation DC Accuracy | ACC_{DC} | Low noise (LN) mode, 1.8 V target output | 1.7 | — | 1.9 | V |
| Regulation Window ² | WIN_{REG} | Low power (LP) mode, $LPCMPBIAS^3 = 0$, 1.8 V target output, $I_{DCDC_LOAD} \leq 75\ \mu\text{A}$ | 1.63 | — | 2.2 | V |
| | | Low power (LP) mode, $LPCMPBIAS^3 = 3$, 1.8 V target output, $I_{DCDC_LOAD} \leq 10\ \text{mA}$ | 1.63 | — | 2.1 | V |
| Steady-state output ripple | V_R | | — | 3 | — | mVpp |
| Output voltage under/overshoot | V_{OV} | CCM Mode ($LNFORCECCM^3 = 1$), Load changes between 0 mA and 100 mA | — | — | 150 | mV |
| | | DCM Mode ($LNFORCECCM^3 = 0$), Load changes between 0 mA and 10 mA | — | — | 150 | mV |
| | | Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode | — | 200 | — | mV |
| | | Undershoot during BYP/LP to LN CCM ($LNFORCECCM^3 = 1$) mode transitions compared to DC level in LN mode | — | 50 | — | mV |
| | | Undershoot during BYP/LP to LN DCM ($LNFORCECCM^3 = 0$) mode transitions compared to DC level in LN mode | — | 125 | — | mV |
| DC line regulation | V_{REG} | Input changes between $V_{VREGVDD_MAX}$ and 2.4 V | — | 0.1 | — | % |
| DC load regulation | I_{REG} | Load changes between 0 mA and 100 mA in CCM mode | — | 0.1 | — | % |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-----------------------|--|-----|-----|-----|------|
| Max load current | I _{LOAD_MAX} | Low noise (LN) mode, Heavy Drive ⁴ , T _{amb} ≤ 85 °C | — | — | 200 | mA |
| | | Low noise (LN) mode, Heavy Drive ⁴ , T _{amb} > 85 °C | — | — | 100 | mA |
| | | Low noise (LN) mode, Medium Drive ⁴ | — | — | 100 | mA |
| | | Low noise (LN) mode, Light Drive ⁴ | — | — | 50 | mA |
| | | Low power (LP) mode, LPCMPBIAS ³ = 0 | — | — | 75 | μA |
| | | Low power (LP) mode, LPCMPBIAS ³ = 3 | — | — | 10 | mA |
| DCDC nominal output capacitor | C _{DCDC} | 25% tolerance | 1 | 1 | 1 | μF |
| DCDC nominal output inductor | L _{DCDC} | 20% tolerance | 4.7 | 4.7 | 4.7 | μH |
| Resistance in Bypass mode | R _{BYP} | | — | 1.2 | 2.5 | Ω |

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, V_{VREGVDD}
2. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits
3. In EMU_DCDCMISCCTRL register
4. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.

4.1.5 Current Consumption

4.1.5.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T_{OP} = 25 °C. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C. See [Figure 5.1 EFM32PG1 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 52](#).

Table 4.5. Current Consumption 3.3V without DC/DC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|--|-----|------|------|--------|
| Current consumption in EM0 Active mode with all peripherals disabled | I _{ACTIVE} | 38.4 MHz crystal, CPU running while loop from flash ¹ | — | 127 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 88 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 100 | 105 | μA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 112 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 102 | 106 | μA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 222 | 350 | μA/MHz |
| Current consumption in EM1 Sleep mode with all peripherals disabled | I _{EM1} | 38.4 MHz crystal ¹ | — | 61 | — | μA/MHz |
| | | 38 MHz HFRCO | — | 35 | 38 | μA/MHz |
| | | 26 MHz HFRCO | — | 37 | 41 | μA/MHz |
| | | 1 MHz HFRCO | — | 157 | 275 | μA/MHz |
| Current consumption in EM2 Deep Sleep mode. | I _{EM2} | Full RAM retention and RTCC running from LFXO | — | 3.3 | — | μA |
| | | 4 kB RAM retention and RTCC running from LFRCO | — | 3 | 6.3 | μA |
| Current consumption in EM3 Stop mode | I _{EM3} | Full RAM retention and CRYO-TIMER running from ULFRCO | — | 2.8 | 6 | μA |
| Current consumption in EM4H Hibernate mode | I _{EM4} | 128 byte RAM retention, RTCC running from LFXO | — | 1.1 | — | μA |
| | | 128 byte RAM retention, CRYO-TIMER running from ULFRCO | — | 0.65 | — | μA |
| | | 128 byte RAM retention, no RTCC | — | 0.65 | 1.3 | μA |
| Current consumption in EM4S Shutoff mode | I _{EM4S} | no RAM retention, no RTCC | — | 0.04 | 0.11 | μA |

Note:

1. CMU_HFXOCTRL_LOWPOWER=1

4.1.5.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C. See [Figure 5.2 EFM32PG1 Typical Application Circuit Using the DC-DC Converter on page 52](#).

Table 4.6. Current Consumption 3.3V with DC-DC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|--|-----|------|-----|--------|
| Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise DCM mode ¹ . | I _{ACTIVE} | 38.4 MHz crystal, CPU running while loop from flash ² | — | 86 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 63 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 71 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 78 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 76 | — | μA/MHz |
| Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise CCM mode ³ . | I _{ACTIVE} | 38.4 MHz crystal, CPU running while loop from flash ² | — | 96 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 75 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 81 | — | μA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 88 | — | μA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 94 | — | μA/MHz |
| Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise DCM mode ¹ . | I _{EM1} | 38.4 MHz crystal ² | — | 47 | — | μA/MHz |
| | | 38 MHz HFRCO | — | 32 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 38 | — | μA/MHz |
| Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise CCM mode ³ . | I _{EM1} | 38.4 MHz crystal ² | — | 59 | — | μA/MHz |
| | | 38 MHz HFRCO | — | 45 | — | μA/MHz |
| | | 26 MHz HFRCO | — | 58 | — | μA/MHz |
| Current consumption in EM2 Deep Sleep mode. DCDC in Low Power mode ⁴ . | I _{EM2} | Full RAM retention and RTCC running from LFXO | — | 2.5 | — | μA |
| | | 4 kB RAM retention and RTCC running from LFRCO | — | 2.2 | — | μA |
| Current consumption in EM3 Stop mode | I _{EM3} | Full RAM retention and CRYO-TIMER running from ULFRCO | — | 2.1 | — | μA |
| Current consumption in EM4H Hibernate mode | I _{EM4} | 128 byte RAM retention, RTCC running from LFXO | — | 0.86 | — | μA |
| | | 128 byte RAM retention, CRYO-TIMER running from ULFRCO | — | 0.58 | — | μA |
| | | 128 byte RAM retention, no RTCC | — | 0.58 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------|---------------------------|-----|------|-----|---------------|
| Current consumption in EM4S Shutoff mode | I_{EM4S} | no RAM retention, no RTCC | — | 0.04 | — | μA |

Note:

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD
2. CMU_HFXOCTRL_LOWPOWER=1
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD
4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPBIAS=3, LPCILIMSEL=1, ANASW=DVDD

4.1.5.3 Current Consumption 1.85 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.85 V. T_{OP} = 25 °C. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C. See [Figure 5.1 EFM32PG1 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 52](#).

Table 4.7. Current Consumption 1.85V without DC/DC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|--|-----|------|-----|--------|
| Current consumption in EM0 Active mode with all peripherals disabled | I _{ACTIVE} | 38.4 MHz crystal, CPU running while loop from flash ¹ | — | 127 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 88 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 100 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 112 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 102 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 220 | — | µA/MHz |
| Current consumption in EM1 Sleep mode with all peripherals disabled | I _{EM1} | 38.4 MHz crystal ¹ | — | 61 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 35 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 37 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 154 | — | µA/MHz |
| Current consumption in EM2 Deep Sleep mode | I _{EM2} | Full RAM retention and RTCC running from LFXO | — | 3.2 | — | µA |
| | | 4 kB RAM retention and RTCC running from LFRCO | — | 2.8 | — | µA |
| Current consumption in EM3 Stop mode | I _{EM3} | Full RAM retention and CRYO-TIMER running from ULFRCO | — | 2.7 | — | µA |
| Current consumption in EM4H Hibernate mode | I _{EM4} | 128 byte RAM retention, RTCC running from LFXO | — | 1 | — | µA |
| | | 128 byte RAM retention, CRYO-TIMER running from ULFRCO | — | 0.62 | — | µA |
| | | 128 byte RAM retention, no RTCC | — | 0.62 | — | µA |
| Current consumption in EM4S Shutoff mode | I _{EM4S} | No RAM retention, no RTCC | — | 0.02 | — | µA |

Note:

1. CMU_HFXOCTRL_LOWPOWER=1

4.1.6 Wake up times

Table 4.8. Wake up times

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---------------------------|-----|------|-----|---------------|
| Wake up from EM2 Deep Sleep | t_{EM2_WU} | Code execution from flash | — | 10.7 | — | μs |
| | | Code execution from RAM | — | 3 | — | μs |
| Wakeup time from EM1 Sleep | t_{EM1_WU} | Executing from flash | — | 3 | — | AHB Clocks |
| | | Executing from RAM | — | 3 | — | AHB Clocks |
| Wake up from EM3 Stop | t_{EM3_WU} | Executing from flash | — | 10.7 | — | μs |
| | | Executing from RAM | — | 3 | — | μs |
| Wake up from EM4H Hibernate ¹ | t_{EM4H_WU} | Executing from flash | — | 60 | — | μs |
| Wake up from EM4S Shut-off ¹ | t_{EM4S_WU} | | — | 290 | — | μs |
| Note: | | | | | | |
| 1. Time from wakeup request until first instruction is executed. Wakeup results in device reset. | | | | | | |

4.1.7 Brown Out Detector

Table 4.9. Brown Out Detector

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------|----------------------|--|------|-----|------|---------------|
| DVDD BOD threshold | $V_{DVDDBOD}$ | DVDD rising | — | — | 1.62 | V |
| | | DVDD falling | 1.35 | — | — | V |
| DVDD BOD hysteresis | $V_{DVDDBOD_HYST}$ | | — | 24 | — | mV |
| DVDD response time | $t_{DVDDBOD_DELAY}$ | Supply drops at 0.1V/ μs rate | — | 2.4 | — | μs |
| AVDD BOD threshold | $V_{AVDDBOD}$ | AVDD rising | — | — | 1.85 | V |
| | | AVDD falling | 1.62 | — | — | V |
| AVDD BOD hysteresis | $V_{AVDDBOD_HYST}$ | | — | 21 | — | mV |
| AVDD response time | $t_{AVDDBOD_DELAY}$ | Supply drops at 0.1V/ μs rate | — | 2.4 | — | μs |
| EM4 BOD threshold | V_{EM4BOD} | AVDD rising | — | — | 1.7 | V |
| | | AVDD falling | 1.45 | — | — | V |
| EM4 BOD hysteresis | V_{EM4BOD_HYST} | | — | 46 | — | mV |
| EM4 response time | t_{EM4BOD_DELAY} | Supply drops at 0.1V/ μs rate | — | 300 | — | μs |

4.1.8 Oscillators

4.1.8.1 LFXO

Table 4.10. LFXO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---|-----|--------|-----|------------|
| Crystal frequency | f_{LFXO} | | — | 32.768 | — | kHz |
| Supported crystal equivalent series resistance (ESR) | ESR_{LFXO} | | — | — | 70 | k Ω |
| Supported range of crystal load capacitance ¹ | C_{LFXO_CL} | | 6 | — | 18 | pF |
| On-chip tuning cap range ² | C_{LFXO_T} | On each of LFX TAL_N and LFX TAL_P pins | 8 | — | 40 | pF |
| On-chip tuning cap step size | SS_{LFXO} | | — | 0.25 | — | pF |
| Current consumption after startup ³ | I_{LFXO} | ESR = 70 k Ω , C_L = 7 pF, GAIN ⁴ = 3, AGC ⁴ = 1 | — | 273 | — | nA |
| Start- up time | t_{LFXO} | ESR=70 k Ω , C_L = 7 pF, GAIN ⁴ = 2 | — | 308 | — | ms |

Note:

1. Total load capacitance as seen by the crystal
2. The effective load capacitance seen by the crystal will be $C_{LFXO_T} / 2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register
4. In CMU_LFXOCTRL register

4.1.8.2 HFXO

Table 4.11. HFXO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------------------|---|-----|------|-----|---------------|
| Crystal Frequency | f_{HFXO} | | 38 | 38.4 | 40 | MHz |
| Supported crystal equivalent series resistance (ESR) | ESR_{HFXO} | Crystal frequency 38.4 MHz | — | — | 60 | Ω |
| Supported range of crystal load capacitance ¹ | $C_{\text{HFXO_CL}}$ | | 6 | — | 12 | pF |
| On-chip tuning cap range ² | $C_{\text{HFXO_T}}$ | On each of HFXTAL_N and HFXTAL_P pins | 9 | 20 | 25 | pF |
| On-chip tuning capacitance step | SS_{HFXO} | | — | 0.04 | — | pF |
| Startup time | t_{HFXO} | 38.4 MHz, ESR = 50 Ω , C_L = 10 pF | — | 300 | — | μs |
| Frequency Tolerance for the crystal | FT_{HFXO} | 38.4 MHz, ESR = 50 Ω , C_L = 10 pF | -40 | — | 40 | ppm |
| Note: | | | | | | |
| 1. Total load capacitance as seen by the crystal | | | | | | |
| 2. The effective load capacitance seen by the crystal will be $C_{\text{HFXO_T}}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal. | | | | | | |

4.1.8.3 LFRCO

Table 4.12. LFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|--|--------|--------|--------|---------------|
| Oscillation frequency | f_{LFRCO} | ENVREF = 1 in CMU_LFRCOCTRL, $T_{\text{AMB}} \leq 85$ °C | 30.474 | 32.768 | 34.243 | kHz |
| | | ENVREF = 1 in CMU_LFRCOCTRL, $T_{\text{AMB}} > 85$ °C | 30.474 | — | 39.7 | kHz |
| | | ENVREF = 0 in CMU_LFRCOCTRL | 30.474 | 32.768 | 33.915 | kHz |
| Startup time | t_{LFRCO} | | — | 500 | — | μs |
| Current consumption ¹ | I_{LFRCO} | ENVREF = 1 in CMU_LFRCOCTRL | — | 342 | — | nA |
| | | ENVREF = 0 in CMU_LFRCOCTRL | — | 494 | — | nA |
| Note: | | | | | | |
| 1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register | | | | | | |

4.1.8.4 HFRCO and AUXHFRCO

Table 4.13. HFRCO and AUXHFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|-------------------------|---|------|-----|-----|---------------|
| Frequency Accuracy | $f_{\text{HFRCO_ACC}}$ | Any frequency band, across supply voltage and temperature | -2.5 | — | 2.5 | % |
| Start-up time | t_{HFRCO} | $f_{\text{HFRCO}} \geq 19 \text{ MHz}$ | — | 300 | — | ns |
| | | $4 < f_{\text{HFRCO}} < 19 \text{ MHz}$ | — | 1 | — | μs |
| | | $f_{\text{HFRCO}} \leq 4 \text{ MHz}$ | — | 2.5 | — | μs |
| Current consumption on all supplies | I_{HFRCO} | $f_{\text{HFRCO}} = 38 \text{ MHz}$ | — | 204 | 228 | μA |
| | | $f_{\text{HFRCO}} = 32 \text{ MHz}$ | — | 171 | 190 | μA |
| | | $f_{\text{HFRCO}} = 26 \text{ MHz}$ | — | 147 | 164 | μA |
| | | $f_{\text{HFRCO}} = 19 \text{ MHz}$ | — | 126 | 138 | μA |
| | | $f_{\text{HFRCO}} = 16 \text{ MHz}$ | — | 110 | 120 | μA |
| | | $f_{\text{HFRCO}} = 13 \text{ MHz}$ | — | 100 | 110 | μA |
| | | $f_{\text{HFRCO}} = 7 \text{ MHz}$ | — | 81 | 91 | μA |
| | | $f_{\text{HFRCO}} = 4 \text{ MHz}$ | — | 33 | 35 | μA |
| | | $f_{\text{HFRCO}} = 2 \text{ MHz}$ | — | 31 | 35 | μA |
| | | $f_{\text{HFRCO}} = 1 \text{ MHz}$ | — | 30 | 35 | μA |
| Step size | SS_{HFRCO} | Coarse (% of period) | — | 0.8 | — | % |
| | | Fine (% of period) | — | 0.1 | — | % |
| Period Jitter | PJ_{HFRCO} | | — | 0.2 | — | % RMS |

4.1.8.5 ULFRCO

Table 4.14. ULFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------|---------------------|----------------|------|-----|------|------|
| Oscillation frequency | f_{ULFRCO} | | 0.95 | 1 | 1.07 | kHz |

4.1.9 Flash Memory Characteristics

Table 4.15. Flash Memory Characteristics¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------------|---------------------------|-------|-----|-----|--------|
| Flash erase cycles before failure | EC _{FLASH} | | 10000 | — | — | cycles |
| Flash data retention | RET _{FLASH} | T _{AMB} ≤ 85 °C | 10 | — | — | years |
| | | T _{AMB} ≤ 125 °C | 10 | — | — | years |
| Word (32-bit) programming time | t _{W_PROG} | | 20 | 26 | 40 | μs |
| Page erase time | t _{PERASE} | | 20 | 27 | 40 | ms |
| Mass erase time | t _{MERASE} | | 20 | 27 | 40 | ms |
| Device erase time ² | t _{DERASE} | T _{AMB} ≤ 85 °C | — | 60 | 74 | ms |
| | | T _{AMB} ≤ 125 °C | — | 60 | 78 | ms |
| Page erase current ³ | I _{ERASE} | | — | — | 3 | mA |
| Mass or Device erase current ³ | | | — | — | 5 | mA |
| Write current ³ | I _{WRITE} | | — | — | 3 | mA |

Note:

- Flash data retention information is published in the Quarterly Quality and Reliability Report.
- Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW)
- Measured at 25°C

4.1.10 GPIO

Table 4.16. GPIO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------------|---|-----------|-----|-----------|------|
| Input low voltage | V _{IOIL} | GPIO pins | — | — | IOVDD*0.3 | V |
| | | RESETn | — | — | AVDD*0.3 | V |
| Input high voltage | V _{IOIH} | GPIO pins | IOVDD*0.7 | — | — | V |
| | | RESETn | AVDD*0.7 | — | — | V |
| Output high voltage relative to IOVDD | V _{IOOH} | Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ¹ = WEAK | IOVDD*0.8 | — | — | V |
| | | Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ¹ = WEAK | IOVDD*0.6 | — | — | V |
| | | Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ¹ = STRONG | IOVDD*0.8 | — | — | V |
| | | Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ¹ = STRONG | IOVDD*0.6 | — | — | V |
| Output low voltage relative to IOVDD | V _{IOOL} | Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ¹ = WEAK | — | — | IOVDD*0.2 | V |
| | | Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ¹ = WEAK | — | — | IOVDD*0.4 | V |
| | | Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH ¹ = STRONG | — | — | IOVDD*0.2 | V |
| | | Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH ¹ = STRONG | — | — | IOVDD*0.4 | V |
| Input leakage current | I _{IOLEAK} | All GPIO except LFXO pins, GPIO ≤ IOVDD, T _{amb} ≤ 85 °C | — | 0.1 | 30 | nA |
| | | LFXO Pins, GPIO ≤ IOVDD, T _{amb} ≤ 85 °C | — | 0.1 | 50 | nA |
| | | All GPIO except LFXO pins, GPIO ≤ IOVDD, T _{AMB} > 85 °C | — | — | 110 | nA |
| | | LFXO Pins, GPIO ≤ IOVDD, T _{AMB} > 85 °C | — | — | 250 | nA |
| Input leakage current on 5VTOL pads above IOVDD | I _{5VTOLLEAK} | IOVDD < GPIO ≤ IOVDD + 2 V | — | 3.3 | 15 | μA |
| I/O pin pull-up resistor | R _{PU} | | 30 | 43 | 65 | kΩ |
| I/O pin pull-down resistor | R _{PD} | | 30 | 43 | 65 | kΩ |
| Pulse width of pulses removed by the glitch suppression filter | t _{IOGLITCH} | | 20 | 25 | 35 | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------|---|-----|-----|-----|------|
| Output fall time, From 70% to 30% of V_{IO} | t_{IOF} | $C_L = 50$ pF, DRIVESTRENGTH ¹ = STRONG, SLEWRATE ¹ = 0x6 | — | 1.8 | — | ns |
| | | $C_L = 50$ pF, DRIVESTRENGTH ¹ = WEAK, SLEWRATE ¹ = 0x6 | — | 4.5 | — | ns |
| Output rise time, From 30% to 70% of V_{IO} | t_{IOR} | $C_L = 50$ pF, DRIVESTRENGTH ¹ = STRONG, SLEWRATE = 0x6 ¹ | — | 2.2 | — | ns |
| | | $C_L = 50$ pF, DRIVESTRENGTH ¹ = WEAK, SLEWRATE ¹ = 0x6 | — | 7.4 | — | ns |
| RESETn low time to ensure pin reset | T_{RESET} | | 100 | — | — | ns |
| Note: 1. In GPIO_Pn_CTRL register | | | | | | |

4.1.11 VMON

Table 4.17. VMON

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|-------------------|--|------|------|------|---------|
| VMON Supply Current | I_{VMON} | In EM0 or EM1, 1 supply monitored | — | 5.8 | 8.26 | μ A |
| | | In EM0 or EM1, 4 supplies monitored | — | 11.8 | 16.8 | μ A |
| | | In EM2, EM3 or EM4, 1 supply monitored | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, 4 supplies monitored | — | 99 | — | nA |
| VMON Loading of Monitored Supply | I_{SENSE} | In EM0 or EM1 | — | 2 | — | μ A |
| | | In EM2, EM3 or EM4 | — | 2 | — | nA |
| Threshold range | V_{VMON_RANGE} | | 1.62 | — | 3.4 | V |
| Threshold step size | N_{VMON_STESP} | Coarse | — | 200 | — | mV |
| | | Fine | — | 20 | — | mV |
| Response time | t_{VMON_RES} | Supply drops at 1V/ μ s rate | — | 460 | — | ns |
| Hysteresis | V_{VMON_HYST} | | — | 26 | — | mV |

4.1.12 ADC

Table 4.18. ADC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|--|------------|-----|-------------------|---------|
| Resolution | $V_{RESOLUTION}$ | | 6 | — | 12 | Bits |
| Input voltage range | V_{ADCIN} | Single ended | 0 | — | $2 \cdot V_{REF}$ | V |
| | | Differential | $-V_{REF}$ | — | V_{REF} | V |
| Input range of external reference voltage, single ended and differential | $V_{ADCREFIN_P}$ | | 1 | — | V_{AVDD} | V |
| Power supply rejection ¹ | $PSRR_{ADC}$ | At DC | — | 80 | — | dB |
| Analog input common mode rejection ratio | $CMRR_{ADC}$ | At DC | — | 80 | — | dB |
| Current from all supplies, using internal reference buffer. Continuous operation. $WARMUPMODE^2 = KEEPADCWARM$ | $I_{ADC_CONTINUOUS_LP}$ | 1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³ | — | 301 | 350 | μA |
| | | 250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 ³ | — | 149 | — | μA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 ³ | — | 91 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. $WARMUPMODE^2 = NORMAL$ | $I_{ADC_NORMAL_LP}$ | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³ | — | 51 | — | μA |
| | | 5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 ³ | — | 9 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. $AWARMUPMODE^2 = KEEPINSTANDBY$ or $KEEPINSLOWACC$ | $I_{ADC_STANDBY_LP}$ | 125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³ | — | 117 | — | μA |
| | | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³ | — | 79 | — | μA |
| Current from all supplies, using internal reference buffer. Continuous operation. $WARMUPMODE^2 = KEEPADCWARM$ | $I_{ADC_CONTINUOUS_HP}$ | 1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ³ | — | 345 | — | μA |
| | | 250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 ³ | — | 191 | — | μA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 ³ | — | 132 | — | μA |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------------------|---|-----|-------|-----|--------|
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE ² = NORMAL | I _{ADC_NORMAL_HP} | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ₃ | — | 102 | — | μA |
| | | 5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 ₃ | — | 17 | — | μA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ² = KEEPINSTANDBY or KEEPINSLOWACC | I _{ADC_STANDBY_HP} | 125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ₃ | — | 162 | — | μA |
| | | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ₃ | — | 123 | — | μA |
| Current from HFPERCLK | I _{ADC_CLK} | HFPERCLK = 16 MHz | — | 140 | — | μA |
| ADC Clock Frequency | f _{ADCCLK} | | — | — | 16 | MHz |
| Throughput rate | f _{ADCRATE} | | — | — | 1 | MSPS |
| Conversion time ⁴ | t _{ADCCONV} | 6 bit | — | 7 | — | cycles |
| | | 8 bit | — | 9 | — | cycles |
| | | 12 bit | — | 13 | — | cycles |
| Startup time of reference generator and ADC core | t _{ADCSTART} | WARMUPMODE ² = NORMAL | — | — | 5 | μs |
| | | WARMUPMODE ² = KEEPINSTANDBY | — | — | 2 | μs |
| | | WARMUPMODE ² = KEEPINSLOWACC | — | — | 1 | μs |
| SNDR at 1MSPS and f _{in} = 10kHz | SNDR _{ADC} | Internal reference, 2.5 V full-scale, differential (-1.25, 1.25) | 58 | 67 | — | dB |
| | | v _{refp_in} = 1.25 V direct mode with 2.5 V full-scale, differential | — | 68 | — | dB |
| Spurious-Free Dynamic Range (SFDR) | SFDR _{ADC} | 1 MSamples/s, 10 kHz full-scale sine wave | — | 75 | — | dB |
| Input referred ADC noise, rms | V _{REF_NOISE} | Including quantization noise and distortion | — | 380 | — | μV |
| Offset Error | V _{ADCOFFSETERR} | | -3 | 0.25 | 3 | LSB |
| Gain error in ADC | V _{ADC_GAIN} | Using internal reference | — | -0.2 | 5 | % |
| | | Using external reference | — | -1 | — | % |
| Differential non-linearity (DNL) | DNL _{ADC} | 12 bit resolution, No Missing Codes | -1 | — | 2 | LSB |
| Integral non-linearity (INL), End point method | INL _{ADC} | 12 bit resolution | -6 | — | 6 | LSB |
| Temperature Sensor Slope | V _{TS_SLOPE} | | — | -1.84 | — | mV/°C |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-----|------|
| Note: | | | | | | |
| 1. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL | | | | | | |
| 2. In ADCn_CNTL register | | | | | | |
| 3. In ADCn_BIASPROG register | | | | | | |
| 4. Derived from ADCCLK | | | | | | |

4.1.13 IDAC

Table 4.19. IDAC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|---|------|------|-----|------|
| Number of Ranges | N_{IDAC_RANGES} | | — | 4 | — | - |
| Output Current | I_{IDAC_OUT} | RANGSEL ¹ = RANGE0 | 0.05 | — | 1.6 | μA |
| | | RANGSEL ¹ = RANGE1 | 1.6 | — | 4.7 | μA |
| | | RANGSEL ¹ = RANGE2 | 0.5 | — | 16 | μA |
| | | RANGSEL ¹ = RANGE3 | 2 | — | 64 | μA |
| Linear steps within each range | N_{IDAC_STEPS} | | — | 32 | — | |
| Step size | SS_{IDAC} | RANGSEL ¹ = RANGE0 | — | 50 | — | nA |
| | | RANGSEL ¹ = RANGE1 | — | 100 | — | nA |
| | | RANGSEL ¹ = RANGE2 | — | 500 | — | nA |
| | | RANGSEL ¹ = RANGE3 | — | 2 | — | μA |
| Total Accuracy, STEPSEL ¹ = 0x10 | ACC_{IDAC} | EM0 or EM1, AVDD=3.3 V, T = 25 °C | -2 | — | 2 | % |
| | | EM0 or EM1 | -18 | — | 22 | % |
| | | EM2 or EM3, Source mode, RANGSEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C | — | -2 | — | % |
| | | EM2 or EM3, Source mode, RANGSEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C | — | -1.7 | — | % |
| | | EM2 or EM3, Source mode, RANGSEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.8 | — | % |
| | | EM2 or EM3, Source mode, RANGSEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C | — | -0.7 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C | — | -0.6 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| Start up time | t_{IDAC_SU} | Output within 1% of steady state value | — | 5 | — | μs |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------|---|-----|------|-----|---------|
| Settling time, (output settled within 1% of steady state value) | t_{IDAC_SETTLE} | Range setting is changed | — | 5 | — | μs |
| | | Step value is changed | — | 1 | — | μs |
| Current consumption in EM0 or EM1 ² | I_{IDAC} | Source mode, excluding output current | — | 8.9 | 13 | μA |
| | | Sink mode, excluding output current | — | 12 | 16 | μA |
| Current consumption in EM2 or EM3 ² | I_{IDAC} | Source mode, excluding output current, duty cycle mode, T = 25 °C | — | 1.04 | — | μA |
| | | Sink mode, excluding output current, duty cycle mode, T = 25 °C | — | 1.08 | — | μA |
| | | Source mode, excluding output current, duty cycle mode, T ≥ 85 °C | — | 8.9 | — | μA |
| | | Sink mode, excluding output current, duty cycle mode, T ≥ 85 °C | — | 12 | — | μA |
| Output voltage compliance in source mode, source current change relative to current sourced at 0 V | I_{COMP_SRC} | RANGESEL1=0, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2-100\text{ mV})$ | — | 0.04 | — | % |
| | | RANGESEL1=1, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2-100\text{ mV})$ | — | 0.02 | — | % |
| | | RANGESEL1=2, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2-150\text{ mV})$ | — | 0.02 | — | % |
| | | RANGESEL1=3, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2-250\text{ mV})$ | — | 0.02 | — | % |
| Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD | I_{COMP_SINK} | RANGESEL1=0, output voltage = 100 mV | — | 0.18 | — | % |
| | | RANGESEL1=1, output voltage = 100 mV | — | 0.12 | — | % |
| | | RANGESEL1=2, output voltage = 150 mV | — | 0.08 | — | % |
| | | RANGESEL1=3, output voltage = 250 mV | — | 0.02 | — | % |

Note:

1. In IDAC_CURPROG register
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.14 Analog Comparator (ACMP)

Table 4.20. ACMP

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|--|-------|-----|--------------------|------|
| Input voltage range | V_{ACMPIN} | ACMPVDD = ACMPn_CTRL_PWRSEL ¹ | 0 | — | $V_{ACMPVDD}$ | V |
| Supply Voltage | $V_{ACMPVDD}$ | BIASPROG ² ≤ 0x10 or FULL- BIAS ² = 0 | 1.85 | — | $V_{VREGVDD_MAX}$ | V |
| | | 0x10 < BIASPROG ² ≤ 0x20 and FULLBIAS ² = 1 | 2.1 | — | $V_{VREGVDD_MAX}$ | V |
| Active current not including voltage reference | I_{ACMP} | BIASPROG ² = 0x10, FULLBIAS ² = 0 | — | 306 | — | nA |
| | | BIASPROG ² = 0x20, FULLBIAS ² = 1 | — | 74 | 95 | μA |
| Current consumption of internal voltage reference | $I_{ACMPREF}$ | VLP selected as input using 2.5 V Reference / 4 (0.625 V) | — | 50 | — | nA |
| | | VLP selected as input using VDD | — | 20 | — | nA |
| | | VBDIV selected as input using 1.25 V reference / 1 | — | 4.1 | — | μA |
| | | VADIV selected as input using VDD/1 | — | 2.4 | — | μA |
| Hysteresis ($V_{CM} = 1.25$ V, BIASPROG ² = 0x10, FULL- BIAS ² = 1) | $V_{ACMPHYST}$ | HYSTSEL ³ = HYST0 | -1.75 | 0 | 1.75 | mV |
| | | HYSTSEL ³ = HYST1 | 10 | 18 | 26 | mV |
| | | HYSTSEL ³ = HYST2 | 21 | 32 | 46 | mV |
| | | HYSTSEL ³ = HYST3 | 27 | 44 | 63 | mV |
| | | HYSTSEL ³ = HYST4 | 32 | 55 | 80 | mV |
| | | HYSTSEL ³ = HYST5 | 38 | 65 | 100 | mV |
| | | HYSTSEL ³ = HYST6 | 43 | 77 | 121 | mV |
| | | HYSTSEL ³ = HYST7 | 47 | 86 | 148 | mV |
| | | HYSTSEL ³ = HYST8 | -4 | 0 | 4 | mV |
| | | HYSTSEL ³ = HYST9 | -27 | -18 | -10 | mV |
| | | HYSTSEL ³ = HYST10 | -47 | -32 | -18 | mV |
| | | HYSTSEL ³ = HYST11 | -64 | -43 | -27 | mV |
| | | HYSTSEL ³ = HYST12 | -78 | -54 | -32 | mV |
| | | HYSTSEL ³ = HYST13 | -93 | -64 | -37 | mV |
| | | HYSTSEL ³ = HYST14 | -113 | -74 | -42 | mV |
| HYSTSEL ³ = HYST15 | -135 | -85 | -47 | mV | | |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------|------------------|---|-----|------|------|------------|
| Comparator delay ⁴ | $t_{ACMPDELAY}$ | BIASPROG ² = 0x10, FULLBIAS ² = 0 | — | 3.7 | — | μ s |
| | | BIASPROG ² = 0x20, FULLBIAS ² = 1 | — | 35 | — | ns |
| Offset voltage | $V_{ACMPOFFSET}$ | BIASPROG ² = 0x10, FULLBIAS ² = 1 | -35 | — | 35 | mV |
| Reference Voltage | $V_{ACMPREF}$ | Internal 1.25 V reference | 1 | 1.25 | 1.47 | V |
| | | Internal 2.5 V reference | 2 | 2.5 | 2.8 | V |
| Capacitive Sense Internal Resistance | R_{CSRES} | CSRESSEL ⁵ = 0 | — | inf | — | k Ω |
| | | CSRESSEL ⁵ = 1 | — | 15 | — | k Ω |
| | | CSRESSEL ⁵ = 2 | — | 27 | — | k Ω |
| | | CSRESSEL ⁵ = 3 | — | 39 | — | k Ω |
| | | CSRESSEL ⁵ = 4 | — | 51 | — | k Ω |
| | | CSRESSEL ⁵ = 5 | — | 102 | — | k Ω |
| | | CSRESSEL ⁵ = 6 | — | 164 | — | k Ω |
| | | CSRESSEL ⁵ = 7 | — | 239 | — | k Ω |

Note:

1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD
2. In ACMPn_CTRL register
3. In ACMPn_HYSTERESIS register
4. ± 100 mV differential drive
5. In ACMPn_INPUTSEL register

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given as:

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

$I_{ACMPREF}$ is zero if an external voltage reference is used.

4.1.15 I2C

I2C Standard-mode (Sm)

Table 4.21. I2C Standard-mode (Sm)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------|----------------|-----|-----|------|---------|
| SCL clock frequency ² | f_{SCL} | | 0 | — | 100 | kHz |
| SCL clock low time | t_{LOW} | | 4.7 | — | — | μ s |
| SCL clock high time | t_{HIGH} | | 4 | — | — | μ s |
| SDA set-up time | $t_{SU,DAT}$ | | 250 | — | — | ns |
| SDA hold time ³ | $t_{HD,DAT}$ | | 100 | — | 3450 | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | | 4.7 | — | — | μ s |
| (Repeated) START condition hold time | $t_{HD,STA}$ | | 4 | — | — | μ s |
| STOP condition set-up time | $t_{SU,STO}$ | | 4 | — | — | μ s |
| Bus free time between a STOP and START condition | t_{BUF} | | 4.7 | — | — | μ s |

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register
2. For the minimum HPPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

I2C Fast-mode (Fm)

Table 4.22. I2C Fast-mode (Fm)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|-----|-----|-----|------|
| SCL clock frequency ² | f _{SCL} | | 0 | — | 400 | kHz |
| SCL clock low time | t _{LOW} | | 1.3 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 0.6 | — | — | μs |
| SDA set-up time | t _{SU,DAT} | | 100 | — | — | ns |
| SDA hold time ³ | t _{HD,DAT} | | 100 | — | 900 | ns |
| Repeated START condition set-up time | t _{SU,STA} | | 0.6 | — | — | μs |
| (Repeated) START condition hold time | t _{HD,STA} | | 0.6 | — | — | μs |
| STOP condition set-up time | t _{SU,STO} | | 0.6 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 1.3 | — | — | μs |

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register
2. For the minimum HPPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

I2C Fast-mode Plus (Fm+)

Table 4.23. I2C Fast-mode Plus (Fm+)¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|----------------|------|-----|------|------|
| SCL clock frequency ² | f _{SCL} | | 0 | — | 1000 | kHz |
| SCL clock low time | t _{LOW} | | 0.5 | — | — | μs |
| SCL clock high time | t _{HIGH} | | 0.26 | — | — | μs |
| SDA set-up time | t _{SU,DAT} | | 50 | — | — | ns |
| SDA hold time | t _{HD,DAT} | | 100 | — | — | ns |
| Repeated START condition set-up time | t _{SU,STA} | | 0.26 | — | — | μs |
| (Repeated) START condition hold time | t _{HD,STA} | | 0.26 | — | — | μs |
| STOP condition set-up time | t _{SU,STO} | | 0.26 | — | — | μs |
| Bus free time between a STOP and START condition | t _{BUF} | | 0.5 | — | — | μs |

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register
2. For the minimum HPPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual

4.1.16 USART SPI

SPI Master Timing

Table 4.24. SPI Master Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|----------------|----------------|--------------------|-----|-----|------|
| SCLK period ^{1 2} | t_{SCLK} | | 2 * $t_{HFPERCLK}$ | — | — | ns |
| CS to MOSI ^{1 2} | t_{CS_MO} | | 0 | — | 8 | ns |
| SCLK to MOSI ^{1 2} | t_{SCLK_MO} | | 3 | — | 20 | ns |
| MISO setup time ^{1 2} | t_{SU_MI} | IOVDD = 1.62 V | 56 | — | — | ns |
| | | IOVDD = 3.0 V | 37 | — | — | ns |
| MISO hold time ^{1 2} | t_{H_MI} | | 6 | — | — | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

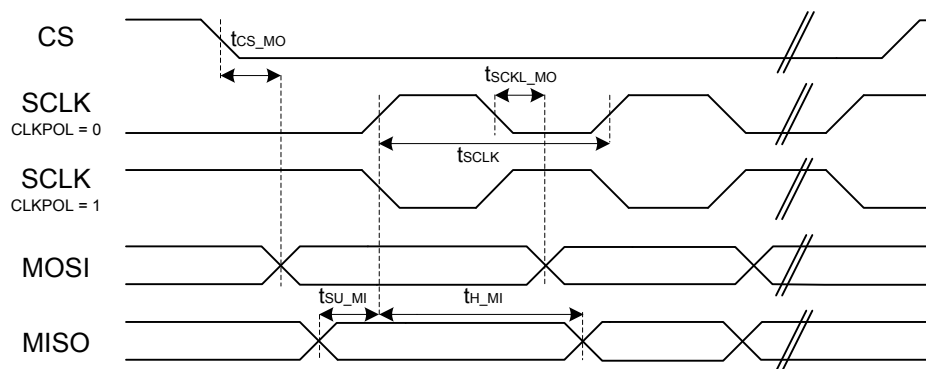


Figure 4.1. SPI Master Timing Diagram (SMSDELAY = 0)

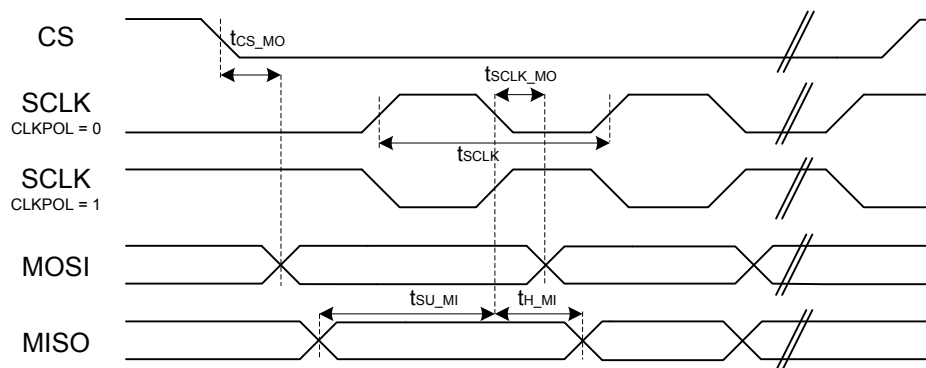


Figure 4.2. SPI Master Timing Diagram (SMSDELAY = 1)

SPI Slave Timing

Table 4.25. SPI Slave Timing

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|-------------------|----------------|---------------------------|-----|----------------------------|------|
| SCKL period ^{1 2} | t_{SCLK_sl} | | 2 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK high period ^{1 2} | t_{SCLK_hi} | | 3 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK low period ^{1 2} | t_{SCLK_lo} | | 3 * $t_{HFPERCLK}$ | — | — | ns |
| CS active to MISO ^{1 2} | $t_{CS_ACT_MI}$ | | 4 | — | 50 | ns |
| CS disable to MISO ^{1 2} | $t_{CS_DIS_MI}$ | | 4 | — | 50 | ns |
| MOSI setup time ^{1 2} | t_{SU_MO} | | 4 | — | — | ns |
| MOSI hold time ^{1 2} | t_{H_MO} | | 3 + 2 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK to MISO ^{1 2} | t_{SCLK_MI} | | 16 + $t_{HFPERCLK}$ | — | 66 + 2 * $t_{HFPERCLK}$ | ns |

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

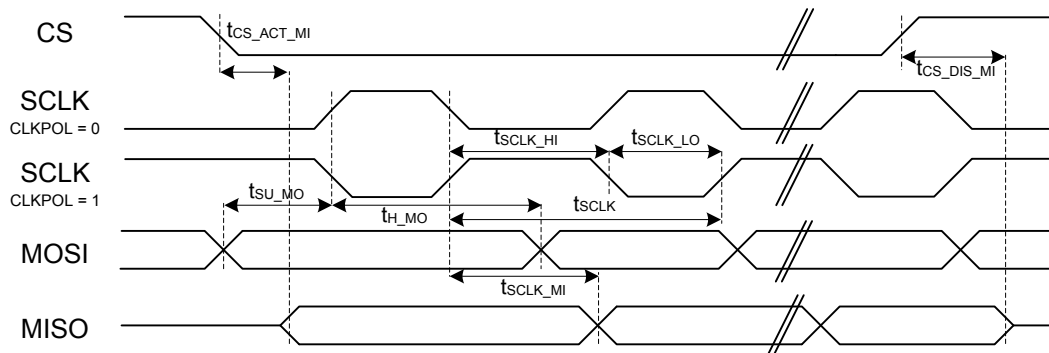


Figure 4.3. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

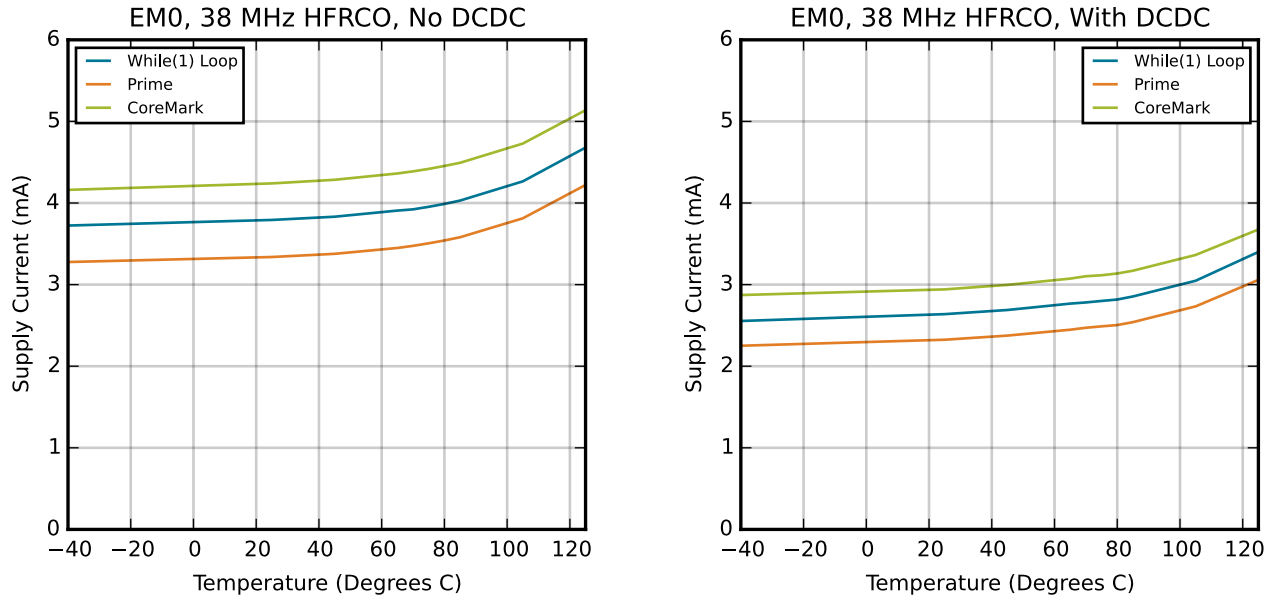


Figure 4.4. EM0 Active Mode Typical Supply Current

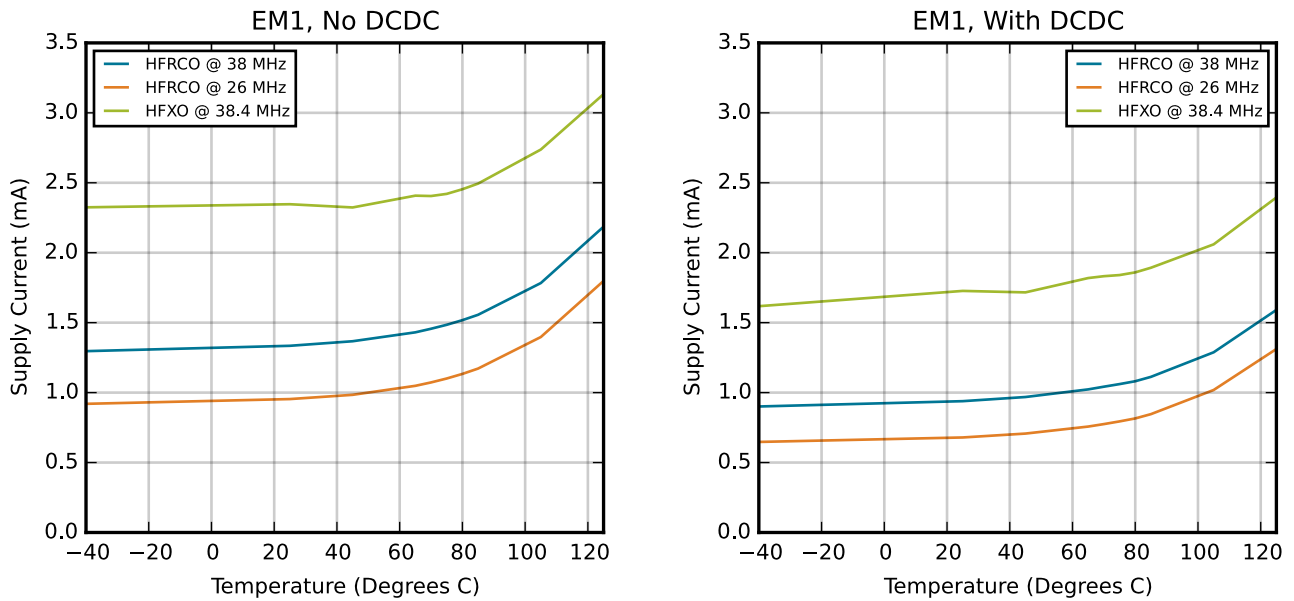


Figure 4.5. EM1 Sleep Mode Typical Supply Current

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

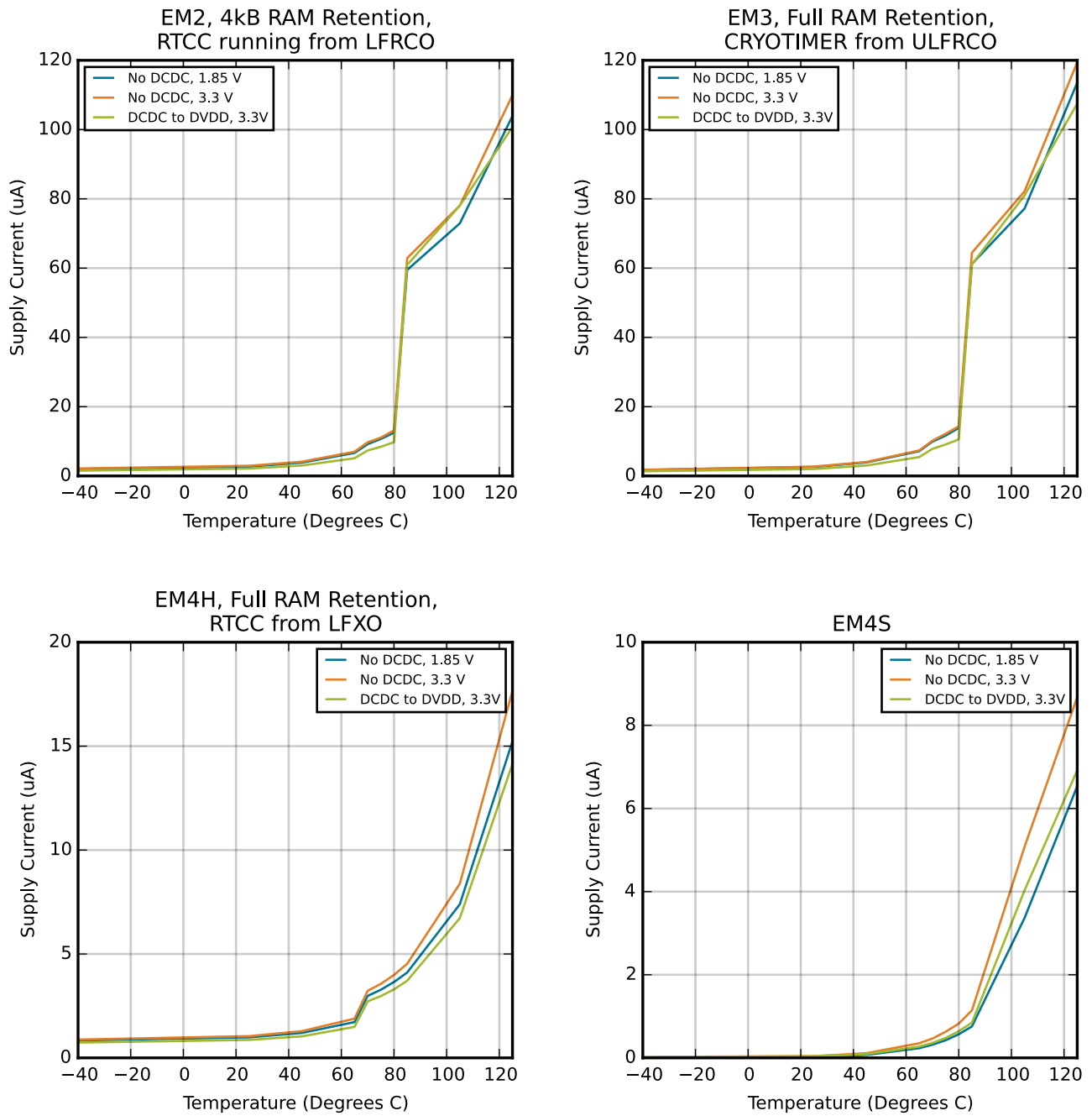


Figure 4.6. EM2, EM3, EM4H and EM4S Typical Supply Current

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 μ H, CDCDC = 1.0 μ F, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

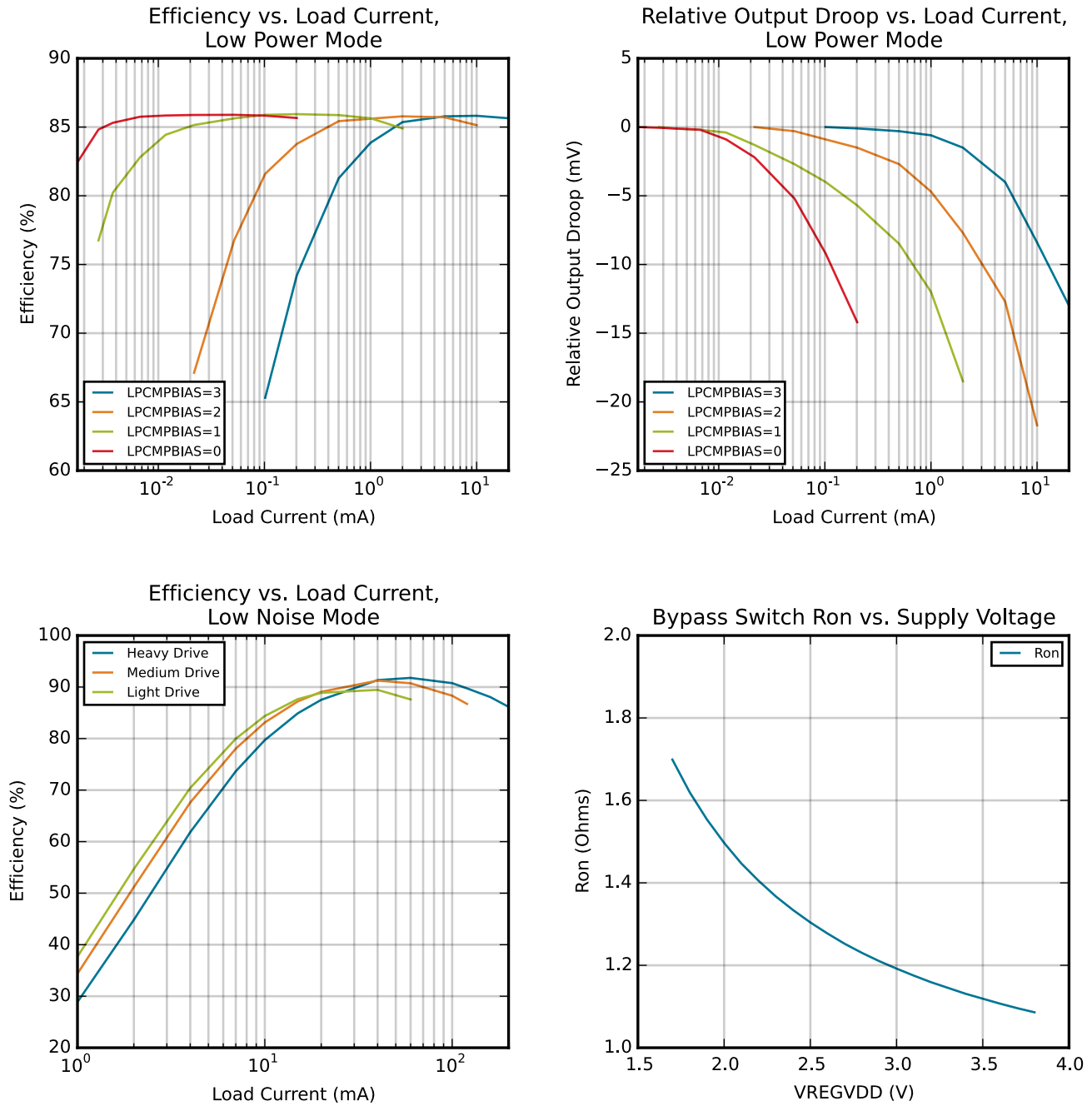
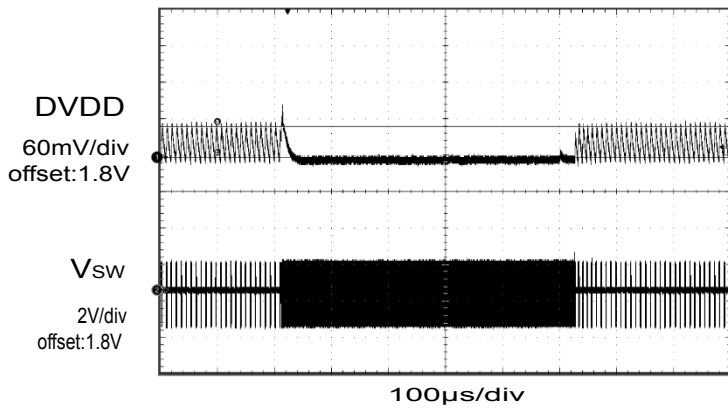


Figure 4.7. DC-DC Converter Typical Performance Characteristics

LN (CCM) and LP mode transition (load: 5mA)



Load Step Response in LN (CCM) mode (Heavy Drive)

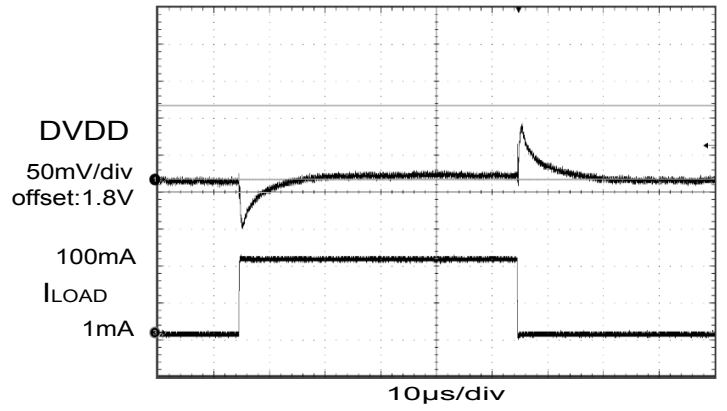


Figure 4.8. DC-DC Converter Transition Waveforms

4.2.3 Internal Oscillators

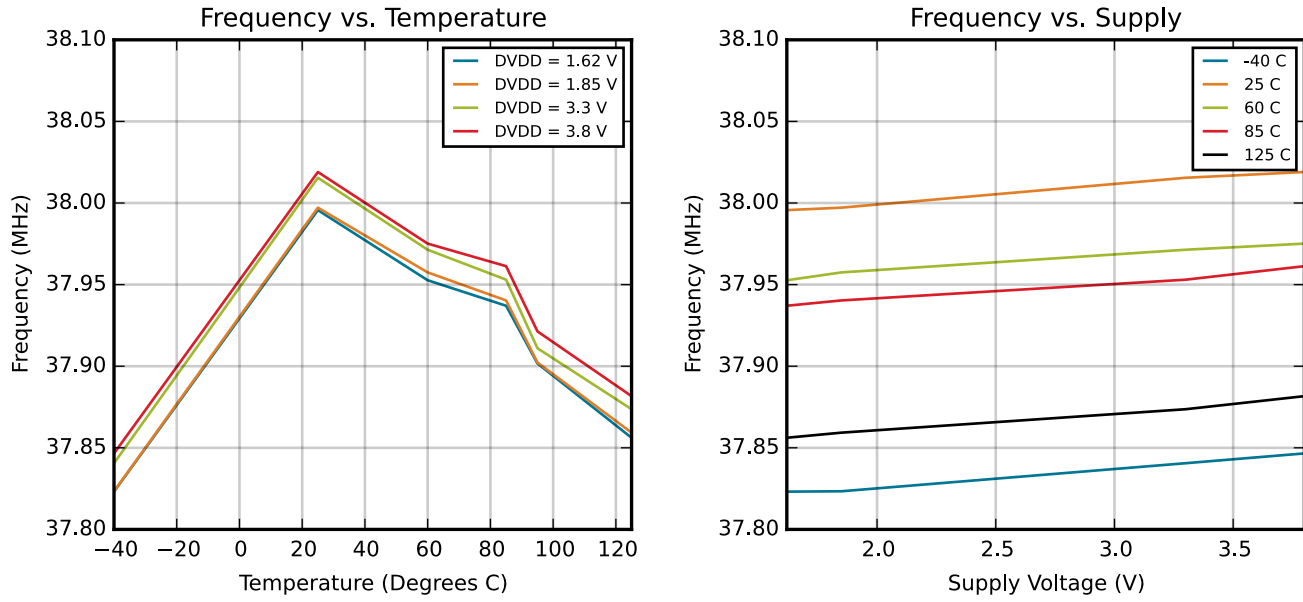


Figure 4.9. HFCO and AUXHFCO Typical Performance at 38 MHz

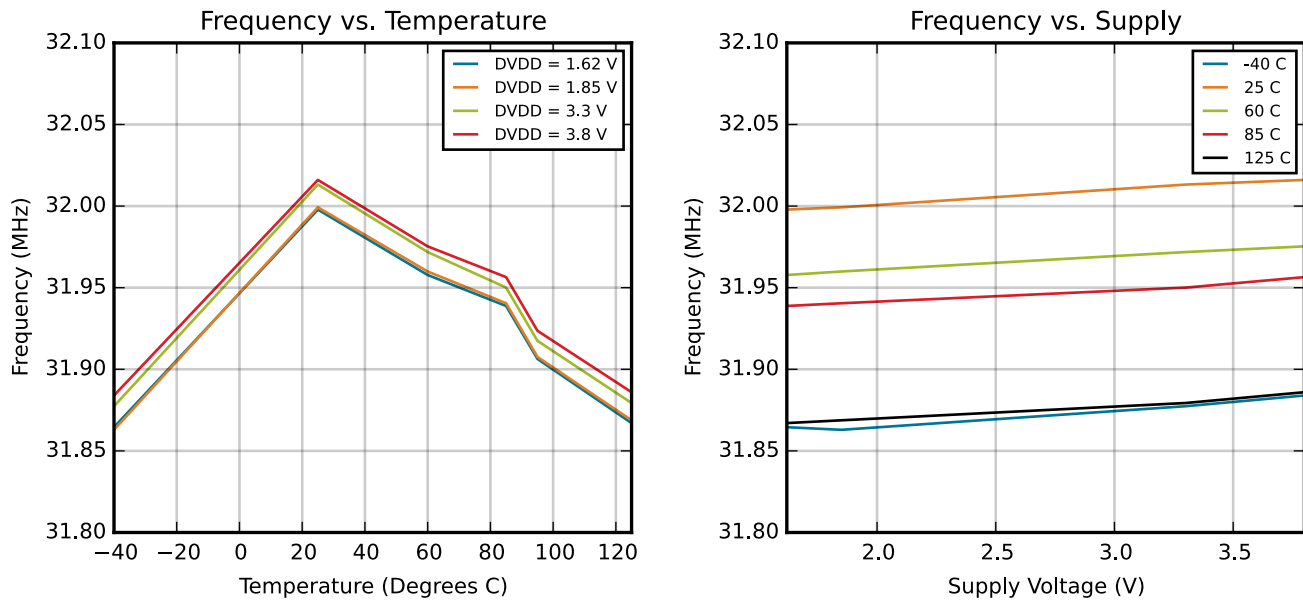


Figure 4.10. HFCO and AUXHFCO Typical Performance at 32 MHz

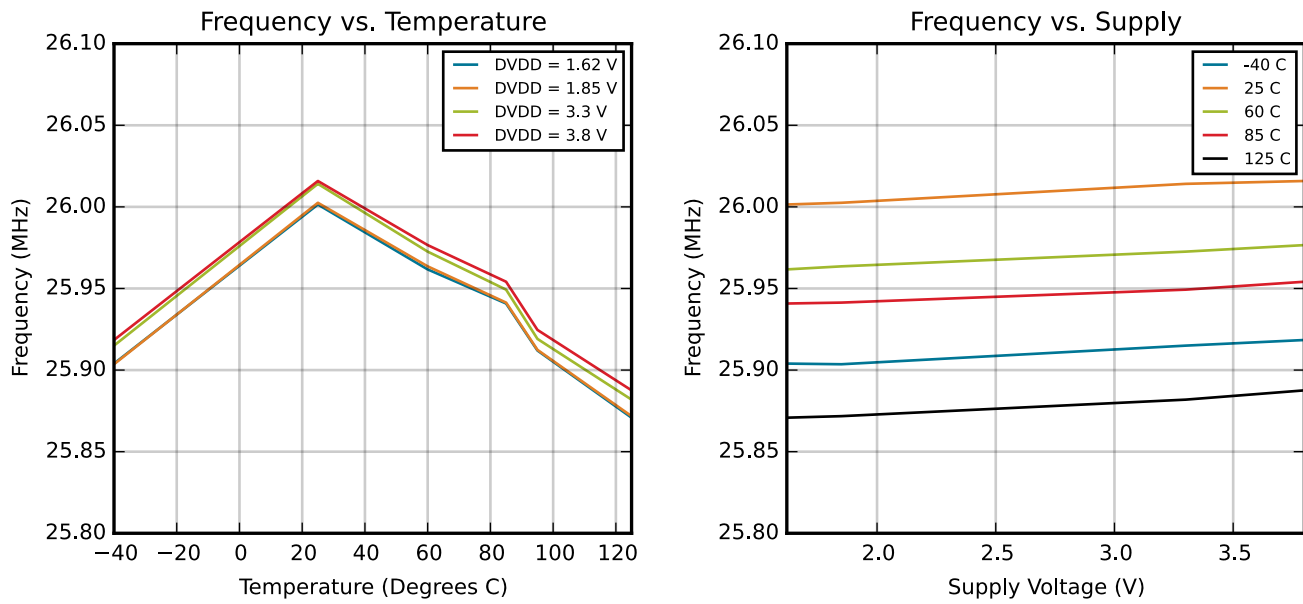


Figure 4.11. HFCO and AUXHFCO Typical Performance at 26 MHz

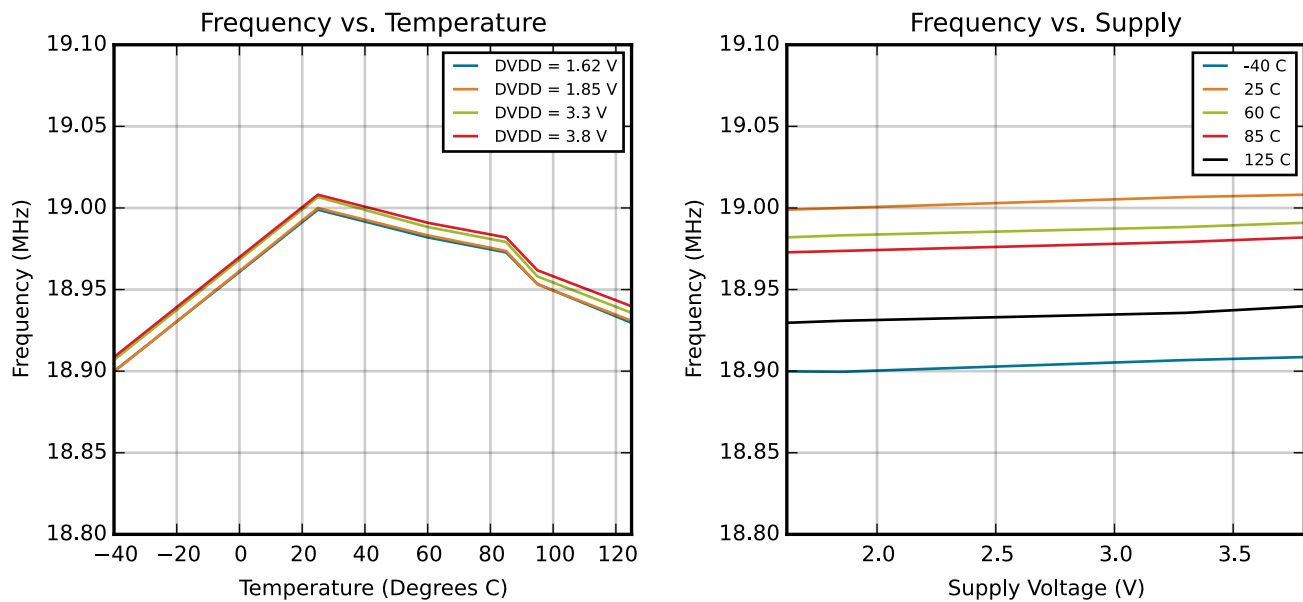


Figure 4.12. HFCO and AUXHFCO Typical Performance at 19 MHz

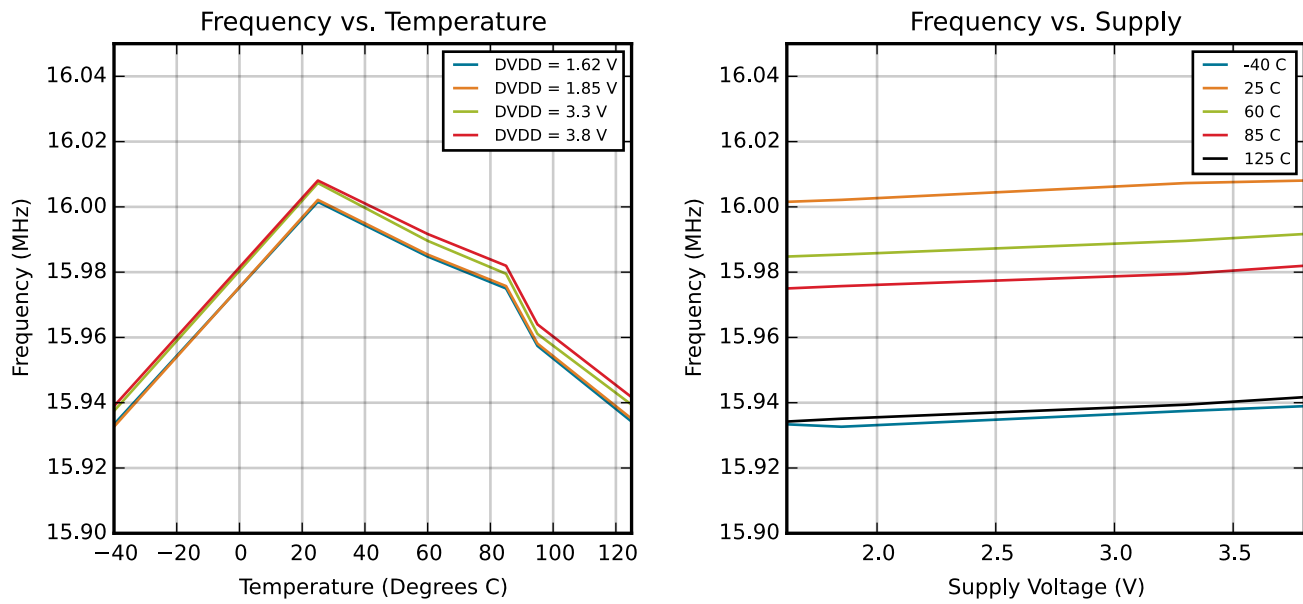


Figure 4.13. HFCO and AUXHFCO Typical Performance at 16 MHz

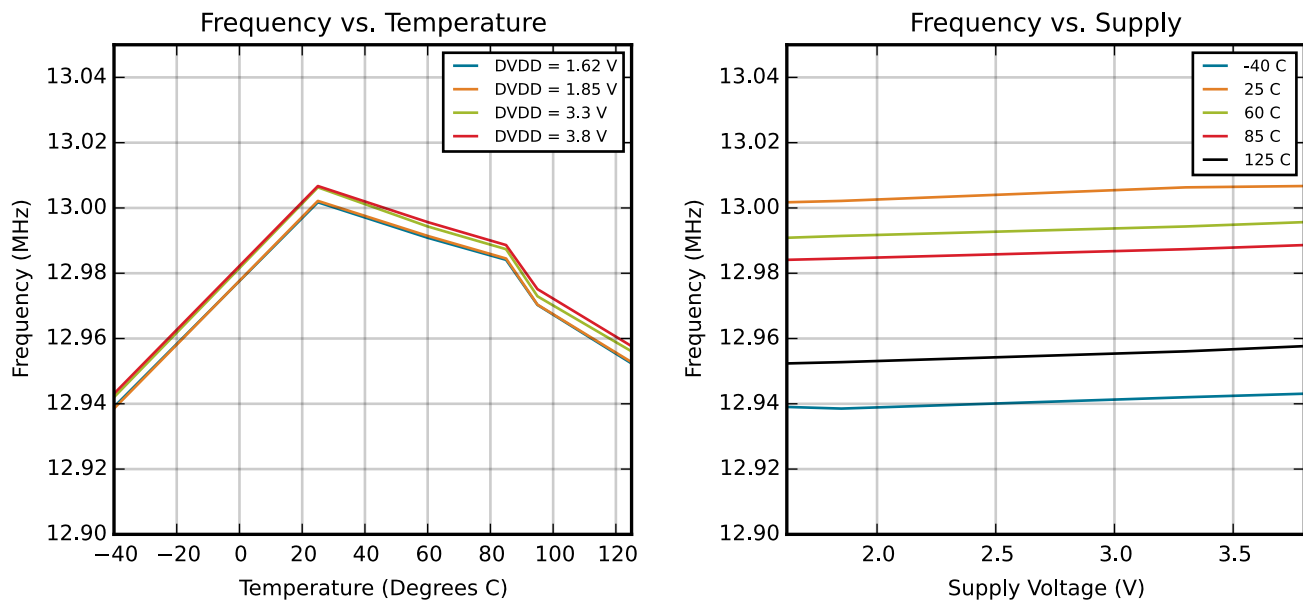


Figure 4.14. HFCO and AUXHFCO Typical Performance at 13 MHz

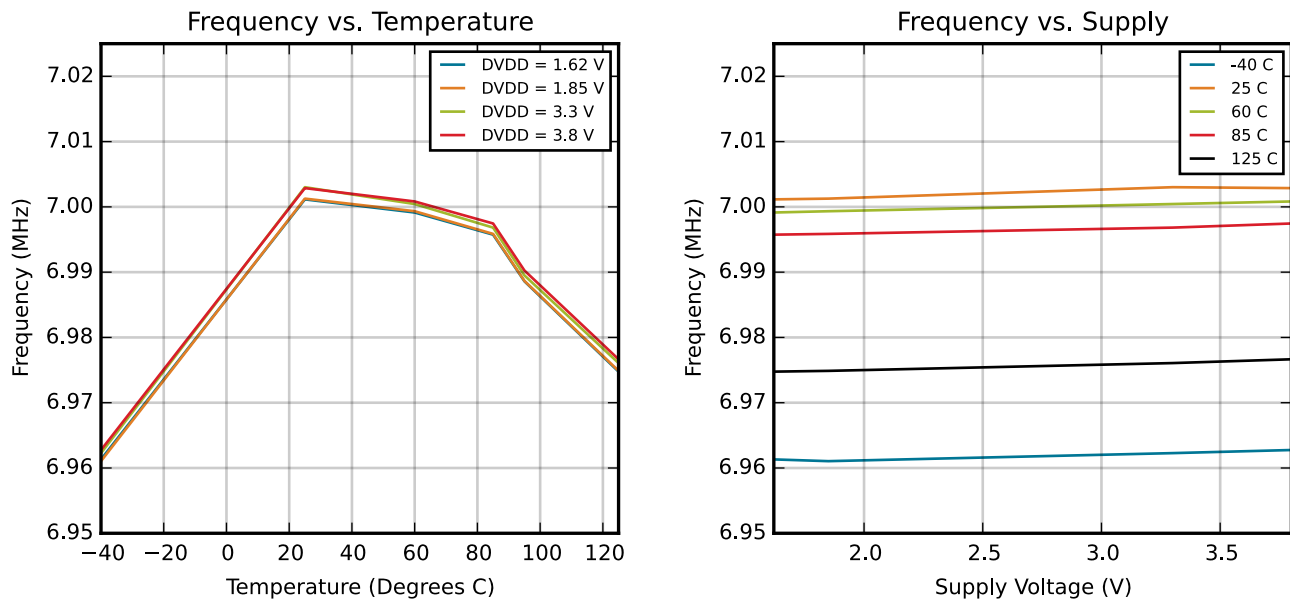


Figure 4.15. HFRCO and AUXHFRCO Typical Performance at 7 MHz

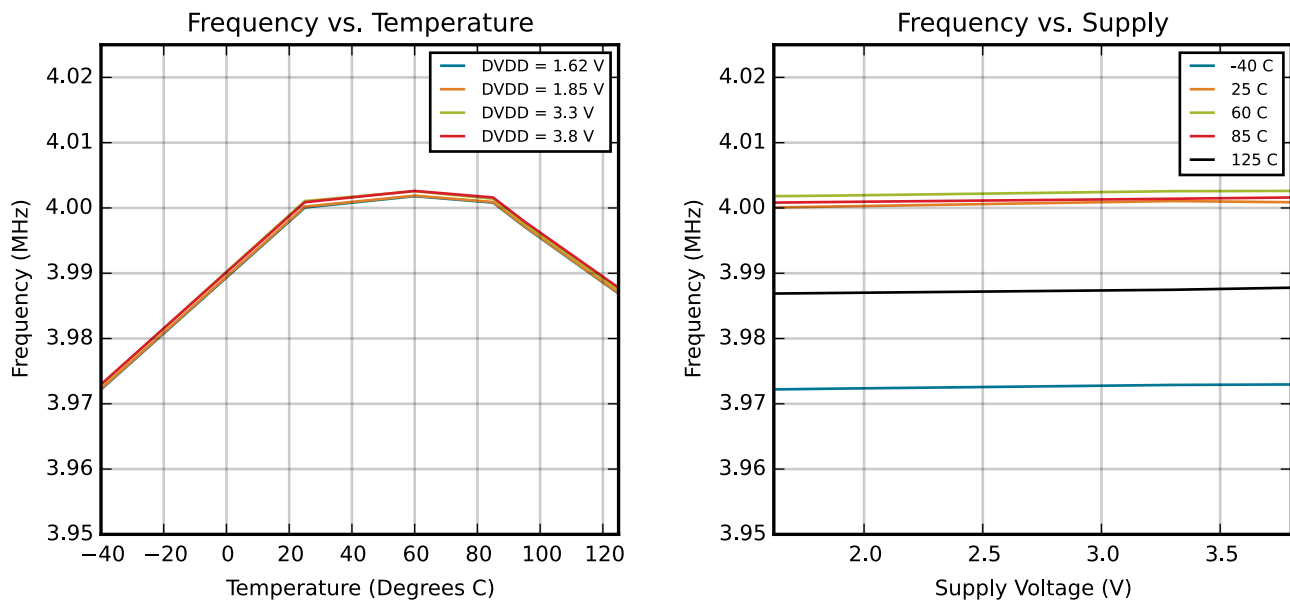


Figure 4.16. HFRCO and AUXHFRCO Typical Performance at 4 MHz

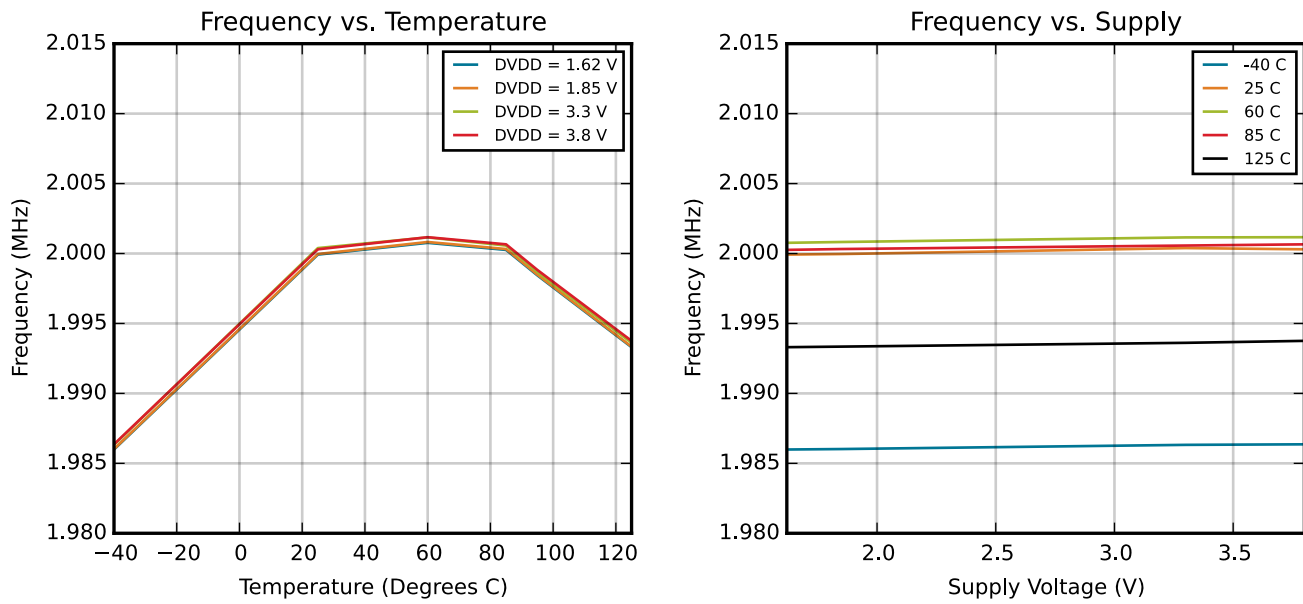


Figure 4.17. HFCO and AUXHFCO Typical Performance at 2 MHz

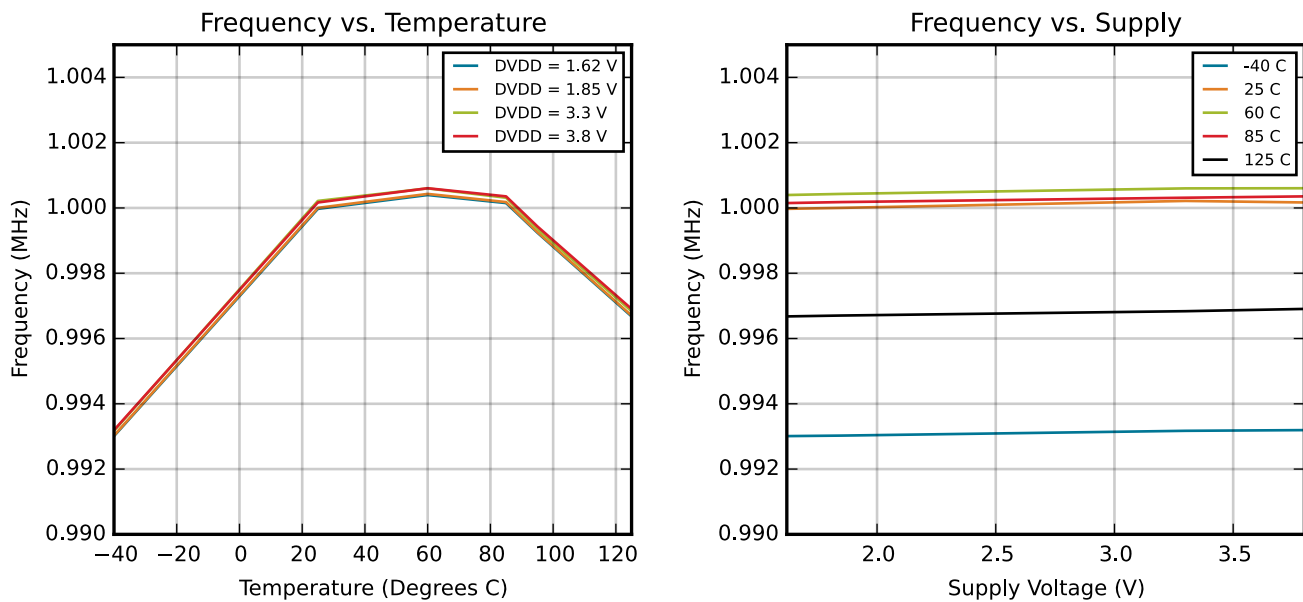


Figure 4.18. HFCO and AUXHFCO Typical Performance at 1 MHz

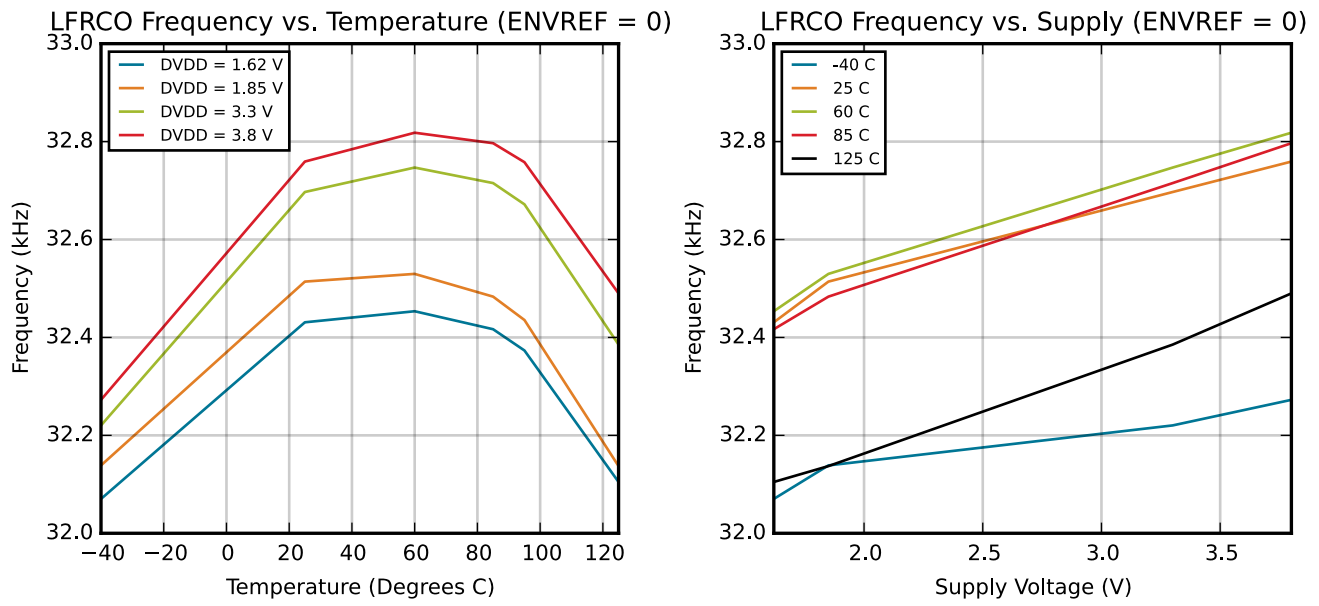


Figure 4.19. LFRCO Typical Performance at 32.768 kHz

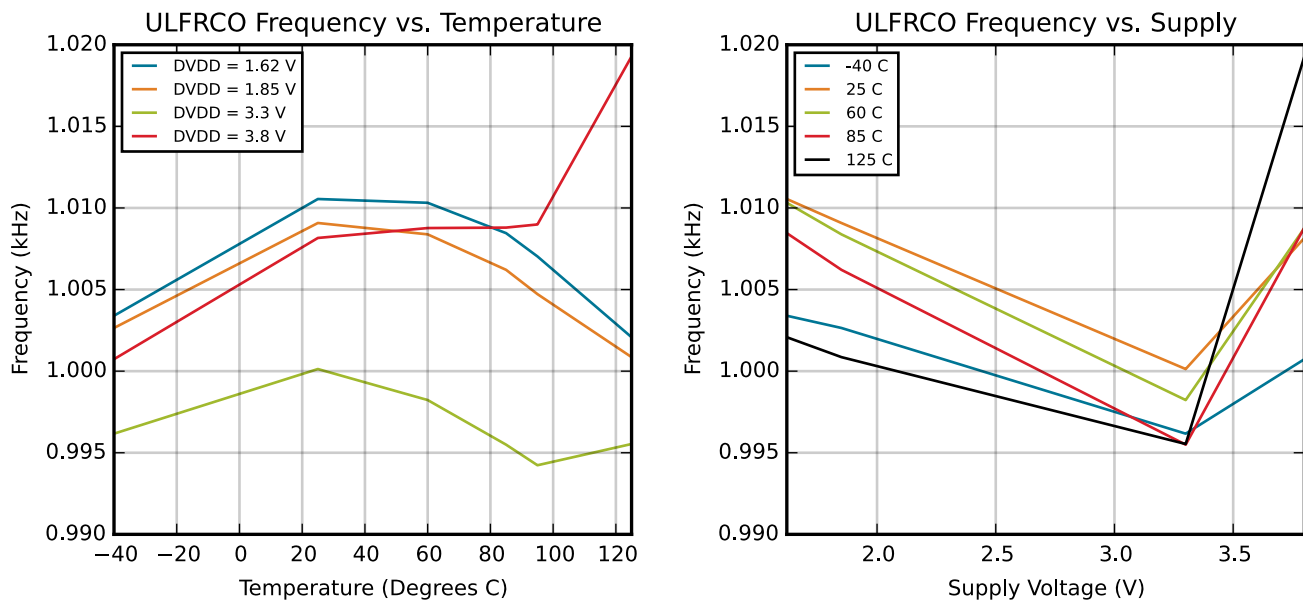


Figure 4.20. ULFRCO Typical Performance at 1 kHz

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal dc-dc converter, are shown in [Figure 5.1 EFM32PG1 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 52](#).

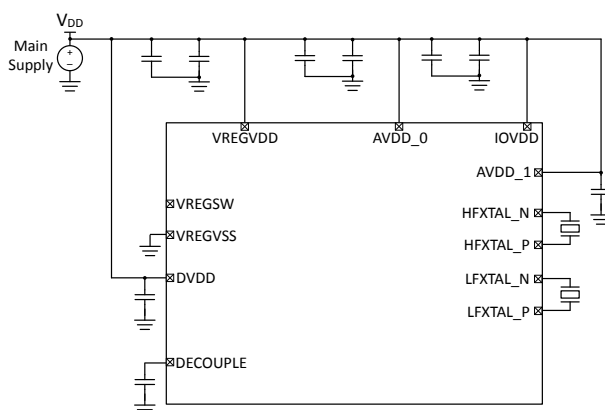


Figure 5.1. EFM32PG1 Typical Application Circuit, Direct Supply, No DC-DC Converter

A typical application circuit using the internal dc-dc converter is shown in [Figure 5.2 EFM32PG1 Typical Application Circuit Using the DC-DC Converter on page 52](#). The MCU operates from the dc-dc converter supply.

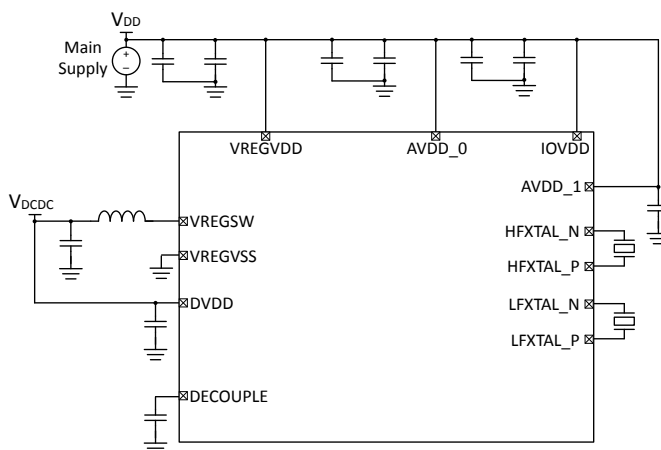


Figure 5.2. EFM32PG1 Typical Application Circuit Using the DC-DC Converter

5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 EFM32PG1 QFN48 with DC-DC Definition

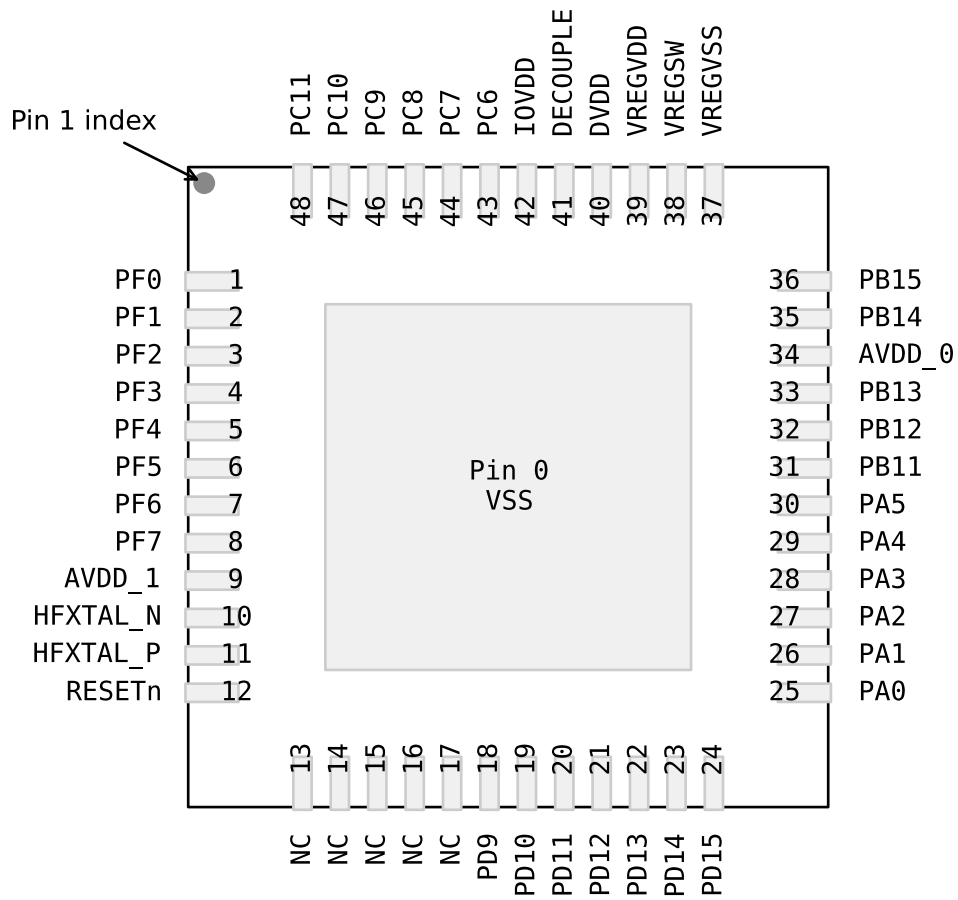


Figure 6.1. EFM32PG1 QFN48 with DC-DC Pinout

Table 6.1. QFN48 with DC-DC Device Pinout

| QFN48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | RFVSS | Radio Ground | | | |
| 1 | PF0 | BUSAX BUSBY | TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LE- TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23 | US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23 | PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0 BOOT_TX |
| 2 | PF1 | BUSAY BUSBX | TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24 | US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24 | PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0 BOOT_RX |
| 3 | PF2 | BUSAX BUSBY | TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LE- TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25 | US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25 | CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0 |

| QFN48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | PF3 | BUSAY BUSBX | TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE- TIM0_OUT0 #27 LE- TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26 | US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26 | CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0 |
| 5 | PF4 | BUSAX BUSBY | TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE- TIM0_OUT0 #28 LE- TIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27 | US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27 | PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28 |
| 6 | PF5 | BUSAY BUSBX | TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 LE- TIM0_OUT0 #29 LE- TIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28 | US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28 | PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29 |
| 7 | PF6 | BUSAX BUSBY | TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 LE- TIM0_OUT0 #30 LE- TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29 | US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29 | CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30 |

| QFN48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 8 | PF7 | BUSAY BUSBX | TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 LE- TIM0_OUT0 #31 LE- TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30 | US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30 | CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1 |
| 9 | AVDD | Analog power supply . | | | |
| 10 | HFXTAL_N | High Frequency Crystal input pin. | | | |
| 11 | HFXTAL_P | High Frequency Crystal output pin. | | | |
| 12 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 13 | NC | No Connect. | | | |
| 14 | NC | No Connect. | | | |
| 15 | NC | No Connect. | | | |
| 16 | NC | No Connect. | | | |
| 17 | NC | No Connect. | | | |
| 18 | PD9 | BUSCY BUSDX | TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 LE- TIM0_OUT0 #17 LE- TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16 | US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16 | CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17 |
| 19 | PD10 | BUSCX BUSDY | TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 LE- TIM0_OUT0 #18 LE- TIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17 | US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17 | CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18 |

| QFN48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 20 | PD11 | BUSCY BUSDX | TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 LE- TIMO_OUT0 #19 LE- TIMO_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18 | US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18 | PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19 |
| 21 | PD12 | BUSCX BUSDY | TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 LE- TIMO_OUT0 #20 LE- TIMO_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19 | US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19 | PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20 |
| 22 | PD13 | BUSCY BUSDX | TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE- TIMO_OUT0 #21 LE- TIMO_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20 | US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20 | PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 |
| 23 | PD14 | BUSCX BUSDY | TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE- TIMO_OUT0 #22 LE- TIMO_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21 | US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21 | CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4 |

| QFN48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 24 | PD15 | BUSCY BUSDX | TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE- TIM0_OUT0 #23 LE- TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22 | US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22 | CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2 |
| 25 | PA0 | ADC0_EXTN BUSCX BUSDY | TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31 | US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31 | CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 |
| 26 | PA1 | ADC0_EXTP BUSCY BUSDX | TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE- TIM0_OUT0 #1 LE- TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0 | US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0 | CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1 |
| 27 | PA2 | BUSCX BUSDY | TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 LE- TIM0_OUT0 #2 LE- TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1 | US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1 | PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2 |

| QFN48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|--|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 28 | PA3 | BUSCY BUSDX | TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 LE- TIM0_OUT0 #3 LE- TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2 | US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2 | PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 GPIO_EM4WU8 |
| 29 | PA4 | BUSCX BUSDY | TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 LE- TIM0_OUT0 #4 LE- TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3 | US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3 | PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4 |
| 30 | PA5 | BUSCY BUSDX | TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 LE- TIM0_OUT0 #5 LE- TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4 | US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4 | PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5 |
| 31 | PB11 | BUSCY BUSDX | TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE- TIM0_OUT0 #6 LE- TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5 | US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5 | PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6 |

| QFN48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|--|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 32 | PB12 | BUSCX BUSDY | TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE- TIM0_OUT0 #7 LE- TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6 | US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6 | PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7 |
| 33 | PB13 | BUSCY BUSDX | TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE- TIM0_OUT0 #8 LE- TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7 | US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7 | PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9 |
| 34 | AVDD | Analog power supply . | | | |
| 35 | PB14 | LFXTAL_N BUSCX BUSDY | TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 LE- TIM0_OUT0 #9 LE- TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8 | US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8 | CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9 |
| 36 | PB15 | LFXTAL_P BUSCY BUSDX | TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 LE- TIM0_OUT0 #10 LE- TIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9 | US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9 | CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10 |

| QFN48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|--|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 37 | VREGVSS | Voltage regulator VSS | | | |
| 38 | VREGSW | DCDC regulator switching node | | | |
| 39 | VREGVDD | Voltage regulator VDD input | | | |
| 40 | DVDD | Digital power supply . | | | |
| 41 | DECOUPLE | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. | | | |
| 42 | IOVDD | Digital IO power supply . | | | |
| 43 | PC6 | BUSAX BUSBY | TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 LE- TIM0_OUT0 #11 LE- TIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10 | US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10 | CMU_CLK0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11 |
| 44 | PC7 | BUSAY BUSBX | TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 LE- TIM0_OUT0 #12 LE- TIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11 | US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11 | CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12 |
| 45 | PC8 | BUSAX BUSBY | TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 LE- TIM0_OUT0 #13 LE- TIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12 | US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12 | PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13 |

| QFN48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 46 | PC9 | BUSAY BUSBX | TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE- TIMO_OUT0 #14 LE- TIMO_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13 | US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13 | PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14 |
| 47 | PC10 | BUSAX BUSBY | TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIMO_OUT0 #15 LE- TIMO_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14 | US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14 | CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12 |
| 48 | PC11 | BUSAY BUSBX | TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIMO_OUT0 #16 LE- TIMO_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15 | US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 | CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3 |

6.1.1 EFM32PG1 QFN48 with DC-DC GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters (A, B, C...), and the individual pins on each port are indicated by a number from 15 down to 0.

Table 6.2. QFN48 with DC-DC GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| Port A | - | - | - | - | - | - | - | - | - | - | PA5 (5V) | PA4 (5V) | PA3 (5V) | PA2 (5V) | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 (5V) | PB12 (5V) | PB11 (5V) | - | - | - | - | - | - | - | - | - | - | - |
| Port C | - | - | - | - | PC11 (5V) | PC10 (5V) | PC9 (5V) | PC8 (5V) | PC7 (5V) | PC6 (5V) | - | - | - | - | - | - |
| Port D | PD15 (5V) | PD14 (5V) | PD13 (5V) | PD12 (5V) | PD11 (5V) | PD10 (5V) | PD9 (5V) | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | PF7 (5V) | PF6 (5V) | PF5 (5V) | PF4 (5V) | PF3 (5V) | PF2 (5V) | PF1 (5V) | PF0 (5V) |

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PA4, PA3, PA2, PB13, PB12, PB11, PD15, PD14, and PD13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

6.2 EFM32PG1 QFN32 without DC-DC Definition

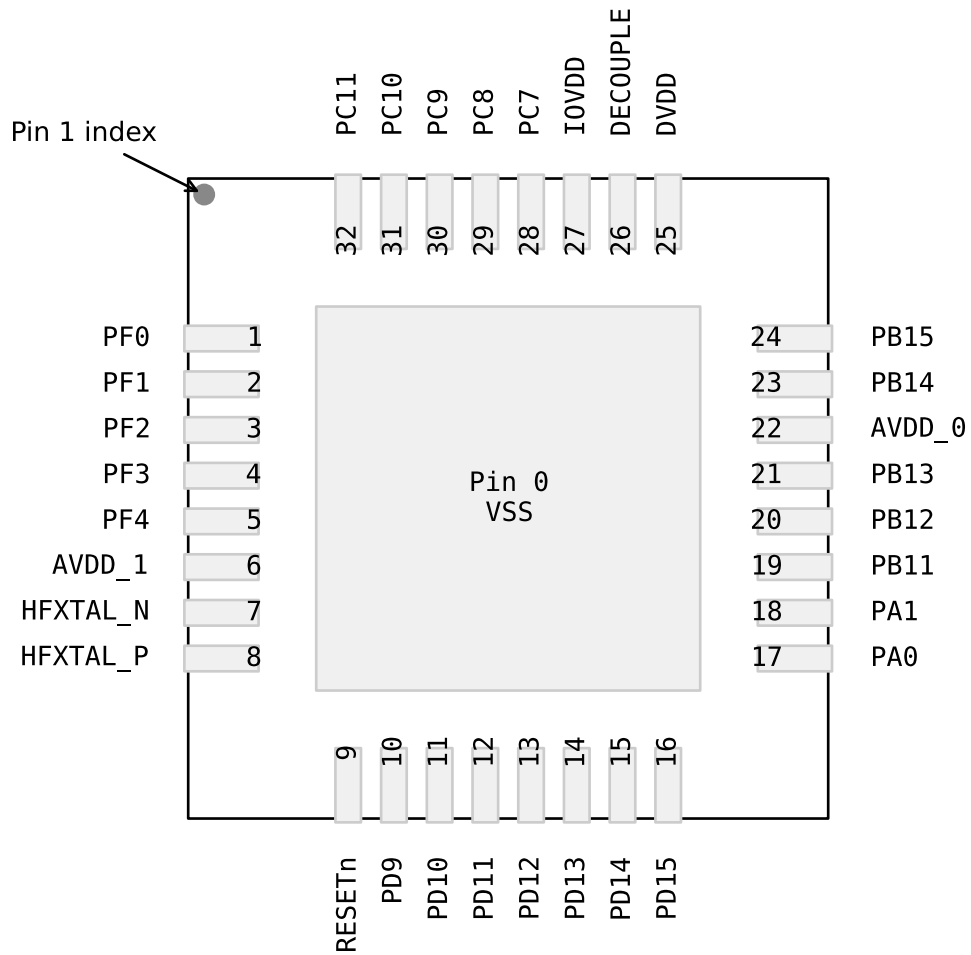


Figure 6.2. EFM32PG1 QFN32 without DC-DC Pinout

Table 6.3. QFN32 without DC-DC Device Pinout

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VREGVSS | Voltage regulator VSS | | | |
| 1 | PF0 | BUSAX BUSBY | TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LE- TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23 | US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23 | PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0 BOOT_TX |
| 2 | PF1 | BUSAY BUSBX | TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24 | US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24 | PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0 BOOT_RX |
| 3 | PF2 | BUSAX BUSBY | TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LE- TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25 | US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25 | CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | PF3 | BUSAY BUSBX | TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE- TIM0_OUT0 #27 LE- TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26 | US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26 | CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0 |
| 5 | PF4 | BUSAX BUSBY | TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE- TIM0_OUT0 #28 LE- TIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27 | US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27 | PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28 |
| 6 | AVDD | Analog power supply . | | | |
| 7 | HFXTAL_N | High Frequency Crystal input pin. | | | |
| 8 | HFXTAL_P | High Frequency Crystal output pin. | | | |
| 9 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 10 | PD9 | BUSCY BUSDX | TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 LE- TIM0_OUT0 #17 LE- TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16 | US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16 | CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 11 | PD10 | BUSCX BUSDY | TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 LE- TIM0_OUT0 #18 LE- TIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17 | US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17 | CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18 |
| 12 | PD11 | BUSCY BUSDX | TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 LE- TIM0_OUT0 #19 LE- TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18 | US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18 | PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19 |
| 13 | PD12 | BUSCX BUSDY | TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 LE- TIM0_OUT0 #20 LE- TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19 | US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19 | PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20 |
| 14 | PD13 | BUSCY BUSDX | TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE- TIM0_OUT0 #21 LE- TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20 | US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20 | PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 15 | PD14 | BUSCX BUSDY | TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE- TIM0_OUT0 #22 LE- TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21 | US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21 | CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4 |
| 16 | PD15 | BUSCY BUSDX | TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE- TIM0_OUT0 #23 LE- TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22 | US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22 | CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2 |
| 17 | PA0 | ADC0_EXTN BUSCX BUSDY | TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31 | US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31 | CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 |
| 18 | PA1 | ADC0_EXTP BUSCY BUSDX | TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE- TIM0_OUT0 #1 LE- TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0 | US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0 | CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 19 | PB11 | BUSCY BUSDX | TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE- TIM0_OUT0 #6 LE- TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5 | US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5 | PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6 |
| 20 | PB12 | BUSCX BUSDY | TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE- TIM0_OUT0 #7 LE- TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6 | US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6 | PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7 |
| 21 | PB13 | BUSCY BUSDX | TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE- TIM0_OUT0 #8 LE- TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7 | US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7 | PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9 |
| 22 | AVDD | Analog power supply . | | | |
| 23 | PB14 | LFXTAL_N BUSCX BUSDY | TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 LE- TIM0_OUT0 #9 LE- TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8 | US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8 | CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|--|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 24 | PB15 | LFXTAL_P BUSCY BUSDX | TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 LE- TIM0_OUT0 #10 LE- TIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9 | US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9 | CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10 |
| 25 | DVDD | Digital power supply . | | | |
| 26 | DECOUPLE | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. | | | |
| 27 | IOVDD | Digital IO power supply . | | | |
| 28 | PC7 | BUSAY BUSBX | TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 LE- TIM0_OUT0 #12 LE- TIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11 | US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11 | CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12 |
| 29 | PC8 | BUSAX BUSBY | TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 LE- TIM0_OUT0 #13 LE- TIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12 | US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12 | PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 30 | PC9 | BUSAY BUSBX | TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE- TIMO_OUT0 #14 LE- TIMO_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13 | US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13 | PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14 |
| 31 | PC10 | BUSAX BUSBY | TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIMO_OUT0 #15 LE- TIMO_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14 | US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14 | CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12 |
| 32 | PC11 | BUSAY BUSBX | TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIMO_OUT0 #16 LE- TIMO_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15 | US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 | CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3 |

6.2.1 EFM32PG1 QFN32 without DC-DC GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters (A, B, C...), and the individual pins on each port are indicated by a number from 15 down to 0.

Table 6.4. QFN32 without DC-DC GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|----------|-------|-------|----------|----------|----------|----------|----------|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 (5V) | PB12 (5V) | PB11 (5V) | - | - | - | - | - | - | - | - | - | - | - |
| Port C | - | - | - | - | PC11 (5V) | PC10 (5V) | PC9 (5V) | PC8 (5V) | PC7 (5V) | - | - | - | - | - | - | - |
| Port D | PD15 (5V) | PD14 (5V) | PD13 (5V) | PD12 (5V) | PD11 (5V) | PD10 (5V) | PD9 (5V) | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | PF4 (5V) | PF3 (5V) | PF2 (5V) | PF1 (5V) | PF0 (5V) |

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PB13, PB12, PB11, PD15, PD14, and PD13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

6.3 EFM32PG1 QFN32 with DC-DC Definition

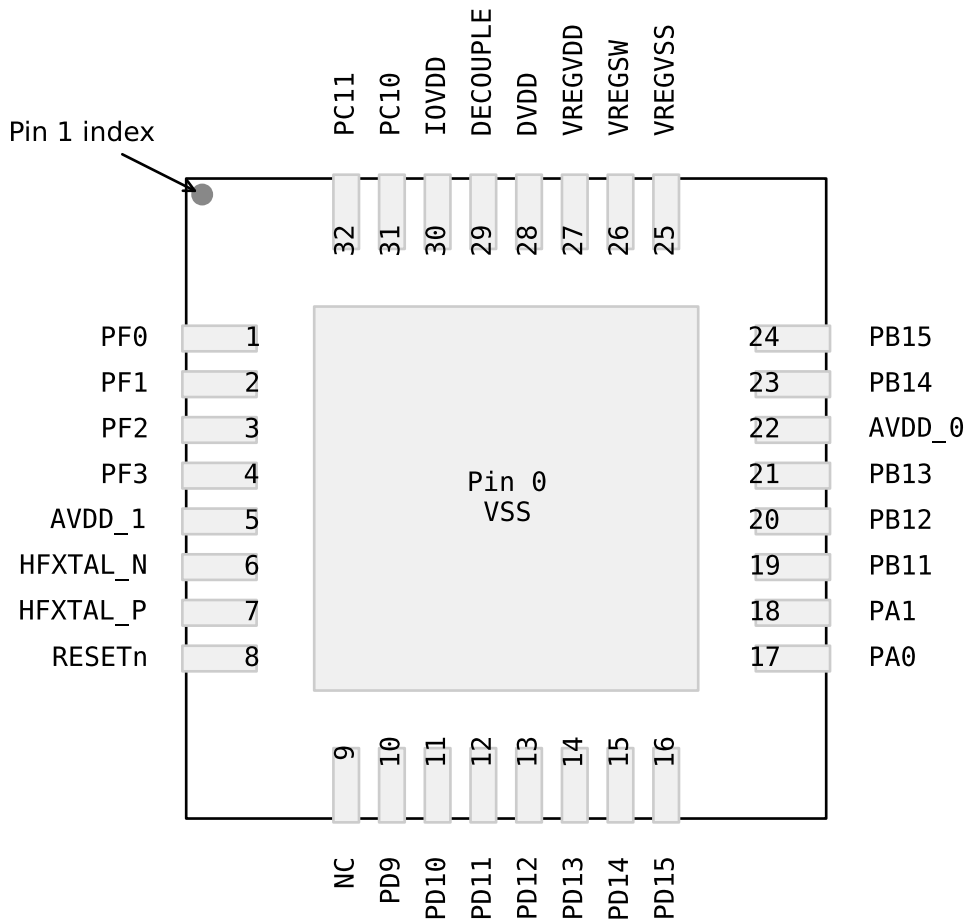


Figure 6.3. EFM32PG1 QFN32 with DC-DC Pinout

Table 6.5. QFN32 with DC-DC Device Pinout

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground | | | |
| 1 | PF0 | BUSAX BUSBY | TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LE- TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23 | US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23 | PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0 BOOT_TX |
| 2 | PF1 | BUSAY BUSBX | TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24 | US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24 | PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0 BOOT_RX |
| 3 | PF2 | BUSAX BUSBY | TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LE- TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25 | US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25 | CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | PF3 | BUSAY BUSBX | TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE- TIM0_OUT0 #27 LE- TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26 | US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26 | CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0 |
| 5 | AVDD | Analog power supply . | | | |
| 6 | HFXTAL_N | High Frequency Crystal input pin. | | | |
| 7 | HFXTAL_P | High Frequency Crystal output pin. | | | |
| 8 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 9 | NC | No Connect. | | | |
| 10 | PD9 | BUSCY BUSDX | TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 LE- TIM0_OUT0 #17 LE- TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16 | US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16 | CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17 |
| 11 | PD10 | BUSCX BUSDY | TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 LE- TIM0_OUT0 #18 LE- TIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17 | US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17 | CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 12 | PD11 | BUSCY BUSDX | TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 LE- TIM0_OUT0 #19 LE- TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18 | US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18 | PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19 |
| 13 | PD12 | BUSCX BUSDY | TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 LE- TIM0_OUT0 #20 LE- TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19 | US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19 | PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20 |
| 14 | PD13 | BUSCY BUSDX | TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE- TIM0_OUT0 #21 LE- TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20 | US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20 | PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 |
| 15 | PD14 | BUSCX BUSDY | TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE- TIM0_OUT0 #22 LE- TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21 | US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21 | CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 16 | PD15 | BUSCY BUSDX | TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE- TIM0_OUT0 #23 LE- TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22 | US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22 | CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2 |
| 17 | PA0 | ADC0_EXTN BUSCX BUSDY | TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31 | US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31 | CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 |
| 18 | PA1 | ADC0_EXTP BUSCY BUSDX | TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE- TIM0_OUT0 #1 LE- TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0 | US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0 | CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1 |
| 19 | PB11 | BUSCY BUSDX | TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE- TIM0_OUT0 #6 LE- TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5 | US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5 | PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|--|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 20 | PB12 | BUSCX BUSDY | TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE- TIM0_OUT0 #7 LE- TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6 | US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6 | PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7 |
| 21 | PB13 | BUSCY BUSDX | TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE- TIM0_OUT0 #8 LE- TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7 | US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7 | PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9 |
| 22 | AVDD | Analog power supply . | | | |
| 23 | PB14 | LFXTAL_N BUSCX BUSDY | TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 LE- TIM0_OUT0 #9 LE- TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8 | US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8 | CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9 |
| 24 | PB15 | LFXTAL_P BUSCY BUSDX | TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 LE- TIM0_OUT0 #10 LE- TIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9 | US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9 | CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|--|--|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 25 | VREGVSS | Voltage regulator VSS | | | |
| 26 | VREGSW | DCDC regulator switching node | | | |
| 27 | VREGVDD | Voltage regulator VDD input | | | |
| 28 | DVDD | Digital power supply . | | | |
| 29 | DECOUPLE | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. | | | |
| 30 | IOVDD | Digital IO power supply . | | | |
| 31 | PC10 | BUSAX BUSBY | TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIM0_OUT0 #15 LE- TIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14 | US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14 | CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12 |
| 32 | PC11 | BUSAY BUSBX | TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15 | US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 | CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3 |

6.3.1 EFM32PG1 QFN32 with DC-DC GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters (A, B, C...), and the individual pins on each port are indicated by a number from 15 down to 0.

Table 6.6. QFN32 with DC-DC GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|-----------|-----------|-----------|-----------|-----------|-----------|----------|-------|-------|-------|-------|-------|----------|----------|----------|----------|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PA1 | PA0 |
| Port B | PB15 | PB14 | PB13 (5V) | PB12 (5V) | PB11 (5V) | - | - | - | - | - | - | - | - | - | - | - |
| Port C | - | - | - | - | PC11 (5V) | PC10 (5V) | - | - | - | - | - | - | - | - | - | - |
| Port D | PD15 (5V) | PD14 (5V) | PD13 (5V) | PD12 (5V) | PD11 (5V) | PD10 (5V) | PD9 (5V) | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | PF3 (5V) | PF2 (5V) | PF1 (5V) | PF0 (5V) |

Note:

- GPIO with 5V tolerance are indicated by (5V).
- The pins PB13, PB12, PB11, PD15, PD14, and PD13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

6.4 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.7. Alternate functionality overview

| Alternate | LOCATION | | | | | | | | |
|---------------|--|--|---|---|---|--|--|--|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| ACMP0_O | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Analog comparator ACMP0, digital output. |
| ACMP1_O | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Analog comparator ACMP1, digital output. |
| ADC0_EXTN | 0: PA0 | | | | | | | | Analog to digital converter ADC0 external reference input negative pin |
| ADC0_EXTP | 0: PA1 | | | | | | | | Analog to digital converter ADC0 external reference input positive pin |
| BOOT_RX | 0: PF1 | | | | | | | | Bootloader RX |
| BOOT_TX | 0: PF0 | | | | | | | | Bootloader TX |
| CMU_CLK0 | 0: PA1 1: PB15 2: PC6 3: PC11 | 4: PD9 5: PD14 6: PF2 7: PF7 | | | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | 0: PA0 1: PB14 2: PC7 3: PC10 | 4: PD10 5: PD15 6: PF3 7: PF6 | | | | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLKTCK | 0: PF0 | | | | | | | | Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down. |

| Alternate | LOCATION | | | | | | | | Description |
|--------------|---|-------|--------|---------|---------|---------|---------|---------|--|
| | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | |
| DBG_SWDIOTMS | 0: PF1 | | | | | | | | <p>Debug-interface Serial Wire data input / output and JTAG Test Mode Select.</p> <p>Note that this function is enabled to the pin out of reset, and has a built-in pull up.</p> |
| DBG_SWO | 0: PF2 1: PB13 2: PD15 3: PC11 | | | | | | | | <p>Debug-interface Serial Wire viewer Output.</p> <p>Note that this function is not enabled after reset, and must be enabled by software to be used.</p> |
| DBG_TDI | 0: PF3 | | | | | | | | <p>Debug-interface JTAG Test Data In.</p> <p>Note that this function is enabled to pin out of reset, and has a built-in pull up.</p> |
| DBG_TDO | 0: PF2 | | | | | | | | <p>Debug-interface JTAG Test Data Out.</p> <p>Note that this function is enabled to pin out of reset.</p> |
| GPIO_EM4WU0 | 0: PF2 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | 0: PF7 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | 0: PD14 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU8 | 0: PA3 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU9 | 0: PB13 | | | | | | | | Pin can be used to wake the system up from EM4 |

| Alternate | LOCATION | | | | | | | | Description |
|--------------|--------------------------------------|---|---|--|---|--|--|--|---|
| | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | |
| GPIO_EM4WU12 | 0: PC10 | | | | | | | | Pin can be used to wake the system up from EM4 |
| I2C0_SCL | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | I2C0 Serial Data input / output. |
| LETIM0_OUT0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | LEUART0 Receive input. |
| LEU0_TX | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | 0: PB14 | | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | 0: PB15 | | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | 0: PF0 1: PF1 2: PF2 3: PF3 | 4: PF4 5: PF5 6: PF6 7: PF7 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 | | | | | Peripheral Reflex System PRS, channel 0. |

| Alternate | LOCATION | | | | | | | | |
|---------------|--|--|---|--|---|--|--|--|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| PRS_CH1 | 0: PF1 1: PF2 2: PF3 3: PF4 | 4: PF5 5: PF6 6: PF7 7: PF0 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | 0: PF2 1: PF3 2: PF4 3: PF5 | 4: PF6 5: PF7 6: PF0 7: PF1 | | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | 0: PF3 1: PF4 2: PF5 3: PF6 | 4: PF7 5: PF0 6: PF1 7: PF2 | 8: PD9 9: PD10 10: PD11 11: PD12 | 12: PD13 13: PD14 14: PD15 | | | | | Peripheral Reflex System PRS, channel 3. |
| PRS_CH4 | 0: PD9 1: PD10 2: PD11 3: PD12 | 4: PD13 5: PD14 6: PD15 | | | | | | | Peripheral Reflex System PRS, channel 4. |
| PRS_CH5 | 0: PD10 1: PD11 2: PD12 3: PD13 | 4: PD14 5: PD15 6: PD9 | | | | | | | Peripheral Reflex System PRS, channel 5. |
| PRS_CH6 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PD9 | 12: PD10 13: PD11 14: PD12 15: PD13 | 16: PD14 17: PD15 | | | | Peripheral Reflex System PRS, channel 6. |
| PRS_CH7 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PA0 | | | | | | Peripheral Reflex System PRS, channel 7. |
| PRS_CH8 | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PA0 10: PA1 | | | | | | Peripheral Reflex System PRS, channel 8. |
| PRS_CH9 | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PA0 9: PA1 10: PA2 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 | | | | Peripheral Reflex System PRS, channel 9. |
| PRS_CH10 | 0: PC6 1: PC7 2: PC8 3: PC9 | 4: PC10 5: PC11 | | | | | | | Peripheral Reflex System PRS, channel 10. |
| PRS_CH11 | 0: PC7 1: PC8 2: PC9 3: PC10 | 4: PC11 5: PC6 | | | | | | | Peripheral Reflex System PRS, channel 11. |
| TIM0_CC0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Timer 0 Capture Compare input / output channel 1. |

| Alternate | LOCATION | | | | | | | | |
|---------------|---|--|---|---|--|--|--|--|--|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| TIM0_CC2 | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDT10 | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDT11 | 0: PA4 1: PA5 2: PB11 3: PB12 | 4: PB13 5: PB14 6: PB15 7: PC6 | 8: PC7 9: PC8 10: PC9 11: PC10 | 12: PC11 13: PD9 14: PD10 15: PD11 | 16: PD12 17: PD13 18: PD14 19: PD15 | 20: PF0 21: PF1 22: PF2 23: PF3 | 24: PF4 25: PF5 26: PF6 27: PF7 | 28: PA0 29: PA1 30: PA2 31: PA3 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDT12 | 0: PA5 1: PB11 2: PB12 3: PB13 | 4: PB14 5: PB15 6: PC6 7: PC7 | 8: PC8 9: PC9 10: PC10 11: PC11 | 12: PD9 13: PD10 14: PD11 15: PD12 | 16: PD13 17: PD14 18: PD15 19: PF0 | 20: PF1 21: PF2 22: PF3 23: PF4 | 24: PF5 25: PF6 26: PF7 27: PA0 | 28: PA1 29: PA2 30: PA3 31: PA4 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | Timer 1 Capture Compare input / output channel 2. |
| TIM1_CC3 | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | Timer 1 Capture Compare input / output channel 3. |
| US0_CLK | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | USART0 clock input / output. |
| US0_CS | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | USART0 chip select input / output. |
| US0_CTS | 0: PA4 1: PA5 2: PB11 3: PB12 | 4: PB13 5: PB14 6: PB15 7: PC6 | 8: PC7 9: PC8 10: PC9 11: PC10 | 12: PC11 13: PD9 14: PD10 15: PD11 | 16: PD12 17: PD13 18: PD14 19: PD15 | 20: PF0 21: PF1 22: PF2 23: PF3 | 24: PF4 25: PF5 26: PF6 27: PF7 | 28: PA0 29: PA1 30: PA2 31: PA3 | USART0 Clear To Send hardware flow control input. |
| US0_RTS | 0: PA5 1: PB11 2: PB12 3: PB13 | 4: PB14 5: PB15 6: PC6 7: PC7 | 8: PC8 9: PC9 10: PC10 11: PC11 | 12: PD9 13: PD10 14: PD11 15: PD12 | 16: PD13 17: PD14 18: PD15 19: PF0 | 20: PF1 21: PF2 22: PF3 23: PF4 | 24: PF5 25: PF6 26: PF7 27: PA0 | 28: PA1 29: PA2 30: PA3 31: PA4 | USART0 Request To Send hardware flow control output. |

| Alternate | LOCATION | | | | | | | | |
|---------------|---|--|---|---|--|--|--|--|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| US0_RX | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | 0: PA2 1: PA3 2: PA4 3: PA5 | 4: PB11 5: PB12 6: PB13 7: PB14 | 8: PB15 9: PC6 10: PC7 11: PC8 | 12: PC9 13: PC10 14: PC11 15: PD9 | 16: PD10 17: PD11 18: PD12 19: PD13 | 20: PD14 21: PD15 22: PF0 23: PF1 | 24: PF2 25: PF3 26: PF4 27: PF5 | 28: PF6 29: PF7 30: PA0 31: PA1 | USART1 clock input / output. |
| US1_CS | 0: PA3 1: PA4 2: PA5 3: PB11 | 4: PB12 5: PB13 6: PB14 7: PB15 | 8: PC6 9: PC7 10: PC8 11: PC9 | 12: PC10 13: PC11 14: PD9 15: PD10 | 16: PD11 17: PD12 18: PD13 19: PD14 | 20: PD15 21: PF0 22: PF1 23: PF2 | 24: PF3 25: PF4 26: PF5 27: PF6 | 28: PF7 29: PA0 30: PA1 31: PA2 | USART1 chip select input / output. |
| US1_CTS | 0: PA4 1: PA5 2: PB11 3: PB12 | 4: PB13 5: PB14 6: PB15 7: PC6 | 8: PC7 9: PC8 10: PC9 11: PC10 | 12: PC11 13: PD9 14: PD10 15: PD11 | 16: PD12 17: PD13 18: PD14 19: PD15 | 20: PF0 21: PF1 22: PF2 23: PF3 | 24: PF4 25: PF5 26: PF6 27: PF7 | 28: PA0 29: PA1 30: PA2 31: PA3 | USART1 Clear To Send hardware flow control input. |
| US1_RTS | 0: PA5 1: PB11 2: PB12 3: PB13 | 4: PB14 5: PB15 6: PC6 7: PC7 | 8: PC8 9: PC9 10: PC10 11: PC11 | 12: PD9 13: PD10 14: PD11 15: PD12 | 16: PD13 17: PD14 18: PD15 19: PF0 | 20: PF1 21: PF2 22: PF3 23: PF4 | 24: PF5 25: PF6 26: PF7 27: PA0 | 28: PA1 29: PA2 30: PA3 31: PA4 | USART1 Request To Send hardware flow control output. |
| US1_RX | 0: PA1 1: PA2 2: PA3 3: PA4 | 4: PA5 5: PB11 6: PB12 7: PB13 | 8: PB14 9: PB15 10: PC6 11: PC7 | 12: PC8 13: PC9 14: PC10 15: PC11 | 16: PD9 17: PD10 18: PD11 19: PD12 | 20: PD13 21: PD14 22: PD15 23: PF0 | 24: PF1 25: PF2 26: PF3 27: PF4 | 28: PF5 29: PF6 30: PF7 31: PA0 | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | 0: PA0 1: PA1 2: PA2 3: PA3 | 4: PA4 5: PA5 6: PB11 7: PB12 | 8: PB13 9: PB14 10: PB15 11: PC6 | 12: PC7 13: PC8 14: PC9 15: PC10 | 16: PC11 17: PD9 18: PD10 19: PD11 | 20: PD12 21: PD13 22: PD14 23: PD15 | 24: PF0 25: PF1 26: PF2 27: PF3 | 28: PF4 29: PF5 30: PF6 31: PF7 | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

6.5 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. A complete description of APORT functionality can be found in the Reference Manual.

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 6.8. ACMP0 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | Port |
|---------|---------|---------|---------|---------|---------|---------|---------|------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | Bus |
| | PB15 | PB15 | | | | | | CH31 |
| PB14 | | | PB14 | | | | | CH30 |
| | PB13 | PB13 | | | | | | CH29 |
| PB12 | | | PB12 | | | | | CH28 |
| | PB11 | PB11 | | | | | | CH27 |
| | | | | | | | | CH26 |
| | | | | | | | | CH25 |
| | | | | | | | | CH24 |
| | | | | | PF7 | PF7 | | CH23 |
| | | | | PF6 | | | PF6 | CH22 |
| | | | | | PF5 | PF5 | | CH21 |
| | | | | PF4 | | | PF4 | CH20 |
| | | | | | PF3 | PF3 | | CH19 |
| | | | | PF2 | | | PF2 | CH18 |
| | | | | | PF1 | PF1 | | CH17 |
| | | | | PF0 | | | PF0 | CH16 |
| | | | | | | | | CH15 |
| | | | | | | | | CH14 |
| | PA5 | PA5 | | | | | | CH13 |
| PA4 | | | PA4 | | | | | CH12 |
| | PA3 | PA3 | | | PC11 | PC11 | | CH11 |
| PA2 | | | PA2 | PC10 | | | PC10 | CH10 |
| | PA1 | PA1 | | | PC9 | PC9 | | CH9 |
| PA0 | | | PA0 | PC8 | | | PC8 | CH8 |
| | PD15 | PD15 | | | PC7 | PC7 | | CH7 |
| PD14 | | | PD14 | PC6 | | | PC6 | CH6 |
| | PD13 | PD13 | | | | | | CH5 |
| PD12 | | | PD12 | | | | | CH4 |
| | PD11 | PD11 | | | | | | CH3 |
| PD10 | | | PD10 | | | | | CH2 |
| | PD9 | PD9 | | | | | | CH1 |
| | | | | | | | | CH0 |

Table 6.9. ACMP1 Bus and Pin Mapping

| APORT4Y | APORT4X | APORT3Y | APORT3X | APORT2Y | APORT2X | APORT1Y | APORT1X | Port |
|---------|---------|---------|---------|---------|---------|---------|---------|------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | Bus |
| | PB15 | PB15 | | | | | | CH31 |
| | | | PB14 | | | | | CH30 |
| | PB13 | PB13 | | | | | | CH29 |
| | | | PB12 | | | | | CH28 |
| | PB11 | PB11 | | | | | | CH27 |
| | | | | | | | | CH26 |
| | | | | | | | | CH25 |
| | | | | | | | | CH24 |
| | | | | | PF7 | PF7 | | CH23 |
| | | | | PF6 | | | PF6 | CH22 |
| | | | | | PF5 | PF5 | | CH21 |
| | | | | PF4 | | | PF4 | CH20 |
| | | | | | PF3 | PF3 | | CH19 |
| | | | | PF2 | | | PF2 | CH18 |
| | | | | | PF1 | PF1 | | CH17 |
| | | | | PF0 | | | PF0 | CH16 |
| | | | | | | | | CH15 |
| | | | | | | | | CH14 |
| | PA5 | PA5 | | | | | | CH13 |
| | | | PA4 | | | | | CH12 |
| | PA3 | PA3 | | | PC11 | PC11 | | CH11 |
| | | | PA2 | PC10 | | | PC10 | CH10 |
| | PA1 | PA1 | | | PC9 | PC9 | | CH9 |
| | | | PA0 | PC8 | | | PC8 | CH8 |
| | PD15 | PD15 | | | PC7 | PC7 | | CH7 |
| | | | PD14 | PC6 | | | PC6 | CH6 |
| | | | | | | | | CH5 |
| | PD13 | PD13 | | | | | | CH4 |
| | | | PD12 | | | | | CH3 |
| | PD11 | PD11 | | | | | | CH2 |
| | | | PD10 | | | | | CH1 |
| | PD9 | PD9 | | | | | | CH0 |

Table 6.10. ADC0 Bus and Pin Mapping

| APORT4Y | | APORT4X | | APORT3Y | | APORT3X | | APORT2Y | | APORT2X | | APORT1Y | | APORT1X | | Port |
|---------|-------|---------|-------|---------|-------|---------|-------|---------|--|---------|--|---------|--|---------|--|------|
| BUSDY | BUSDX | BUSCY | BUSCX | BUSBY | BUSBX | BUSAY | BUSAX | Bus | | | | | | | | |
| | PB15 | PB15 | | | | | | CH31 | | | | | | | | |
| PB14 | | | PB14 | | | | | CH30 | | | | | | | | |
| | PB13 | PB13 | | | | | | CH29 | | | | | | | | |
| PB12 | | | PB12 | | | | | CH28 | | | | | | | | |
| | PB11 | PB11 | | | | | | CH27 | | | | | | | | |
| | | | | | | | | CH26 | | | | | | | | |
| | | | | | | | | CH25 | | | | | | | | |
| | | | | | | | | CH24 | | | | | | | | |
| | | | | | PF7 | PF7 | | CH23 | | | | | | | | |
| | | | | PF6 | | | PF6 | CH22 | | | | | | | | |
| | | | | | PF5 | PF5 | | CH21 | | | | | | | | |
| | | | | PF4 | | | PF4 | CH20 | | | | | | | | |
| | | | | | PF3 | PF3 | | CH19 | | | | | | | | |
| | | | | PF2 | | | PF2 | CH18 | | | | | | | | |
| | | | | | PF1 | PF1 | | CH17 | | | | | | | | |
| | | | | PF0 | | | PF0 | CH16 | | | | | | | | |
| | | | | | | | | CH15 | | | | | | | | |
| | | | | | | | | CH14 | | | | | | | | |
| | PA5 | PA5 | | | | | | CH13 | | | | | | | | |
| | | | PA4 | | | | | CH12 | | | | | | | | |
| | PA3 | PA3 | | | PC11 | PC11 | | CH11 | | | | | | | | |
| PA2 | | | PA2 | PC10 | | | PC10 | CH10 | | | | | | | | |
| | PA1 | PA1 | | | PC9 | PC9 | | CH9 | | | | | | | | |
| PA0 | | | PA0 | PC8 | | | PC8 | CH8 | | | | | | | | |
| | PD15 | PD15 | | | PC7 | PC7 | | CH7 | | | | | | | | |
| PD14 | | | PD14 | PC6 | | | PC6 | CH6 | | | | | | | | |
| | PD13 | PD13 | | | | | | CH5 | | | | | | | | |
| PD12 | | | PD12 | | | | | CH4 | | | | | | | | |
| | PD11 | PD11 | | | | | | CH3 | | | | | | | | |
| PD10 | | | PD10 | | | | | CH2 | | | | | | | | |
| | PD9 | PD9 | | | | | | CH1 | | | | | | | | |
| | | | | | | | | CH0 | | | | | | | | |

Table 6.11. IDAC0 Bus and Pin Mapping

| APORT1Y | | APORT1X | | Port |
|---------|-------|---------|--|------|
| BUSCY | BUSCX | Bus | | |
| PB15 | | CH31 | | |
| | PB14 | CH30 | | |
| PB13 | | CH29 | | |
| | PB12 | CH28 | | |
| PB11 | | CH27 | | |
| | | CH26 | | |
| | | CH25 | | |
| | | CH24 | | |
| | | CH23 | | |
| | | CH22 | | |
| | | CH21 | | |
| | | CH20 | | |
| | | CH19 | | |
| | | CH18 | | |
| | | CH17 | | |
| | | CH16 | | |
| | | CH15 | | |
| | | CH14 | | |
| PA5 | | CH13 | | |
| | PA4 | CH12 | | |
| PA3 | | CH11 | | |
| | PA2 | CH10 | | |
| PA1 | | CH9 | | |
| | PA0 | CH8 | | |
| PD15 | | CH7 | | |
| | PD14 | CH6 | | |
| PD13 | | CH5 | | |
| | PD12 | CH4 | | |
| PD11 | | CH3 | | |
| | PD10 | CH2 | | |
| PD9 | | CH1 | | |
| | | CH0 | | |

7. QFN48 Package Specifications

7.1 QFN48 Package Dimensions

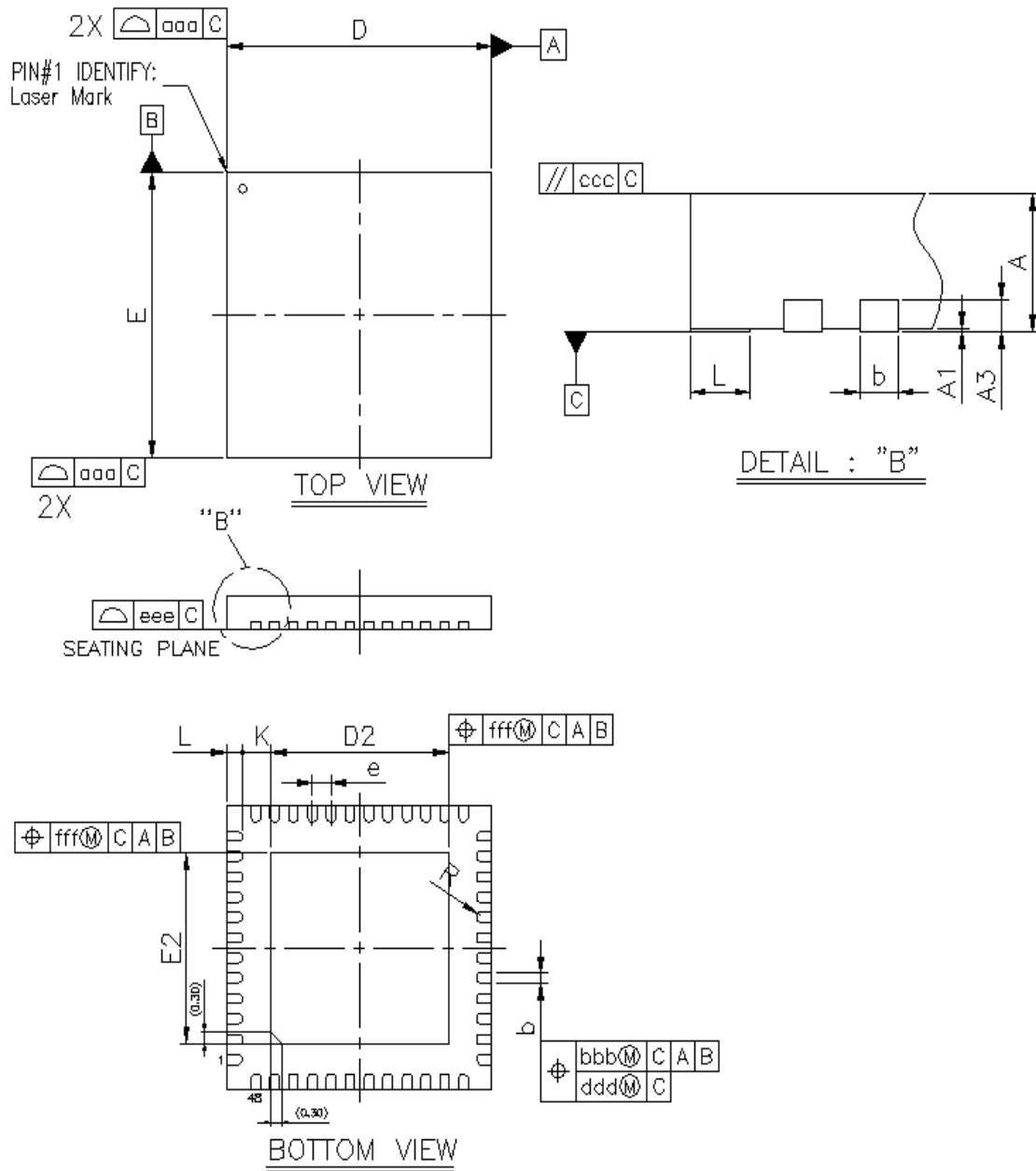


Figure 7.1. QFN48 Package Drawing

Table 7.1. QFN48 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.18 | 0.25 | 0.30 |
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| D2 | 4.60 | 4.70 | 4.80 |
| E2 | 4.60 | 4.70 | 4.80 |
| e | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| R | 0.09 | — | 0.14 |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN48 PCB Land Pattern

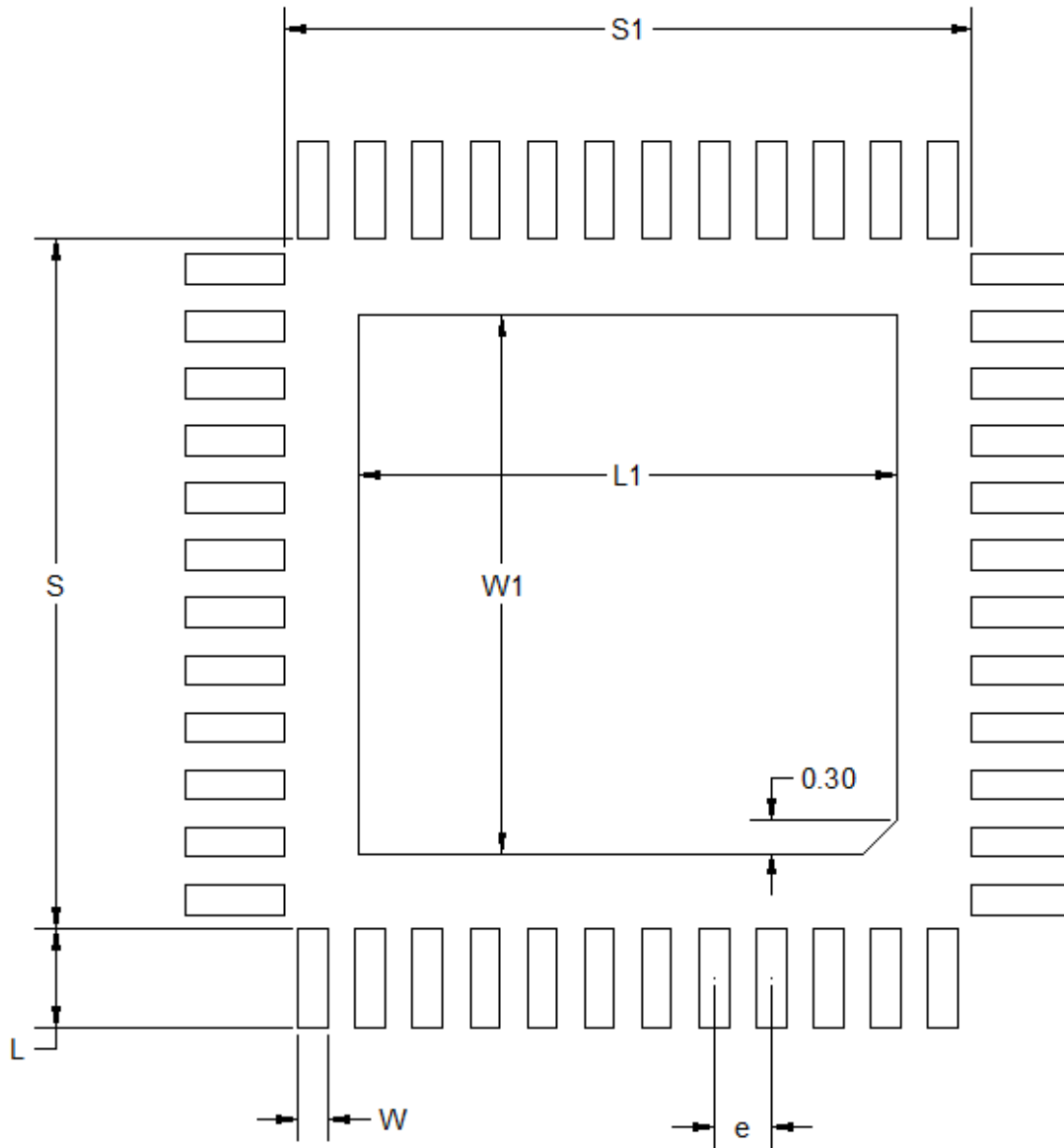


Figure 7.2. QFN48 PCB Land Pattern Drawing

Table 7.2. QFN48 PCB Land Pattern Dimensions

| Dimension | Typ |
|-----------|------|
| S1 | 6.01 |
| S | 6.01 |
| L1 | 4.70 |
| W1 | 4.70 |
| e | 0.50 |
| W | 0.26 |
| L | 0.86 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 4x4 array of 0.75 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Note: Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

7.3 QFN48 Package Marking



Figure 7.3. QFN48 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – Reserved for future use. Current value is 0.

8. QFN32 Package Specifications

8.1 QFN32 Package Dimensions

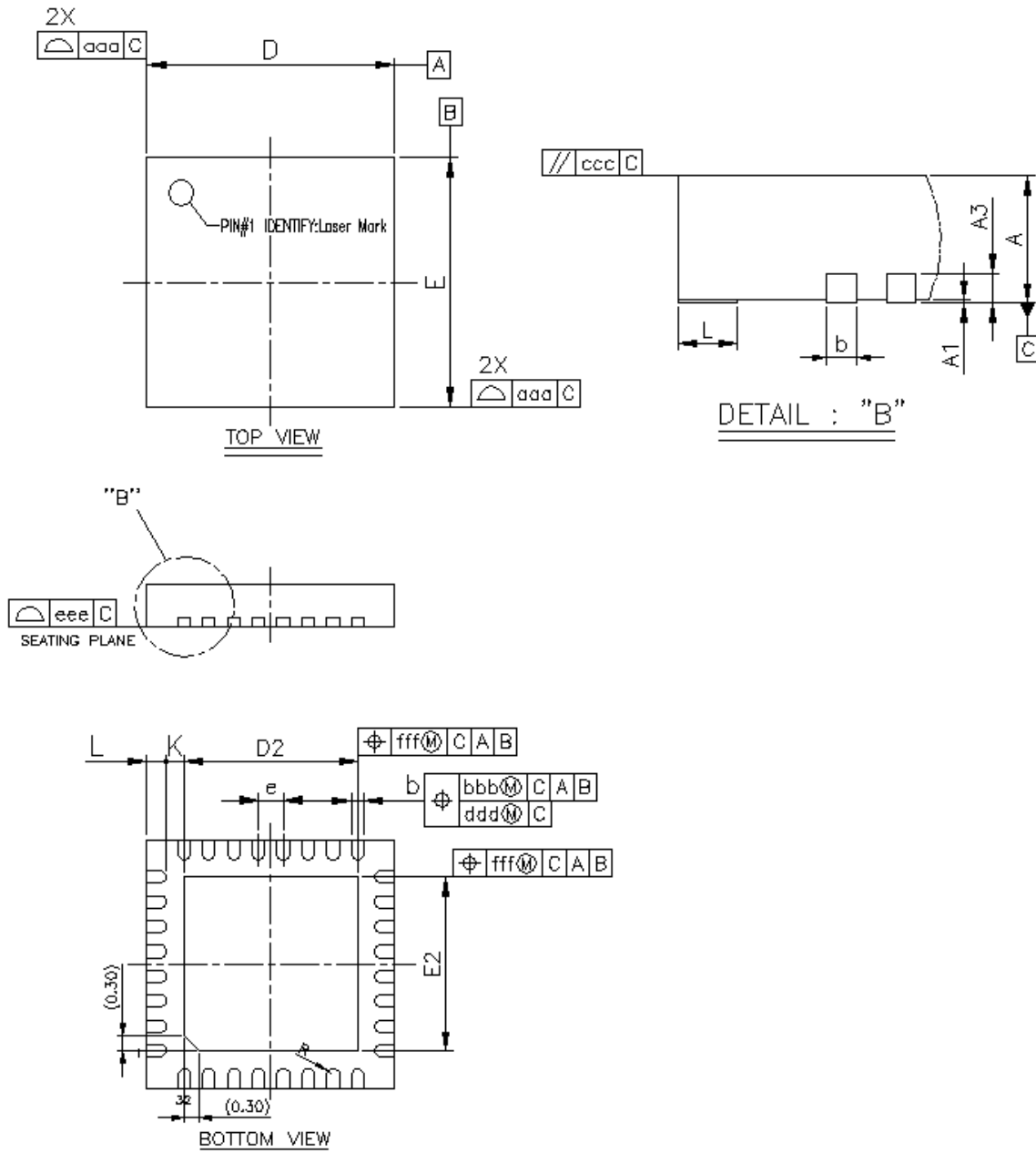


Figure 8.1. QFN32 Package Drawing

Table 8.1. QFN32 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.18 | 0.25 | 0.30 |
| D/E | 4.90 | 5.00 | 5.10 |
| D2/E2 | 3.40 | 3.50 | 3.60 |
| E | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| R | 0.09 | — | 0.14 |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN32 PCB Land Pattern

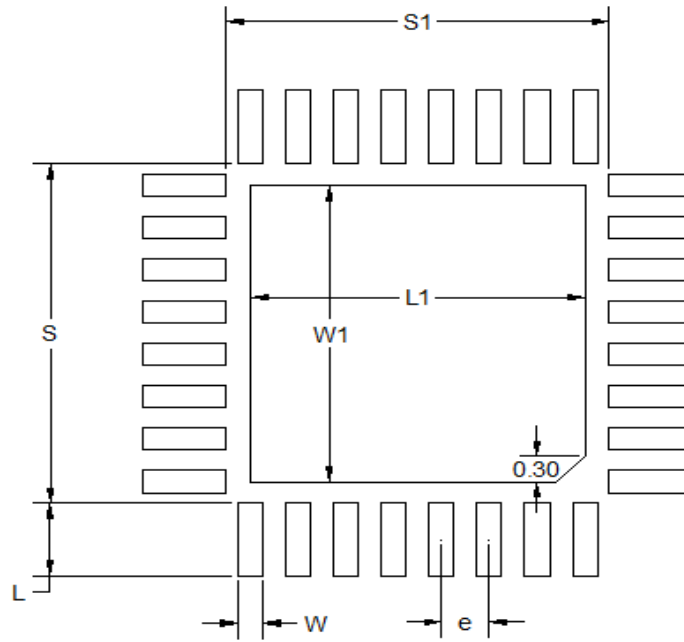


Figure 8.2. QFN32 PCB Land Pattern Drawing

Table 8.2. QFN32 PCB Land Pattern Dimensions

| Dimension | Typ |
|-----------|------|
| S1 | 4.01 |
| S | 4.01 |
| L1 | 3.50 |
| W1 | 3.50 |
| e | 0.50 |
| W | 0.26 |
| L | 0.86 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 3x3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Note: Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

8.3 QFN32 Package Marking



Figure 8.3. QFN32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
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- # – Reserved for future use. Current value is 0.

9. Revision History

9.1 Revision 1.2

June, 2022

- In the front page block diagram, updated the lowest energy mode for LETIMER.
- Updated [3.5.2 Real Time Counter and Calendar \(RTCC\)](#) to remove AUXHFRCO as a clock source.
- Updated [3.5.3 Low Energy Timer \(LETIMER\)](#) lowest energy mode.
- Added [3.10.4 Bootloader](#) section to the System Overview.
- Added timing specifications for RESETn low time and clarified V_{IL} and V_{IH} logic levels for RESETn pins in [Table 4.16 GPIO on page 28](#).
- Removed BIASPROG = 1, FULLBIAS = 0 specifications from [4.1.14 Analog Comparator \(ACMP\)](#).
- Added [Figure 4.2 SPI Master Timing Diagram \(SMSDELAY = 1\)](#) on page 40.
- Added a note to [Table 7.2 QFN48 PCB Land Pattern Dimensions on page 93](#) and [Table 8.2 QFN32 PCB Land Pattern Dimensions on page 98](#).

9.2 Revision 1.1

2016-Oct-26

- System Overview Sections: Minor wording and typographical error fixes.
- Electrical Characteristics: Minor wording and typographical error fixes.
- "HFRCO and AUXHFRCO" table in Electrical Characteristics: f_HFRCO symbol changed to f_HFRCO_ACC.
- Pinout tables: APORT channel details removed from "Analog" column. This information is now found in the APORT client map sections.
- Updated APORT client map sections.

9.3 Revision 1.0

2016-Jul-22

- Electrical Characteristics: Minimum and maximum value statement changed to cover full operating temperature range.
- Finalized Specification Tables. Tables with condition/min/typ/max or footnote changes include:
 - Absolute Maximum Ratings
 - General Operating Conditions
 - DC-DC Converter
 - LFRCO
 - HFRCO and AUXHFRCO
 - ADC
 - IDAC
- Updated Typical Performance Graphs.
- Added note for 5V tolerance to pinout GPIO Overview sections.
- Updated OPN decoder with latest revision.
- Updated Package Marking text with latest descriptions.

9.4 Revision 0.95

2016-04-11

- All OPNs changed to rev C0.
- Electrical specification tables updated with latest characterization data and production test limits.

9.5 Revision 0.31

- Engineering samples note added to ordering information table.

9.6 Revision 0.3

- Re-formatted ordering information table and OPN decoder.
- Removed extraneous sections from dc-dc from system overview.
- Updated table formatting for electrical specifications.
- Updated electrical specifications with latest available data.
- Added I2C and USART SPI timing tables.
- Moved dc-dc graph to typical performance curves.
- Updated APORT tables and APORT references to correct nomenclature.
- Updated top marking description.

9.7 Revision 0.2

Updated ordering table.

Changed "1.62 V to 3.8 V Single Power Supply" to "1.62 V to 3.8 V Power Supply" in the Feature List.

9.8 Revision 0.1

Initial release.

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