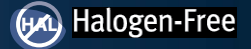




# EPC2214 – Automotive 80 V (D-S) Enhancement Mode Power Transistor

 $V_{DS}, 80\text{ V}$ 
 $R_{DS(on)}, 20\text{ m}\Omega$ 
 $I_D, 10\text{ A}$ 

AEC-Q101



Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

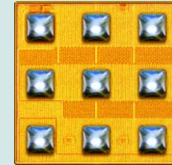
## Maximum Ratings

PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	80	V
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ )	10	A
	Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300\ \mu\text{s}$ )	47	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	

## Thermal Characteristics

PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.7	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	7.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	81	

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details



EPC2214 eGaN® FETs are supplied only in passivated die form with solder bumps  
Die Size: 1.35 mm x 1.35 mm

## Applications

- Lidar/Pulsed Power Applications
- DC-DC Conversion
- Wireless Power Transfer

## Benefits

- Ultra High Efficiency
- Ultra Low  $R_{DS(on)}$
- Ultra Low  $Q_G$
- Ultra Small Footprint

## Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 0.2\text{ mA}$	80			V
$I_{DSS}$	Drain-Source Leakage	$V_{DS} = 64\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$		0.003	0.15	mA
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}, T_J = 25^\circ\text{C}$		0.003	1.1	mA
	Gate-to-Source Forward Leakage <sup>#</sup>	$V_{GS} = 5\text{ V}, T_J = 125^\circ\text{C}$		0.01	2.5	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}, T_J = 25^\circ\text{C}$		0.003	0.15	mA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 2\text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 6\text{ A}$		15	20	m $\Omega$
$V_{SD}$	Source-Drain Forward Voltage	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$		1.9		V

<sup>#</sup> Defined by design. Not subject to production test.

Dynamic Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{ISS}$	Input Capacitance <sup>#</sup>	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		198	238	pF
$C_{RSS}$	Reverse Transfer Capacitance			1.8		
$C_{OSS}$	Output Capacitance <sup>#</sup>			129	194	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }40\text{ V}, V_{GS} = 0\text{ V}$		171		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			211		
$R_G$	Gate Resistance			0.65		$\Omega$
$Q_G$	Total Gate Charge <sup>#</sup>	$V_{DS} = 40\text{ V}, V_{GS} = 5\text{ V}, I_D = 6\text{ A}$		1.8	2.2	nC
$Q_{GS}$	Gate to Source Charge	$V_{DS} = 40\text{ V}, I_D = 6\text{ A}$		0.5		
$Q_{GD}$	Gate to Drain Charge			0.3		
$Q_{G(TH)}$	Gate Charge at Threshold			0.4		
$Q_{OSS}$	Output Charge <sup>#</sup>	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		8	12	
$Q_{RR}$	Source-Drain Recovery Charge			0		

# Defined by design. Not subject to production test.

Note 2:  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Note 3:  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Figure 1: Typical Output Characteristics at 25°C

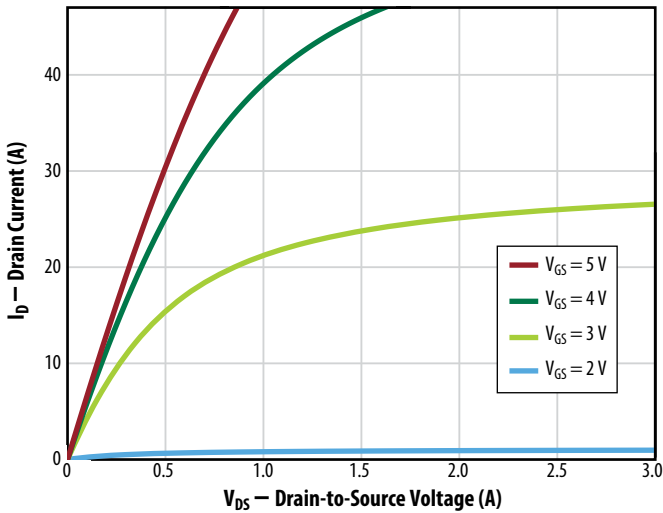


Figure 2: Transfer Characteristics

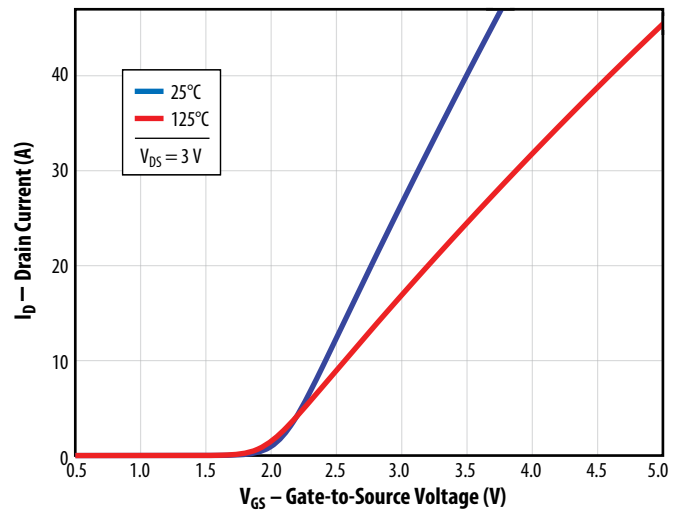


Figure 3:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

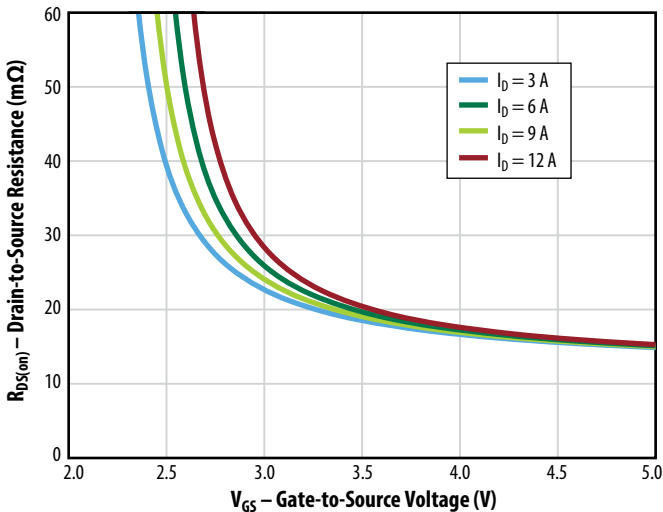


Figure 4:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

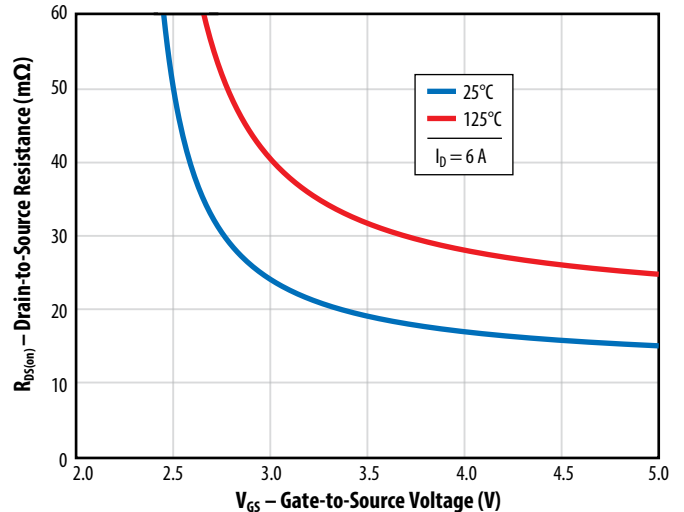


Figure 5a: Capacitance (Linear Scale)

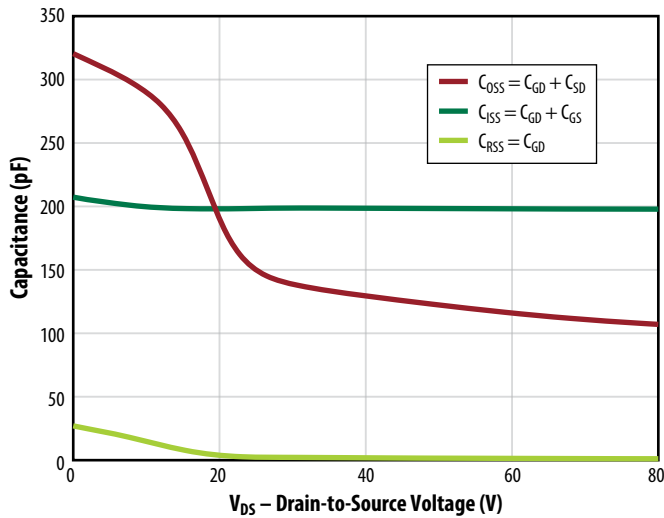


Figure 5b: Capacitance (Log Scale)

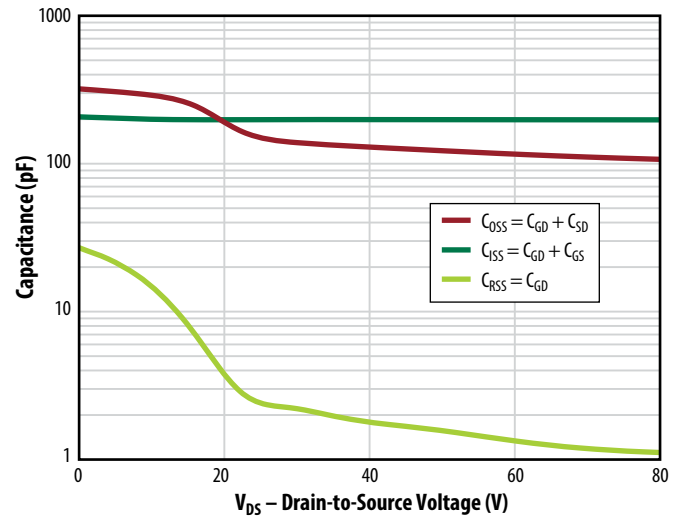


Figure 6: Output Charge and C<sub>OSS</sub> Stored Energy

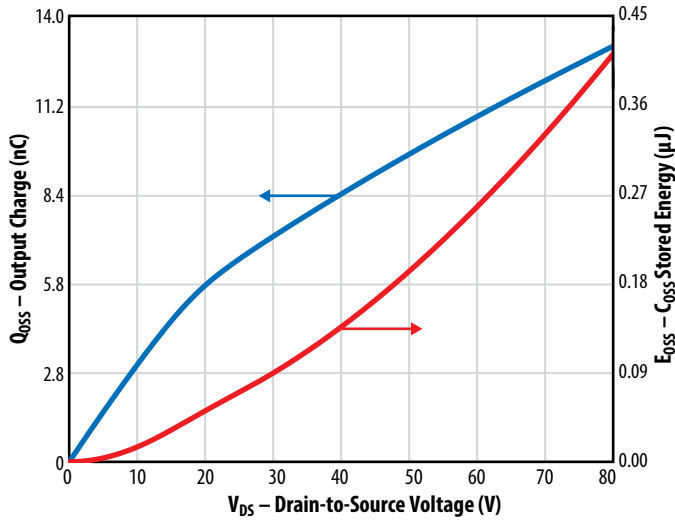


Figure 7: Gate Charge

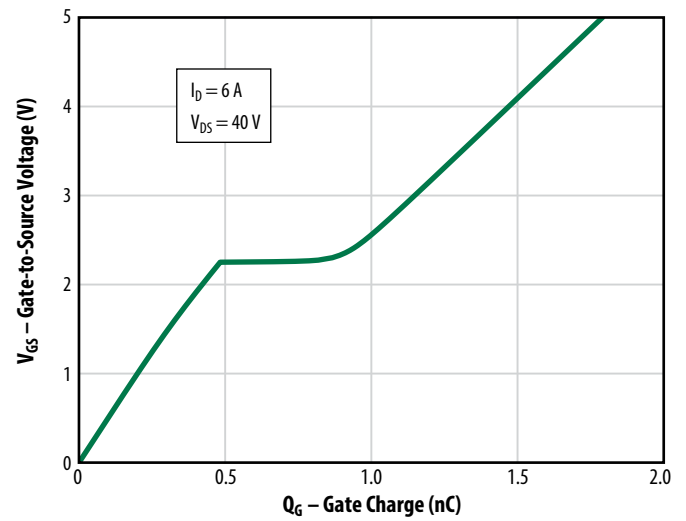


Figure 8: Reverse Drain-Source Characteristics

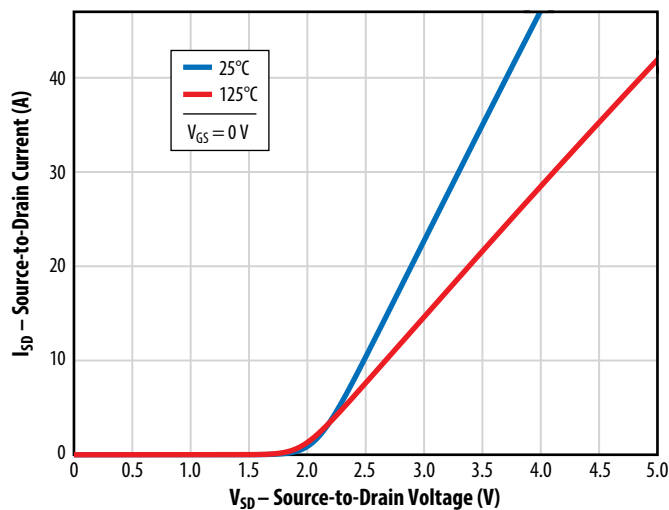
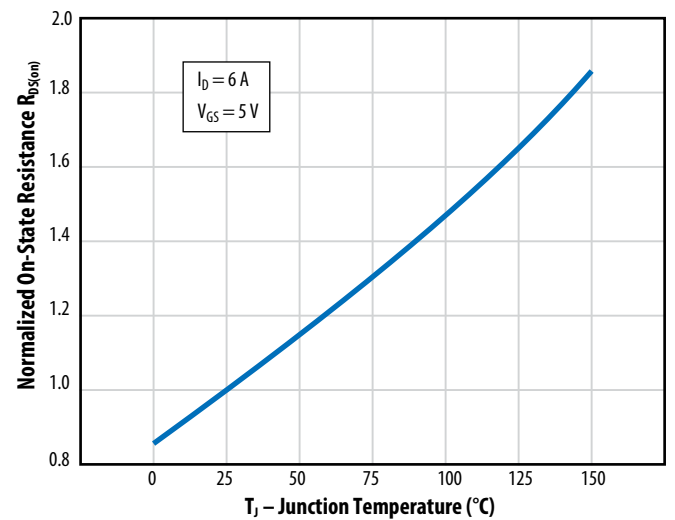


Figure 9: Normalized On-State Resistance vs. Temperature



All measurements were done with substrate shorted to source.

Figure 10: Normalized Threshold Voltage vs. Temperature

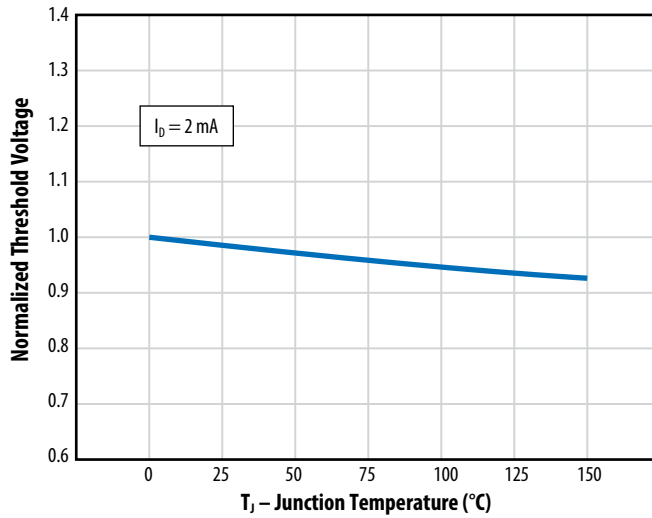


Figure 11: Transient Thermal Response Curves

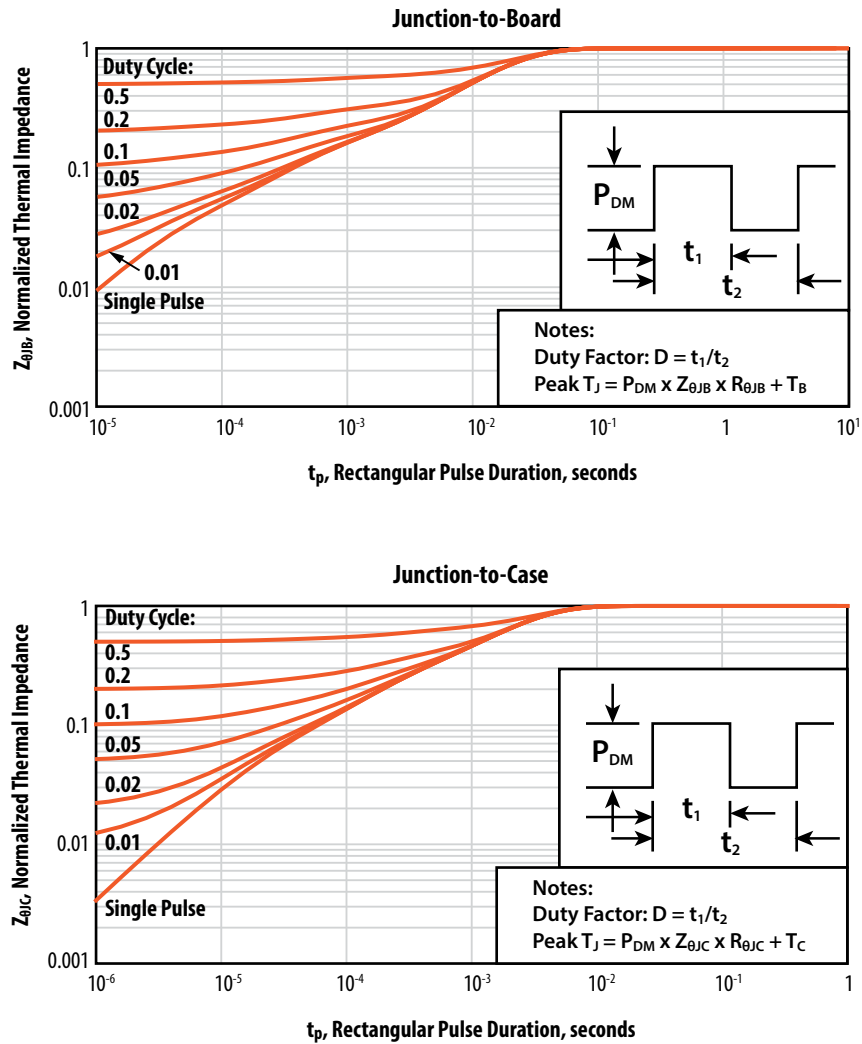
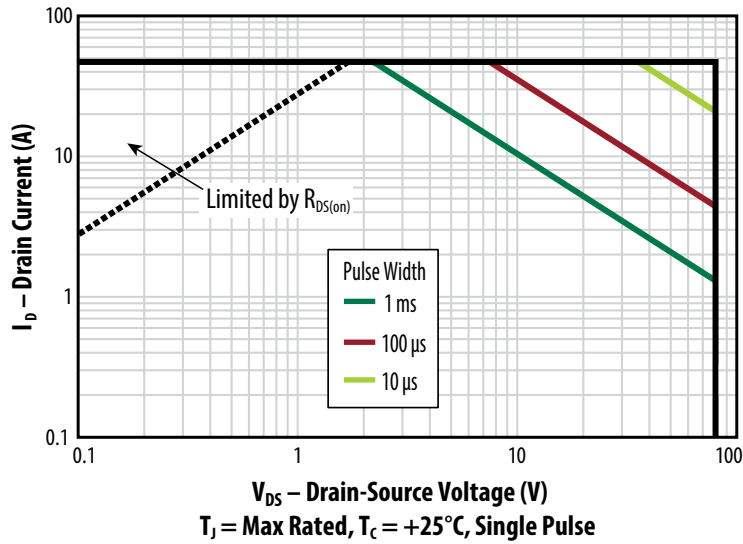
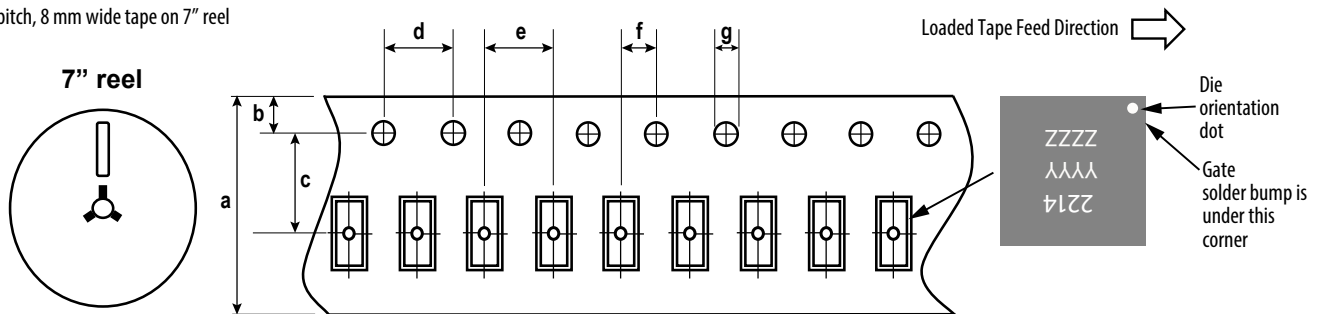


Figure 12: Safe Operating Area



**TAPE AND REEL CONFIGURATION**

4 mm pitch, 8 mm wide tape on 7" reel

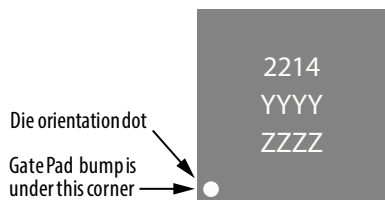


Die is placed into pocket solder bump side down (face side down)

Dimension (mm)	EPC2214 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.  
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

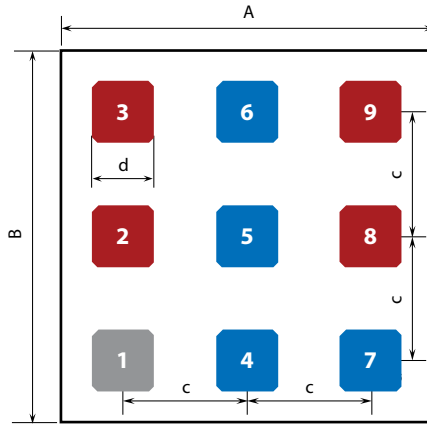
**DIE MARKINGS**



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2214	2214	YYYY	ZZZZ

**DIE OUTLINE**

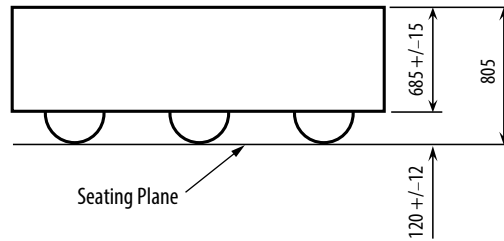
Pad View



DIM	Micrometers		
	MIN	Nominal	MAX
A	1320	1350	1380
B	1320	1350	1380
c		450	
d		225	

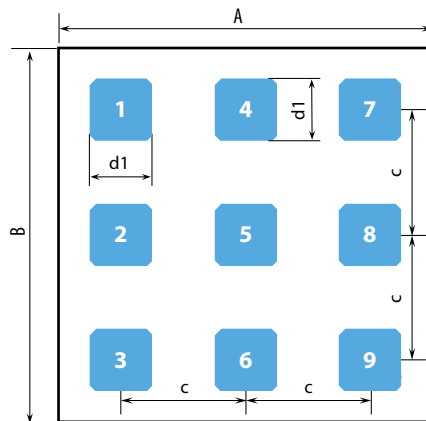
Pad 1 is Gate;  
 Pads 4, 5, 6, 7 are Drain;  
 Pads 2, 3, 8, 9 are Source.

Side View



**RECOMMENDED LAND PATTERN**

(measurements in  $\mu\text{m}$ )



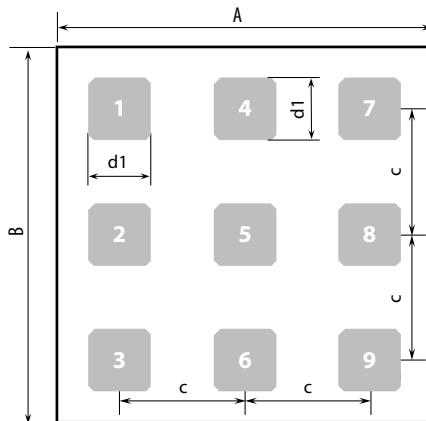
DIM	Micrometers
A	1350
B	1350
c	450
d1	205

The land pattern is solder mask defined  
 Solder mask is 10  $\mu\text{m}$  smaller per side than bump

Pad 1 is Gate;  
 Pads 4, 5, 6, 7 are Drain;  
 Pads 2, 3, 8, 9 are Source.

**RECOMMENDED STENCIL DRAWING**

(measurements in  $\mu\text{m}$ )



DIM	Micrometers
A	1350
B	1350
c	450
d1	225

Recommended stencil should be 4 mil (100  $\mu\text{m}$ ) thick,  
 must be laser cut, openings per drawing.  
 The corner has a radius of R60.  
 Intended for use with SAC305 Type 4 solder,  
 reference 88.5% metals content.

Additional assembly resources available at  
<https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

Efficient Power Conversion Corporation (EPC) reserves the right to make changes without further notice to any products herein to improve reliability, function or design. EPC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

eGaN® is a registered trademark of Efficient Power Conversion Corporation.  
 EPC Patent Listing: [epc-co.com/epc/AboutEPC/Patents.aspx](http://epc-co.com/epc/AboutEPC/Patents.aspx)

Information subject to change without notice.

Revised May, 2020

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View EPC2214 on WIN SOURCE](#)

 [EPC Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management