



**THE DATASHEET OF  
FDMA86265P**



# MOSFET – P-Channel, POWERTRENCH®

**-150 V, -1 A, 1.2 Ω**

## FDMA86265P

### General Description

This P-Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been optimized for the on-state resistance and yet maintain superior switching performance.

### Features

- Max  $r_{DS(on)}$  = 1.2 mΩ at  $V_{GS} = -10$  V,  $I_D = -1$  A
- Max  $r_{DS(on)}$  = 1.4 mΩ at  $V_{GS} = -6$  V,  $I_D = -0.9$  A
- Low Profile – 0.8 mm Maximum in the New Package MicroFET™ 2x2 mm
- Very Low RDS-on Mid Voltage P-channel Silicon Technology Optimised for Low Qg
- This Product is Optimised for Fast Switching Applications as Well as Load Switch Applications
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### Applications

- Active Clamp Switch
- Load Switch

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

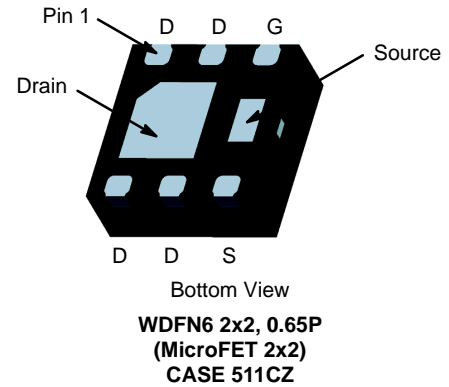
Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	-150	V
$V_{GS}$	Gate to Source Voltage	±25	V
$I_D$	Drain Current – Continuous $T_A = 25^\circ\text{C}$ (Note 1a) – Pulsed	-1 -2	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	6	mJ
$P_D$	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a) $T_A = 25^\circ\text{C}$ (Note 1b)	2.4 0.9	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

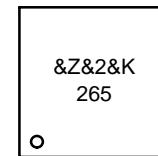
### THERMAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

$V_{DS}$	$r_{DS(on)}$ MAX	$I_D$ MAX
-150 V	1.2 mΩ @ -10 V	-1 A
	1.4 mΩ @ -6 V	

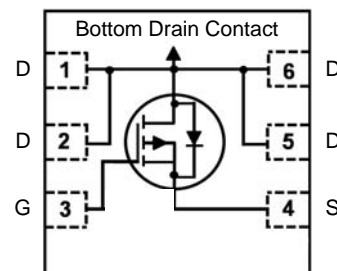


### MARKING DIAGRAM



&Z = Assembly Plant Code  
&2 = 2-Digit Date Code  
&K = 2-Digits Lot Run Traceability Code  
265 = Specific Device Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# FDMA86265P

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = -250 μA, V <sub>GS</sub> = 0 V	-150	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C	-	-125	-	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -120 V, V <sub>GS</sub> = 0 V	-	-	-1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±25 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-2	-3.2	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C	-	5	-	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1 A	-	0.86	1.2	Ω
		V <sub>GS</sub> = -6 V, I <sub>D</sub> = -0.9 A	-	0.95	1.4	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1 A, T <sub>J</sub> = 125°C	-	1.53	2.2	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 A	-	1.9	-	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -75 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	158	210	pF
C <sub>oss</sub>	Output Capacitance		-	16	25	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	0.7	5	pF
R <sub>g</sub>	Gate Resistance		0.1	3	7.5	Ω

### SWITCHING CHARACTERISTICS

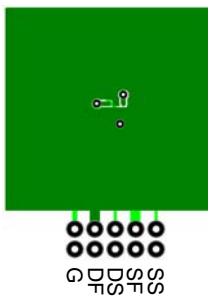
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -75 V, I <sub>D</sub> = -1 A, V <sub>GS</sub> = -10 V, R <sub>GEN</sub> = 6 Ω	-	5.8	12	ns
t <sub>r</sub>	Rise Time		-	2.2	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	8	16	ns
t <sub>f</sub>	Fall Time		-	6.4	13	ns
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to -10 V, V <sub>DD</sub> = -75 V, I <sub>D</sub> = -1 A	-	2.8	4	nC
Q <sub>gs</sub>	Total Gate Charge	V <sub>DD</sub> = -75 V, I <sub>D</sub> = -1 A	-	0.8	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	0.7	-	nC

### DRAIN-SOURCE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1 A (Note 2)	-	-0.87	-1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -1 A, di/dt = 100 A/μs	-	50	80	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	78	124	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 52°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 145°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- Starting T<sub>J</sub> = 25°C; P-ch: L = 3 mH, I<sub>AS</sub> = -2 A, V<sub>DD</sub> = -150 V, V<sub>GS</sub> = -10 V.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

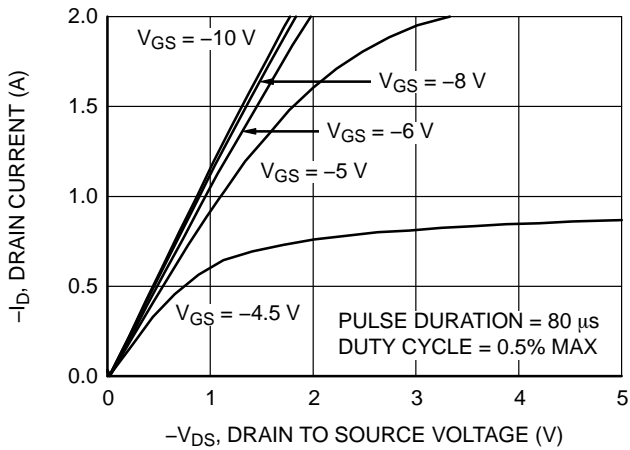


Figure 1. On Region Characteristics

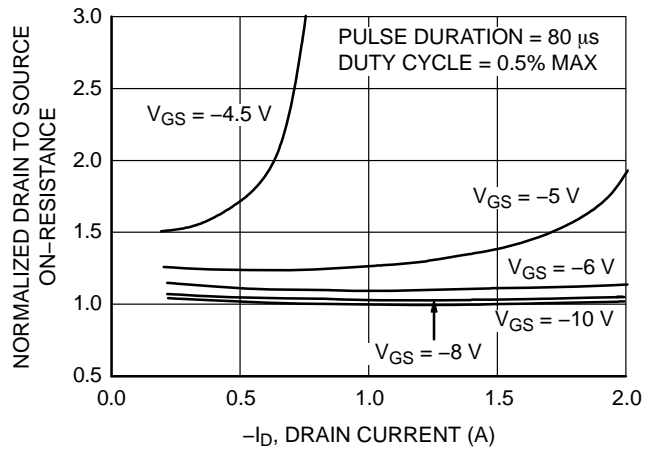


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

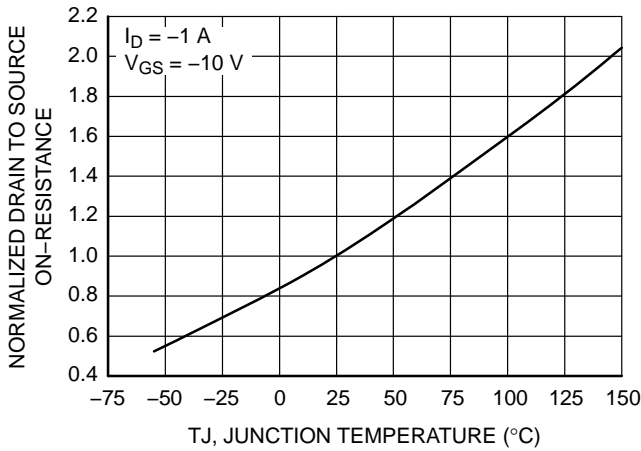


Figure 3. Normalized On Resistance vs. Junction Temperature

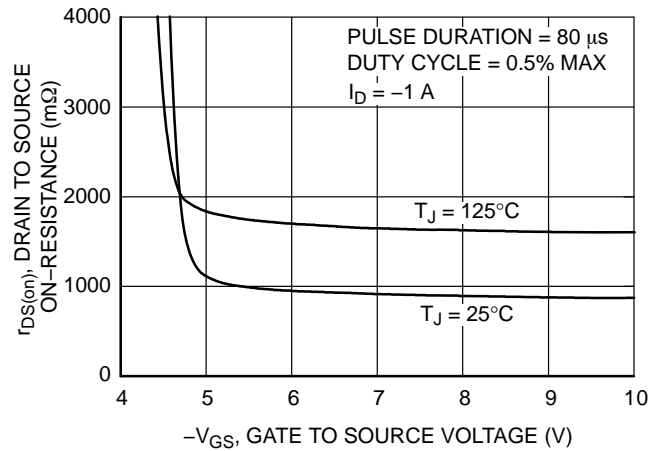


Figure 4. On-Resistance vs. Gate to Source Voltage

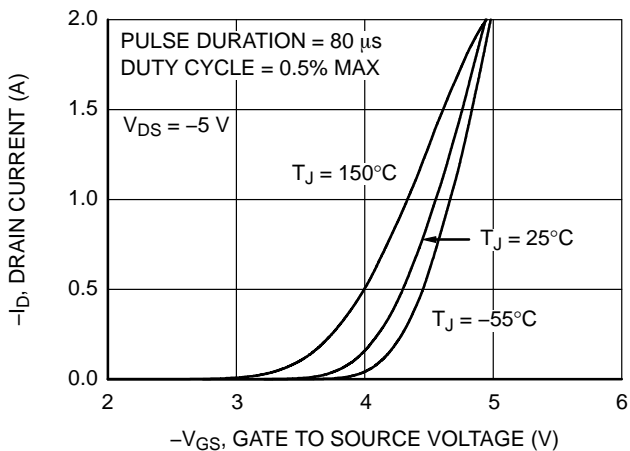


Figure 5. Transfer Characteristics

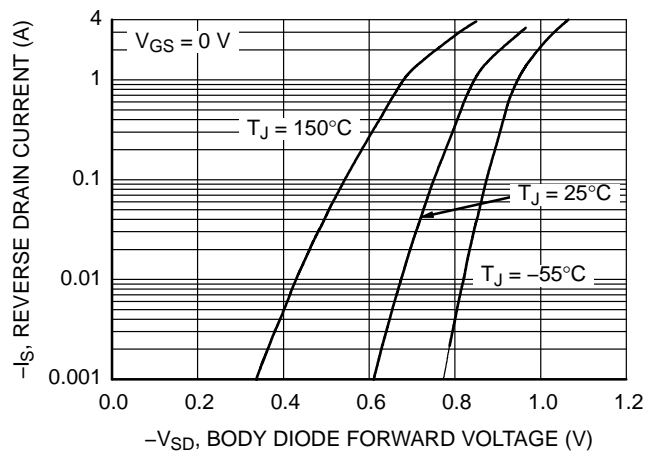


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

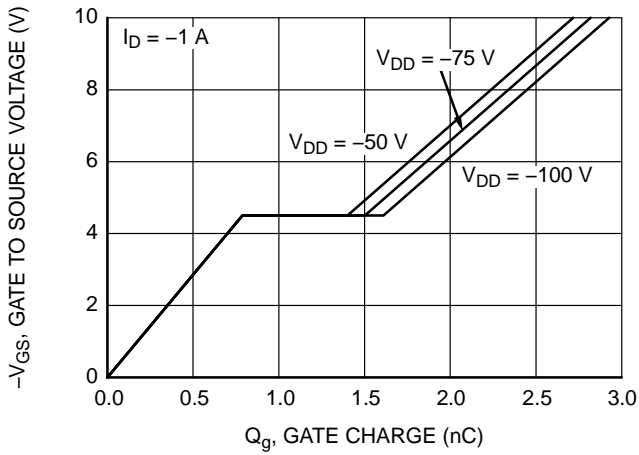


Figure 7. Gate Charge Characteristics

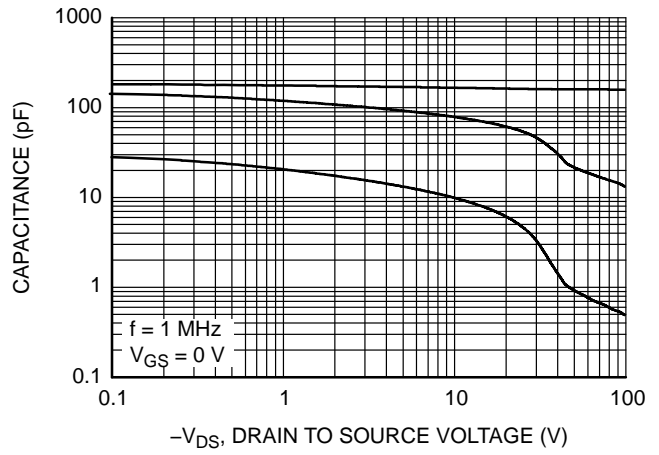


Figure 8. Capacitance vs. Drain to Source Voltage

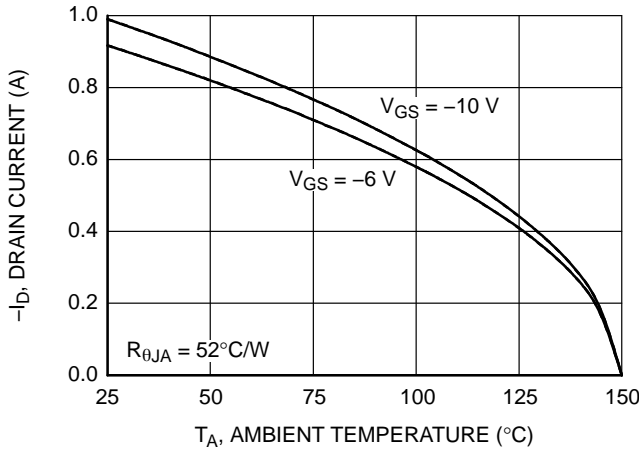


Figure 9. Maximum Continuous Drain Current vs. Ambient Temperature

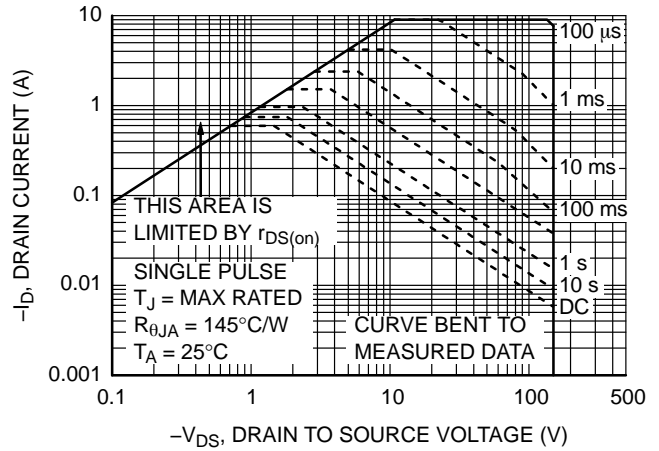


Figure 10. Forward Bias Safe Operating Area

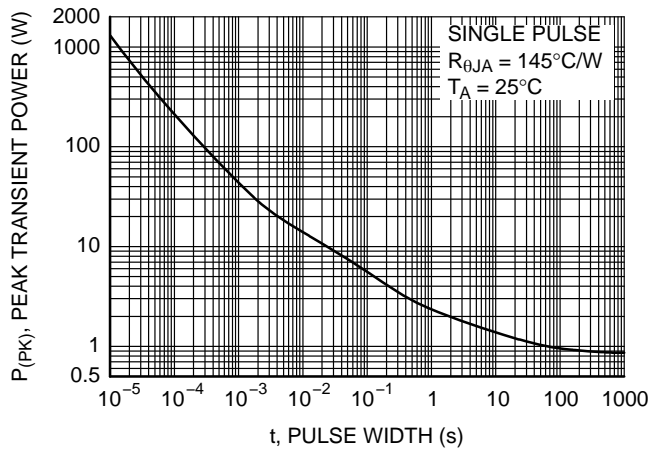


Figure 11. Single Pulse Maximum Power Dissipation

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## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

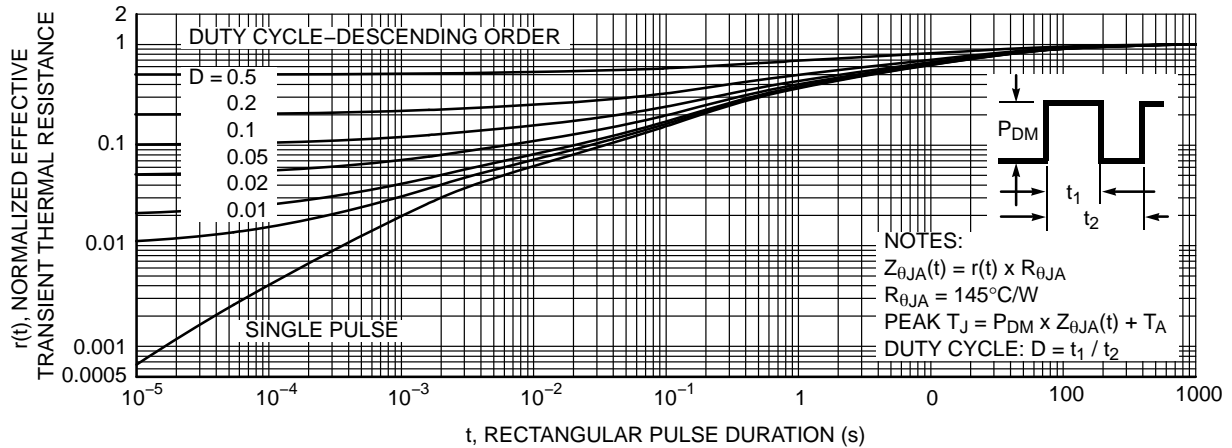


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

### PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping <sup>†</sup>
FDMA86265P	265	WDFN6 2x2, 0.65P (MicroFET 2x2) (Pb-Free, Halide Free)	7"	12 mm	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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# MECHANICAL CASE OUTLINE

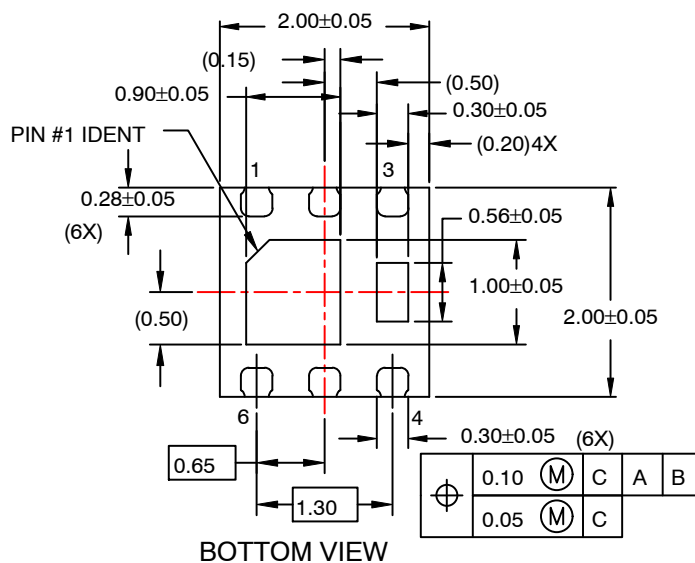
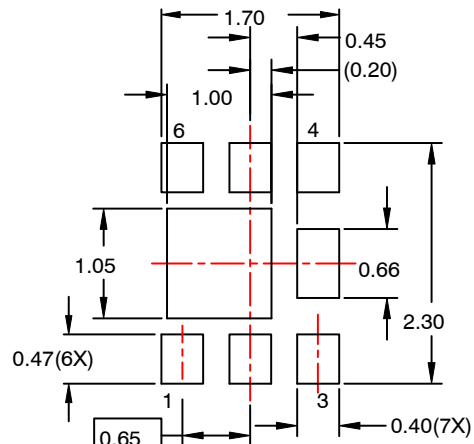
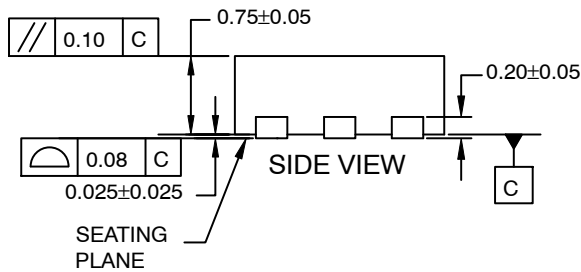
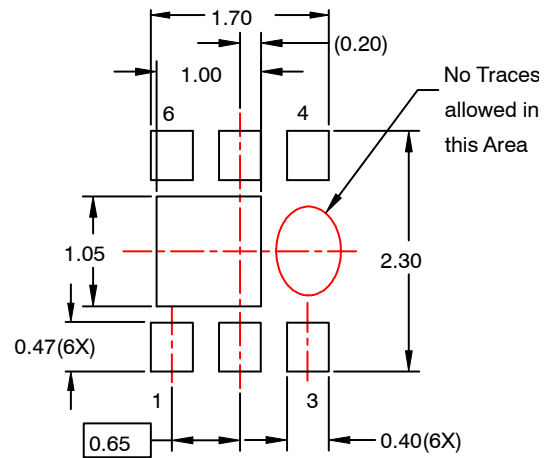
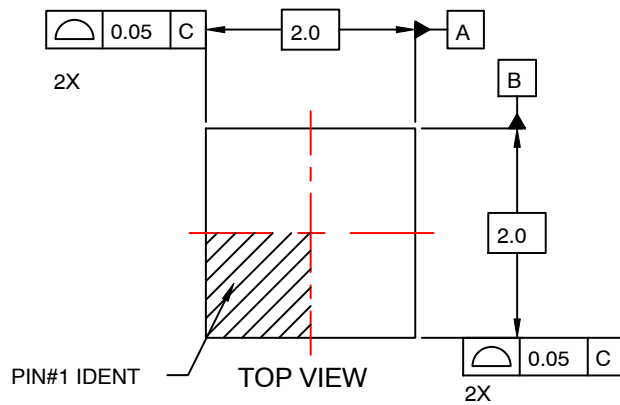
## PACKAGE DIMENSIONS

ON Semiconductor®



WDFN6 2x2, 0.65P  
CASE 511CZ  
ISSUE O

DATE 31 JUL 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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