



**THE DATASHEET OF
FDMC8097AC**



MOSFET – Dual, N & P-Channel, POWERTRENCH®

N-Channel: 150 V, 2.4 A, 155 mΩ
P-Channel: -150 V, -0.9 A, 1200 mΩ

FDMC8097AC

General Description

These dual N and P-Channel enhancement mode Power MOSFETs are produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance. Shrinking the area needed for implementation of active clamp topology; enabling best in class power density.

Features

Q1: N-Channel

- Max $R_{DS(on)}$ = 155 mΩ at $V_{GS} = 10$ V, $I_D = 2.4$ A
- Max $R_{DS(on)}$ = 212 mΩ at $V_{GS} = 6$ V, $I_D = 2$ A

Q2: P-Channel

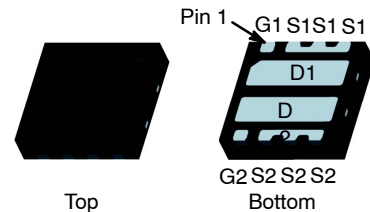
- Max $R_{DS(on)}$ = 1200 mΩ at $V_{GS} = -10$ V, $I_D = -0.9$ A
- Max $R_{DS(on)}$ = 1400 mΩ at $V_{GS} = -6$ V, $I_D = -0.8$ A
- Optimised for Active Clamp Forward Converters
- Pb-Free, Halide Free and RoHS Compliant

Applications

- DC-DC Converter
- Active Clamp

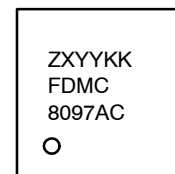
N-Channel		
V_{DS} MAX	$R_{DS(on)}$	I_D MAX
150 V	155 mΩ @ 10 V	2.4 A
	212 mΩ @ 6 V	

P-Channel		
V_{DS} MAX	$R_{DS(on)}$	I_D MAX
-150 V	1200 mΩ @ -10 V	-0.9 A
	1400 mΩ @ -6 V	



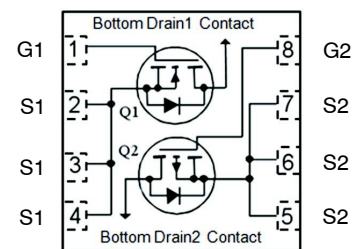
WDFN8 3.3 × 3.3, 0.65P
(Power 33)
CASE 511DG

MARKING DIAGRAM



Z = Assembly Plant Code
 XYY = 3-Digit Date Code Format
 KK = 2-Alphanumeric Lot Run Traceability Code
 FDMC8097AC = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
FDMC8097AC	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Q1	Q2	Unit	
V_{DS}	Drain to Source Voltage		150	-150	V	
V_{GS}	Gate to Source Voltage		± 20	± 25	V	
I_D	Drain Current	Continuous (Note 5)	$T_C = 25^\circ\text{C}$	6.3	-2.0	A
		Continuous (Note 5)	$T_C = 100^\circ\text{C}$	3.9	-1.2	
		Continuous	$T_A = 25^\circ\text{C}$	2.4 (Note 1a)	-0.9 (Note 1b)	
		Pulsed (Note 4)		33	-8.8	
E_{AS}	Single Pulse Avalanche Energy (Note 3)		24	6	mJ	
P_D	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$	1.9 (Note 1a)	1.9 (Note 1b)	W	
		$T_A = 25^\circ\text{C}$	0.8 (Note 1c)	0.8 (Note 1d)		
		$T_C = 25^\circ\text{C}$	14	10		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Q1	Q2	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	65 (Note 1a)	65 (Note 1b)	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	155 (Note 1c)	155 (Note 1d)	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	8.9	12.5	

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V I _D = -250 μA, V _{GS} = 0 V	Q1 Q2	150 -150	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = -250 μA, referenced to 25°C	Q1 Q2	-	98 122	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 120 V, V _{GS} = 0 V V _{DS} = -120 V, V _{GS} = 0 V	Q1 Q2	-	-	1 -1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V V _{GS} = ±25 V, V _{DS} = 0 V	Q1 Q2	-	-	±100 ±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA V _{GS} = V _{DS} , I _D = -250 μA	Q1 Q2	2.0 -2.0	3.1 -3.0	4.0 -4.0	V
ΔV _{GS(th)} / ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = -250 μA, referenced to 25°C	Q1 Q2	-	-9 -6	-	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 2.4 A V _{GS} = 6 V, I _D = 2 A V _{GS} = 10 V, I _D = 2.4 A, T _J = 125°C	Q1	-	124 155 245	155 212 306	mΩ
		V _{GS} = -10 V, I _D = -0.9 A V _{GS} = -6 V, I _D = -0.8 A V _{GS} = -10 V, I _D = -0.9 A, T _J = 125°C	Q2	-	930 1030 1682	1200 1400 2171	
g _{FS}	Forward Transconductance	V _{DD} = 10 V, I _D = 2.4 A V _{DD} = -10 V, I _D = -0.9 A	Q1 Q2	-	6.4 0.75	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	Q1 V _{DS} = 75 V, V _{GS} = 0 V, f = 1 MHz Q2 V _{DS} = -75 V, V _{GS} = 0 V, f = 1 MHz	Q1 Q2	-	279 162	395 230	pF
C _{oss}	Output Capacitance		Q1 Q2	-	26 13	40 25	pF
C _{rss}	Reverse Transfer Capacitance		Q1 Q2	-	1.4 0.6	5 5	pF
R _g	Gate Resistance		Q1 Q2	0.1 0.1	0.6 3.3	1.5 8.3	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	Q1 V _{DD} = 75 V, I _D = 2.4 A, V _{GS} = 10 V, R _{GEN} = 6 Ω Q2 V _{DD} = -75 V, I _D = -0.9 A, V _{GS} = -10 V, R _{GEN} = 6 Ω	Q1 Q2	-	5.4 5.2	11 11	ns
t _r	Rise Time		Q1 Q2	-	1.3 1.6	10 10	ns
t _{d(off)}	Turn-Off Delay Time		Q1 Q2	-	9.1 7.4	18 15	ns
t _f	Fall Time		Q1 Q2	-	2.2 6.3	10 13	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V V _{GS} = 0 V to -10 V	Q1 Q2	-	4.4 2.8	6.2 4.0	nC
		V _{GS} = 0 V to 6 V V _{GS} = 0 V to -6 V	Q1 Q2	-	2.9 1.8	4.1 2.6	nC
Q _{gs}	Gate to Source Charge	Q1 V _{DD} = 75 V, I _D = 2.4 A	Q1 Q2	-	1.3 0.8	-	nC
Q _{gd}	Gate to Drain "Miller" Charge	Q2 V _{DD} = -75 V I _D = -0.9 A	Q1 Q2	-	1.0 0.7	-	nC

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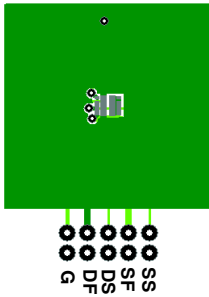
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.4\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}$, $I_S = -0.9\text{ A}$ (Note 2)	Q1 Q2	- -	0.8 -0.9	1.3 -1.3	V
t_{rr}	Reverse Recovery Time	Q1 $I_F = 2.4\text{ A}$, $di/dt = 100\text{ A/s}$	Q1 Q2	- -	50 44	80 71	ns
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = -0.9\text{ A}$, $di/dt = 100\text{ A/s}$	Q1 Q2	- -	43 68	69 109	nC

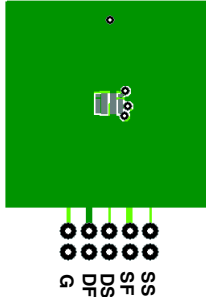
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

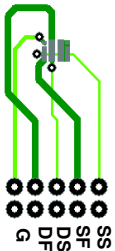
- $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 65°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 65°C/W when mounted on a 1 in² pad of 2 oz copper.



c) 155°C/W when mounted on a minimum pad of 2 oz copper.



d) 155°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- Q1: E_{AS} of 24 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 4\text{ A}$, $V_{DD} = 150\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 14\text{ A}$.
Q2: E_{AS} of 6 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = -2\text{ A}$, $V_{DD} = -150\text{ V}$, $V_{GS} = -10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = -8\text{ A}$.
- Q1: Pulsed I_d please refer to Fig 11 SOA graph for more details.
Q2: Pulsed I_d please refer to Fig 24 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

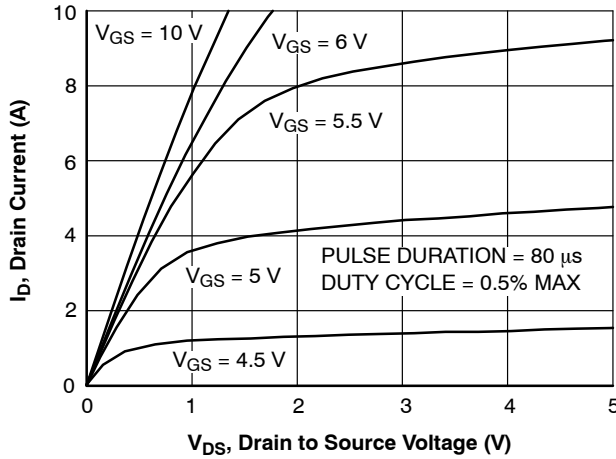


Figure 1. On-Region Characteristics

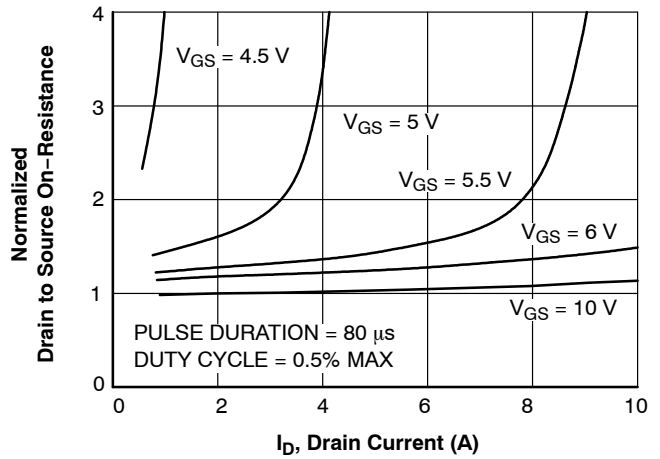


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

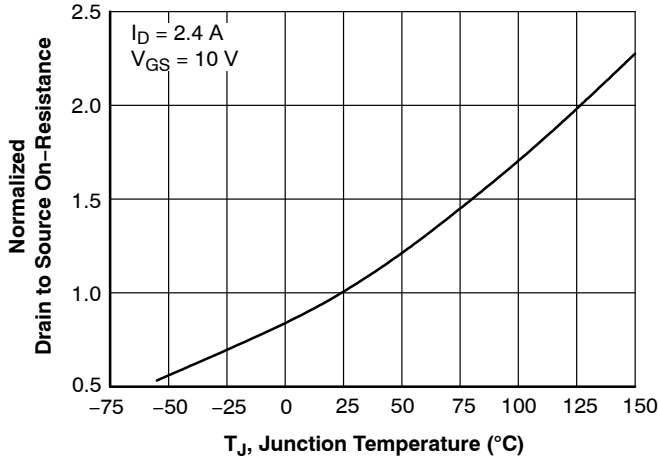


Figure 3. Normalized On-Resistance vs. Junction Temperature

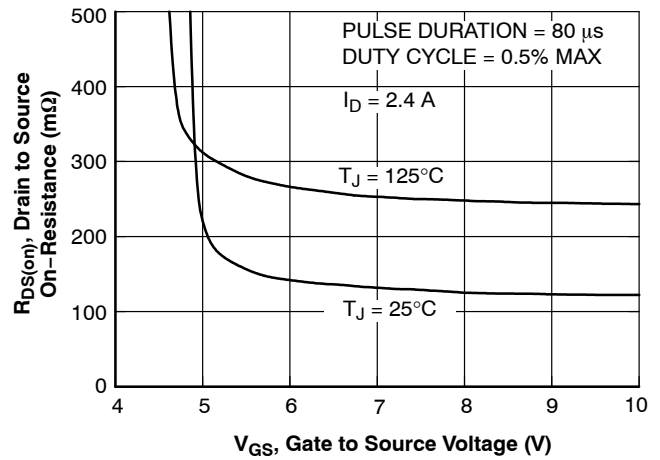


Figure 4. On-Resistance vs. Gate to Source Voltage

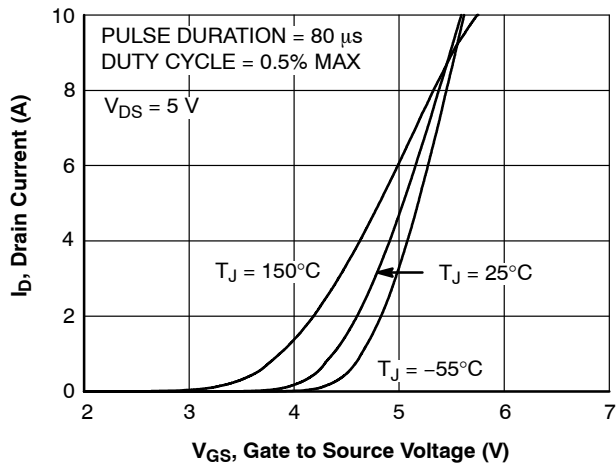


Figure 5. Transfer Characteristics

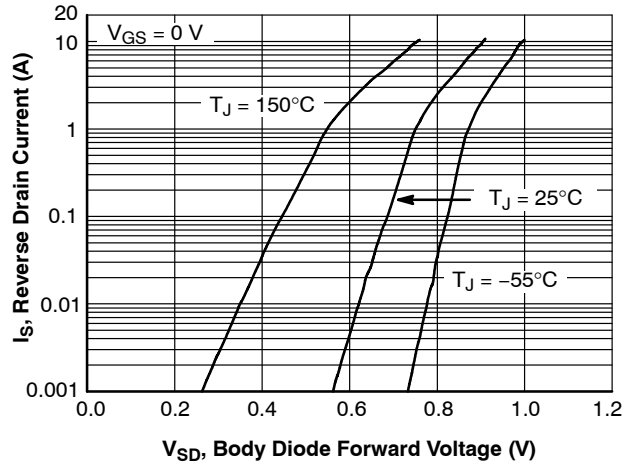


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

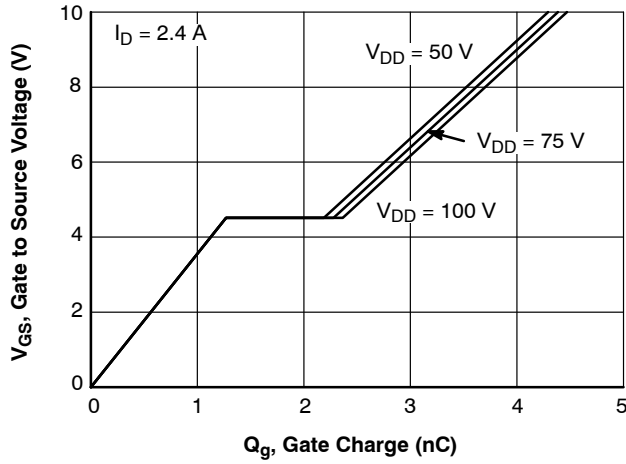


Figure 7. Gate Charge Characteristics

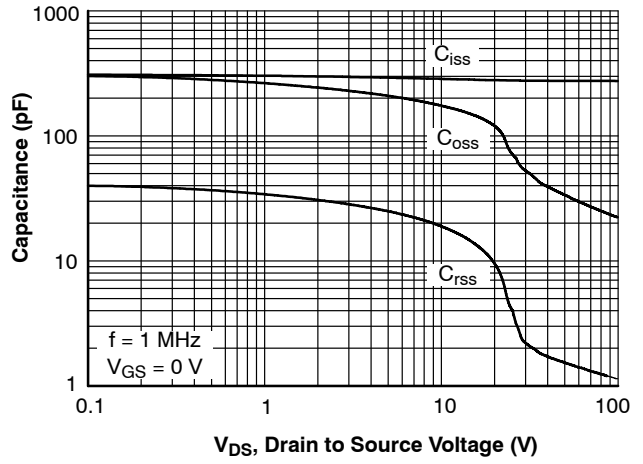


Figure 8. Capacitance vs. Drain to Source Voltage

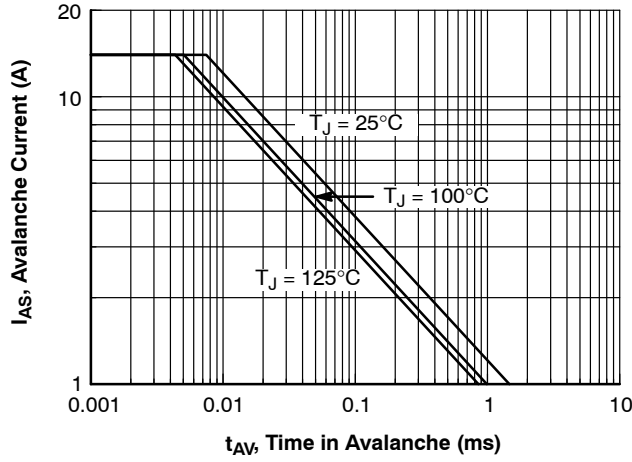


Figure 9. Unclamped Inductive Switching Capability

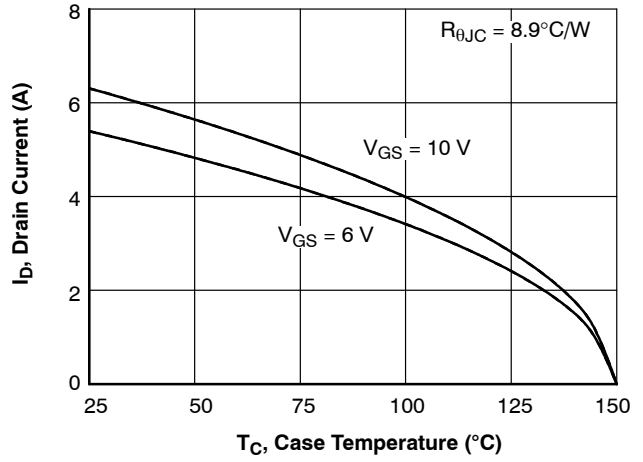


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

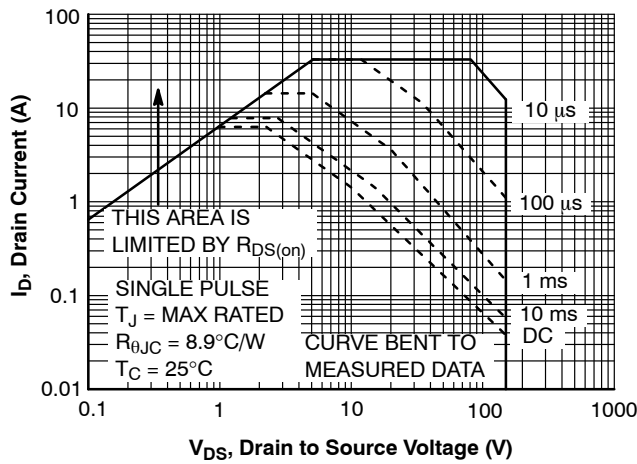


Figure 11. Forward Bias Safe Operating Area

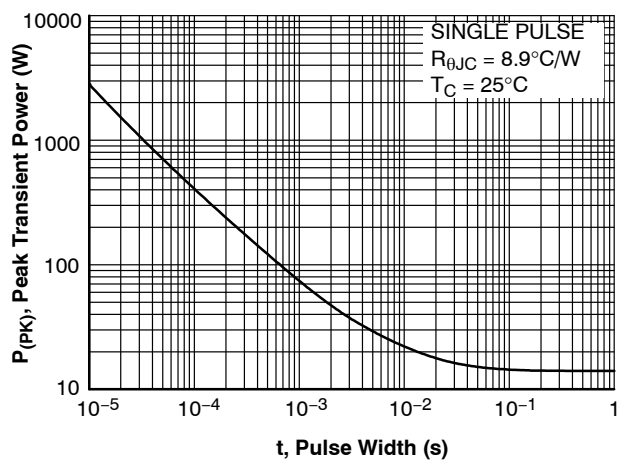


Figure 12. Single Pulse Maximum Power Dissipation

FDMC8097AC

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

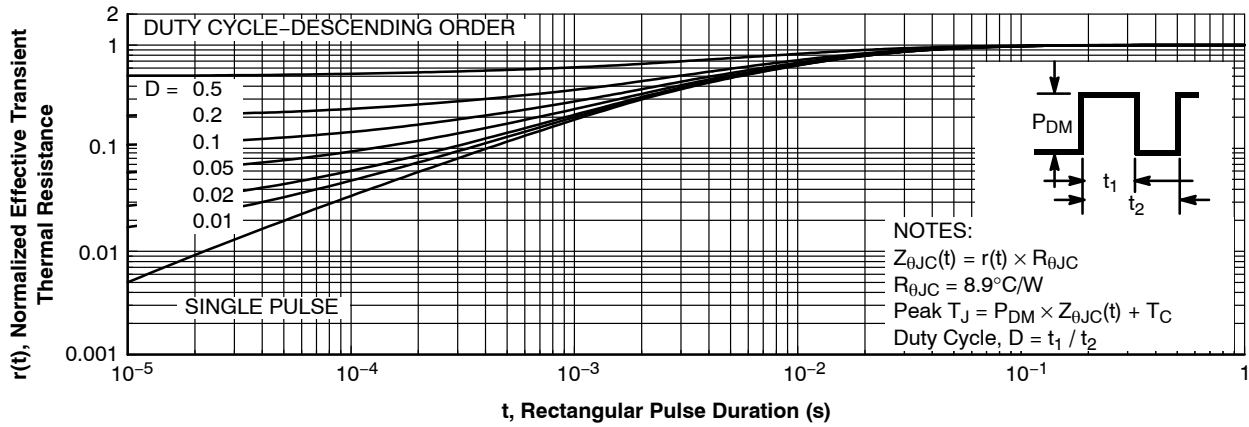


Figure 13. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 P-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

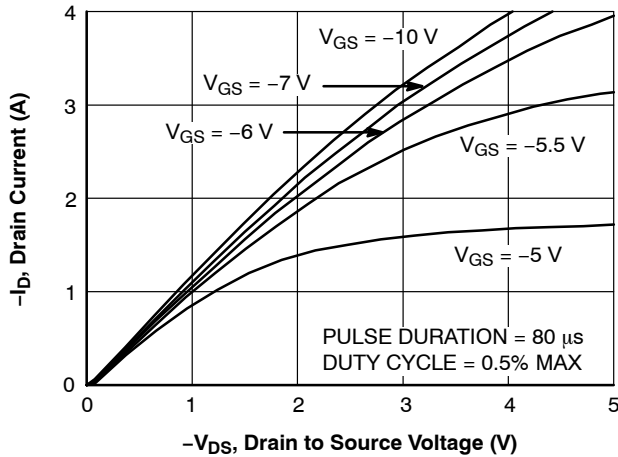


Figure 14. On-Region Characteristics

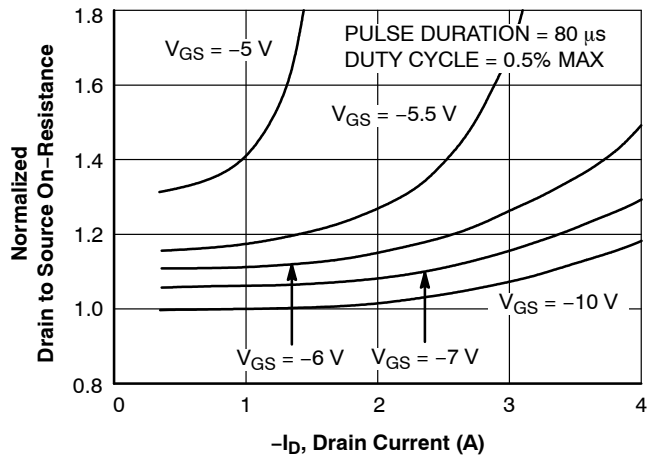


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

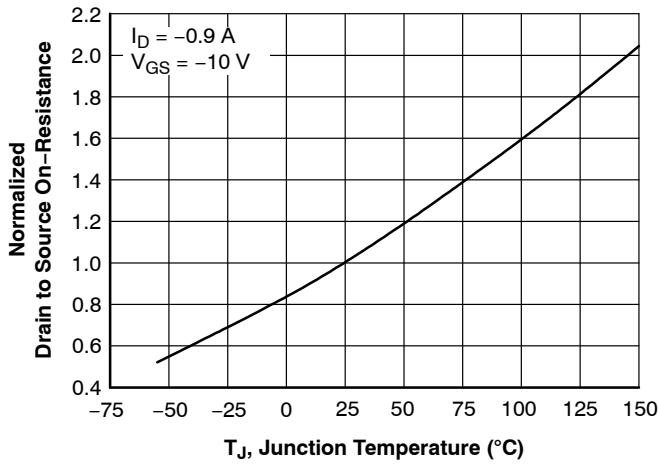


Figure 16. Normalized On-Resistance vs. Junction Temperature

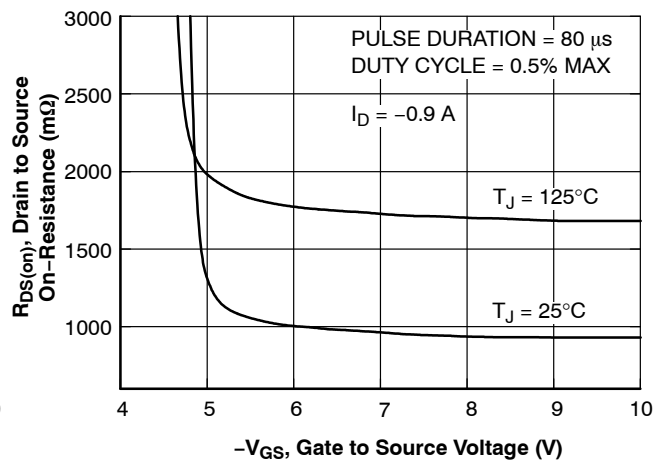


Figure 17. On-Resistance vs. Gate to Source Voltage

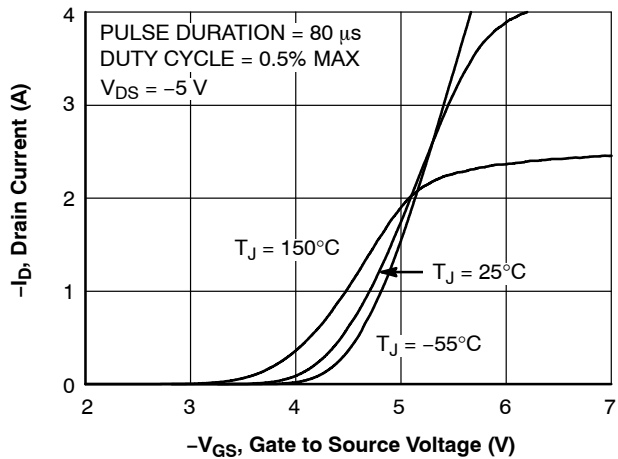


Figure 18. Transfer Characteristics

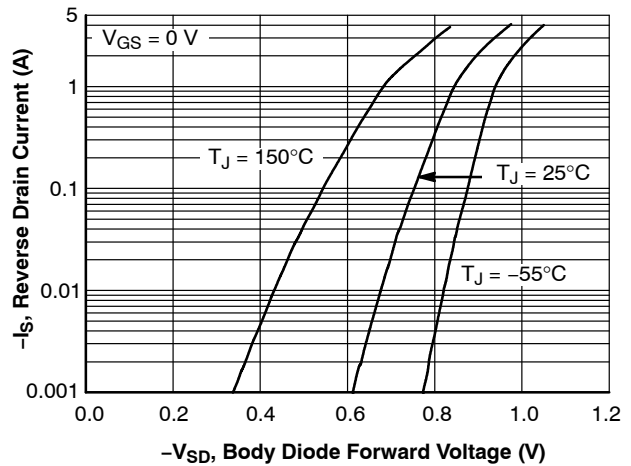


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 P-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

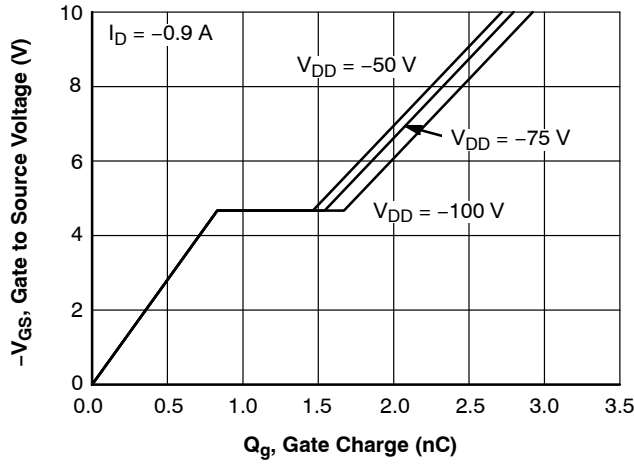


Figure 20. Gate Charge Characteristics

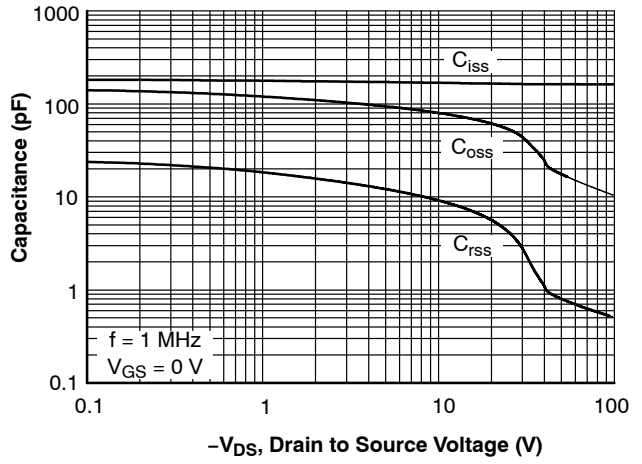


Figure 21. Capacitance vs. Drain to Source Voltage

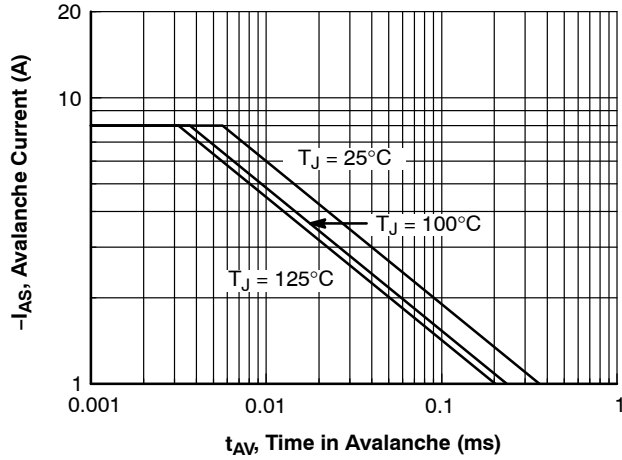


Figure 22. Unclamped Inductive Switching Capability

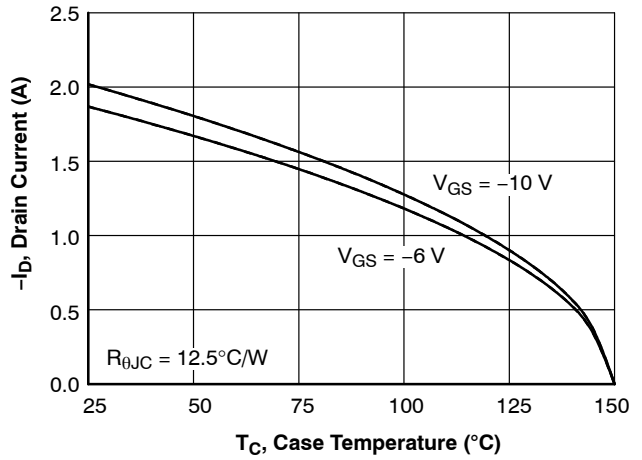


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

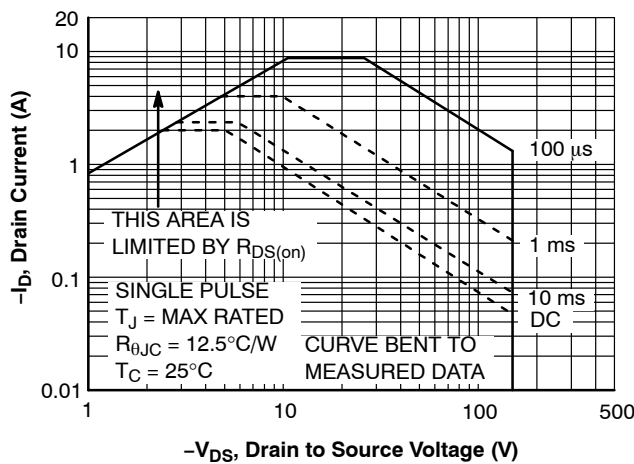


Figure 24. Forward Bias Safe Operating Area

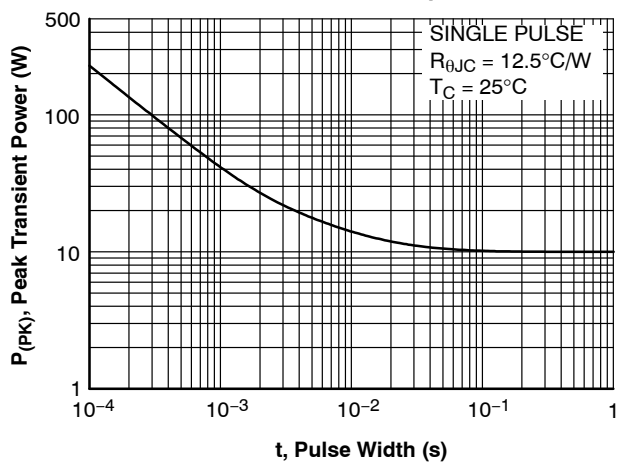


Figure 25. Single Pulse Maximum Power Dissipation

FDMC8097AC

TYPICAL CHARACTERISTICS (Q2 P-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

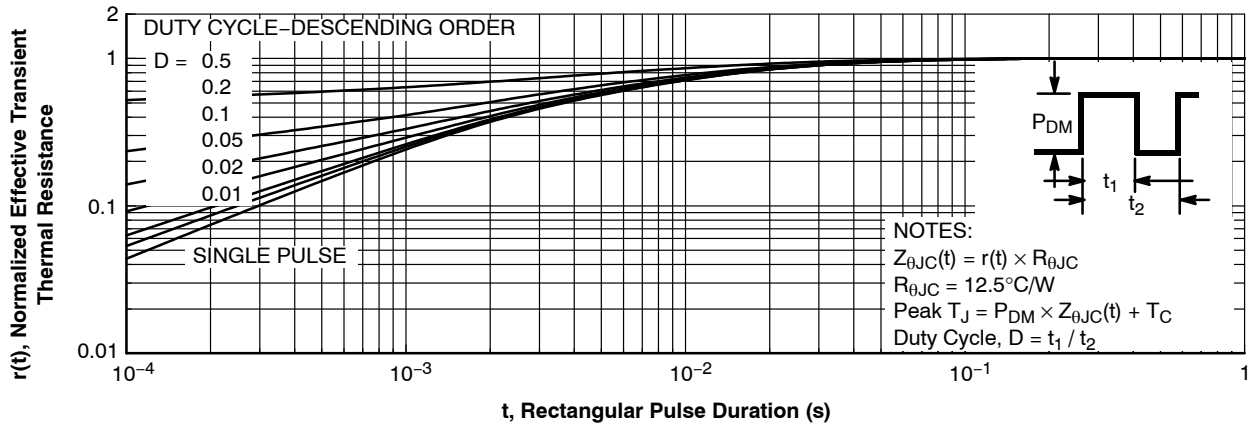
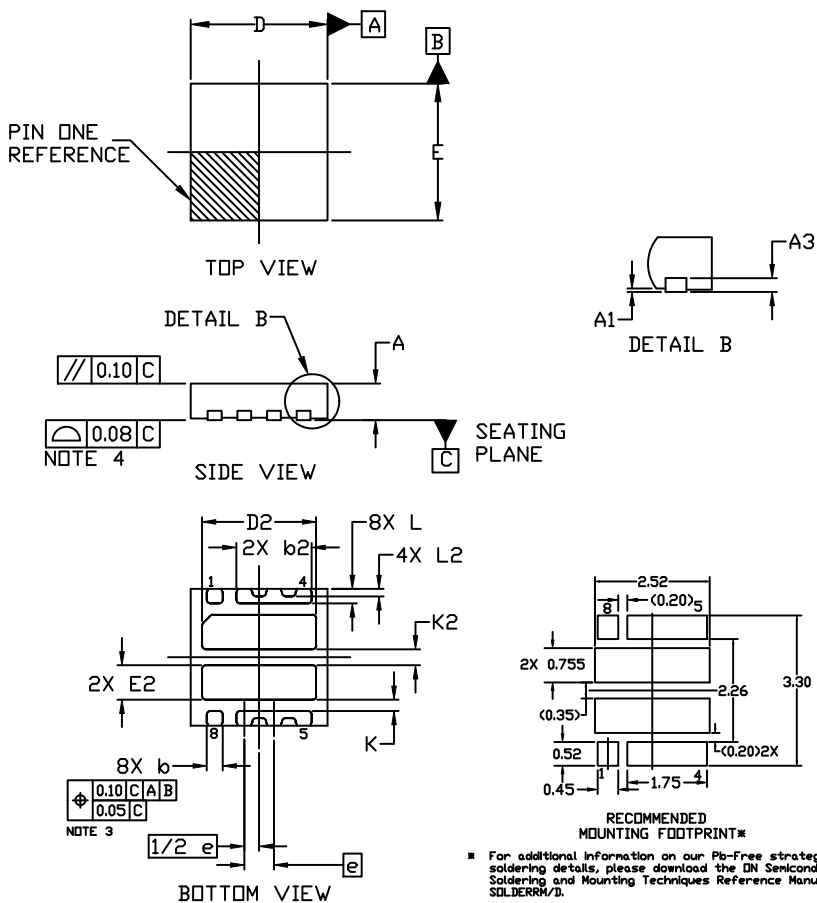


Figure 26. Junction-to-Case Transient Thermal Response Curve

WDFN8 3x3, 0.65P
CASE 511DG
ISSUE A

DATE 12 FEB 2019



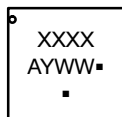
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION **b** APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.30	0.35	0.40
b2	1.65 REF		
D	2.90	3.00	3.10
D2	2.45	2.50	2.55
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
e	0.65 BSC		
K	0.25	---	---
K2	0.35 REF		
L	0.27	0.32	0.37
L2	0.163 REF		

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SLD166RM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 • = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN8 3x3, 0.65P	PAGE 1 OF 1

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