



**THE DATASHEET OF
IPD50N10S3L16ATMA1**



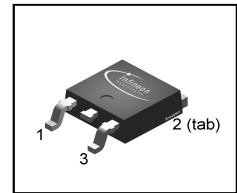
OptiMOS™-T Power-Transistor

Features

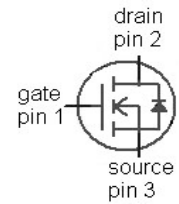
- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	15	mΩ
I_D	50	A

PG-TO252-3-11


Type	Package	Marking
IPD50N10S3L-16	PG-TO252-3-11	QN10L16


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}, V_{GS}=10\text{V}$	50	A
		$T_C=100\text{ °C}, V_{GS}=10\text{V}^{1)}$	38	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	200	
Avalanche energy, single pulse ¹⁾	E_{AS}	$I_D=25\text{A}$	330	mJ
Avalanche current, single pulse	I_{AS}	-	50	A
Gate source voltage ²⁾	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	100	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics¹⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	1.5	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=60\mu A$	1.2	1.7	2.4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	0.01	0.1	μA
		$V_{DS}=80V, V_{GS}=0V, T_j=125^\circ\text{C}^{1)}$	-	0.1	10	
Gate-source leakage current	I_{GSS}	$V_{GS}=16V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=50A$	-	15.3	19.9	m Ω
		$V_{GS}=10V, I_D=50A$	-	12.5	15.0	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics¹⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	3215	4180	pF
Output capacitance	C_{oss}		-	730	950	
Reverse transfer capacitance	C_{rss}		-	63	95	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=50A, R_G=3.5\Omega$	-	10	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	29	-	
Fall time	t_f		-	5	-	

Gate Charge Characteristics¹⁾

Gate to source charge	Q_{gs}	$V_{DD}=80V, I_D=50A,$ $V_{GS}=0$ to 10V	-	9	12	nC
Gate to drain charge	Q_{gd}		-	8	12	
Gate charge total	Q_g		-	49	64	
Gate plateau voltage	$V_{plateau}$		-	3.7	-	V

Reverse Diode

Diode continuous forward current ¹⁾	I_S	$T_C=25^\circ C$	-	-	50	A
Diode pulse current ¹⁾	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=50A,$ $T_j=25^\circ C$	0.6	1	1.2	V
Reverse recovery time ¹⁾	t_{rr}	$V_R=50V, I_F=I_S,$ $di_F/dt=100A/\mu s$	-	97	-	ns
Reverse recovery charge ¹⁾	Q_{rr}		-	178	-	nC

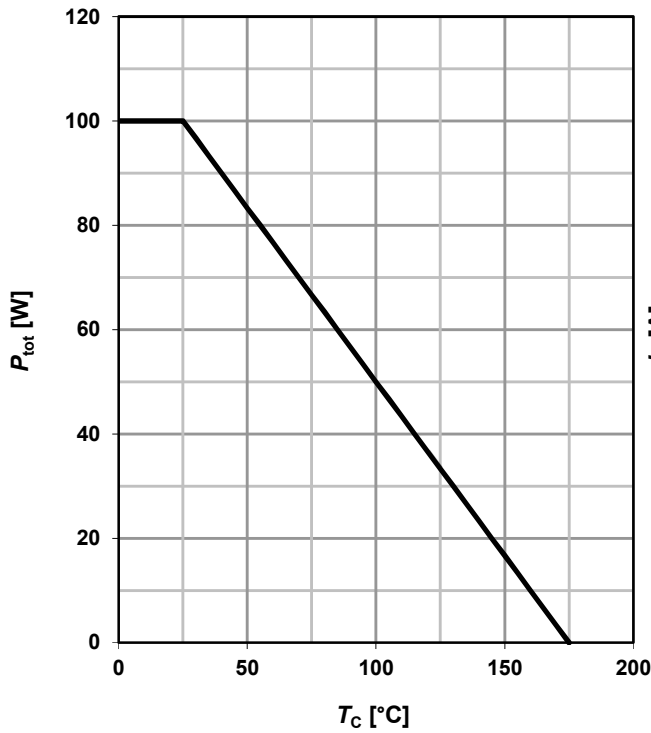
¹⁾ Defined by design. Not subject to production test.

²⁾ -5V to -20V for max. 168 non-consecutive hours.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

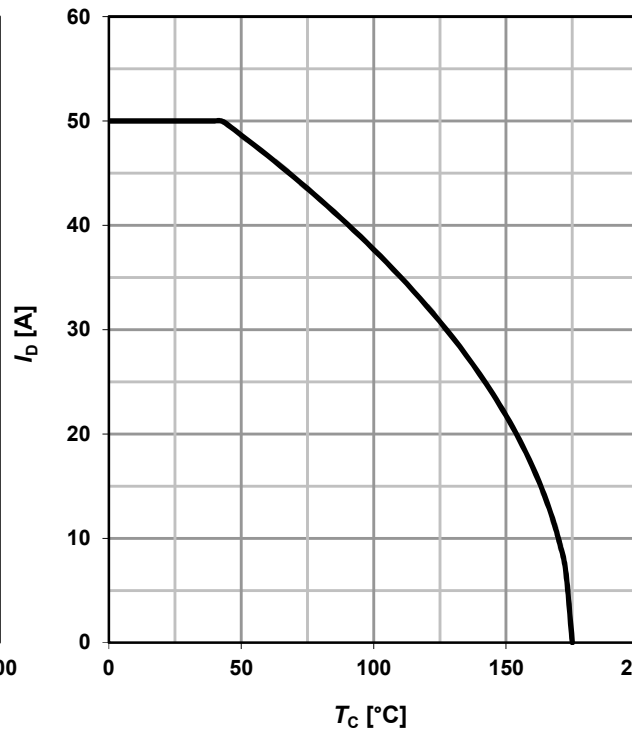
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} = 10\text{ V}$



2 Drain current

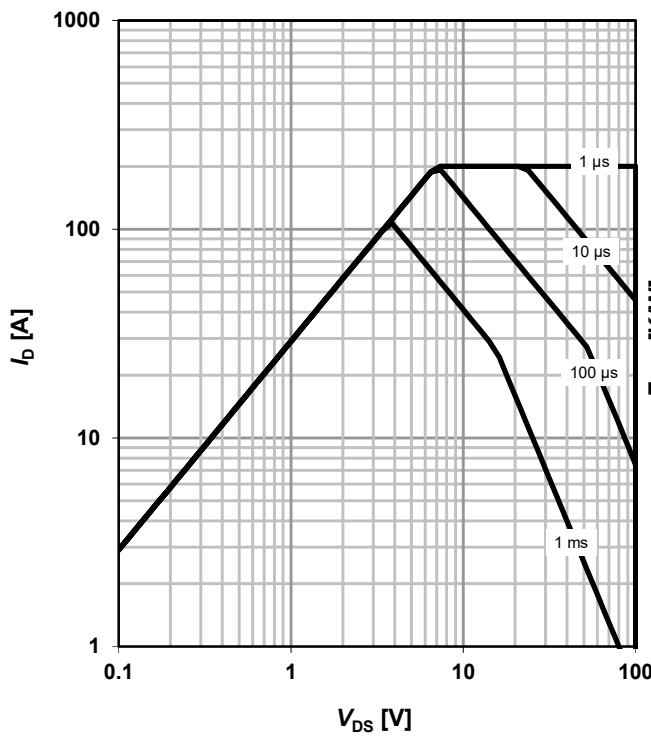
$I_D = f(T_C); V_{GS} = 10\text{ V}$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

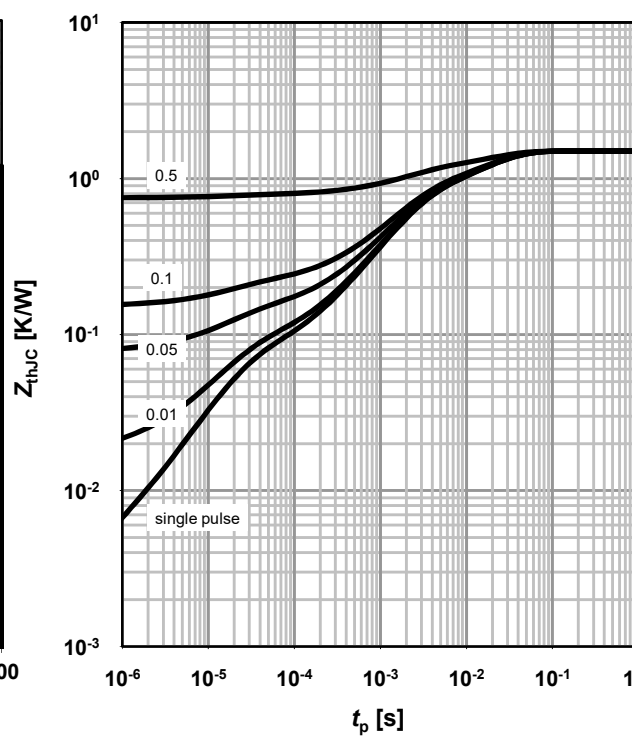
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

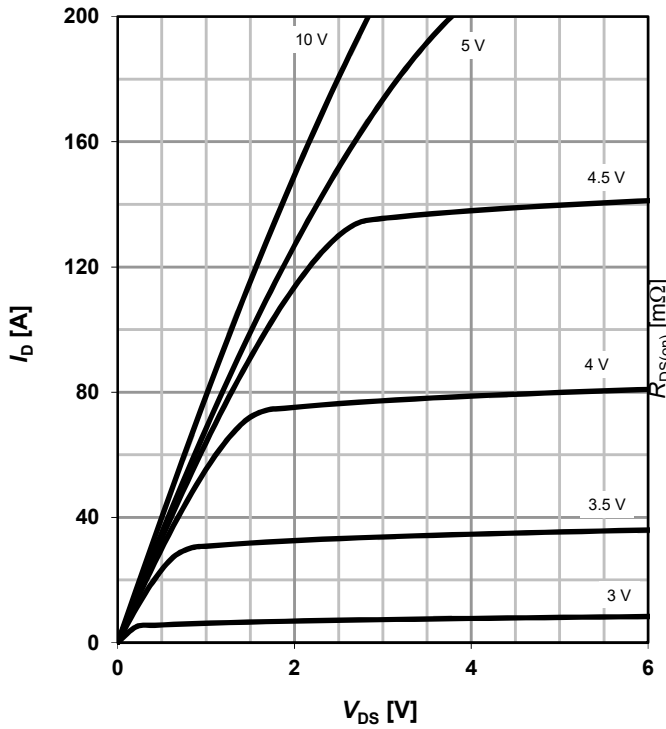
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

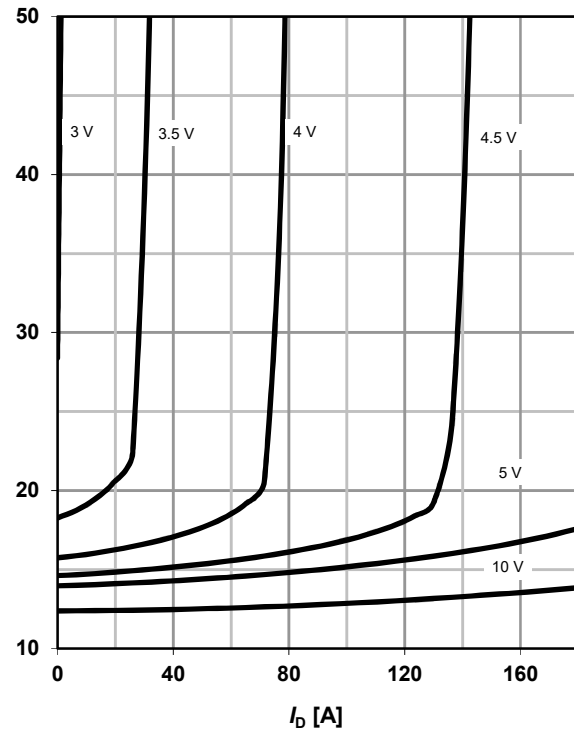
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

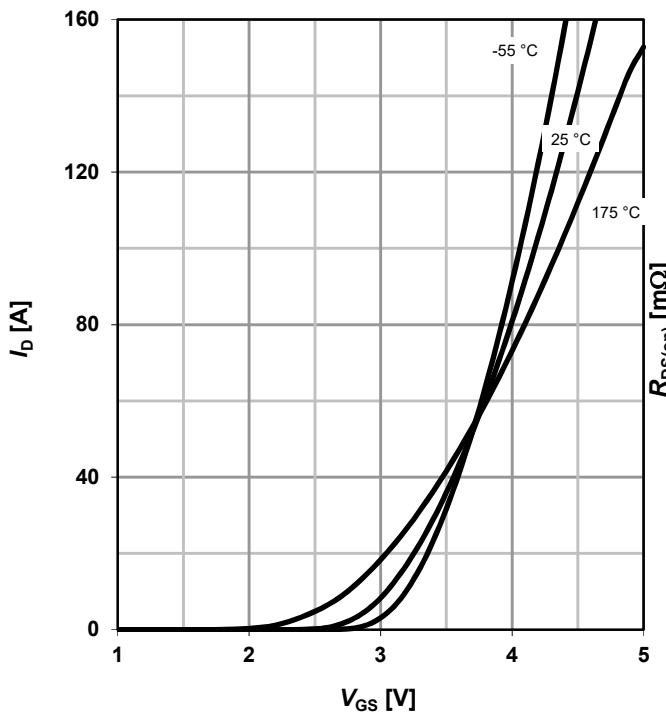
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

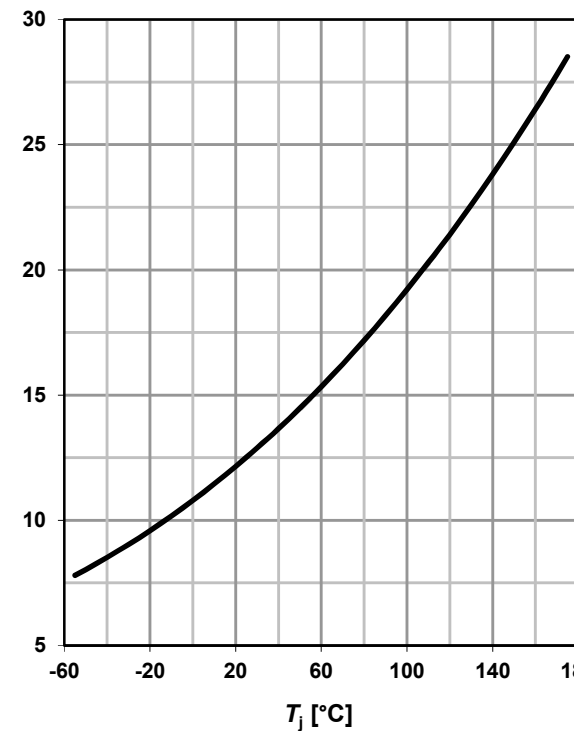
parameter: T_j



8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j); I_D = 50\text{ A}; V_{GS} = 10\text{ V}$

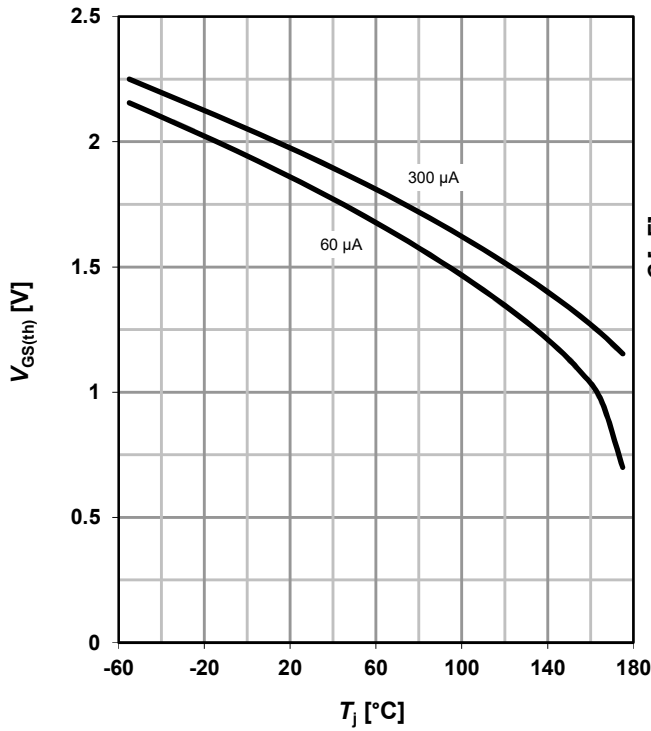
$\alpha = 0.56$



9 Typ. gate threshold voltage

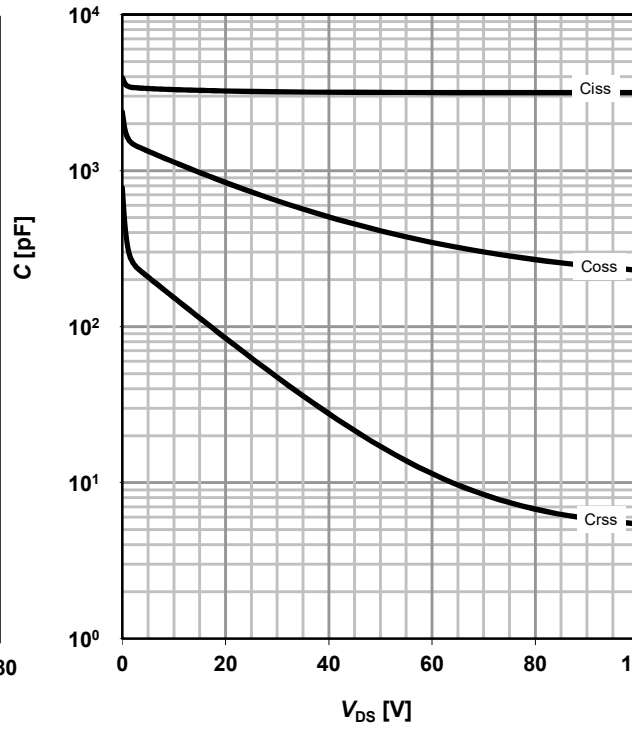
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

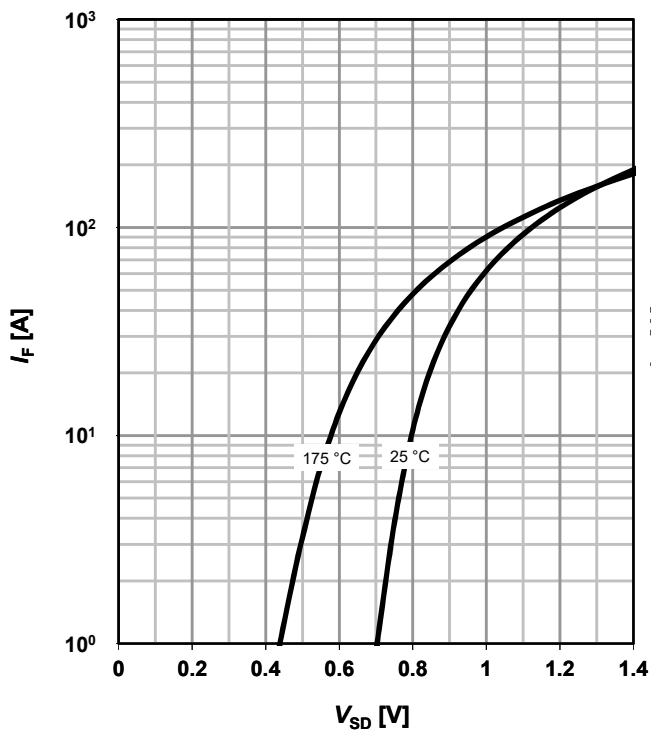
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

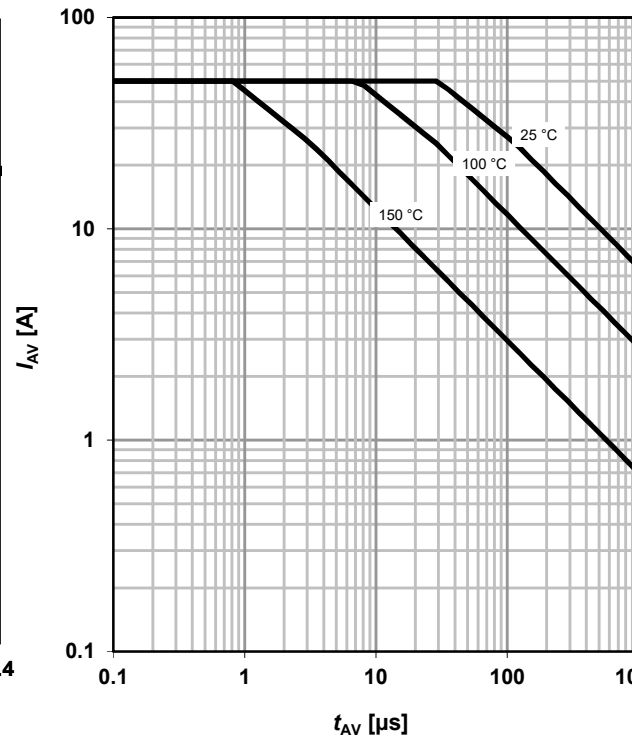
parameter: T_j



12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

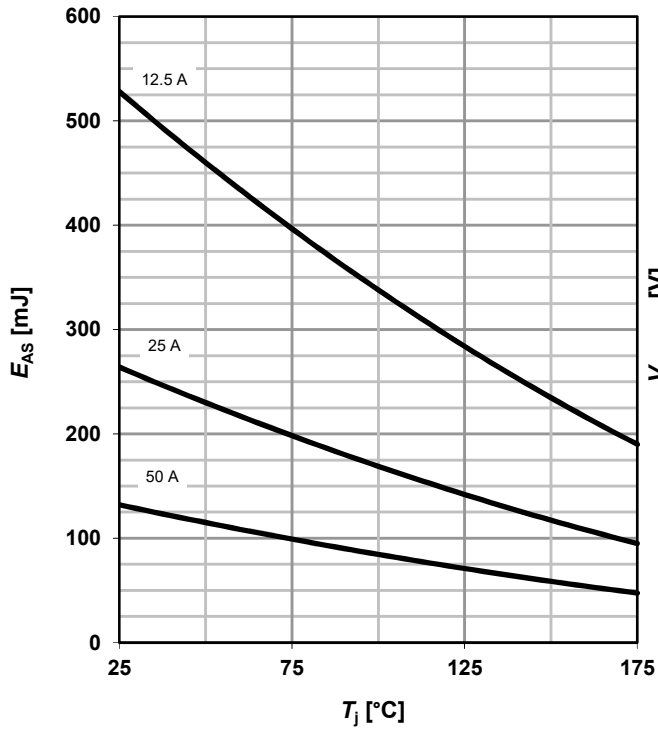
parameter: $T_{j(start)}$



13 Typical avalanche energy

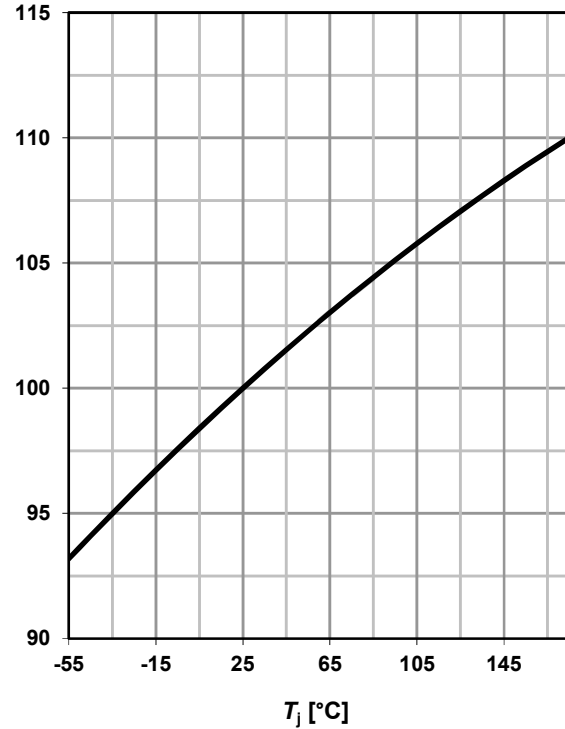
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Typ. drain-source breakdown voltage

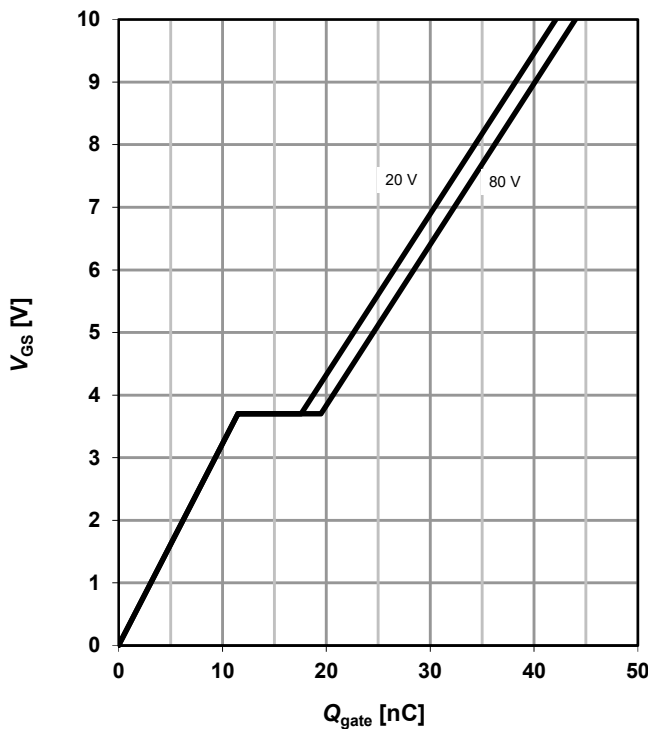
$$V_{(BR)DSS} = f(T_j); I_D = 1 \text{ mA}$$



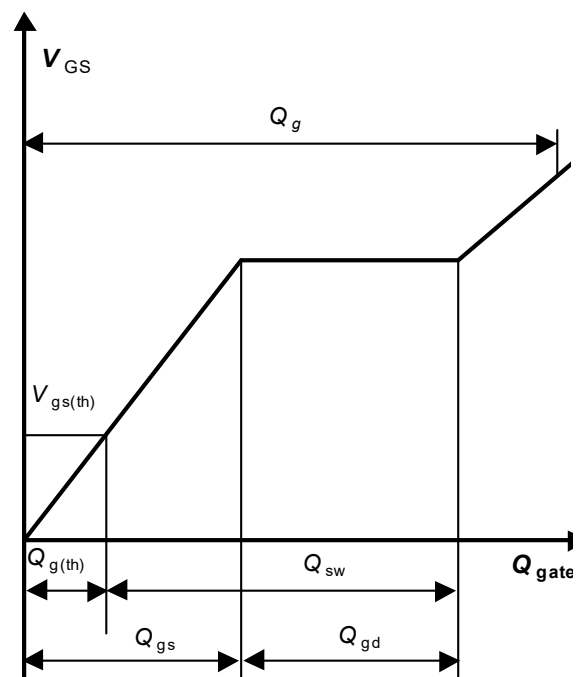
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 50 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Edition 2023-06-15**Published by****Infineon Technologies AG****81726 Munich, Germany****© 2023 Infineon Technologies AG****All Rights Reserved.****Do you have any questions about any aspect of this document?****Email: erratum@infineon.com****Document reference****IPD50N10S3L-16-Data-Sheet-14-Infineon****IMPORTANT NOTICE**

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Revision History

Version	Date	Changes
Revision 1.1	2008-04-08	Page 1: V_{GS} changed from $\pm 16V$ to $\pm 20V$
Revision 1.1	2008-04-08	Page 3: Footnote ²⁾ added
Revision 1.1	2008-04-09	Page 1: E_{AS} changed from 264mJ to 330mJ
Revision 1.2	2011-03-06	I_{DSS} typ changed from 1 μA to 0.1 μA
Revision 1.3	2015-10-07	Update of SOA diagram
Revision 1.4	2023-06-15	Diagram 8 Typ. drain-source on-state resistance: used α value clarified
Revision 1.4	2023-06-15	Ratings of Gate Source Voltage V_{GS} refined in footnote ²⁾
Revision 1.4	2023-06-15	Corrected diagram 3 safe operating area
Revision 1.4	2023-06-15	Corrected diagram 10 typical capacitances

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