THE DATASHEET OF

ISL28217FBZ-T7

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ISL28117, ISL28217, ISL28417, ISL28417SEH

40V Precision Low Power Operational Amplifiers

FN6632
Rev.13.00
Sep 13, 2019

The ISL28117, ISL28217, ISL28417, and ISL28417SEH are a family of very high precision amplifiers featuring low noise vs power consumption, low offset voltage, low bias current, and low temperature drift making them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of precision, low noise, and small footprint provides you with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial controls.

The ISL28117 single and ISL28217 dual are offered in 8 Ld SOIC, MSOP and TDFN packages. The ISL28417 is offered in 14 Ld SOIC, 14 Ld TSSOP packages. All devices are offered in standard pin configurations and operate across the extended temperature range from -40°C to +125°C.

The ISL28417SEH is offered in a 14 Ld Hermetic Ceramic Flatpack package. The device is offered in an industry standard pin configuration and operates across the extended temperature range from -55°C to +125°C.

Related Literature

For a full list of related documents, visit our website

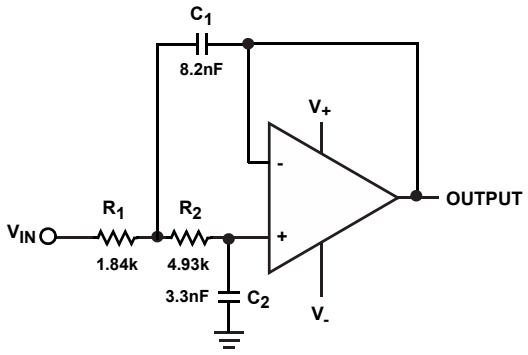
- ISL28117, ISL28217, ISL28417, and ISL28417SEH device pages

Features

- Low input offset voltage . . . . . ±50µV, maximum
  ISL28417SEH ±110µV, maximum
- Superb offset voltage TC . . . . . 0.6µV/°C, maximum
  ISL28417SEH 1µV/°C, maximum
- Input bias current . . . . . ±1nA, maximum
  ISL28417SEH ±5nA, maximum
- Input bias current TC . . . . . ±5pA/°C, maximum
- Low current consumption 440µA
- Voltage noise 8nV/Hz
- Wide supply range . . . . . 4.5V to 40V
- Operating temperature range. . . . . -40°C to +125°C
  ISL28417SEH -55°C to +125°C
- Small package offerings in single, dual and quad
- Pb-free (RoHS compliant)
- No phase reversal

Applications

- Precision instruments
- Medical instrumentation
- Power supply control
- Active filter blocks
- Thermocouples and RTD reference buffers
- Data acquisition



SALLEN-KEY LOW PASS FILTER (10kHz)

FIGURE 1. TYPICAL APPLICATION

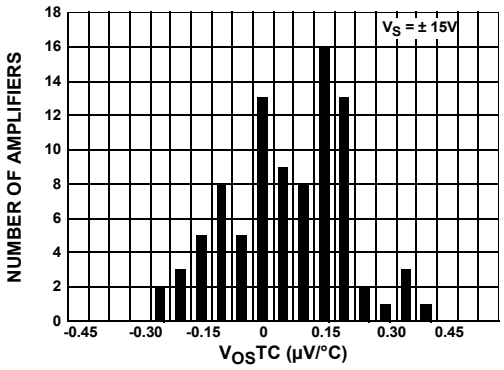


FIGURE 2. V_{OS} TEMPERATURE COEFFICIENT ($V_{OS}TC$)

Table of Contents

Ordering Information

PART NUMBER (Notes 2, 5)	PART MARKING	V_{OS} (MAX) (µV)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL28117FBBZ	28117 FBZ	50 (B Grade)	-	8 Ld SOIC	M8.15E
ISL28117FBBZ-T13	28117 FBZ	50 (B Grade)	2.5k	8 Ld SOIC	M8.15E
ISL28117FBBZ-T7	28117 FBZ	50 (B Grade)	1k	8 Ld SOIC	M8.15E
ISL28117FBBZ-T7A	28117 FBZ	50 (B Grade)	250	8 Ld SOIC	M8.15E
ISL28117FBZ	28117 FBZ -C	100 (C Grade)	-	8 Ld SOIC	M8.15E
ISL28117FBZ-T13	28117 FBZ -C	100 (C Grade)	2.5k	8 Ld SOIC	M8.15E
ISL28117FBZ-T7	28117 FBZ -C	100 (C Grade)	1k	8 Ld SOIC	M8.15E
ISL28117FBZ-T7A	28117 FBZ -C	100 (C Grade)	250	8 Ld SOIC	M8.15E
ISL28117FUBZ	8117Z	70 (B Grade)	-	8 Ld MSOP	M8.118B
ISL28117FUBZ-T13	8117Z	70 (B Grade)	2.5k	8 Ld MSOP	M8.118B
ISL28117FUBZ-T7	8117Z	70 (B Grade)	1.5k	8 Ld MSOP	M8.118B
ISL28117FUBZ-T7A	8117Z	70 (B Grade)	250	8 Ld MSOP	M8.118B
ISL28117FUZ	8117Z -C	150 (C Grade)	-	8 Ld MSOP	M8.118B
ISL28117FUZ-T13	8117Z -C	150 (C Grade)	2.5k	8 Ld MSOP	M8.118B
ISL28117FUZ-T7	8117Z -C	150 (C Grade)	1.5k	8 Ld MSOP	M8.118B
ISL28117FUZ-T7A	8117Z -C	150 (C Grade)	250	8 Ld MSOP	M8.118B
ISL28117FRTBZ	8117	75 (B Grade)	-	8 Ld TDFN	L8.3x3K
ISL28117FRTBZ-T13	8117	75 (B Grade)	6k	8 Ld TDFN	L8.3x3K
ISL28117FRTBZ-T7	8117	75 (B Grade)	1k	8 Ld TDFN	L8.3x3K
ISL28117FRTBZ-T7A	8117	75 (B Grade)	250	8 Ld TDFN	L8.3x3K
ISL28117FRTZ	-C 8117	150 (C Grade)	-	8 Ld TDFN	L8.3x3K
ISL28117FRTZ-T13	-C 8117	150 (C Grade)	2.5k	8 Ld TDFN	L8.3x3K
ISL28117FRTZ-T7	-C 8117	150 (C Grade)	1k	8 Ld TDFN	L8.3x3K
ISL28117FRTZ-T7A	-C 8117	150 (C Grade)	250	8 Ld TDFN	L8.3x3K
ISL28217FBBZ	28217 FBZ	50 (B Grade)	-	8 Ld SOIC	M8.15E
ISL28217FBBZ-T13	28217 FBZ	50 (B Grade)	2.5k	8 Ld SOIC	M8.15E
ISL28217FBBZ-T7	28217 FBZ	50 (B Grade)	1k	8 Ld SOIC	M8.15E
ISL28217FBBZ-T7A	28217 FBZ	50 (B Grade)	250	8 Ld SOIC	M8.15E
ISL28217FBZ	28217 FBZ -C	100 (C Grade)	-	8 Ld SOIC	M8.15E
ISL28217FBZ-T13	28217 FBZ -C	100 (C Grade)	2.5k	8 Ld SOIC	M8.15E
ISL28217FBZ-T7	28217 FBZ -C	100 (C Grade)	1k	8 Ld SOIC	M8.15E
ISL28217FBZ-T7A	28217 FBZ -C	100 (C Grade)	250	8 Ld SOIC	M8.15E
ISL28217FUZ	8217Z -C	150 (C Grade)	-	8 Ld MSOP	M8.118B
ISL28217FUZ-T13	8217Z -C	150 (C Grade)	2.5k	8 Ld MSOP	M8.118B
ISL28217FUZ-T7	8217Z -C	150 (C Grade)	1k	8 Ld MSOP	M8.118B
ISL28217FUZ -T7A	8217Z -C	150 (C Grade)	250	8 Ld MSOP	M8.118B
ISL28217FRTBZ	8217	70 (B Grade)	-	8 Ld TDFN	L8.3x3K
ISL28217FRTBZ-T13	8217	70 (B Grade)	2.5k	8 Ld TDFN	L8.3x3K
ISL28217FRTBZ-T7	8217	70 (B Grade)	1k	8 Ld TDFN	L8.3x3K
ISL28217FRTZ	-C 8217	150 (C Grade)	-	8 Ld TDFN	L8.3x3K

Ordering Information

PART NUMBER (Notes 2, 5)	PART MARKING	V_{OS} (MAX) (µV)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL28217FRTZ-T13	-C 8217	150 (C Grade)	2.5k	8 Ld TDFN	L8.3x3K
ISL28217FRTZ-T7	-C 8217	150 (C Grade)	1k	8 Ld TDFN	L8.3x3K
ISL28417FBBZ	28417 FBZ	120 (B Grade)	-	14 Ld SOIC	MDP0027
ISL28417FBBZ-T13	28417 FBZ	120 (B Grade)	2.5k	14 Ld SOIC	MDP0027
ISL28417FBBZ-T7	28417 FBZ	120 (B Grade)	1k	14 Ld SOIC	MDP0027
ISL28417FBBZ-T7A	28417 FBZ	120 (B Grade)	250	14 Ld SOIC	MDP0027
ISL28417FBZ	28417 FBZ -C	200 (C Grade)	-	14 Ld SOIC	MDP0027
ISL28417FBZ-T13	28417 FBZ -C	200 (C Grade)	2.5k	14 Ld SOIC	MDP0027
ISL28417FBZ-T7	28417 FBZ -C	200 (C Grade)	1k	14 Ld SOIC	MDP0027
ISL28417FBZ-T7A	28417 FBZ -C	200 (C Grade)	250	14 Ld SOIC	MDP0027
ISL28417FVBZ	28417 FVZ	120 (B Grade)	-	14 Ld TSSOP	M14.173
ISL28417FVBZ-T13	28417 FVZ	120 (B Grade)	2.5k	14 Ld TSSOP	M14.173
ISL28417FVBZ-T7	28417 FVZ	120 (B Grade)	1k	14 Ld TSSOP	M14.173
ISL28417FVBZ-T7A	28417 FVZ	120 (B Grade)	250	14 Ld TSSOP	M14.173
ISL28417FVZ	28417 FVZ-C	200 (C Grade)	-	14 Ld TSSOP	M14.173
ISL28417FVZ-T13	28417 FVZ-C	200 (C Grade)	2.5k	14 Ld TSSOP	M14.173
ISL28417FVZ-T7	28417 FVZ-C	200 (C Grade)	1k	14 Ld TSSOP	M14.173
ISL28417FVZ-T7A	28417 FVZ-C	200 (C Grade)	250	14 Ld TSSOP	M14.173
ISL28417SEHMF (Note 3)	ISL28417SEHMF	110 (B Grade)	-	14 Ld Flatpack	K14.A
ISL28417SEHF/PROTO (Notes 3, 4)	ISL28417SEHF/PROTO	110 (B Grade)	-	14 Ld Flatpack	K14.A
ISL28417SEHMX		110 (B Grade)	-	DIE	
ISL28417SEHX/SAMPLE (Note 4)		110 (B Grade)	-	DIE	
ISL28117SOICEVAL1Z	Evaluation Board				
ISL28217SOICEVAL2Z	Evaluation Board				

NOTES:

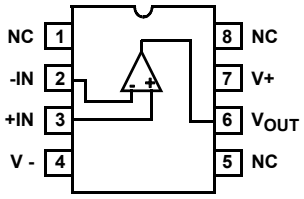
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in this datasheet. The /SAMPLE parts are capable of meeting the electrical limits and conditions at +25°C only. The /SAMPLE parts do not receive 100% screening across temperature to the electrical limits. These part types do not come with a Certificate of Conformance.
5. For Moisture Sensitivity Level (MSL), see the ISL28117, ISL28217, and ISL28417 device pages. For more information about MSL, see TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

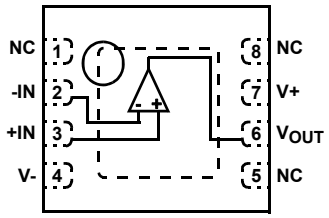
PART NUMBER	NUMBER OF DEVICES	PACKAGE	OPERATING TEMPERATURE RANGE
ISL28117	1	8 Ld SOIC	-40°C to +125°C
ISL28217	2	8 Ld SOIC	-40°C to +125°C
ISL28417	4	14 Ld SOIC	-40°C to +125°C
ISL28417SEH	4	14 Ld Flatpack	-55°C to +125°C

Pin Configurations

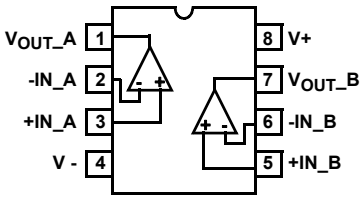
ISL28117
(8 LD SOIC, MSOP)
TOP VIEW



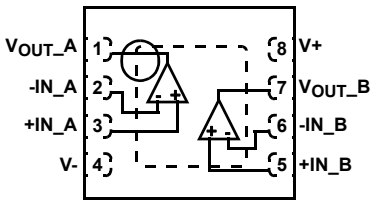
ISL28117
(8 LD TDFN)
TOP VIEW



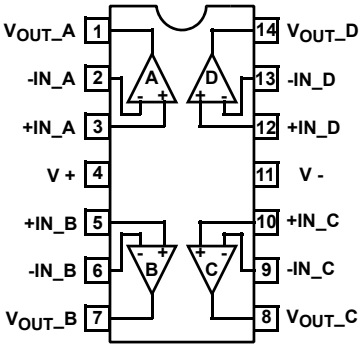
ISL28217
(8 LD SOIC, MSOP)
TOP VIEW



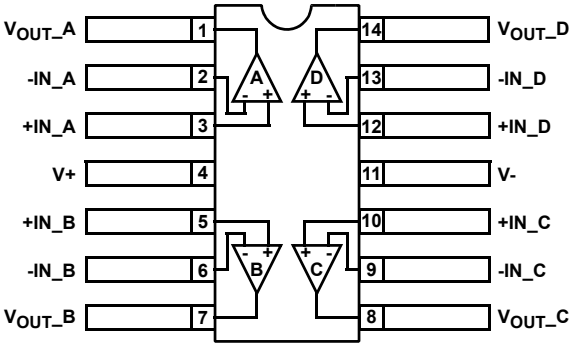
ISL28217
(8 LD TDFN)
TOP VIEW



ISL28417
(14 LD SOIC, TSSOP)
TOP VIEW

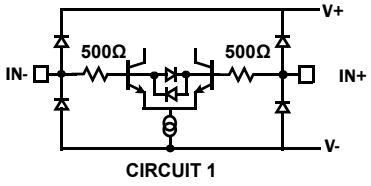


ISL28417SEH
(14 LD FLATPACK)
TOP VIEW

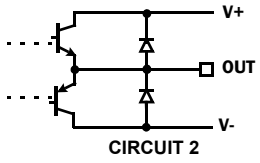


Pin Descriptions

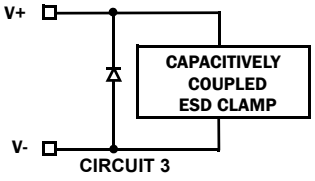
ISL28117 (8 Ld SOIC, MSOP, TDFN)	ISL28217 (8 Ld SOIC, MSOP, TDFN)	ISL28417/SEH (14 Ld SOIC, TSSOP) (14 Ld FLATPACK)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	-	-	+IN	Circuit 1	Amplifier noninverting input
-	3	3	+IN_A		
-	5	5	+IN_B		
-	-	10	+IN_C		
-	-	12	+IN_D		
4	4	11	V-	Circuit 3	Negative power supply
2	-	-	-IN	Circuit 1	Amplifier inverting input
-	2	2	-IN_A		
-	6	6	-IN_B		
-	-	9	-IN_C		
-	-	13	-IN_D		
7	8	4	V+	Circuit 3	Positive power supply
6	-	-	V_{OUT}	Circuit 2	Amplifier output
-	1	1	V_{OUT}_A		
-	7	7	V_{OUT}_B		
-	-	8	V_{OUT}_C		
-	-	14	V_{OUT}_D		
1, 5, 8	-	-	NC	-	No internal connection
PD	PD	-	PD	-	Thermal Pad - TDFN package only. Connect thermal pad to ground or most negative potential.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Supply Voltage ISL28417SEH (Note 12) 40V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage 42V
Maximum Differential Input Voltage (ISL28417SEH) 20V
Min/Max Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
Max/Min Input Current for Input Voltage >V+ or <V- . . . . . ±20mA
Output Short-Circuit Duration (1 output at a time). . . . . Indefinite
ESD Rating
Human Body Model
ISL28117, ISL28417 . . . . . 6kV
ISL28217 . . . . . 4.5kV
ISL28217 MSOP 5.5kV
ISL28417SEH 2kV
Charged Device Model
ISL28117, ISL28217 . . . . . 1.5kV
ISL28217 (MSOP), ISL28417 . . . . . 2kV
ISL28417SEH 1kV
Machine Model
ISL28117, ISL28217 (MSOP) 300V
ISL28217 . . . . . 500V
ISL28417, ISL28417SEH 450V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC ISL28117 (Notes 6, 9)	120	60
8 Ld SOIC ISL28217 (Notes 6, 9)	105	50
8 Ld MSOP ISL28117 (Notes 6, 9)	155	50
8 Ld MSOP ISL28217 (Notes 6, 9)	160	55
8 Ld TDFN ISL28117 (Notes 7, 8)	48	7
8 Ld TDFN ISL28217 (Notes 7, 8)	43	2
14 Ld SOIC (Notes 7, 9)	73	45
14 Ld TSSOP (Notes 6, 9)	90	32
14 Ld Flatpack (Notes 10, 11)	105	15

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +150°C
Pb-Free Reflow Profile (Non-Hermetic Packages Only) . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range (T_A)
ISL28117, ISL28217, ISL28417 . . . . . -40°C to +125°C
ISL28417SEH . . . . . -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See TB379 for details.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See TB379.
8. For θJC, the “case temp” location is the center of the exposed metal pad on the package underside.
9. For θJC, the “case temp” location is taken at the package top center.
10. θJA is measured with the component mounted on a low effective thermal conductivity test board in free air. See TB379 for details.
11. For θJC, the “case temp” location is the center of the ceramic on the package underside.
12. No destructive single-event effects at effective LET of 73.9MeV • cm^2/mg up to a supply of ±20V. Reference manufacturers SEE report.

Electrical Specifications ISL28117, ISL28217, ISL28417 (V_S ± 15V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
V_{OS}	Input Offset Voltage, SOIC, TSSOP Package	ISL28x17 B Grade	-50	8	50	µV
			-110		**110**	µV
		ISL28x17 C Grade	-100	4	100	µV
			-190		**190**	µV
		ISL28417 B Grade	-70	10	70	µV
			-120		**120**	µV
		ISL28417 C Grade	-110	10	110	µV
		T_A = -40°C to +85°C	-160		160	µV
		T_A = -40°C to +125°C	**-200**		**200**	µV
	Input Offset Voltage, MSOP Package	ISL28117 B Grade	-70	-10	70	µV
			-150		**150**	µV
		ISL28117 C Grade	-150	4	150	µV
			-250		**250**	µV
		ISL28217 C Grade	-150	10	150	µV
			-250		**250**	µV
	Input Offset Voltage, TDFN Package	ISL28117 B Grade	-75	-10	75	µV
			-160		**160**	µV
		ISL28217 B Grade	-70	10	70	µV
			-140		**140**	µV
		ISL28x17 C Grade	-150	10	150	µV
			-250		**250**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient; SOIC, TSSOP Package	ISL28x17 B Grade	**-0.6**	0.14	**0.6**	µV/°C
		ISL28x17 C Grade	**-0.9**	0.14	**0.9**	µV/°C
		ISL28417 B Grade	**-0.75**	0.20	**0.75**	µV/°C
		ISL28417 C Grade	**-0.9**	0.3	**0.9**	µV/°C
	Input Offset Voltage Temperature Coefficient; MSOP Package	ISL28117 B Grade	**-0.8**	0.1	**0.8**	µV/°C
		ISL28117 C Grade	**-1**	0.14	**1**	µV/°C
		ISL28217 C Grade	**-1**	0.14	**1**	µV/°C
	Input Offset Voltage Temperature Coefficient; TDFN Package	ISL28117 B Grade	**-0.9**	0.1	**0.9**	µV/°C
		ISL28217 B Grade	**-0.7**	0.1	**0.7**	µV/°C
		ISL28x17 C Grade	**-1**	0.1	**1**	µV/°C
I_B	Input Bias Current		-1	0.08	1	nA
			-1.5		1.5	nA
TCI_B	Input Bias Current Temperature Coefficient		-5	1	5	pA/°C
I_{OS}	Input Offset Current		-1.50	0.08	1.50	nA
			-1.85		**1.85**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient		**-3**	0.42	**3**	pA/°C
		ISL28417 SOIC, TSSOP B and C Grade	**-4.00**	0.45	**4.00**	pA/°C
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	**-13**		**13**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -13V to +13V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±20V	120	145		dB
			120			dB

Electrical Specifications ISL28117, ISL28217, ISL28417 (V_S ± 15V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V, R_L = 10kΩ to ground	130	143		dB
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	13.5	13.7		V
			13.2			V
		R_L = 2kΩ to ground	13.30	13.55		V
			13.1			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-13.7	-13.5	V
					-13.2	V
		R_L = 2kΩ to ground		-13.55	-13.30	V
					-13.1	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit			43		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**±2.25**		**±20**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ		1.5		MHz
e_{nVp-p}	Voltage Noise V_{P-P}	0.1Hz to 10Hz		0.25		μV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		10		nV/√Hz
		f = 100Hz		8.2		nV/√Hz
		f = 1kHz		8		nV/√Hz
		f = 10kHz		8		nV/√Hz
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
THD + N	Total Harmonic Distortion	1kHz, G = 1, V_O = 3.5V_{RMS}, R_L = 2kΩ		0.0009		%
		1kHz, G = 1, V_O = 3.5V_{RMS}, R_L = 10kΩ		0.0005		%
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V = 11, R_L = 2kΩ, V_O = 4V_{P-P}		0.5		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = 50mV_{P-P}, R_L = 10kΩ to V_{CM}		130		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = 50mV_{P-P}, R_L = 10kΩ to V_{CM}		130		ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 10V_{P-P}, R_L = 5kΩ to V_{CM}		21		µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 10V_{P-P}, R_L = 5kΩ to V_{CM}		24		µs
	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 4V_{P-P}, R_L = 5kΩ to V_{CM}		13		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 4V_{P-P}, R_L = 5kΩ to V_{CM}		18		µs
t_{OL}	Output Positive Overload Recovery Time	A_V = -100, V_{IN} = 0.2V_{P-P}, R_L = 2kΩ to V_{CM}		5.6		µs
	Output Negative Overload Recovery Time	A_V = -100, V_{IN} = 0.2V_{P-P}, R_L = 2kΩ to V_{CM}		10.6		µs

Electrical Specifications ISL28117, ISL28217, ISL28417 (V_S ± 5V)

V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
V_{OS}	Input Offset Voltage, SOIC, TSSOP Package	ISL28x17 B Grade	-50	8	50	µV
			-110		**110**	µV
		ISL28x17 C Grade	-100	4	100	µV
			-190		**190**	µV
		ISL28417 B Grade	-70	10	70	µV
			-120		**120**	µV
		ISL28417 C Grade	-110	10	110	µV
		T_A = -40°C to +85°C	-160		160	µV
		T_A = -40°C to +125°C	**-200**		**200**	µV
	Input Offset Voltage, MSOP Package	ISL28117 B Grade	-70	-10	70	µV
			-150		**150**	µV
		ISL28117 C Grade	-150	4	150	µV
			-250		**250**	µV
		ISL28217 C Grade	-150	10	150	µV
			-250		**250**	µV
	Input Offset Voltage, TDFN Package	ISL28117 B Grade	-75	-10	75	µV
			-160		**160**	µV
		ISL28217 B Grade	-70	10	70	µV
			-140		**140**	µV
		ISL28x17 C Grade	-150	10	150	µV
			-250		**250**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient; SOIC, TSSOP Package	ISL28x17 B Grade	**-0.60**	0.14	**0.60**	µV/°C
		ISL28x17 C Grade	**-0.90**	0.14	**0.90**	µV/°C
		ISL28417 B Grade	**-0.75**	0.20	**0.75**	µV/°C
		ISL28417 C Grade	**-0.9**	0.3	**0.9**	µV/°C
	Input Offset Voltage Temperature Coefficient; MSOP Package	ISL28117 B Grade	**-0.8**	0.1	**0.8**	µV/°C
		ISL28117 C Grade	**-1**	0.14	**1**	µV/°C
		ISL28217 C Grade	**-1**	0.14	**1**	µV/°C
	Input Offset Voltage Temperature Coefficient; TDFN Package	ISL28117 B Grade	**-0.9**	0.1	**0.9**	µV/°C
		ISL28217 B Grade	**-0.7**	0.1	**0.7**	µV/°C
		ISL28x17 C Grade	**-1**	0.1	**1**	µV/°C
I_B	Input Bias Current		-1	0.18	1	nA
			-1.5		**1.5**	nA
TCI_B	Input Bias Current Temperature Coefficient		**-5**	1	**5**	pA/°C
I_{OS}	Input Offset Current		-1.5	0.3	1.5	nA
			-1.85		**1.85**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient		-3	0.42	3	pA/°C
		ISL28417 SOIC, TSSOP B and C Grade	**-4.00**	0.45	**4.00**	pA/°C
V_{CM}	Input Voltage Range		**-3**		**3**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -3V to +3V	120	145		dB
			120			dB

Electrical Specifications ISL28117, ISL28217, ISL28417 (V_S ± 5V)

V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	V_O = -3.0V to +3.0V, R_L = 10kΩ to ground	130	143		dB
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	3.5	3.7		V
			3.2			V
		R_L = 2kΩ to ground	3.30	3.55		V
			3.1			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-3.7	-3.5	V
					-3.2	V
		R_L = 2kΩ to ground		-3.55	-3.30	V
					-3.1	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit			43		mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, RL = 2kΩ		1.5		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		0.25		μV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		12		nV/√Hz
		f = 100Hz		8.6		nV/√Hz
		f = 1kHz		8		nV/√Hz
		f = 10kHz		8		nV/√Hz
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V=11, R_L = 2kΩ V_O = $4V_{P-P}$		0.5		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130		ns
t_s	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM}		12		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	AV = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM}		19		µs
t_{OL}	Output Positive Overload Recovery Time	A_V = -100, V_{IN} = $0.2V_{P-P}$ R_L = 2kΩ to V_{CM}		7		µs
	Output Negative Overload Recovery Time	A_V = -100, V_{IN} = $0.2V_{P-P}$ R_L = 2kΩ to V_{CM}		5.8		µs

Electrical Specifications ISL28417SEH (V_S ±15V)

V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the -55°C to +125°C operating temperature range. The limits also define room temperature post-irradiation performance following ^{60}Co irradiation at 0.01rad(Si)/s to a total dose of 50krad(Si) wafer-by-wafer acceptance.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
V_{OS}	Input Offset Voltage			10	85	µV
					110	µV
TCV_{OS}	Offset Voltage Drift			0.1	**1**	µV/°C
I_{IB}	Input Bias Current		-2.5	0.08	2.5	nA
		T_A = -55°C, +125°C	-5		5	nA
		T_A = +25°C, post radiation	-15		15	nA
TCI_{IB}	Input Bias Current Temperature Coefficient		**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current		-2.50	0.08	2.50	nA
		T_A = -55°C, +125°C	-3		3	nA
		T_A = +25°C, post radiation	-6		6	nA
TCI_{OS}	Input Offset Current Temperature Coefficient		**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	**-13**		**13**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -13V to +13V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±20V	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V, R_L = 10kΩ to ground	3,000	14,000		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	13.5	13.7		V
			13.2			V
		R_L = 2kΩ to ground	13.30	13.55		V
			13.0			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-13.7	-13.5	V
					-13.2	V
		R_L = 2kΩ to ground		-13.55	-13.30	V
					-13.0	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit Current			43		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**±2.25**		**±20**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ		1.5		MHz
e_{nVp-p}	Voltage Noise V_{P-P}	0.1Hz to 10Hz		0.25		$µV_{P-P}$
e_n	Voltage Noise Density	f = 10Hz		10		nV/√Hz
		f = 100Hz		8.2		nV/√Hz
		f = 1kHz		8		nV/√Hz
		f = 10kHz		8		nV/√Hz

Electrical Specifications ISL28417SEH (V_S ±15V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the -55°C to +125°C operating temperature range. The limits also define room temperature post-irradiation performance following ^{60}Co irradiation at 0.01rad(Si)/s to a total dose of 50krad(Si) wafer-by-wafer acceptance. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
THD + N	Total Harmonic Distortion	1kHz, G = 1, V_O = 3.5VRMS, R_L = 2kΩ		0.0009		%
		1kHz, G = 1, V_O = 3.5VRMS, R_L = 10kΩ		0.0005		%
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V = 11, R_L = 2kΩ, V_O = 4V_{P-P}	0.3	0.5		V/µs
			0.2			V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = 50mV_{P-P}, R_L = 10kΩ to V_{CM}		130	450	ns
					625	ns
	Fall Time 90% to 10% of VOUT	A_V = 1, V_{OUT} = 50mV_{P-P}, R_L = 10kΩ to V_{CM}		130	600	ns
					700	ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	AV = -1, V_{OUT} = 10V_{P-P}, R_L = 5kΩ to V_{CM}		21		µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 10V_{P-P}, R_L = 5kΩ to V_{CM}		24		µs
	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 4V_{P-P}, R_L = 5kΩ to V_{CM}		13		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = 4V_{P-P}, R_L = 5kΩ to V_{CM}		18		µs
t_{OL}	Output Positive Overload Recovery Time	A_V = -100, V_{IN} = 0.2V_{P-P}, R_L = 2kΩ to V_{CM}		5.6		µs
	Output Negative Overload Recovery Time	A_V = -100, V_{IN} = 0.2V_{P-P}, R_L = 2kΩ to V_{CM}		10.6		µs
OS+	Positive Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		15		%
					33	%
OS-	Negative Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		15		%
					33	%

Electrical Specifications ISL28417SEH (V_S ±5V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the -55°C to +125°C operating temperature range. The limits also define room temperature post-irradiation performance following ^{60}Co irradiation at 0.01rad(Si)/s to a total dose of 50krad(Si) wafer-by-wafer acceptance.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
V_{OS}	Input Offset Voltage			10	150	µV
					250	µV
TCV_{OS}	Offset Voltage Drift			0.1	**1**	µV/°C
I_{IB}	Input Bias Current		-2.50	0.18	2.50	nA
		T_A = -55°C, +125°C	-5		5	nA
		T_A = +25°C, post radiation	-15		15	nA
TCI_{IB}	Input Bias Current Temperature Coefficient		**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current		-2.5	0.3	2.5	nA
		T_A = -55°C, +125°C	-3		3	nA
		T_A = +25°C, post radiation	**6**	**0.42**	**6**	nA

Electrical Specifications ISL28417SEH (V_S ±5V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the -55°C to +125°C operating temperature range. The limits also define room temperature post-irradiation performance following ^{60}Co irradiation at 0.01rad(Si)/s to a total dose of 50krad(Si) wafer-by-wafer acceptance. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
TCI_{OS}	Input Offset Current Temperature Coefficient		**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range		**-3**		**3**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -3V to +3V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	V_O = -3.0V to +3.0V R_L = 10kΩ to ground	3,000	14,000		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	3.5	3.7		V
			3.2			V
		R_L = 2kΩ to ground	3.300	3.550		V
			3.0			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-3.7	-3.5	V
					-3.2	V
		R_L = 2kΩ to ground		-3.55	-3.30	V
					-3.0	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit Current			43		mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ		1.5		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		0.25		μV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		12		nV/√Hz
		f = 100Hz		8.6		nV/√Hz
		f = 1kHz		8		nV/√Hz
		f = 10kHz		8		nV/√Hz
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V = 11, R_L = 2kΩ, VO = $4V_{P-P}$		0.5		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	AV = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}		130		ns
t_s	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM}		12		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM}		19		µs

Electrical Specifications ISL28417SEH (V_S ±5V) V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. Boldface limits apply across the -55°C to +125°C operating temperature range. The limits also define room temperature post-irradiation performance following ^{60}Co irradiation at 0.01rad(Si)/s to a total dose of 50krad(Si) wafer-by-wafer acceptance. (Continued)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
t_{OL}	Output Positive Overload Recovery Time	A_V = -100, V_{IN} = 0.2V_{P-P} R_L = 2kΩ to V_{CM}		7		µs
	Output Negative Overload Recovery Time	A_V = -100, V_{IN} = 0.2V_{P-P} R_L = 2kΩ to V_{CM}		5.8		µs
OS+	Positive Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		15		%
OS-	Negative Overshoot	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		15		%

NOTE:

13. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

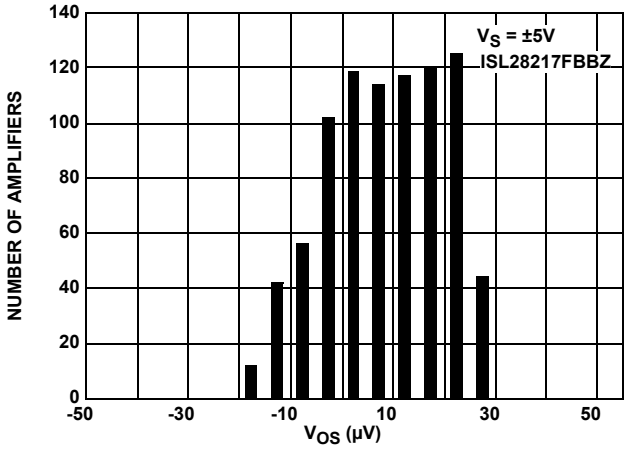


FIGURE 3. V_{OS} DISTRIBUTION FOR GRADE B

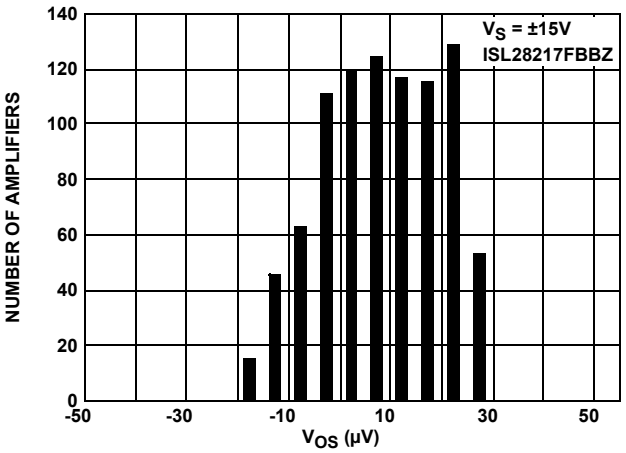


FIGURE 4. V_{OS} DISTRIBUTION FOR GRADE B

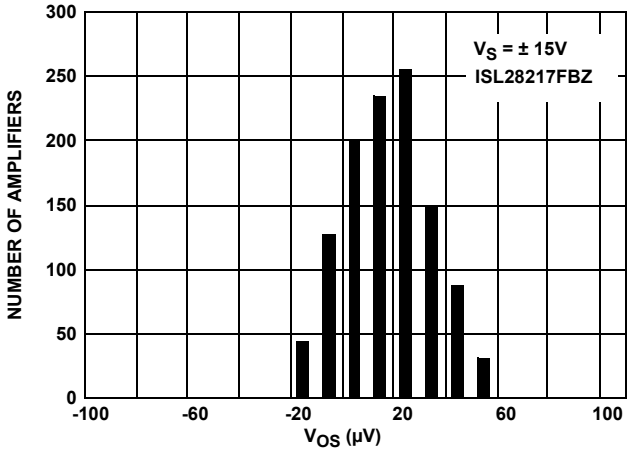


FIGURE 5. V_{OS} DISTRIBUTION FOR GRADE C

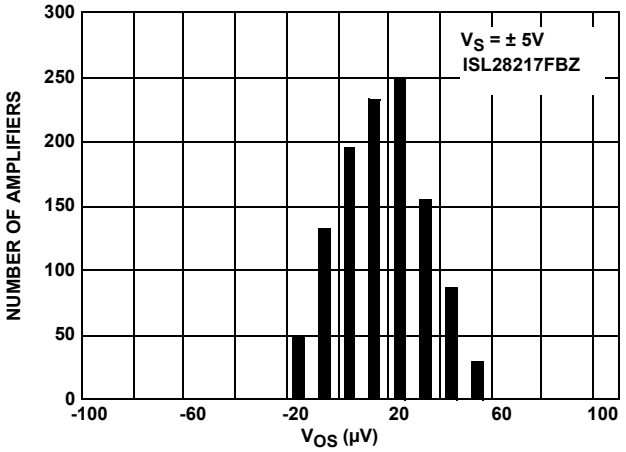


FIGURE 6. V_{OS} DISTRIBUTION FOR GRADE C

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

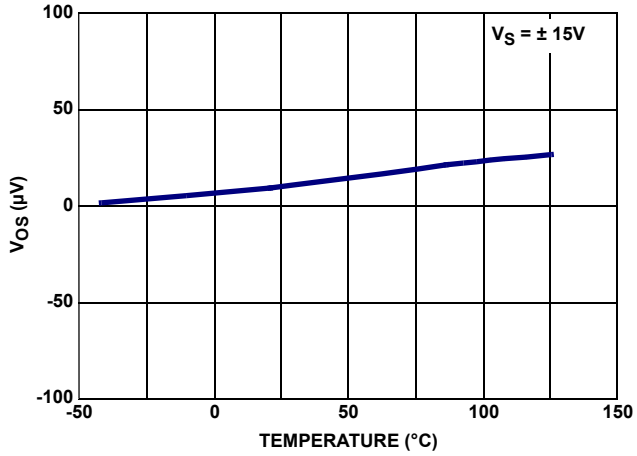


FIGURE 7. V_{OS} RANGE vs TEMPERATURE

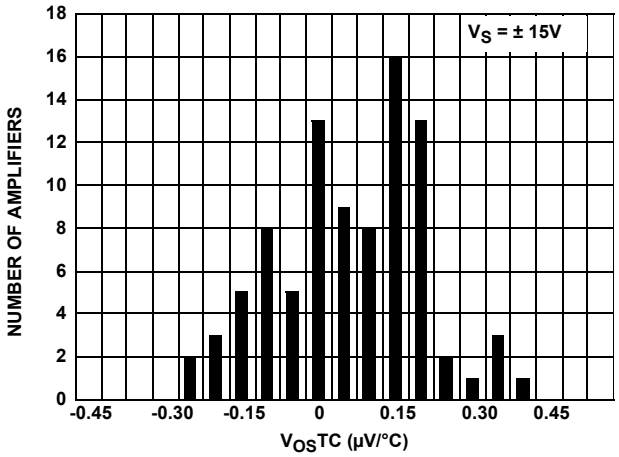


FIGURE 8. TCV_{OS} vs NUMBER OF AMPLIFIERS

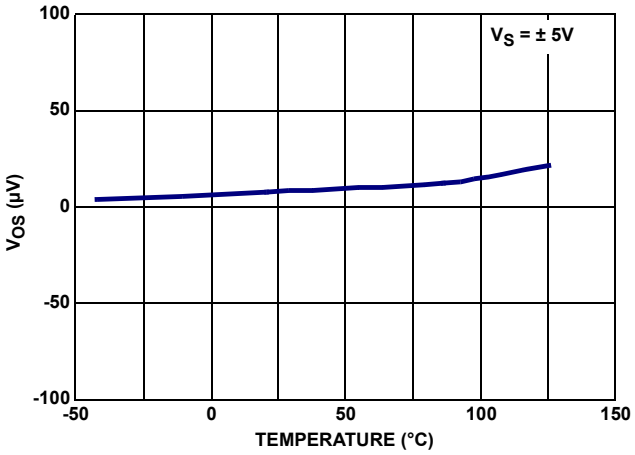


FIGURE 9. V_{OS} RANGE vs TEMPERATURE

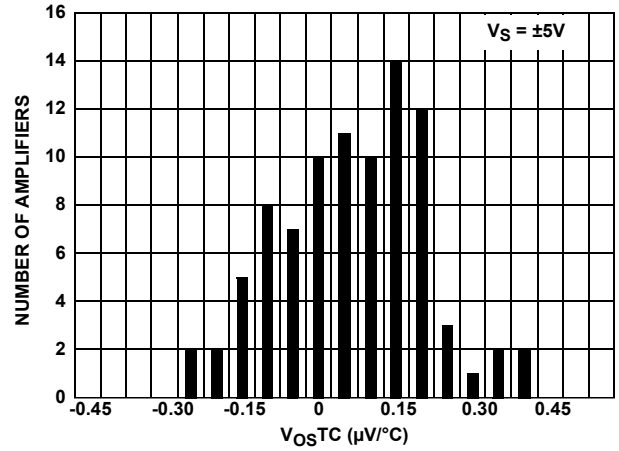


FIGURE 10. TCV_{OS} vs NUMBER OF AMPLIFIERS

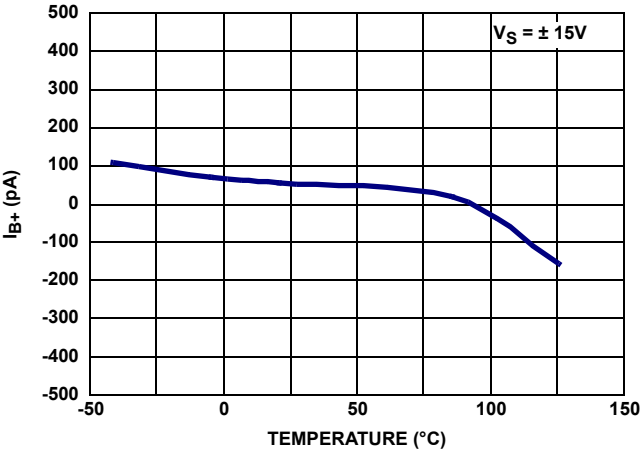


FIGURE 11. I_{B+} RANGE vs TEMPERATURE

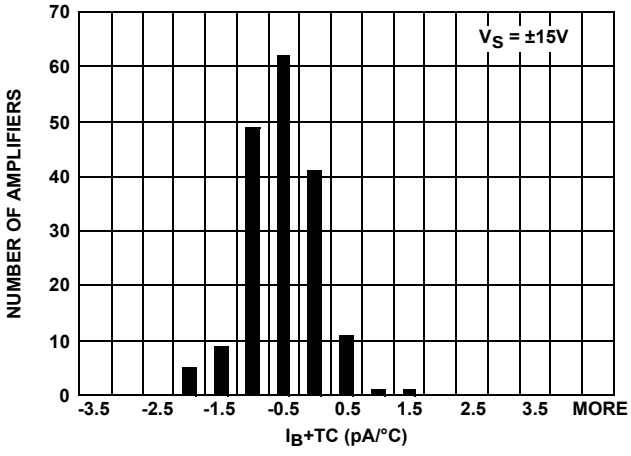


FIGURE 12. TCI_{B+} vs NUMBER OF AMPLIFIERS

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

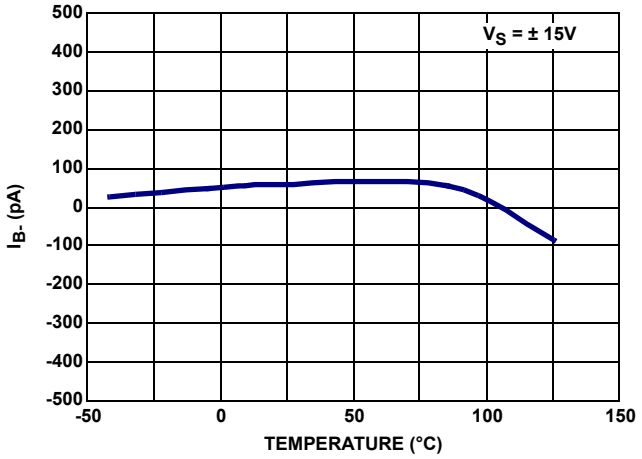


FIGURE 13. I_{B-} RANGE vs TEMPERATURE

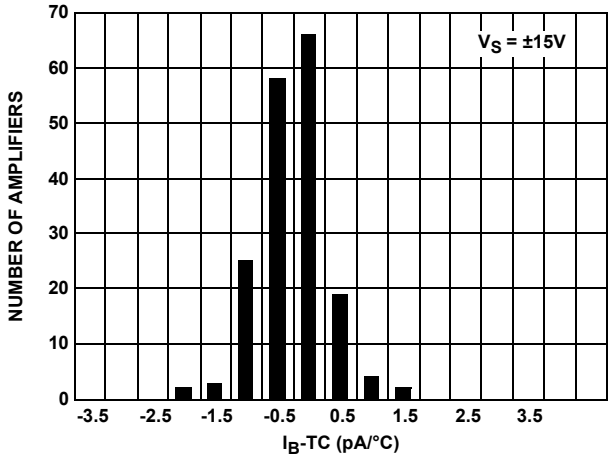


FIGURE 14. TCI_{B-} vs NUMBER OF AMPLIFIERS

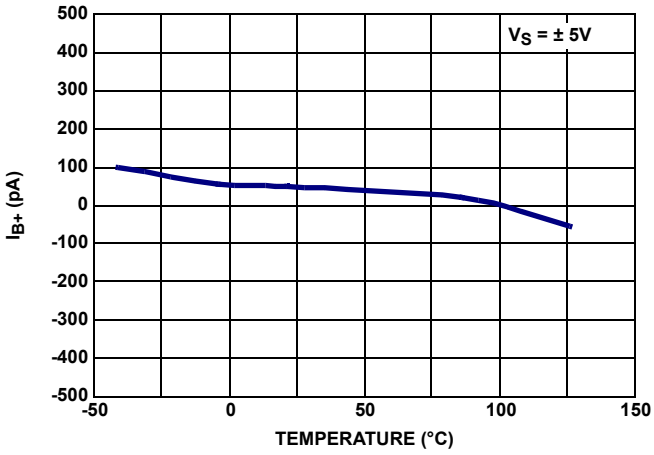


FIGURE 15. I_{B+} RANGE vs TEMPERATURE

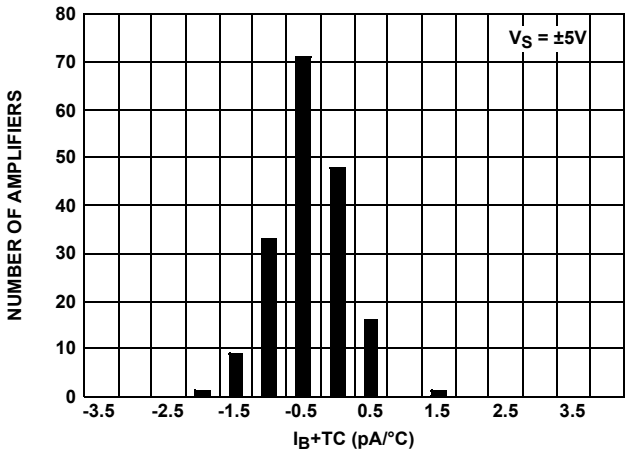


FIGURE 16. TCI_{B+} vs NUMBER OF AMPLIFIERS

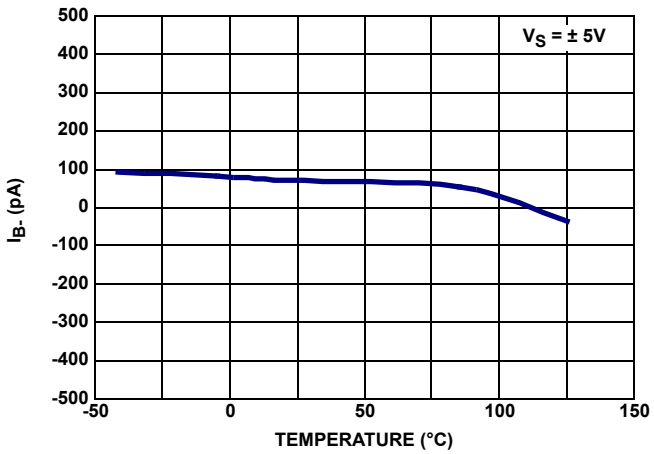


FIGURE 17. I_{B-} RANGE vs TEMPERATURE

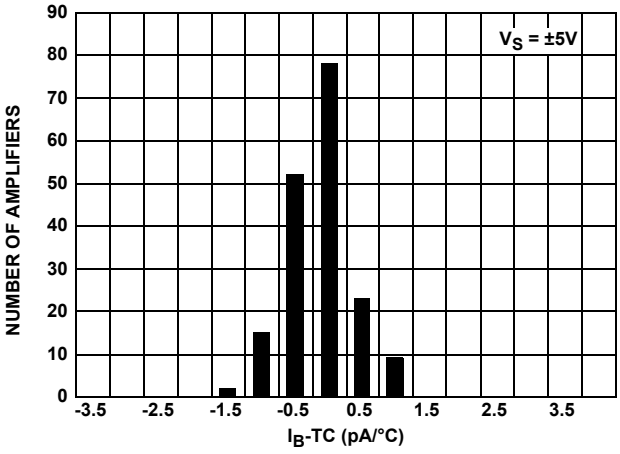


FIGURE 18. TCI_{B-} vs NUMBER OF AMPLIFIERS

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

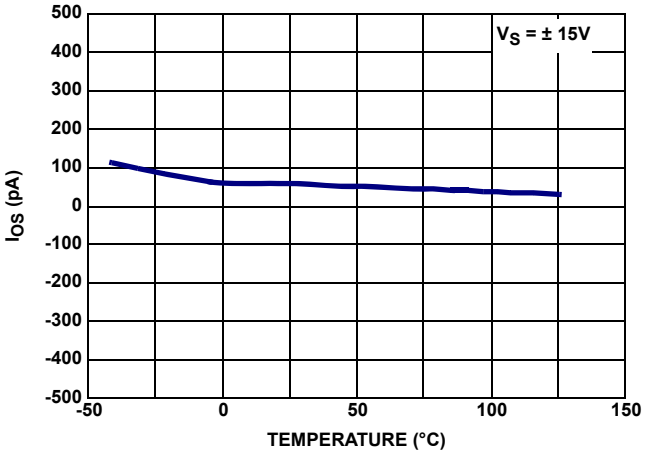


FIGURE 19. I_{OS} RANGE vs TEMPERATURE

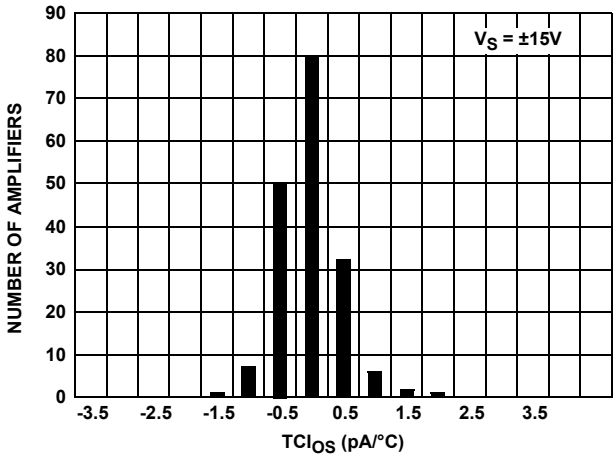


FIGURE 20. $I_{OS}TC$ vs NUMBER OF AMPLIFIERS

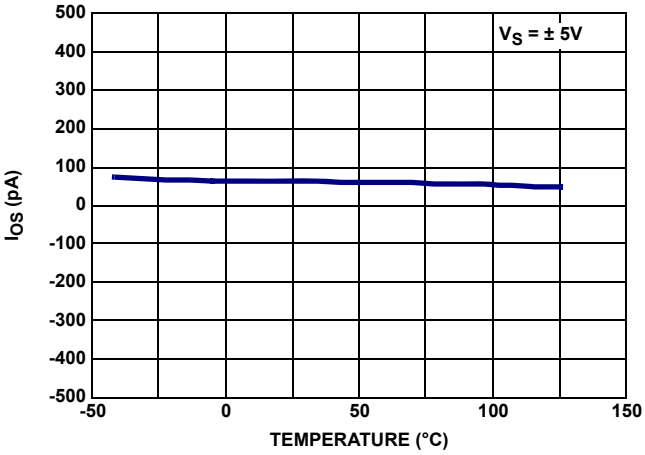


FIGURE 21. I_{OS} RANGE vs TEMPERATURE

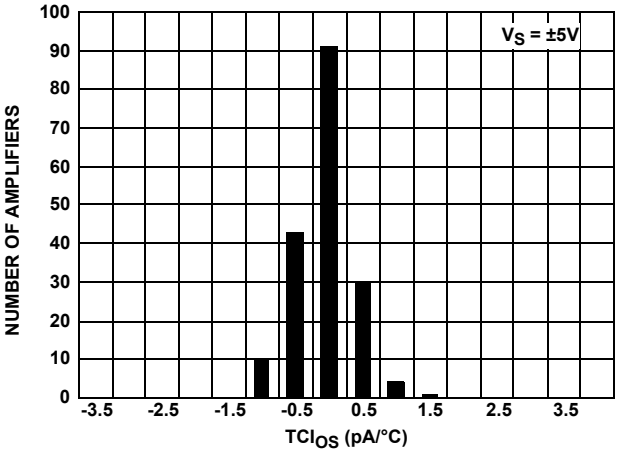


FIGURE 22. $I_{OS}TC$ vs NUMBER OF AMPLIFIERS

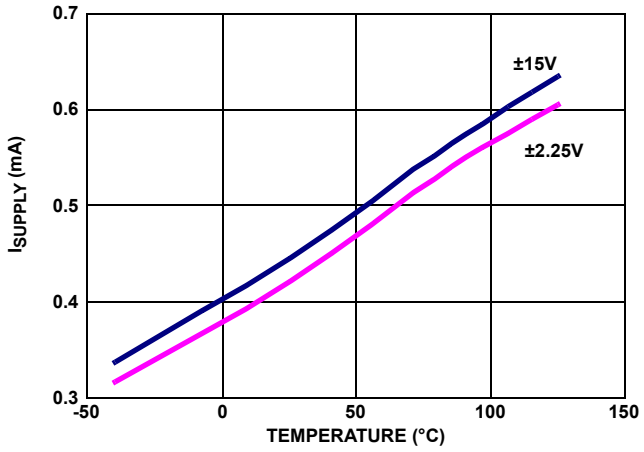


FIGURE 23. SUPPLY CURRENT PER AMPLIFIERS vs TEMPERATURE

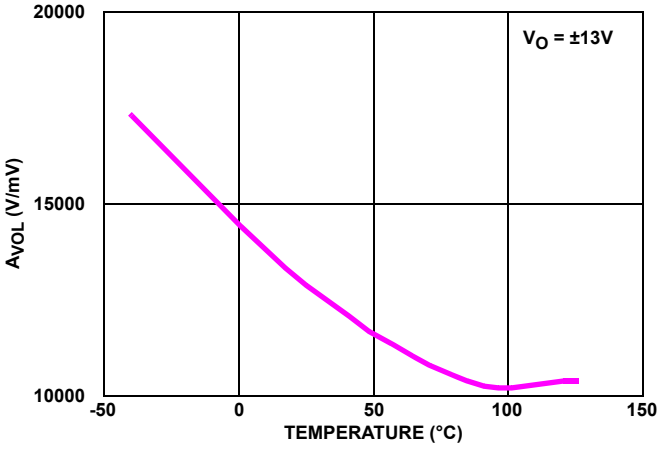


FIGURE 24. A_{VOL} vs TEMPERATURE

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

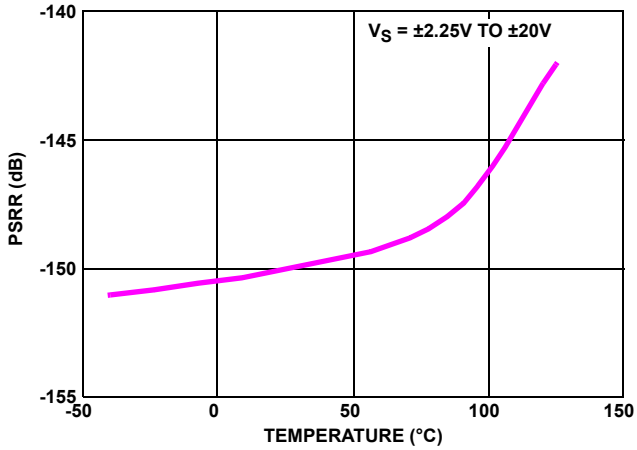


FIGURE 25. PSRR vs TEMPERATURE

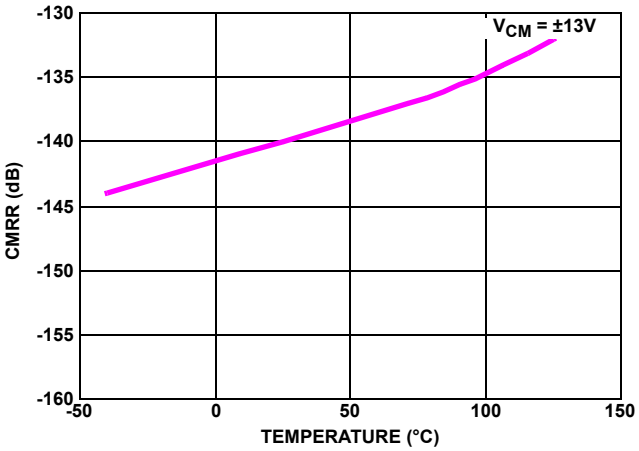


FIGURE 26. CMRR vs TEMPERATURE

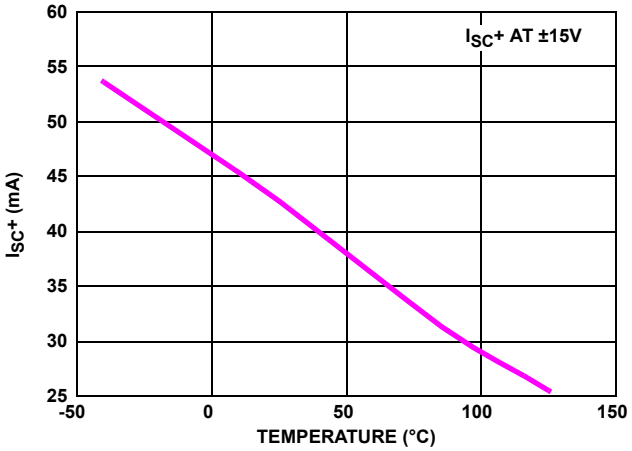


FIGURE 27. POSITIVE SHORT-CIRCUIT CURRENT vs TEMPERATURE

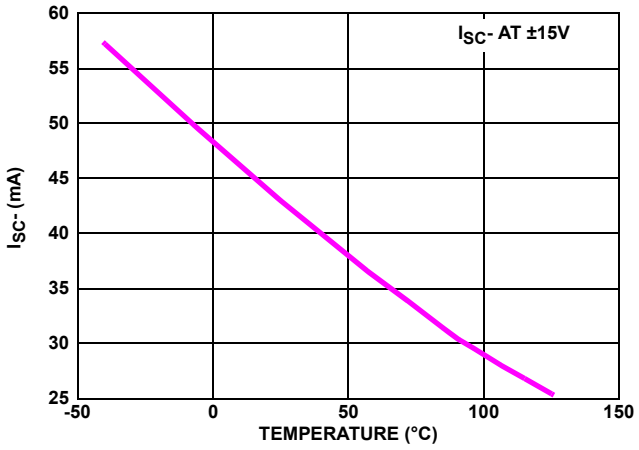


FIGURE 28. NEGATIVE SHORT-CIRCUIT CURRENT vs TEMPERATURE

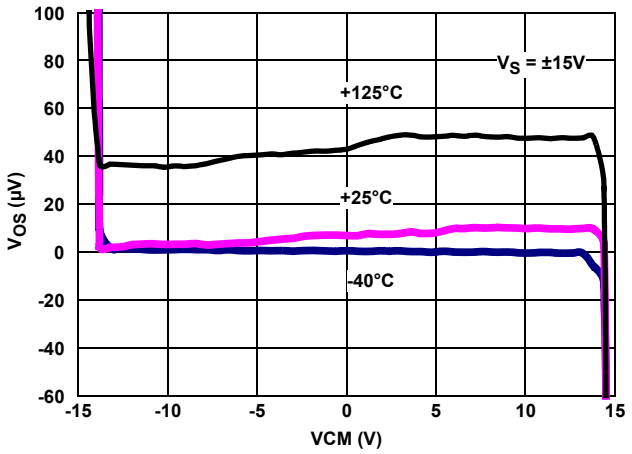


FIGURE 29. INPUT V_{OS} vs INPUT COMMON-MODE VOLTAGE, V_S = ±15

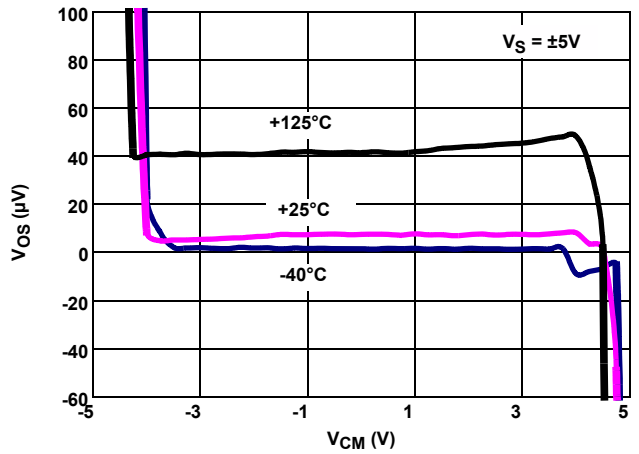


FIGURE 30. INPUT V_{OS} vs INPUT COMMON-MODE VOLTAGE, V_S = ±5V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

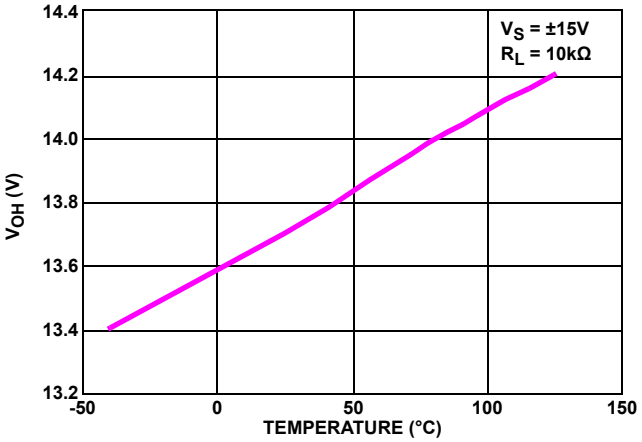


FIGURE 31. V_{OH} vs TEMPERATURE

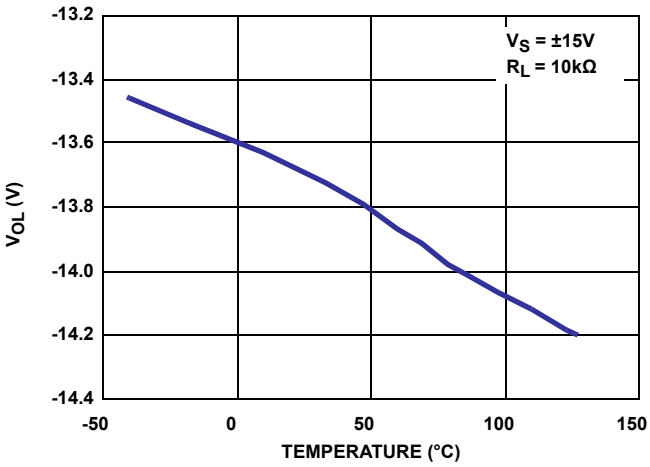


FIGURE 32. V_{OL} vs TEMPERATURE,

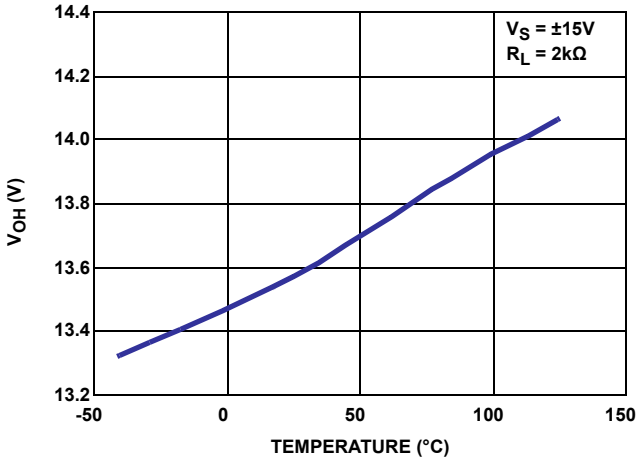


FIGURE 33. V_{OH} vs TEMPERATURE

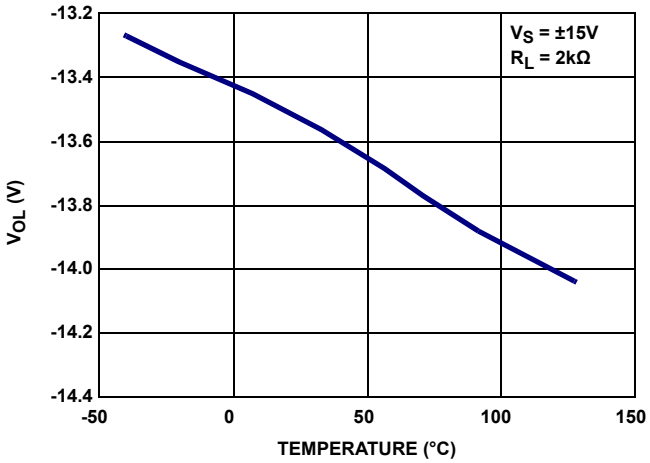


FIGURE 34. V_{OL} vs TEMPERATURE

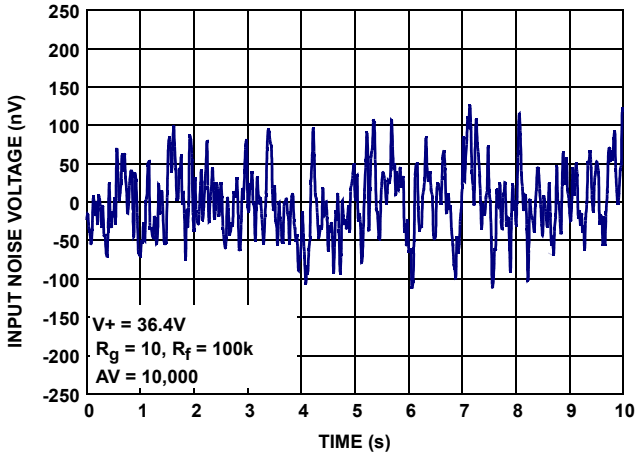


FIGURE 35. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

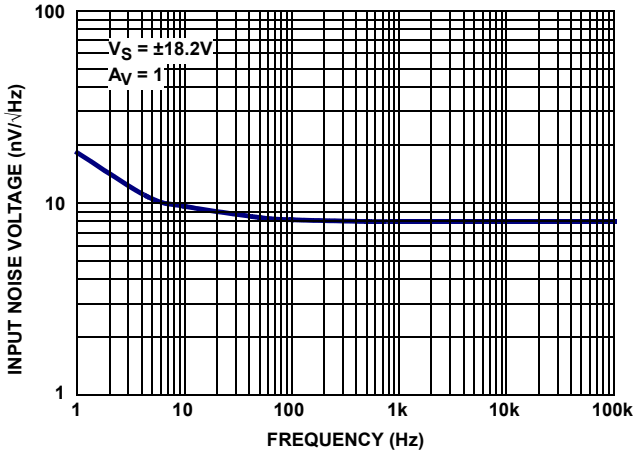


FIGURE 36. INPUT NOISE VOLTAGE SPECTRAL DENSITY

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

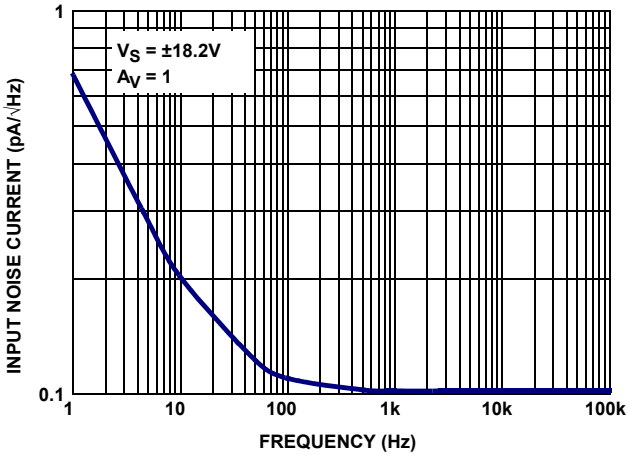


FIGURE 37. INPUT NOISE CURRENT SPECTRAL DENSITY

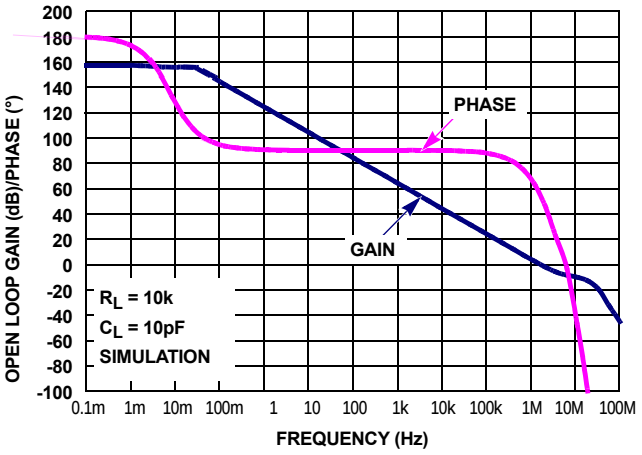


FIGURE 38. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 10pF

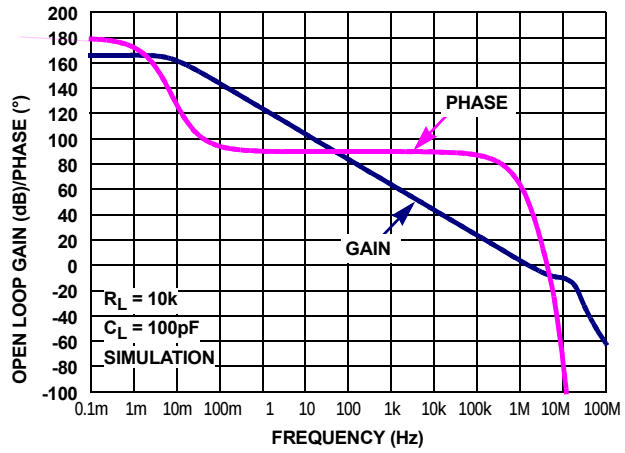


FIGURE 39. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 100pF

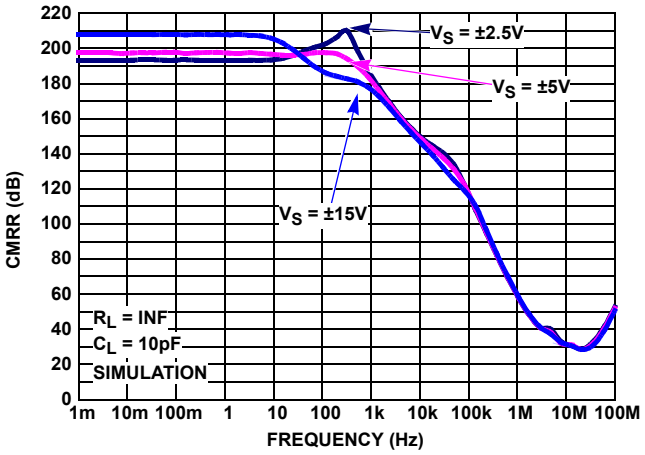


FIGURE 40. CMRR vs FREQUENCY, V_S = ±2.25, ±5V, ±15V

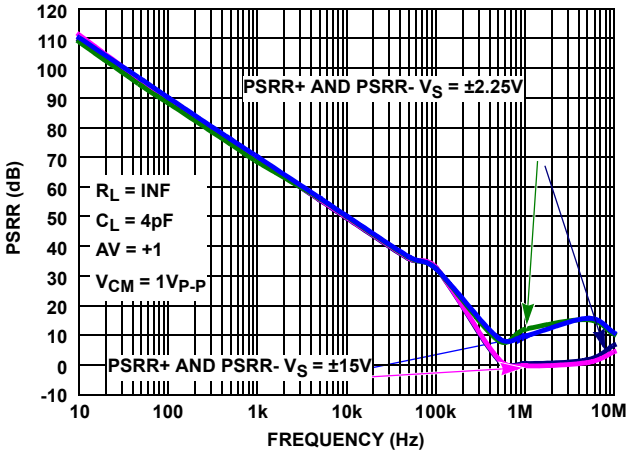


FIGURE 41. PSRR vs FREQUENCY, V_S = ±5V, ±15V

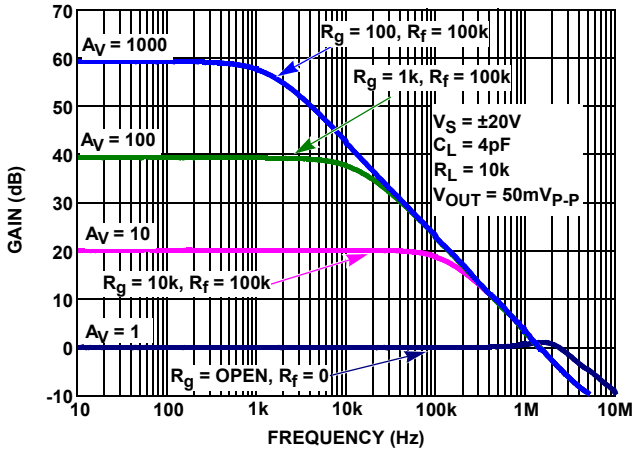


FIGURE 42. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

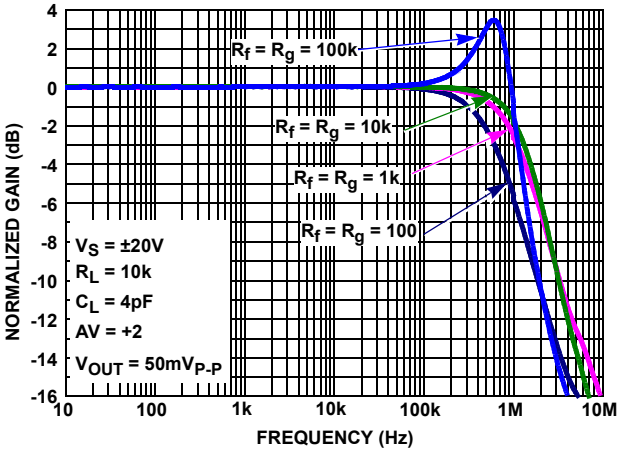


FIGURE 43. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE R_f/R_g

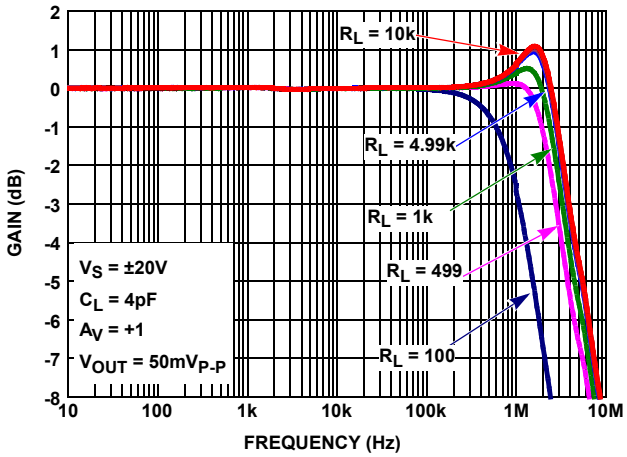


FIGURE 44. GAIN vs FREQUENCY vs R_L

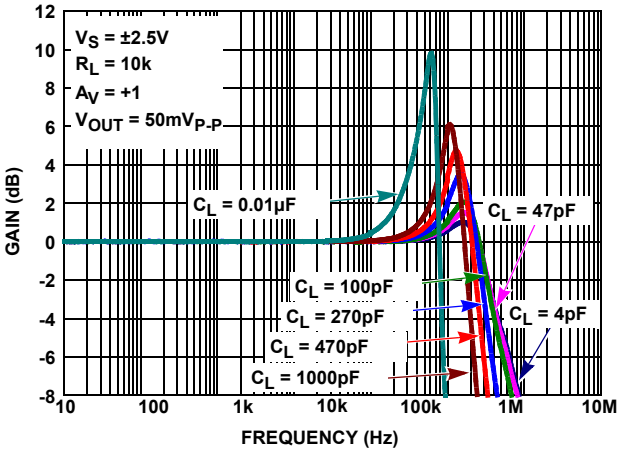


FIGURE 45. GAIN vs FREQUENCY vs C_L

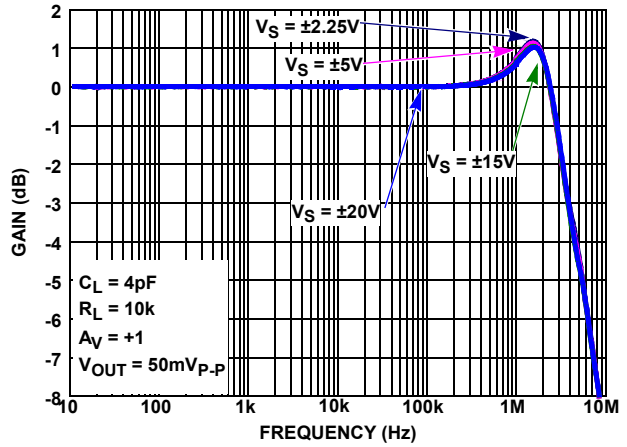


FIGURE 46. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

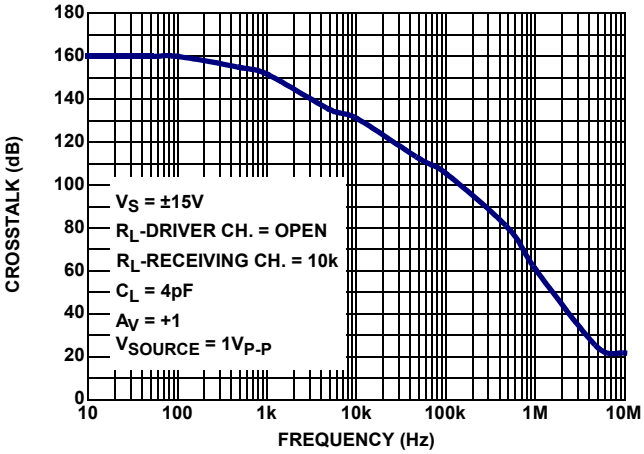


FIGURE 47. CROSSTALK, V_S = ±15V

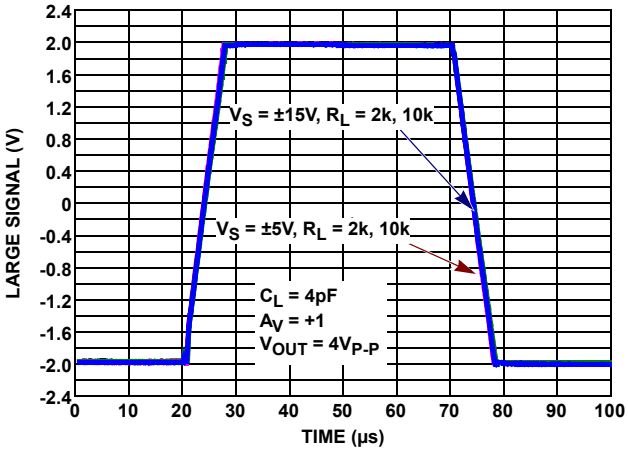


FIGURE 48. LARGE SIGNAL TRANSIENT RESPONSE vs R_L V_S = ±5V, ±15V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

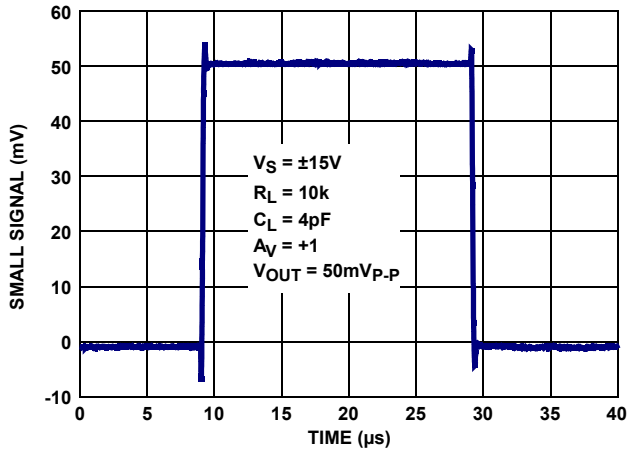


FIGURE 49. SMALL SIGNAL TRANSIENT RESPONSE, V_S = ±5V, ±15V

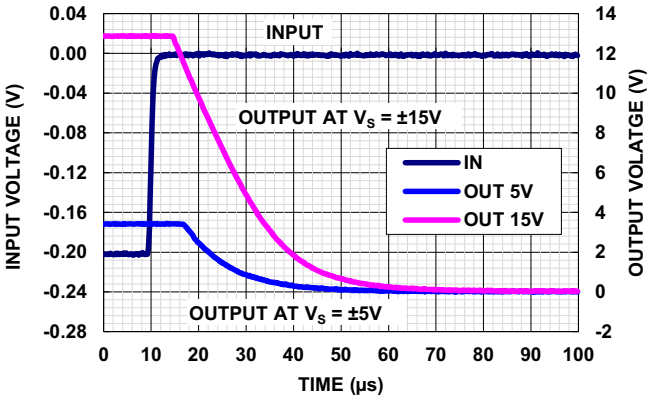


FIGURE 50. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V, ±15V, R_L = 2k, C_L = 4pF, A_V = -100, R_f = 100k, R_g = 1k, V_{IN} = 200mV_{P-P}

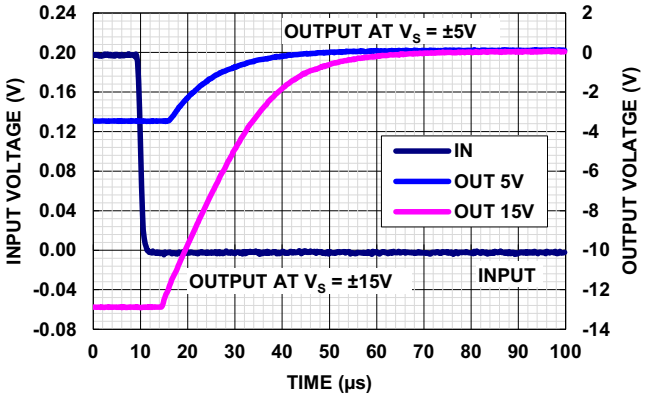


FIGURE 51. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V, ±15V, R_L = 2k, C_L = 4pF, A_V = -100, R_f = 100k, R_g = 1k, V_{IN} = 200mV_{P-P}

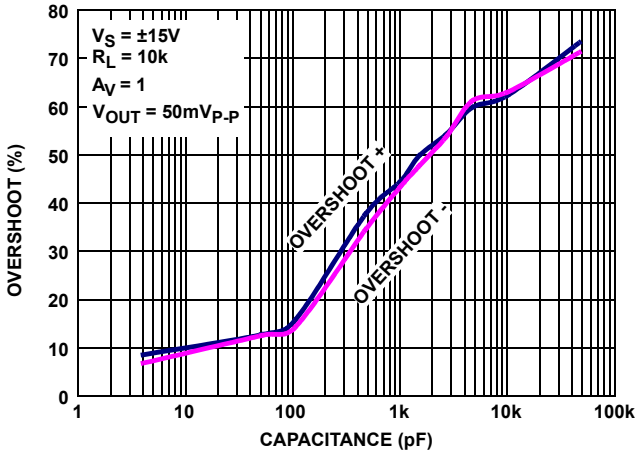


FIGURE 52. % OVERSHOOT vs LOAD CAPACITANCE, V_S = ±15V

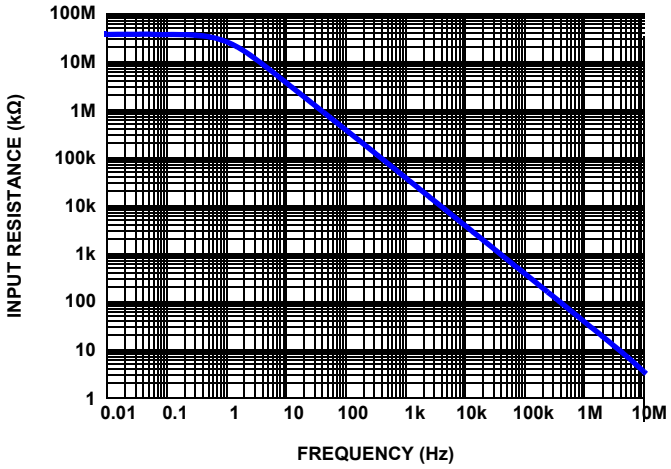


FIGURE 53. COMMON-MODE INPUT IMPEDANCE

Applications Information

Functional Description

The ISL28117, ISL28217, ISL28417, and ISL28417SEH are single, dual and quad, low noise precision op amps. Both devices are fabricated in a new precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (180pA typical), low input offset voltage (13µV typical), low input noise voltage (8nV/√Hz), and low 1/f noise corner frequency (~8Hz). These amplifiers also feature high open loop gain (18kV/mV) for excellent CMRR (145dB) and THD+N performance (0.0005% at $3.5V_{RMS}$, 1kHz into 2kΩ). A complimentary bipolar output stage enables high capacitive load drive without external compensation.

Operating Voltage Range

The devices are designed to operate across the 4.5V (±2.25V) to 40V (±20V) range and are fully characterized at 10V (±5V) and 30V (±15V). The Power Supply Rejection Ratio typically exceeds 140dB across the full operating voltage range and 120dB minimum across the -40°C to +125°C temperature range. The worst case common-mode input voltage range over-temperature is 2V to each rail. With ±15V supplies, CMRR performance is typically >130dB over-temperature. The minimum CMRR performance across the -40°C to +125°C temperature range is >120dB for power supply voltages from ±5V (10V) to ±15V (30V).

Input Performance

The super-beta NPN input pair provides excellent frequency response while maintaining high input precision. High NPN beta (>1000) reduces input bias current while maintaining good frequency response, low input bias current and low noise. Input bias cancellation circuits provide additional bias current reduction to <1nA and excellent temperature stabilization. Figures 11 through 18 show the high degree of bias current stability at ±5V and ±15V supplies that is maintained across the -40°C to +125°C temperature range. The low bias current TC also produces very low input offset current TC, which reduces DC input offset errors in precision, high impedance amplifiers.

The +25°C maximum input offset voltage (V_{OS}) for the “B” grade is 50µV and 100µV for the “C” grade. Input offset voltage temperature coefficients ($V_{OS}TC$) are a maximum of ±0.6µV/°C for the “B” and ±0.9µV/°C for the “C” grade. Figures 3 through 6 show the typical gaussian-like distribution over the ±5V to ±15V supply range and over the full temperature range. The V_{OS} temperature behavior is smooth (Figures 7 through 10) maintaining constant TC across the entire temperature range.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 500Ω current limiting resistors and an anti-parallel diode pair across the inputs (Figure 54).

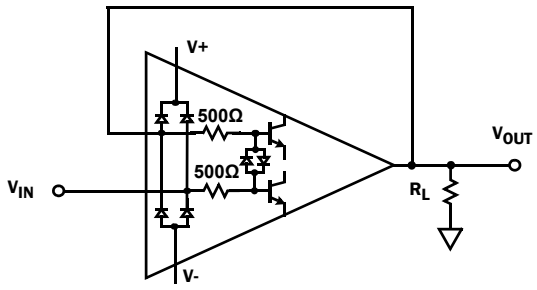


FIGURE 54. INPUT ESD DIODE CURRENT LIMITING- UNITY GAIN

The series resistors limit the high feed-through currents that can occur in pulse applications when the input dv/dt exceeds the 0.5V/µs slew rate of the amplifier. Without the series resistors, the input can forward-bias the anti-parallel diodes causing current to flow to the output resulting in severe distortion and possible diode failure. Figure 48 provides an example of distortion free large signal response using a $4V_{P-P}$ input pulse with an input rise time of <1ns. The series resistors enable the input differential voltage to be equal to the maximum power supply voltage (40V) without damage.

In applications where one or both amplifier input terminals are at risk of exposure to high voltages beyond the power supply rails, current limiting resistors may be needed at the input terminal to limit the current through the power supply ESD diodes to 20mA maximum.

Output Current Limiting

The output current is internally limited to approximately ±45mA at +25°C and can withstand a short-circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long term reliability. Figures 27 and 28 show the current limit variation with temperature.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28117, ISL28217, ISL28417 and ISL28417SEH are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Unused Channels

You must configure unused channel(s) to prevent them from oscillating. The unused channel(s) oscillates if the input and output pins are floating. This results in higher than expected supply currents and possible noise injection into the other channel(s) being used. The proper way to prevent this oscillation is to short the output to the inverting input and ground the positive input, as shown in Figure 55.

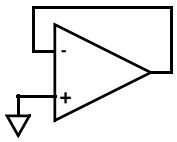


FIGURE 55. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

ISL28117, ISL28217, ISL28417, ISL28417SEH SPICE Model

Figure 56 shows the SPICE model schematic and Figure 57 shows the net list for the ISL28117, ISL28217, ISL28417 and ISL28417SEH SPICE model for a Grade “B” part. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise, Slew Rate, CMRR, Gain and Phase. The DC parameters are VOS, IOS, total supply current and output voltage swing. The model uses typical parameters given in the “Electrical Specifications” table beginning on page 8. The AVOL is adjusted for 155dB with the dominant pole at 0.02Hz. The CMRR is set (210dB, f_{cm} = 10Hz). The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of +25°C.

Figures 58 through 68 show the characterization vs simulation results for the Noise Voltage, Closed Loop Gain vs Frequency, Closed Loop Gain vs RL, Large Signal Step Response, Open Loop Gain Phase and Simulated CMRR vs Frequency.

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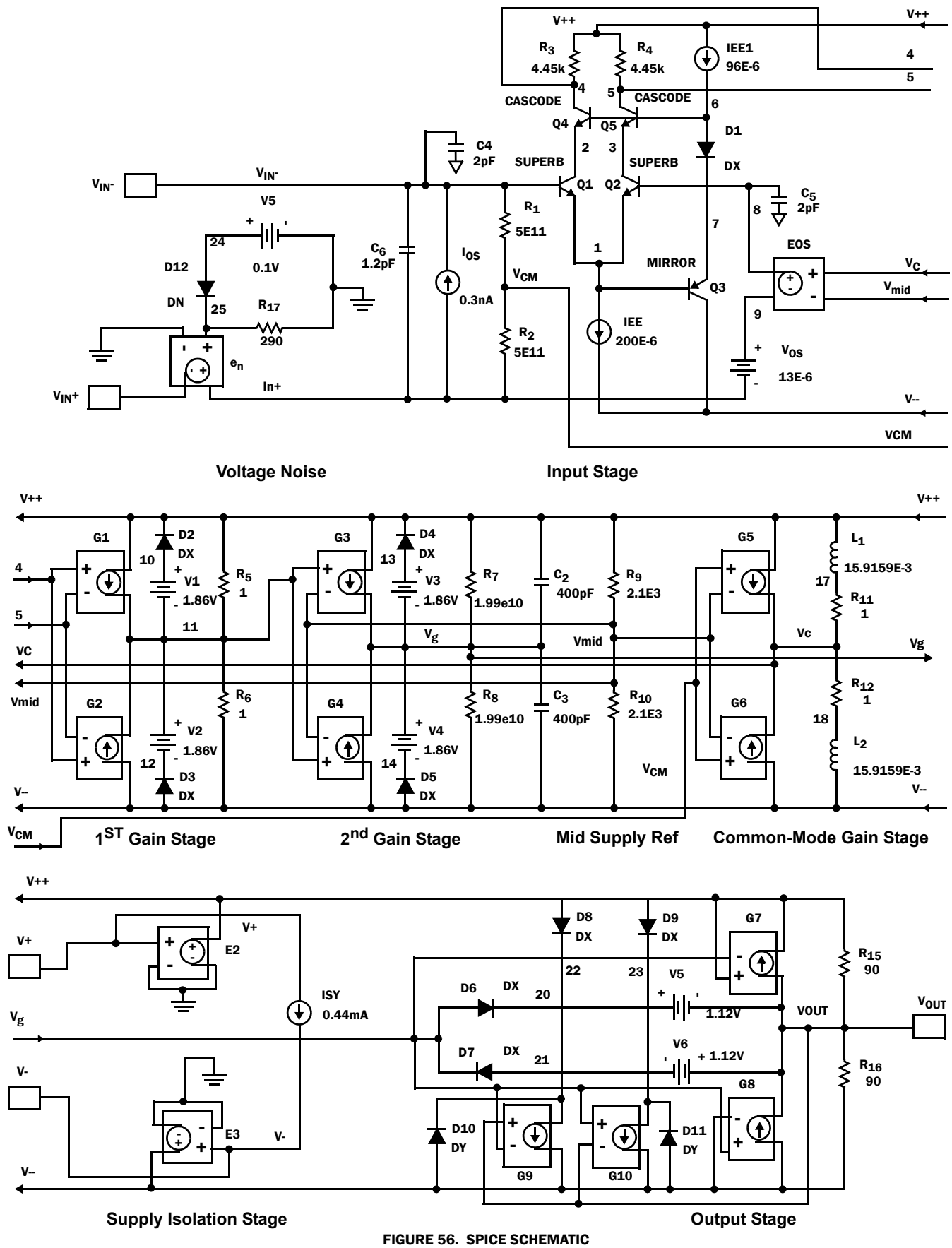

FIGURE 56. SPICE SCHEMATIC

```
*ISL28117 Macromodel - covers following
*products
*ISL28117
*ISL28217
*ISL28417 and ISL28417SEH
**Revision History:
*Revision C, LaFontaine January 31, 2012
*Model for Noise, quiescent supply currents,
*CMRR 210dB, fcm=10Hz, AVOL 155dB
*f=0.02Hz, SR = 0.5V/us, output voltage
*clamp and short ckt current limit.
*
*Copyright 2012 by Intersil Corporation
Refer *to data sheet "LICENSE STATE-
MENT", Use *of this model indicates your
acceptance with *the terms and provisions
in the License *Statement.
*Intended use:
*This Pspice Macromodel is intended to
give
*typical DC and AC performance
*characteristics under a wide range of
*external circuit configurations using
*compatible simulation platforms - such as
*iSim PE.
**
*Device performance features supported by
*this model
*Typical, room temp., nominal power supply
*voltages used to produce the following
*characteristics:
*Open and closed loop I/O impedances
*Open loop gain and phase
*Closed loop bandwidth and frequency
*response
*Loading effects on closed loop frequency
*response
*Input noise terms including 1/f effects
*Slew rate
*Input and Output Headroom limits to I/O
*voltage swing
*Supply current at nominal specified supply
*voltages
**
*Device performance features NOT
*supported by this model:
*Harmonic distortion effects
*Post Radiation effects
*Disable operation (if any)
*Thermal effects and/or over temperature
*parameter variation
*Limited performance variation vs. supply
*voltage is modeled
*Part to part performance variation due to
*normal process parameter spread
*Any performance difference arising from
*different packaging
* source
:
*+input
*|-input
* | | +Vsupply
* | | |-Vsupply
* | | | |output
* | | | | |
.subckt ISL28117 Vin+ Vin- V+ V- VOUT
* source ISL28107subckt
*
*Voltage Noise
E_En        IN+ VIN+ 25 0 1
R_R17        25 0 290
D_D12        24 25 DN
V_V7        24 0 0.1
*
*Input Stage
I_IOS        IN+ VIN- DC 0.08E-9
C_C6        IN+ VIN- 1.2E-12
R_R1        VCM VIN-  5e11
R_R2        IN+ VCM  5e11
Q_Q1         2 VIN- 1 SuperB
Q_Q2         3 8 1 SuperB
Q_Q3         V-- 1 7 Mirror
Q_Q4         4 6 2 Cascode
Q_Q5         5 6 3 Cascode
R_R3         4 V++ 4.45e3
R_R4         5 V++ 4.45e3
C_C4 VIN- 0  2e-12
C_C5 8 0  2e-12
D_D1         6 7 DX
I_IEE        1 V-- DC 200e-6
I_IEE1        V++ 6 DC 96e-6
V_VOS         9 IN+ 8e-6
E_EOS         8 9 VC VMID 1
*
*1st Gain Stage
G_G1         V++ 11 4 5 8.129384e-2
G_G2         V-- 11 4 5 8.129384e-2
R_R5         11 V++ 1
R_R6         V-- 11  1
D_D2         10 V++ DX
D_D3         V-- 12 DX
V_V1         10 11 1.86
V_V2         11 12 1.86
*
*2nd Gain Stage
G_G3         V++ VG 11 VMID 2.83e-3
G_G4         V-- VG 11 VMID 2.83e-3
R_R7         VG V++ 1.99e10
R_R8         V-- VG 1.99e10
C_C2         VG V++ 4e-10
C_C3         V-- VG 4e-10
D_D4         13 V++ DX
D_D5         V-- 14 DX
V_V3         13 VG 1.86
V_V4         VG 14 1.86
*
*Mid supply Ref
R_R9         VMID V++ 2.1E3
R_R10         V-- VMID  2.1E3
I_ISY     V+ V- DC 0.44E-3
E_E2         V++ 0 V+ 0 1
E_E3         V-- 0 V- 0 1
*
*Common Mode Gain Stage with Zero
G_G5         V++ VC VCM VMID 3.162277
G_G6         V-- VC VCM VMID 3.162277
R_R11         VC 17  1
R_R12         18 VC  1
L_L1         17 V++ 15.9159E-3
L_L2         18 V-- 15.9159E-3
*
*Output Stage with Correction Current
Sources
G_G7         VOUT V++ V++ VG 1.11e-2
G_G8         V-- VOUT VG V-- 1.11e-2
G_G9         22 V-- VOUT VG 1.11e-2
G_G10         23 V-- VG VOUT 1.11e-2
D_D6         VG 20 DX
D_D7         21 VG DX
D_D8         V++ 22 DX
D_D9         V++ 23 DX
D_D10         V-- 22 DY
D_D11         V-- 23 DY
V_V5         20 VOUT 1.12
V_V6         VOUT 21 1.12
R_R15         VOUT V++ 9E1
R_R16         V-- VOUT  9E1
*
.model SuperB npn
+ is=184E-15 bf=30e3 va=15 ik=70E-3
rb=50
+ re=0.065 rc=35 cje=1.5E-12 cjc=2E-12
+ kf=0 af=0
.model Cascode npn
+ is=502E-18 bf=150 va=300 ik=17E-3
+rb=140 re=0.011 rc=900 cje=0.2E-12
+cjc=0.16E-12f kf=0 af=0
.model Mirror pnp
+ is=4E-15 bf=150 va=50 ik=138E-3 rb=185
+ re=0.101 rc=180 cje=1.34E-12
+cjc=0.44E-12 kf=0 af=0
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28117
```

FIGURE 57. SPICE NET LIST

Characterization vs Simulation Results

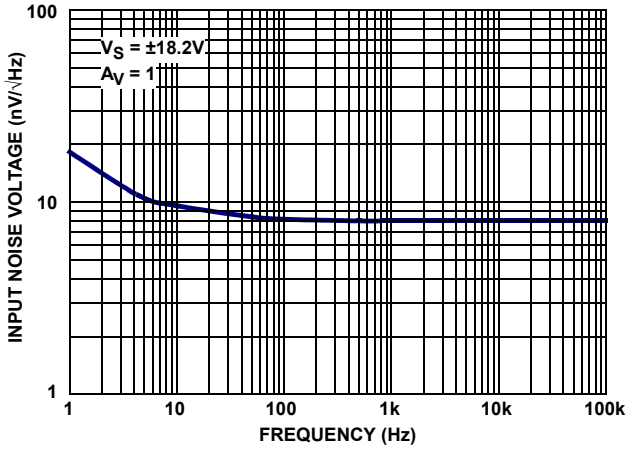

FIGURE 58. CHARACTERIZED INPUT NOISE VOLTAGE

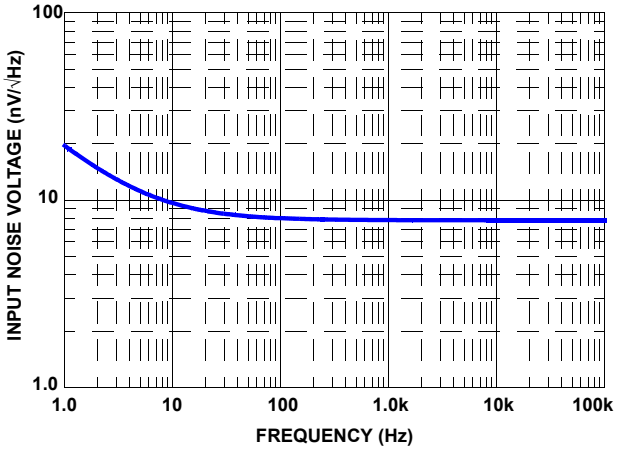

FIGURE 59. SIMULATED INPUT NOISE VOLTAGE

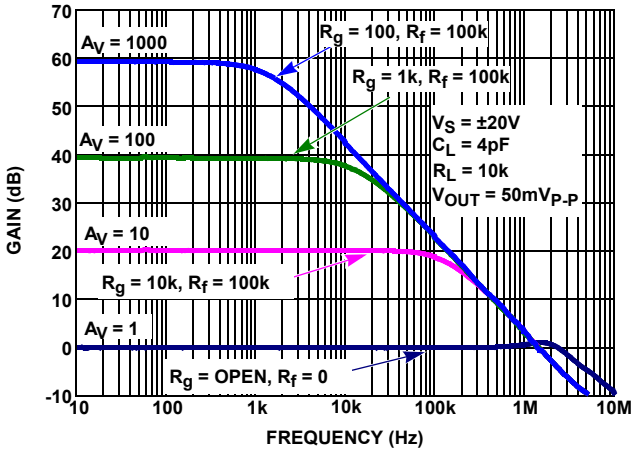

FIGURE 60. CHARACTERIZED CLOSED LOOP GAIN vs FREQUENCY

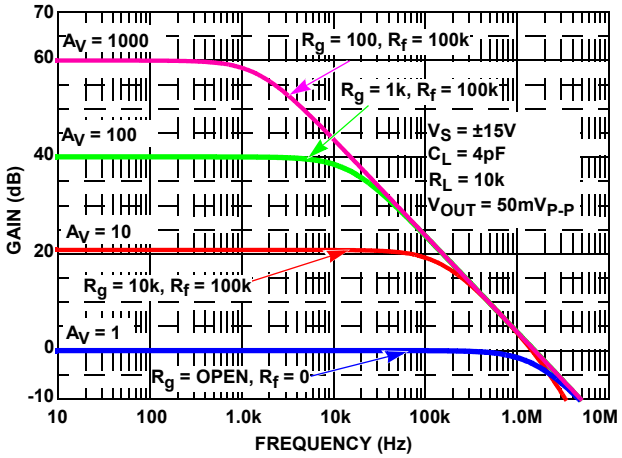

FIGURE 61. SIMULATED CLOSED LOOP GAIN vs FREQUENCY

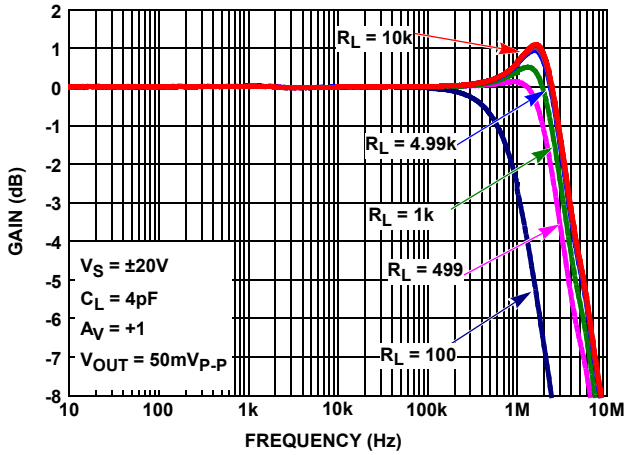

FIGURE 62. CHARACTERIZED CLOSED LOOP GAIN vs R_L

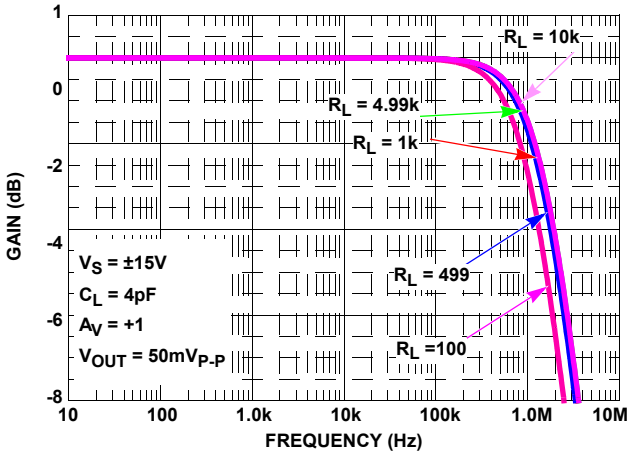

FIGURE 63. SIMULATED CLOSED LOOP GAIN vs R_L

Characterization vs Simulation Results (Continued)

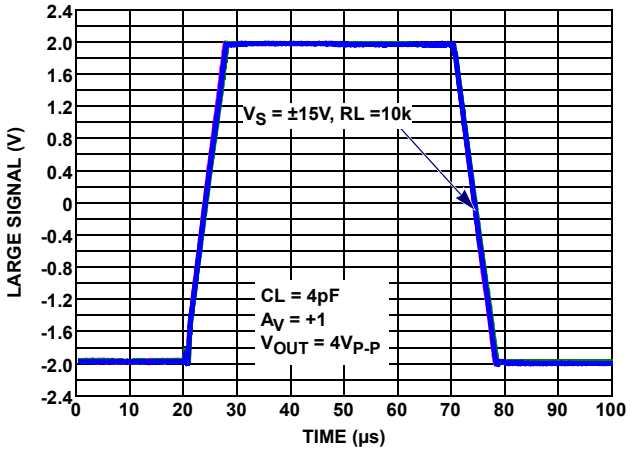

FIGURE 64. CHARACTERIZED LARGE SIGNAL TRANSIENT RESPONSE vs R_L V_S = ±15V

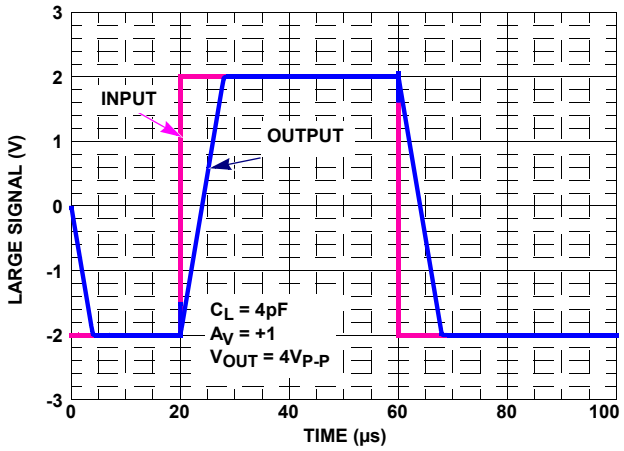

FIGURE 65. SIMULATED LARGE SIGNAL 10V STEP RESPONSE

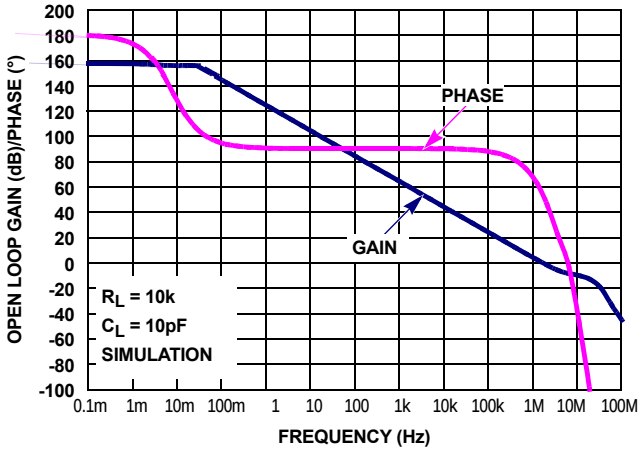

FIGURE 66. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

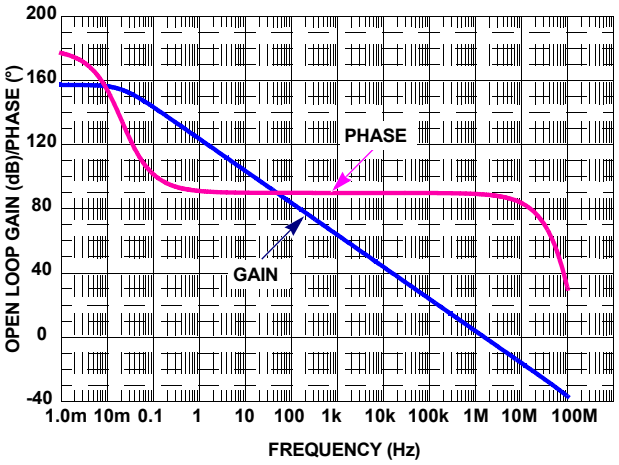

FIGURE 67. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

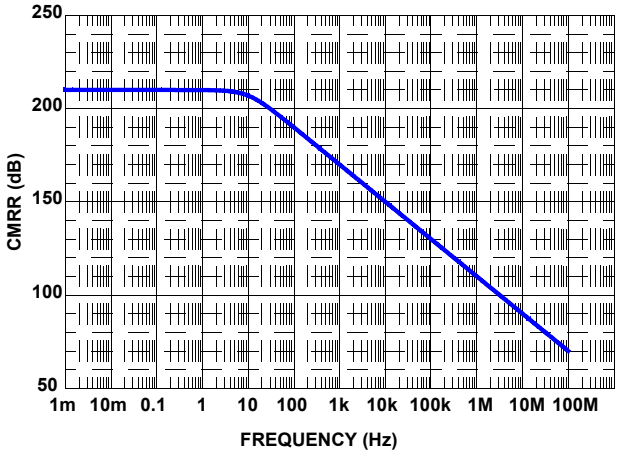

FIGURE 68. SIMULATED CMRR vs FREQUENCY

Metallization Mask Layout

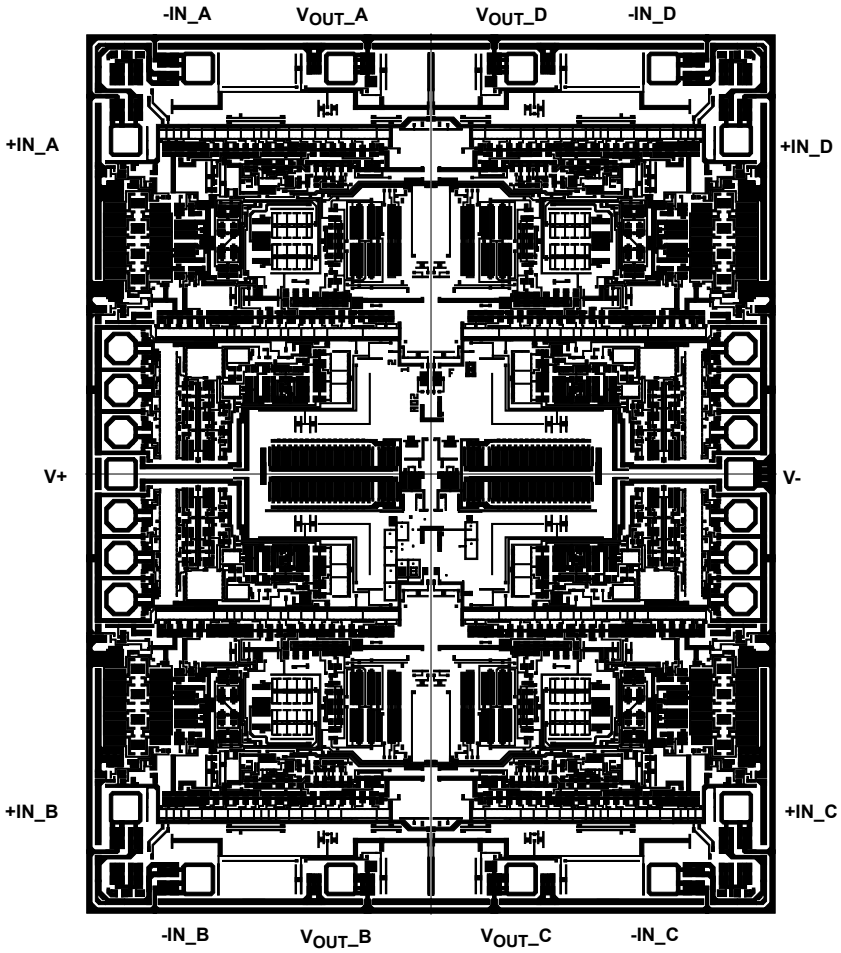

TABLE 2. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
V_{OUT}_A	3	-256	1152	70	70	1
-IN_A	4	-661	1152	70	70	1
+IN_A	5	-867.5	948.5	70	70	1
V+	9	-880.5	0	70	70	1
+IN_B	13	-867.5	-948.5	70	70	1
-IN_B	14	-661	-1152	70	70	1
V_{OUT}_B	15	-256	-1152	70	70	1
V_{OUT}_C	16	256	-1152	70	70	1
-IN_C	17	661	-1152	70	70	1
+IN_C	18	867.5	-948.5	70	70	1
V-	22	880.5	0	70	70	1
+IN_D	26	867.5	948.5	70	70	1
-IN_D	1	661	1152	70	70	1
V_{OUT}_D	2	256	1152	70	70	1

NOTE: Origin of coordinates is the center of die.

Revision History

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DATE	REVISION	CHANGE
Sep 13, 2019	FN6632.13	Updated Related Literature. Updated links throughout document. Updated ordering information table adding tape and reel information to table and updating notes. Added Note 4. Updated Figures 50 and 51. Removed About Intersil Updated Disclaimer.
Mar 30, 2016	FN6632.12	Removed Note that references SMD for the ISL28417SEH from ordering information table on page 3 and removed ISL28417SEH from MSL note due to not applicable.
Mar 16, 2016	FN6632.11	-Added the ISL28417SEH throughout the datasheet. -Updated POD L8.3x3k to most recent revision with change as follows: Tiebar Note 5 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). -Added about Intersil verbiage -Electrical Specifications Table Title on page 8: Added ISL28117, ISL28217, ISL28417 (VS ± 15V). -Electrical Specifications Table Title on page 10: Added ISL28117, ISL28217, ISL28417 (VS ± 5V).
Sep 11, 2012	FN6632.10	Feature on page 1: Added No phase reversal. Removed from ordering information QFN parts ISL28417FRZ (not release part) on Page 3. Removed all instances of QFN through document (front page, table of contents, thermal information, pin description and POD. Added to the typical performance curves table figure 53 on page 23: **Common-mode input impedance**.

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DATE	REVISION	CHANGE
Feb 23, 2012	FN6632.9	"Ordering Information" on page 2: Removed "Coming soon" from ISL28417FVZ and changed Part Marking column from "28417 FVZ" to 28417 FVZ-C". Changed "-40 to +125" to "200 C-grade" Added new Part Number ISL28417 FVBZ Electrical Spec changes: VOS Description Section: page 8 & page 10: Changed "Input Offset Voltage; SOIC Package" to Input Offset Voltage; SOIC, TSSOP Package" TCVOS Description section: page 8 & page 10: Changed;Input Offset Voltage Temperature Coefficient; SOIC Package to Input Offset Voltage Temperature Coefficient; SOIC, TSSOP Package TCIOS Conditions section: page 8 & page 10: Changed "ISL28417 SOIC B and C Grade" to "ISL28417 SOIC, TSSOP B and C Grade".
		"Ordering Information" on page 3: Updated Pkg. Dwg. # for ISL28117FUBZ, ISL28117FUZ, ISL28217FUBZ & ISL28217FUZ from M8.118 to M8.118B Updated Pkg. Dwg. # for ISL28117FRTBZ, ISL28117FRTZ, ISL28217FRTBZ & ISL28217FRTZ from L8.3x3A to L8.3x3K Updated Pkg. Dwg. # for ISL28417FRZ from L16.4x4 to L16.4x4E "Thermal Information" on page 7: Added Θ_{JA} and Θ_{JC} for 16 Ld QFN and 14 Ld TSSOP Figure 52, "% OVERSHOOT vs LOAD CAPACITANCE, V_S = ±15V" on page 23: X-Axis (Capacitance pF) values 1k and 10k were shifted 1 decade to the right. Shifted 1 decade to the left and added new label "100k" at the extreme right (where the "10k" value was located). Added dual and quad to the "SPICE NET LIST" on page 27. "Package Outline Drawing" on page 35: Changed from M8.118 to M8.118B Top View: Package width & height changed from 3.0±0.05 to 3.0±0.1 Package height from lead to lead changed from 4.9±0.15 to 4.9±0.2 Side View 2: Lead thickness changed from 0.09-0.20 to 0.15±0.05mm Side View 1: Package height changed from 0.85±0.10 to 0.86±0.05 Changed lead width from 0.25-0.036 to 0.23-0.36 Detail X: Foot of lead length changed from 0.55±0.15 to 0.53±0.10 "Package Outline Drawing" on page 36: Changed from L8.3x3A to L8.3x3K Bottom View: Changed lead height from 0.3±0.1 to 0.4±0.05 Changed lead width from 0.30±0.05 to 0.25±0.05 Land Pattern: Changed lead width from 0.30 to 0.25

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DATE	REVISION	CHANGE
Oct 11, 2011	FN6632.8	Figure 27 added “Positive” to Short-Circuit Current title Figure 28 added “Negative” to Short-Circuit Current title Figure 36 y axis label units changed from (nV/√Hz) to (nV/√Hz) Figure 37 y axis label units changed from pA/√hz to pA/√Hz Figure 31, 33 changed from VOUT vs Temperature to VOH vs Temperature Figure 32, 34 changed from VOUT vs Temperature to VOL vs Temperature Table of Contents on page 5 updated to list all package outline drawings Changed POD M14.15 to MDP0027 Changed TCIos for ISL28417 SOIC grade B and C on pages 7 and 9 from ±3.5pA/C to ±4.0pA/C
		1. Pg 2 Ordering Information: a.Added ordering information rows for ISL28417FBBZ (B grade) and ISL28417FBZ (C grade). b. Add Table of Contents 2. Pg 5 Abs Max and Thermal Information Tables: a. Added HBM, MM and CDM ESD levels for the ‘417 b. Added θ_{JA} and θ_{JC} values for the 14 Ld SOIC 3. Pg 6 ±15V electrical Specs a. Added ISL28417 B & C grade VOS and limits b. Added ISL28417 B & C grade TCVOS and limits c. Added ISL28417 B & C grade TCIOS and limits 4. Pg 7 a. Converted AVOL limits and units from 3kV/mV Min and 14kV/mV typ to 130dB and 143dB respectively 5. Pg 8 ±5V electrical Specs a. Added ISL28417 B & C grade VOS and limits 6. Pg 9 a. Added ISL28417 B & C grade TCVOS and limits b. Added ISL28417 B & C grade TCIOS and limits c. Converted AVOL limits and units from 3kV/mV Min and 14kV/mV Typ to 130dB and 143dB respectively 7. Pg 17 Applications Information a. Added Unused Channels paragraph and Figure 54.
Jul 12, 2011	FN6632.7	1. Releasing ISL28217FUZ MSOP Grade C package. Remove 'Coming Soon' from Order Information Table 2. Page 5, added: Machine Model (ISL28217 MSOP only). . . . . 300V 3. Under Electrical Spec ±15V and ±5V tables, changed Typical Rise Time and Fall Time from: Rise Time 100ns, Fall Time 120ns, to: Rise Time 130ns, Fall Time 130ns. 4. Under Electrical Spec ±15V and ±5V table for Vos and TCVos, added in row for ISL28217 MSOP Grade C package. Added Vos and TCVos limits for 25C and Full Temp. 5. For Typical performance curves for Vos Histograms, added note that histogram is based on ISL28217FBBZ for Grade B figures and ISL28217FBZ for Grade C figures. (Figures 3-6, added part number label to graph below Vs) 6. Under Electrical Spec ±15V and ±5V tables, changed TYP for Open Loop Gain from 18,000V/mV to 14,000V/mV
Dec 2, 2010	FN6632.6	1. Updated “Ordering Information” table on page 3. Removed Coming Soon for ISL28117FRTBZ and ISL28117FUBZ parts. Added in the Vos (MAX) numbers in those rows (75 and 70 respectively). 2. Corrected part marking in “Ordering Information” table on page 3 for ISL28117FRTZ from 8117 -C to -C 8117 3. Corrected part marking in “Ordering Information” table on page 3 for ISL28217FRTZ from 8217 -C to -C 8217 4. Updated Tape & Reel note in “Ordering Information” table on page 3 from “Add “-T7”, “-T7A” or "-T13" suffix for tape and reel.” to new standard “Add “-T*” suffix for tape and reel.” The "*" covers all possible tape and reel options 5. Updated “Electrical Specifications” Table for “V_{OS}” on page 8 and “TCV_{OS}” on page 8 a. Added data row for Offset Voltage; MSOP Grade B Package; ISL28117 b. Added data row for Offset Voltage; TDFN Grade B Package; ISL28117 c. Added data row for Input Offset Voltage Temperature Coefficient; MSOP Grade B Package; ISL28117 d. Added data row for Input Offset Voltage Temperature Coefficient; TDFN Grade B Package; ISL28117 6. Removed “Temperature data established by characterization” from common conditions of spec table. Removed note “Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." from Min Max columns of spec table. Replaced with new standard note in Min Max columns, “Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.”

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev. **(Continued)**

DATE	REVISION	CHANGE
Aug 31, 2010	FN6632.5	1. General changes: a. Added in Quad devices to the datasheet for SOIC, TSSOP and QFN packages. b. Added in TDFN packages for single and dual devices. c. Added in new VOS and TCVOS limits for TDFN packages d. Added Tja and Tjc Notes for TDFN Package which are “direct attach (Tja) ” and “bottom (Tjc)” 2. Specific changes: a. Added in ISL28417 to title and front page info on page 1 b. Added in ISL28117FRTZ, ISL28117FRTBZ, ISL28217FRTZ, ISL28217FRTBZ, ISL28417FBZ, ISL28417FVZ and ISL28417FRZ packages to Ordering information on page 3 and page 3. Added in -T7 and -T7A tape and reel extensions where applicable. c. Added in TDFN, 14 Ld SOIC, 14 Ld TSSOP and 16 Ld QFN to pin configurations on page 5 and page 3. d. Updated Pin Descriptions tables with new added in packages on page 6. e. Abs Max Table added in thermal packaging info for TDFN packages on page 7. f. Electrical Specifications Table - Added two new line items for VOS spec. TDFN package ISL28217 Grade B limits ±70uV 25C and ±140uV full temp. TDFN package ISL28x17 Grade C limits ±150uV 25C and ±250uV full temp on page 8 and page 10. g. Electrical Specifications Table - Added two new line items for TCVOS spec. TDFN package ISL28217 Grade B limits ±0.7uV/C full temp. TDFN package ISL28x17 Grade C limits ±1uV/C on page 8 and page 10. h. Added in PODs for L8.3x3A, M14.15, M14.173 and L16.4x4
Mar 18, 2010	FN6632.4	1. Updated “Ordering Information” on page 3 by adding two rows for MSOP packages ISL28117FUBZ and ISL28117FUZ, which are scheduled to release Q2 2010. Added Pinout accordingly. 2. Added POD for MSOP M8.118 to the end of datasheet 3. In “Ordering Information” on page 3, Separated each part number with it's own specific -T7 and -T13 suffix and removed “Add “-T7” or “-T13” suffix for Tape and Reel.” from Note 1. 4. Updated ±15 and ±5V Electrical Specification table with the following edits: A) Separated VOS specs for SOIC and MSOP Grade C packages. Added new VOS specs for MSOP Grade C package. B) Separated TCVOS specs for SOIC and MSOP Grade C packages. Added new TCVOS specs for MSOP Grade C package. 5. Added “Thermal Information” on page 7 for ISL28117 MSOP package.
		Added page1. Added Evaluation Boards to “Ordering Information” on page 3. Added Theta JC values to “Thermal Information” on page 7. Added applicable Theta JC Note 7. Updated Theta JA for ISL28217 8 Ld SOIC from 115°C/W to 105°C/W.
		Part marking in “Ordering Information” on page 3 changed as follows: ISL28117FBBZ changed from "28117 FBZ -B" to "28117 FBZ" ISL28117FBZ changed from "28117 FBZ" to "28117 FBZ -C" ISL28217FBBZ changed from "28217 FBZ -B" to "28217 FBZ" ISL28217FBZ changed from "28217 FBZ" to "28217 FBZ -C"
		On page 15: Changed label in Figure 3 from “V_S = +5V” to “V_S = ±5V” On page 15: Changed label in Figure 4 from “V_S = +15V” to “V_S = ±15V”
		Changed Typical VOS spec from “13” to “8” (B Grade), “19” to “4” (C Grade), IB from “0.18” to “0.08, IOS from “0.3” to “0.08”. Edited Spice Schematic - L1 from “95.4957” to “15.9159E”, R1 from “6k” to 1, R9 from “1” to “2.1E3”, R10 from “1” to “2.1E3, R12 from “6k” to “1”, L2 from “95.4957” to “15.9159E”. Edited Spice Net List - Changed Revision from “A” to “B”, Date change from “October 29th 2009” to “November 20th 2009”, added after AOL “SR = 0.5V/µsec, Input Stage changed in I_IOS from “0.3E-9” to 0.08E-9”, V_VOS “13e-6” to “8e-6”, Mid supply Ref R_R9 and R_R10 changed “1” to “2.1E3”, Common-Mode Gain Stage with Zero change in G_G5 and G_G6 “5.27046e-15” to “3.162277”, R_R11 and R_R12 “6.3” to “1”, L_L1 and L_L2 “95.4957” to “15.9159E-3”
Nov 12, 2009	FN6632.3	Updated Typical Performance Curves Figure 5, 7, 9, 11, 13, 15, 17 and 19. Added Spice Model and license statement. Replaced typical application schematic.

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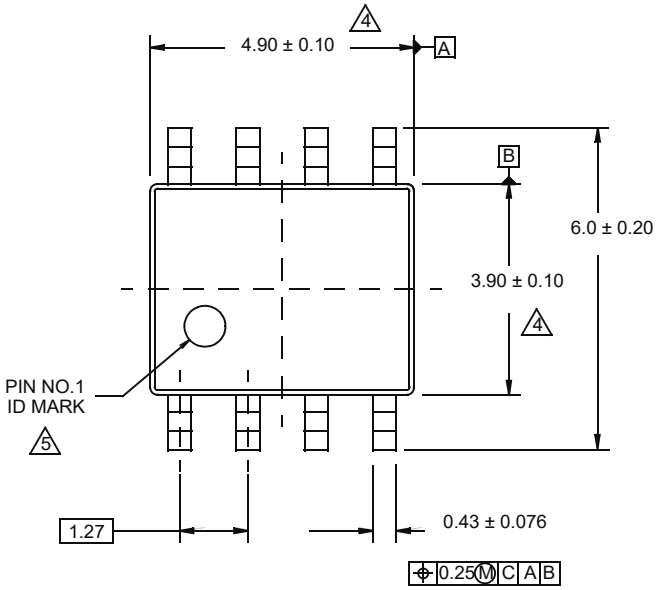
DATE	REVISION	CHANGE
Oct 16, 2009	FN6632.2	On page 3 “Ordering Information”, changed the following: a) corrected part marking for ISL28117FBBZ from "28117 -B FBZ" to "28117 FBZ -B". Corrected part marking for ISL28217FBBZ from "28217-B FBZ" to "28217 FBZ -B" B) Updated package outline drawing to most recent revision (no changes were made to package dimensions; land pattern was added and dimensions were moved from table onto drawing) c) Added "Add “-T7” or “-T13” suffix for tape and reel." to the tape and reel Note 1. d) added Note 3 callout to all parts (Note 3 reads: “For Moisture Sensitivity Level (MSL), please see device information page for ISL28117, ISL28217. For more information on MSL please see techbrief TB363.") e) removed "Coming Soon" from ISL28117FBBZ, ISL28117FBZ & ISL28217FBBZ devices
Oct 8, 2009	FN6632.1	1. Removed “very” from “...low noise..” 1st sentence, page 1. 2. Removed “Low” from 6th bullet under features, page 1. 3. Modified typical characteristics curves to show conservative performance. Specific channel designations removed. On temperature curves, changed formatting to indicate range from typical value. Changes include: a. Removed former Figures 1, 3, 5, 7, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30, 33, 34, 37 & 38 (all Channel A curves) b. Replaced former Figures 19, 20, 23, 24, 27, 28, 31, 32, 35, 36, 39 & 40 with new Figures 9 thru 20 (all “conservative channels”) c. Added Figures 30, 31, 32 4. Updated TCVos histogram on page 1 to match TCVos histogram Figure 6 on page 7 (same graphic) 5. Added temp labels to Figures 28 & 29
Sept 3, 2009	FN6632.0	Initial Release

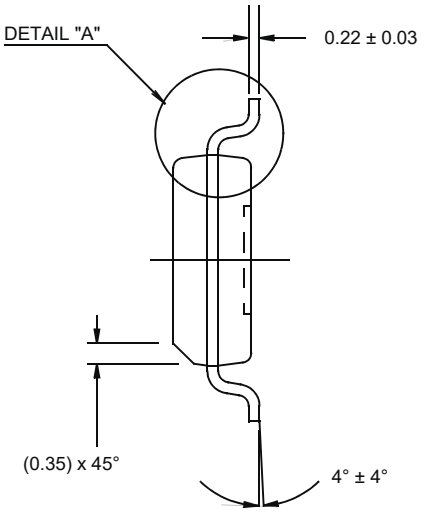
Package Outline Drawings

For the most recent package outline drawing, see M8.15E.

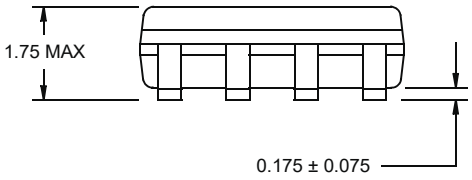
M8.15E
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



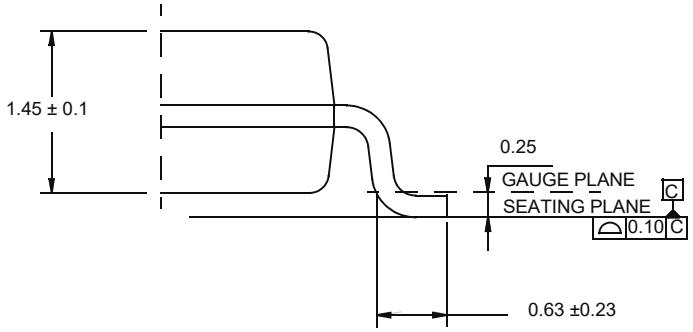
TOP VIEW



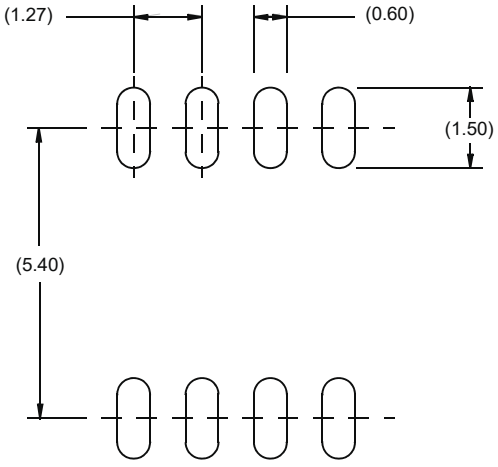
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



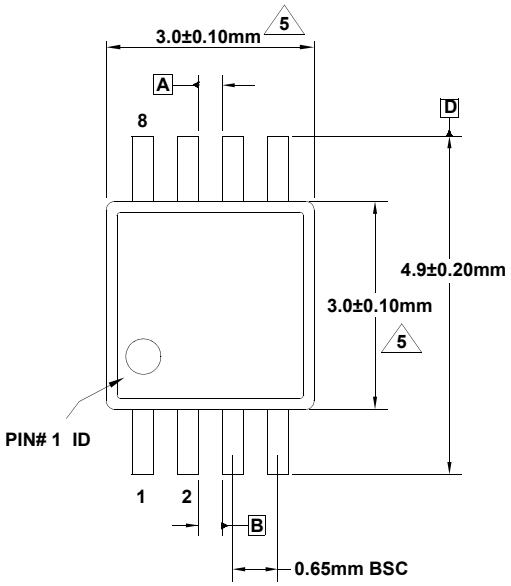
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

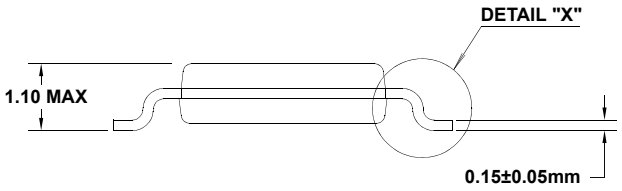
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

M8.118B
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 1, 3/12

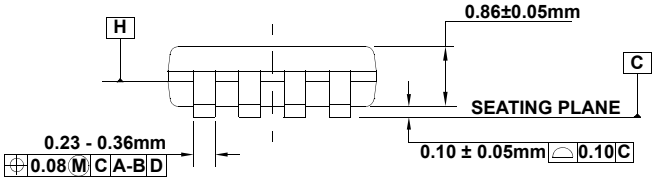
For the most recent package outline drawing, see M8.118B.



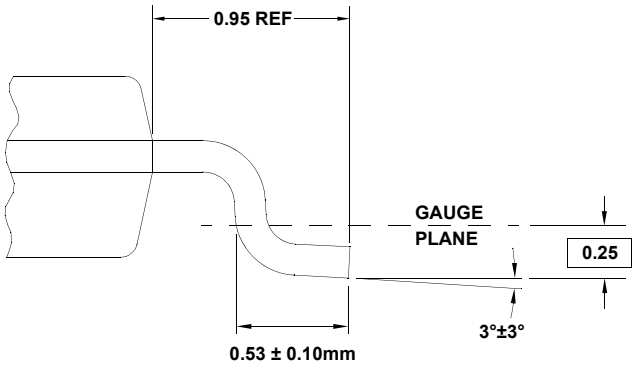
TOP VIEW



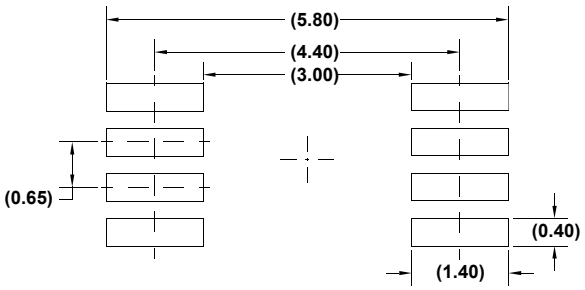
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



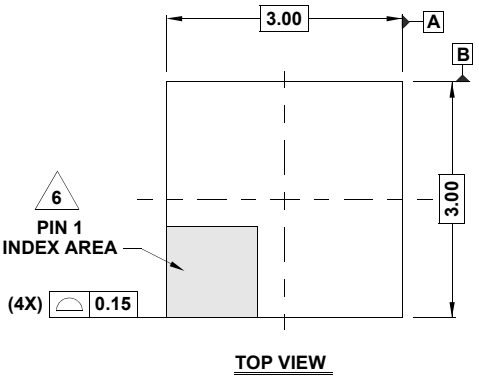
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

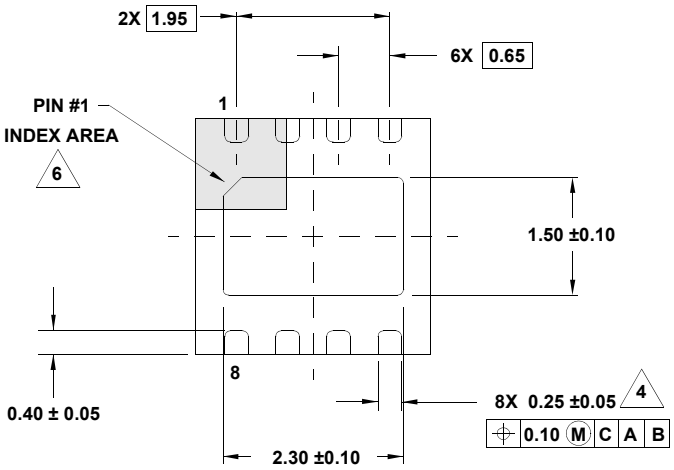
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

L8.3x3K
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 5/15

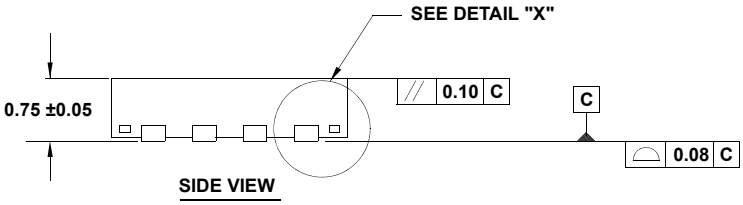
For the most recent package outline drawing, see L8.3x3K.



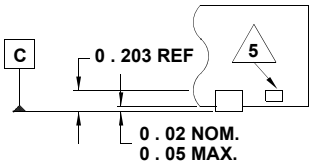
TOP VIEW



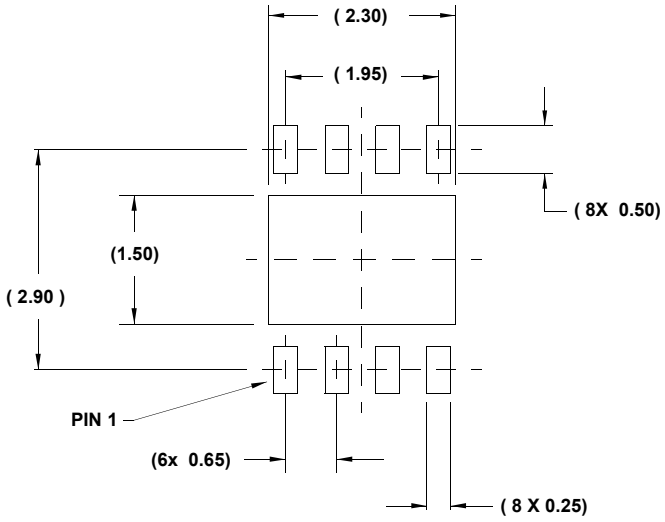
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



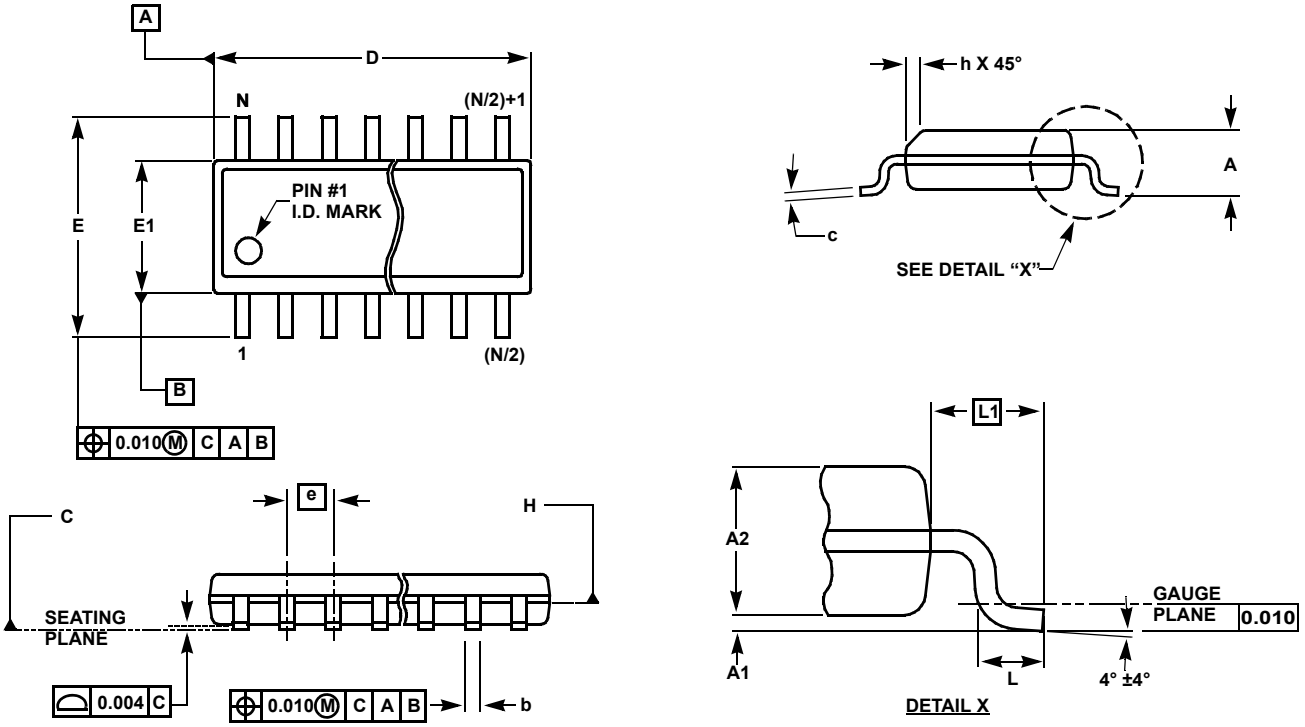
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

Small Outline Package Family (SO)

For the most recent package outline drawing, see MDP0027.



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

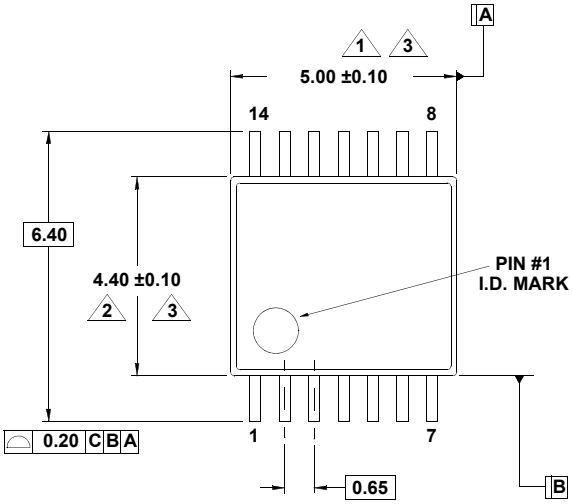
Rev. M 2/07

NOTES:

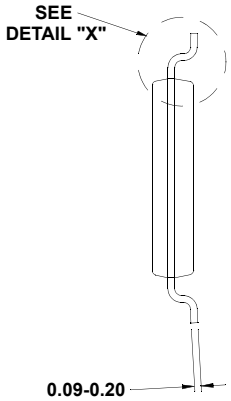
1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

M14.173
14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 3, 10/09

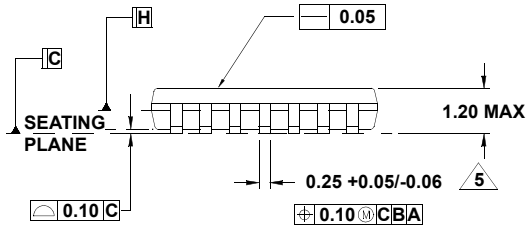
For the most recent package outline drawing, see M14.173.



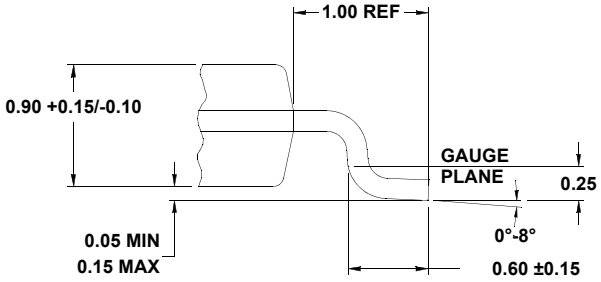
TOP VIEW



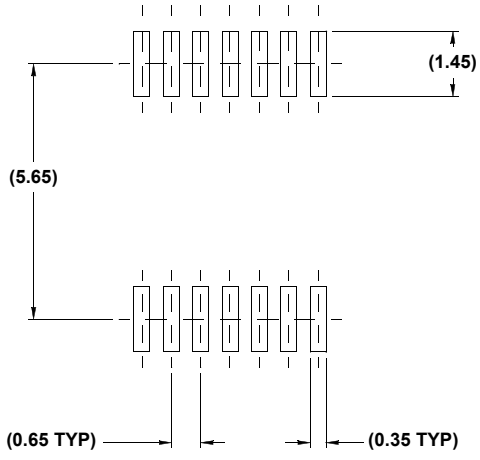
END VIEW



SIDE VIEW



DETAIL "X"

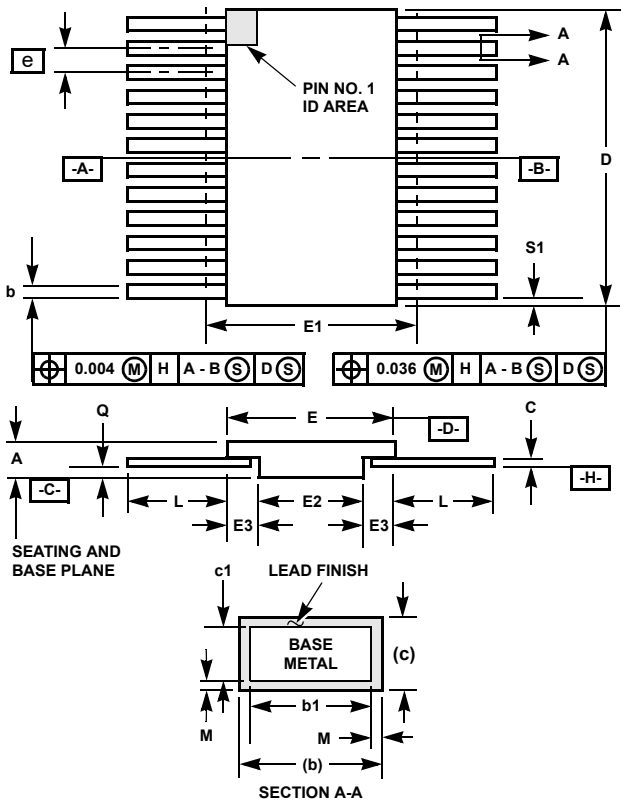


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.

Ceramic Metal Seal Flatpack Packages (Flatpack)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

K14.A
MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

Rev. 0 5/18/94

For the most recent package outline drawing, see K14.A.

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(Rev.4.0-1 November 2017)

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