THE DATASHEET OF

ISL78268ARZ

ISL78268

55V Synchronous Buck Controller with Integrated 3A Driver

FN8657
Rev 3.00
December 12, 2014

The ISL78268 is a grade 1, automotive, synchronous buck controller with integrated high/low side MOSFET drivers. It supports a wide operating input voltage range of 5V to 55V and up to 60V at V_{IN} when not switching. The integrated driver offers adaptive dead-time control and is capable of supplying up to 2A sourcing and 3A sinking current, allowing the ISL78268 to support power stages designed for a wide range of loads, from under 1A to over 25A.

ISL78268's fully synchronous architecture enables power conversion with very high efficiency and improved thermal performance over standard buck converters. The ISL78268 also offers diode emulation mode for improved light load efficiency.

While ISL78268 is a peak current mode PWM controller, it also includes a dedicated average output current modulation loop, which achieves constant output current limiting for applications such as battery charging, super-cap charging, and temperature control systems where a constant current must be provided.

The ISL78268 supports switching frequencies from 50kHz to 1.1MHz allowing the user the flexibility to trade-off switching frequency and efficiency against the size of external components.

The ISL78268 offers comprehensive protection features. It includes robust current protection with cycle-by-cycle peak current limiting, average current limiting, and a selectable hiccup or latch-off fault responses. In addition, it offers protection against over-temperature, as well as input and output overvoltages.

Features

- Wide input range 5V to 55V (switching); withstand 60V (non-switching)
- Integrated 2A sourcing, 3A sinking MOSFET drivers
- Constant current regulation/limiting - dedicated average current control loop
- Adjustable switching frequency or external synchronization from 50kHz up to 1.1MHz
- Low shutdown current, I_Q <1µA
- Peak current mode control with adjustable slope compensation
- Selectable diode emulation mode for high efficiency at light load
- Input and output OVP, cycle-by-cycle current limiting, average current OCP, OTP
- Selectable hiccup or latch-off fault responses
- Pb-free 24 Ld 4x4 QFN package (RoHS compliant)
- AEC-Q100 qualified

Applications

- Automotive power
- Telecom and industrial power supplies
- General purpose power
- Supercap charging

Related Literature

- AN1946, "ISL78268EVAL1Z Evaluation Board User Guide"

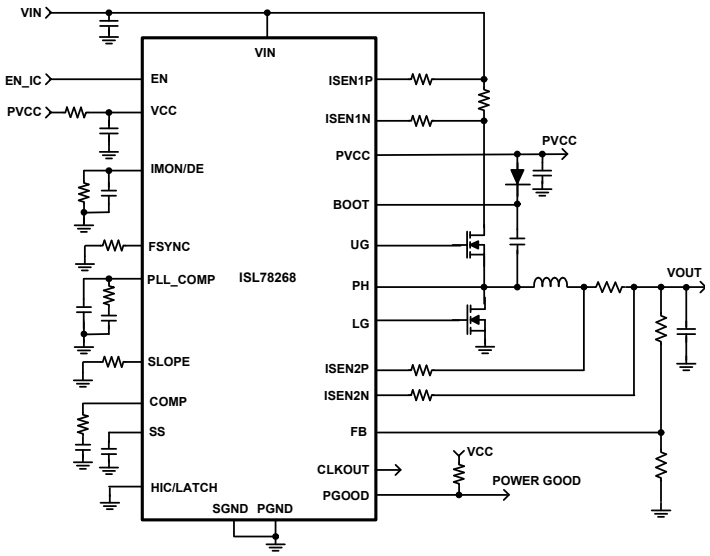


FIGURE 1. SIMPLIFIED TYPICAL APPLICATION SCHEMATIC

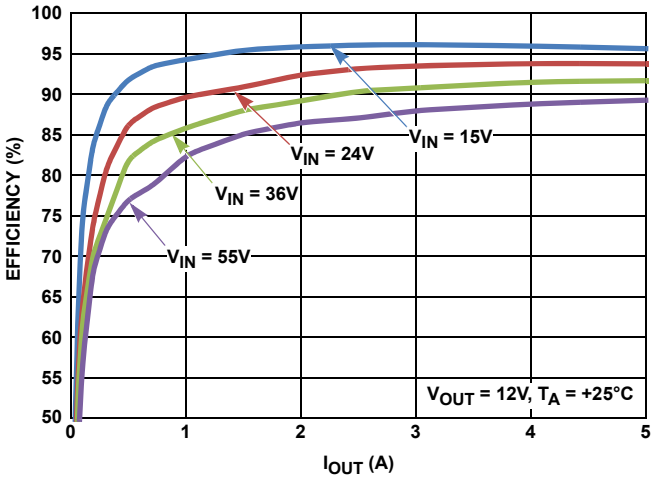
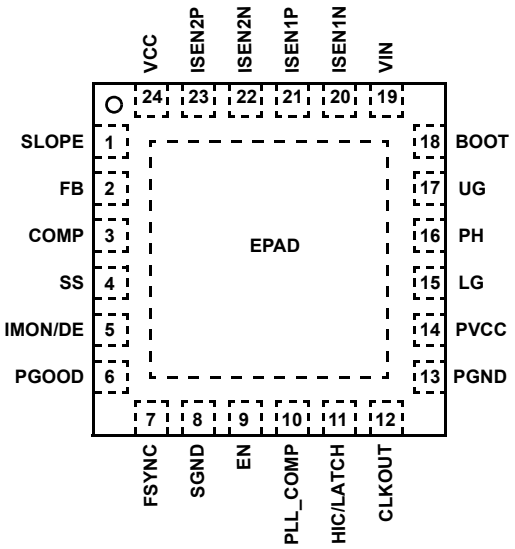


FIGURE 2. EFFICIENCY CURVES (ISL78268EVAL1Z/DE MODE)

Table of Contents

Pin Configuration

ISL78268
(24 LD 4x4 QFN)
TOP VIEW



Functional Pin Description

PIN NAME	PIN #	DESCRIPTION
SLOPE	1	This pin programs the slope of the internal slope compensation. A resistor should be connected from the SLOPE pin to GND. Please refer to "Adjustable Slope Compensation" on page 24 for how to choose this resistor value.
FB	2	The inverting input of the transconductance amplifier. A resistor divider must be placed between the FB pin and the output rail to set the output voltage.
COMP	3	The output of the transconductance amplifier. Place the compensation network between the COMP pin and GND for compensation loop design.
SS	4	Use this pin to set up the desired soft-start time. A capacitor placed from SS to GND will set up the soft-start ramp rate and in turn determine the soft-start time.
IMON/DE	5	IMON/DE is a bifunctional pin as either the average current monitor/protection or switching mode selection (Diode Emulation (DE) mode or Forced PWM mode). 1. If IMON/DE pin is connected to VCC (higher than VCC - 0.7V), the device operates in Forced PWM mode and the average current monitoring/limiting feature is disabled. 2. If a resistor (and a filter capacitor in parallel) is connected between IMON/DE and GND, the device operates in DE mode and the average current monitoring/limiting feature is enabled. A current which is proportional to the current sensed at I_{SEN2} is sourced from the IMON/DE pin. With an R/C network at the IMON/DE pin to GND, the voltage at IMON/DE pin describes average output current. When average current monitoring/limiting feature is enabled and DE mode is selected; 1. If IMON/DE is higher than 2V, the device enters Average Current Protection mode with the hiccup/latch-off as the fault response. 2. If IMON/DE reaches to 1.6V, the device enters the Average Constant Current control loop. 3. If the IMON/DE pin voltage is lower than 1.6V (typ), the device operates as a normal buck regulator in DE mode.
PGOOD	6	Provides an open-drain Power-Good signal. When the output voltage is within +15/-12% of the nominal output regulation point and soft-start is completed, the internal PGOOD open-drain transistor is open. It will be pulled low once output UV/OV or input OV conditions are detected. Requires pull-up resistor connecting to VCC.
FSYNC	7	The oscillator switching frequency is adjusted with a resistor from this pin to GND. The internal oscillator locks to the rising edge of a square pulse waveform if this pin is driven by an external clock. There is a 325ns delay from the FSYNC pin's input clock rising edge to UG rising edge.
SGND	8	Signal ground pin; the reference of internal analog circuits. Connect this pin to a large quiet copper ground plane. In PCB layout planning, avoid having switching current flowing into the SGND area (including the IC PAD that is connected to the quiet large copper ground plane also).

Functional Pin Description (Continued)

PIN NAME	PIN #	DESCRIPTION
EN	9	This pin is a threshold-sensitive enable input for the controller. Connecting the power supply input to the EN pin through an appropriate resistor divider provides a means to have input voltage UVLO. When EN pin is driven above 1.2V, the ISL78268 is active depending on status of the internal POR, and pending fault states. Driving the EN pin below 1.1V will clear all fault states and the ISL78268 will soft-start when reenabled.
PLL_COMP	10	This pin serves as the compensation node for the PLL. A second order passive loop filter connected between the PLL_COMP pin and GND compensates the PLL feedback loop.
HIC/LATCH	11	This pin is used to select either HICCUP or LATCHOFF response for faults including output overvoltage, V_{IN} overvoltage, peak overcurrent protection (OC2) and average overcurrent protection. HIC/LATCH = HIGH to activate HICCUP fault response, HIC/LATCH = LOW to have LATCHOFF fault response. Either toggling EN pin or recycling VCC POR can reset the IC from LATCHOFF status.
CLKOUT	12	This pin provides a clock signal to synchronize with another ISL78268. The rising edge signal on the CLKOUT pin is delayed 180° from the rising edge of UG to facilitate 2-phase interleaved operation using two ICs.
PGND	13	This Power GND pin provides the return path for the low-side MOSFET drive. Note this pin carries the noisy driving current and the trace connected to the low-side MOSFET and PVCC decoupling capacitors should be as short as possible. Any sensitive analog signal trace should not share common traces with this driving return path. Connect this pin directly to the ground copper plane and put several vias as close as possible to this pin.
PVCC	14	Output of the internal linear regulator that provides bias for both high-side and low-side drives. The PVCC operating range is 4.75V to 5.5V. A minimum 4.7µF ceramic capacitor should be used between PVCC and PGND for noise decoupling purpose. This capacitor provides a noisy driving current and its ground pad should have several vias connecting to the ground copper plane.
LG	15	The low-side MOSFET gate drive output.
PH	16	Phase node. Connect this pin to the source of the high-side MOSFETs and the drain of the low-side MOSFETs. This pin represents the return path for the high-side gate drive.
UG	17	High-side MOSFET gate drive output.
BOOT	18	This pin provides bias voltage to the high-side MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive the external N-channel MOSFET. Place a 1µF ceramic capacitor between the BOOT and PH pins, and a switching diode from PVCC to BOOT.
VIN	19	Connect input rail to this pin. This pin is connected to the input of the internal linear regulator, generating the power necessary to operate the chip. It is recommended the DC voltage applied to the VIN pin does not exceed 55V when the IC is switching. VIN can stand up to 60V when IC is not switching.
ISEN1N	20	The ISEN1N pin is a negative potential input pin of the first current sense amplifier (CSA1). This amplifier senses the signal on the current-sense resistor placed in series with the high-side MOSFET. The sensed current information is used for peak current mode control and overcurrent protection.
ISEN1P	21	The ISEN1P pin is a positive potential input pin of the first current sense amplifier (CSA1).
ISEN2N	22	The ISEN2N pin is a negative potential input pin of the second current sense amplifier (CSA2). This amplifier senses the continuous output inductor current either by DCR sensing method or using a sense resistor in series with the inductor for more accurate sensing. The sensed current signal is used for 3 functions: - Accurately limiting the average output current for constant output current control - Achieve diode emulation - Achieve average OCP (comparator at IMON/DE pin with 2V reference)
ISEN2P	23	The ISEN2P pin is a positive potential input pin of the second current-sense amplifier (CSA2).
VCC	24	This pin provides bias power for the IC analog circuitry. An RC filter is recommended between this pin and the bias supply (range of 4.75V to 5.5V, typically from PVCC). A minimum 1µF ceramic capacitor should be used between VCC and GND for noise decoupling purposes.
EPAD		Bottom thermal pad. It is not connected to any electrical potential of the IC. In layout it must be connected to a PCB large ground copper plane that doesn't contain noisy power flows. Put multiple vias (as many as possible) in this pad connecting to the ground copper plane to help reduce the IC's θ_{JA}.

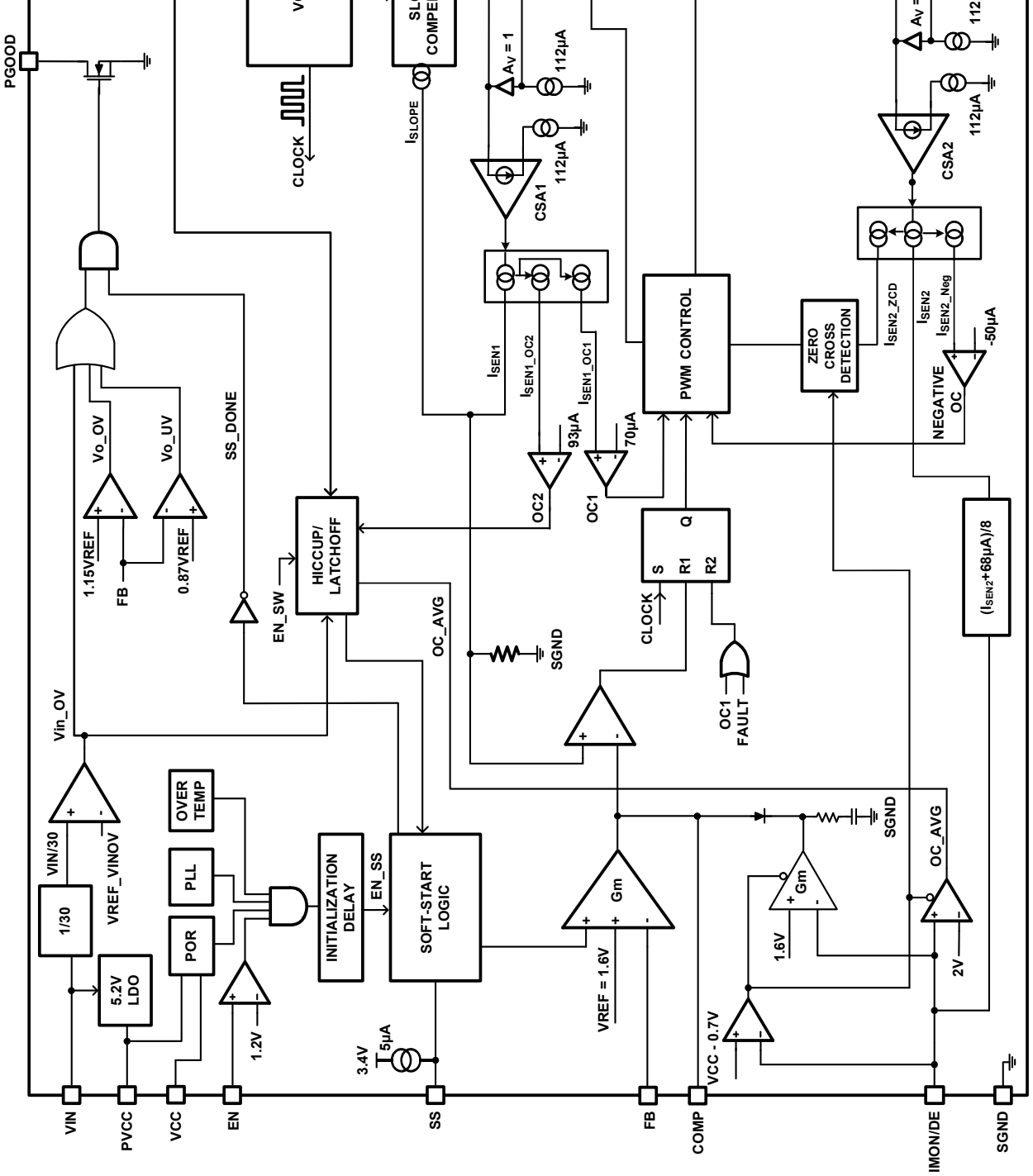
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL78268ARZ	782 68ARZ	-40 to +125	24 Ld 4x4 QFN	L24.4x4H
ISL78268EVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78268. For more information on MSL please see techbrief TB363.

Block Diagram



Typical Application Schematics

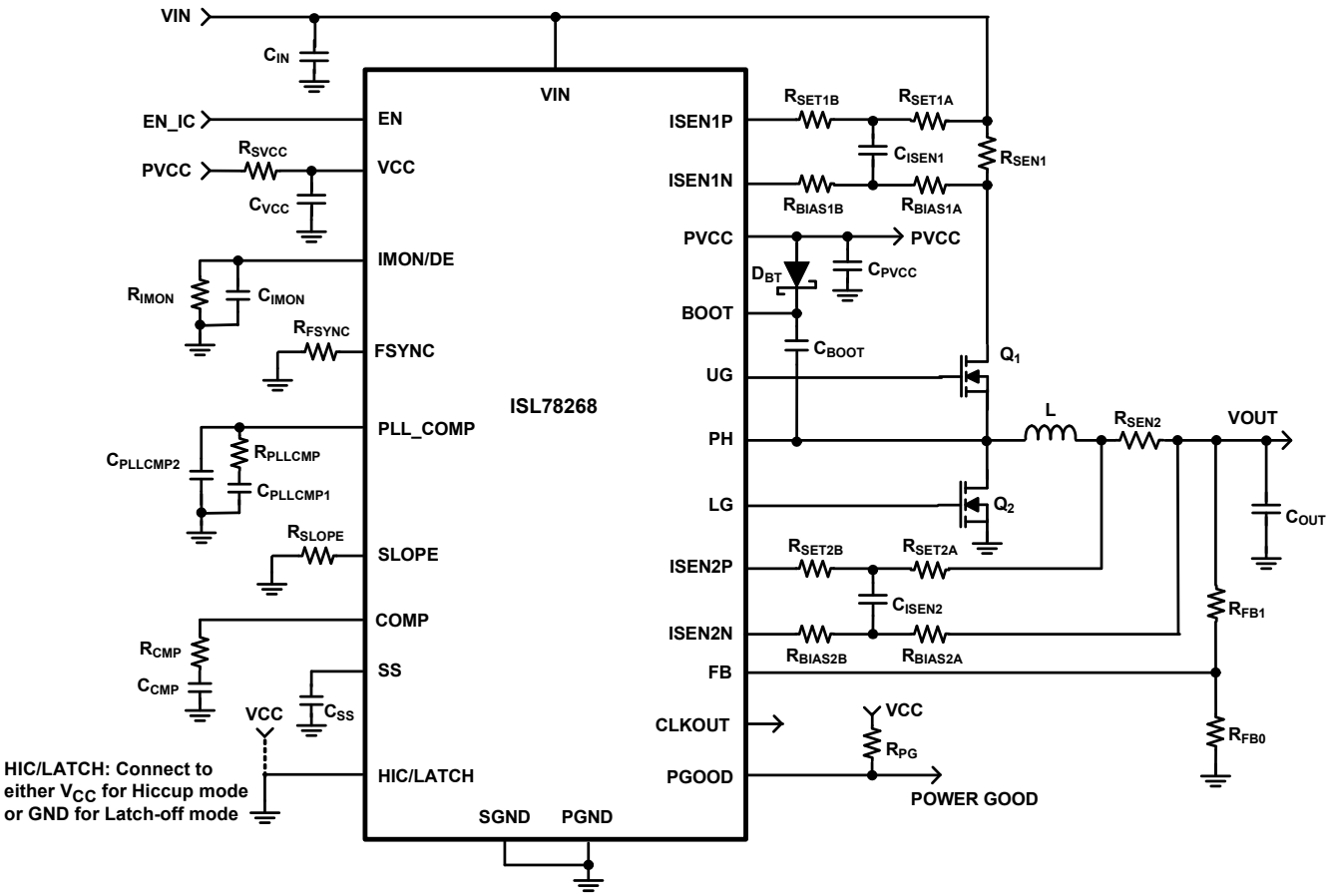


FIGURE 3. SYNCHRONOUS BUCK WITH CONSTANT AVERAGE I_{OUT}

Typical Application Schematics (Continued)

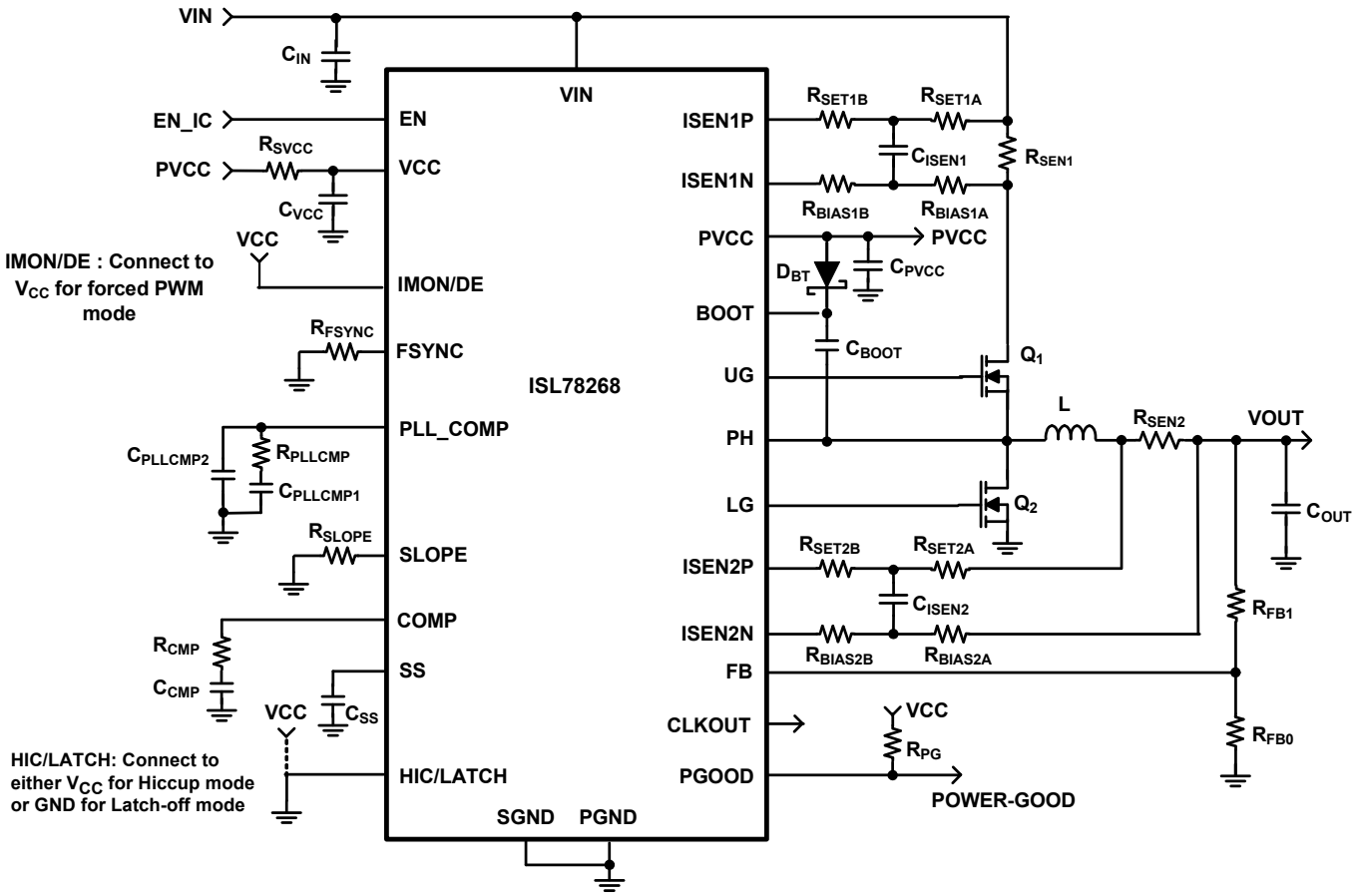


FIGURE 4. SYNCHRONOUS BUCK (FORCED PWM)

Typical Application Schematics (Continued)

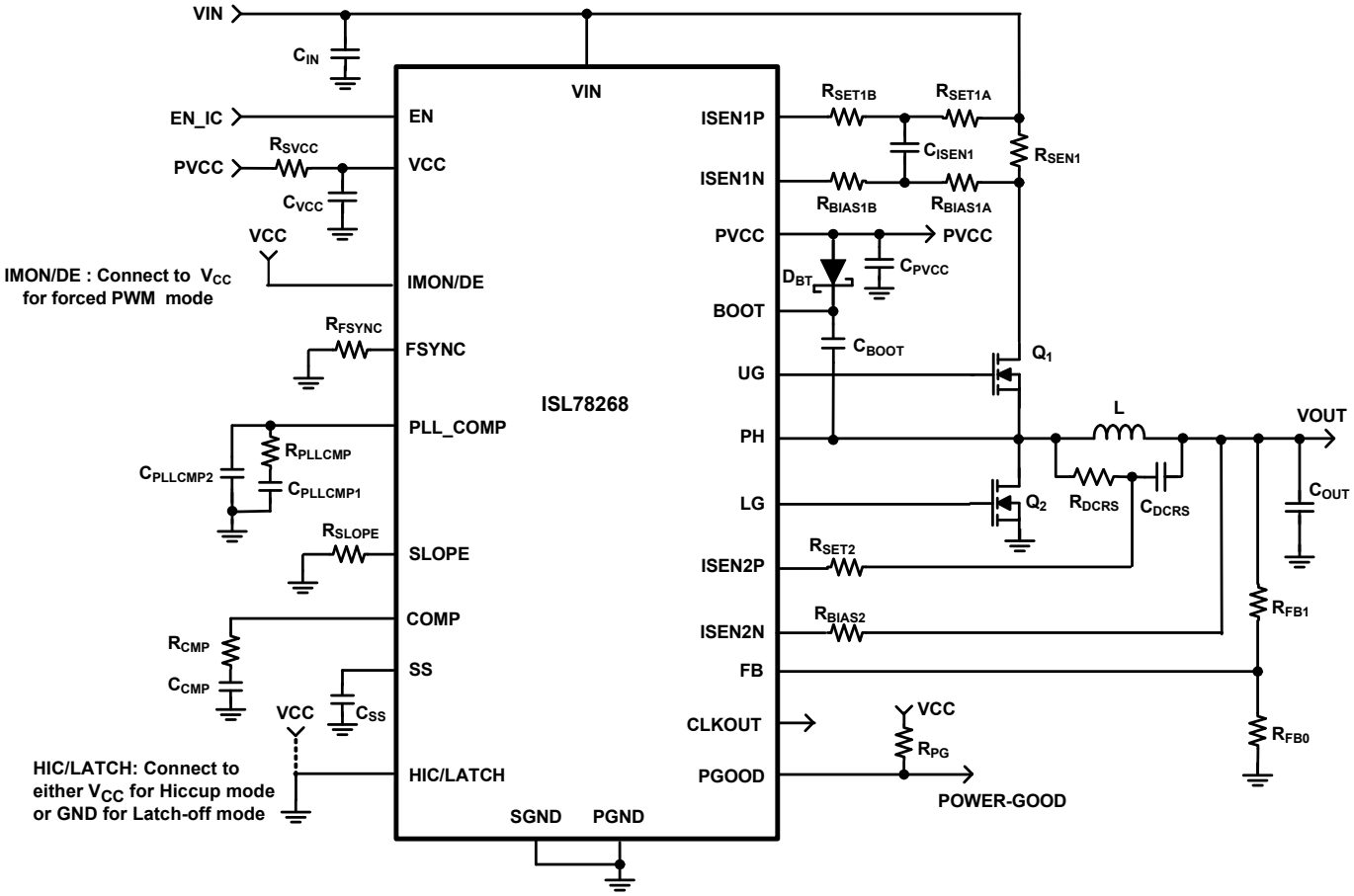


FIGURE 5. SYNCHRONOUS BUCK WITH DCR SENSING

Absolute Maximum Ratings

VIN . . . . . - 0.3V to +60V
PH . . . . . - 0.3V to +60V
BOOT, UG . . . . . - 0.3V to +65V
Upper Driver Supply Voltage, V_{BOOT} - V_{PH} . . . . . - 0.3V to +6.5V
PVCC, VCC . . . . . - 0.3V to +6.5V
V_{ISENxP} - V_{ISENxP} . . . . . ±0.6V
ISEN1P, ISEN1N, ISEN2P, ISEN2N . . . . . - 0.3V to +60V
All Other Pins . . . . . - 0.3V to VCC + 0.3V
ESD Rating
Human Body Model (Tested per AEC-Q100-002) 2kV
Machine Model (Tested per AEC-Q100-003) 200V
Charged Device Model (Tested per AEC-Q100-011) 750V
Latchup Rating (Tested per AEC-Q100-004) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld 4x4 QFN Package (Notes 4, 5)	39	3.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

VIN . . . . . 5V to 55V
PH . . . . . 0V to 55V
PVCC, VCC . . . . . 4.75V to 5.5V
Upper Driver Supply Voltage, V_{BOOT} - V_{PH} . . . . . 3.5V to 6V
ISEN1P, ISEN1N, ISEN2P, ISEN2N Common Mode Voltage . . . . 4V to 55V
ISEN1P to ISEN1N and ISEN2P to ISEN2N Differential Voltage . . . . ± 0.3V
Operational Ambient Temperature Range (Automotive) . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. Unless otherwise noted, all voltages specified in this specification are refer to GND.

Electrical Specifications

Refer to the Block Diagram (page 6) and Typical Application Schematics (page 7). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, EN = 5.0V, T_A = -40°C to +125°C. Typicals are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SUPPLY INPUT						
Input Voltage Range	VIN	For V_{IN} = 5V, the internal LDO dropout (V_{IN} - PVCC) <0.25V	**5**		**55**	V
Input Supply Current (ENABLED Mode) to VIN Pin	I_{Q_SW}	R_{FSYNC} = 40.2kΩ (f_{SW} = 300kHz), LG = OPEN, UG = OPEN		5	**7**	mA
	I_{Q_NON-SW}	FSYNC = 5V, LG = OPEN, UG = OPEN		2.7	**3.5**	mA
Input Supply Current (Shutdown Mode) to VIN Pin	$I_{Q\_SD\_VIN}$	EN = GND, V_{IN} = 12V		0.15	**0.5**	µA
		EN = GND, V_{IN} = 55V		0.2	**1**	µA
Input Leakage Current (Shutdown Mode) to each of ISEN1P/ISEN1N/ISEN2P/ISEN2N Pins	$I_{Q\_SD\_ISENxP/N}$	EN = GND, ISEN1P (or ISEN1N/ISEN2P/ISEN2N) = 55V, V_{IN} = 55V	**-1**	0	**1**	µA
INPUT OVERVOLTAGE PROTECTION						
V_{IN} Switching-Disabled Threshold		EN = 5V, V_{IN} rising	**56**	57.5	**59.5**	V
V_{IN} Overvoltage Recovery Threshold			**52.5**	54.5	**57**	V
V_{IN} Switching-Disabled Threshold Hysteresis				3		V
V_{IN} Overvoltage Hiccup Retry Delay		From the time fault is removed to initiation of soft-start		500		ms
INTERNAL LINEAR REGULATOR						
LDO Output Voltage (PVCC Pin)	V_{PVCC}	V_{IN} = 6V to 55V, C_{PVCC} = 4.7µF from PVCC to PGND, I_{PVCC} = 10mA	**5**	5.2	**5.4**	V
LDO Dropout Voltage (PVCC pin)	$V_{DROPOUT}$	V_{IN} = 4.9V, C_{PVCC} = 4.7µF from PVCC to PGND, I_{VCC} = 80mA		0.3		V
LDO Current Foldback Limit (PVCC Pin)	I_{OC_LDO}	V_{IN} = 6V, C_{PVCC} = 4.7µF from PVCC to PGND V_{PVCC} = 2.5V	**150**	230	**280**	mA
LDO Output Short Current (PVCC pin)	I_{OCFB_LDO}	V_{IN} = 6V, C_{PVCC} = 4.7µF from PVCC to PGND V_{PVCC} = 0V	**100**	150	**220**	mA

Electrical Specifications

Refer to the Block Diagram (page 6) and Typical Application Schematics (page 7). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, EN = 5.0V, T_A = -40°C to +125°C. Typicals are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
POWER-ON RESET (for both PVCC and VCC)						
Rising $V_{PVCC/VCC}$ POR Threshold	V_{PORH_RISE}		**4.35**	4.55	**4.75**	V
Falling $V_{PVCC/VCC}$ POR Threshold	V_{PORL_FALL}		**4.1**	4.15	**4.3**	V
$V_{PVCC/VCC}$ POR Hysteresis	V_{PORL_HYS}			0.4		V
Phase Lock Loop Locking Time	t_{PLL_DLY}	From POR to Initiation of soft-start. R_{PLLCMP} = 3.24k, $C_{PLLCMP1}$ = 6.8nF, $C_{PLLCMP2}$ = 1nF, R_{FSYNC} = 40.2k, f_{SW} = 300kHz		0.8		ms
EN						
Enable Threshold	V_{ENH}	Rising	**1.1**	1.2	**1.3**	V
	V_{ENL}	Falling	**1.04**	1.14	**1.24**	V
	V_{EN_HYS}	Hysteresis		60		mV
Input Resistance		EN = 4V	**3000**	5000	**8000**	kΩ
		EN = 6V		5		kΩ
OSCILLATOR						
PWM Switching Frequency	F_{OSC}	R_{FSYNC} = 249kΩ (0.1%)	**47.5**	50	**52.5**	kHz
		R_{FSYNC} = 40.2kΩ (0.1%)	**285**	300	**315**	kHz
		R_{FSYNC} = 10kΩ (0.1%)	**1036**	1100	**1155**	kHz
Switching Frequency Range		T_A = +25°C, V_{IN} = 12V	**50**		**1100**	kHz
Synchronization Range at FSYNC		T_A = +25°C, V_{IN} = 12V	**50**		**1100**	kHz
CLKOUT						
High Level CLKOUT Output Voltage	$CLKOUT_H$	I_{CLKOUT} = 500µA	**VCC-0.4**	VCC-0.1		V
Low Level CLKOUT Output Voltage	$CLKOUT_L$	I_{CLKOUT} = -500µA		0.1	**0.4**	V
Output Pulse Width		C_{CLKOUT} = 100pF		270		ns
Phase Shift from UG Rising Edge to CLKOUT Pulse Rising Edge		UG = OPEN, C_{CLKOUT} = OPEN		180		°
SYNCHRONIZATION (FSYNC pin)						
Input High Threshold	VIH		**3.5**			V
Input Low Threshold	VIL				**1.5**	V
Input Pulse Width - Rise_To_Fall			**20**		20,000	ns
Input Pulse Width - Fall_To_Rise			**20**		20,000	ns
Delay from Input Pulse Rising to UG Rising Edge		UG = OPEN		325		ns
SOFT-START						
Soft-Start Current	I_{SS}	V_{SS} = 0V	**4.5**	5	**5.5**	µA
Soft-Start Pin PreBias Voltage Range	V_{SS_PRE}	In prebias output condition; V_{SS_PRE} = V_{FB}	**0**		**1.6**	V
Soft-Start PreBias Voltage Accuracy		V_{FB} = 500mV	**-25**		**25**	mV
Soft-Start Clamp Voltage	$V_{SSCLAMP}$		**3**	3.4	**3.8**	V
REFERENCE VOLTAGE						
Reference Accuracy		Measured at FB pin	**1.584**	1.6	**1.616**	V
FB Pin Input Bias Current		V_{FB} = 1.6V	**-0.05**		**0.05**	µA
ERROR AMPLIFIER						
Transconductance Gain				2		ms
COMP Output Impedance				10		MΩ
Unity Gain Bandwidth		C_{CMP} = 100pF from COMP pin to GND		11		MHz

Electrical Specifications

Refer to the Block Diagram (page 6) and Typical Application Schematics (page 7). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, EN = 5.0V, T_A = -40°C to +125°C. Typicals are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Slew Rate		C_{CMP} = 100pF from COMP pin to GND		±2.5		V/µs
COMP Output Current Capability				±300		µA
COMP Output Voltage High			**3.5**	3.7	**3.9**	V
COMP Output Voltage Low					**0.3**	V
SLOPE COMPENSATION SETTING						
SLOPE Pin Voltage				500		mV
SLOPE Accuracy		R_{SLOPE} = 20k (0.1%)	**-30**		**30**	%
		R_{SLOPE} = 40.2k (0.1%)	**-30**		**30**	%
CURRENT SENSE AMPLIFIER						
ISENxN, ISENxP Common Mode Voltage Range			**4**		**55**	V
ISENxN, ISENxP Bias Current	$I_{SENxBIAS}$	Sinking into pin, EN = 5V, V_{ISENxN} = V_{ISENxP} = 4V to 55V	**90**	112	**130**	µA
ZERO CROSSING DETECTION						
Zero Crossing Detection (ZCD) Threshold	V_{ZCD_TH}	R_{SEN} Differential Voltage R_{SET2A}+R_{SET2B} = 665Ω (0.1%) R_{BIAS2A}+R_{BIAS2B} = 665Ω (0.1%) See page 7 for R_{SET} resistors		1.3		mV
OVERCURRENT PROTECTION						
Peak Current Cycle-by-Cycle Limit Voltage Threshold	V_{OC1}	R_{SEN} Differential Voltage R_{SET1A}+R_{SET1B} = 665Ω (0.1%) R_{BIAS2A}+R_{BIAS2B} = 665Ω (0.1%) See page 7 for R_{SET} resistors	**32**	47	**60**	mV
Peak Current Cycle-by-Cycle Limit Delay		UG = OPEN, from V_{OC1} threshold to UG falling		50		ns
Peak Current Hiccup/Latch-off Voltage Threshold	V_{OC2}	R_{SEN} Differential Voltage R_{SET1A}+R_{SET1B} = 665Ω (0.1%) R_{BIAS2A}+R_{BIAS2B} = 665Ω (0.1%) See page 7 for R_{SET} resistors	**45**	62	**75**	mV
OC2 Hiccup/Latch-off Blanking Time		Consecutive OC2 switching cycles		3		cycles
OC2 Hiccup Retry Delay				500		ms
AVERAGE OVERCURRENT PROTECTION AND CONSTANT CURRENT LIMITING LOOP						
IMON Offset Current		$V_{RSEN-CSA2}$ = 0mV, V_{ISEN2N} = 4V to 55V, R_{SET2A}+R_{SET2B} = 665Ω (0.1%) R_{BIAS2A}+R_{BIAS2B} = 665Ω (0.1%)	**7.0**	8.5	**10.0**	µA
IMON Current Accuracy	$IMON_{CSA2}$	$V_{RSEN-CSA2}$ = 25mV, V_{ISEN2N} = 4V to 55V, R_{SET2A}+R_{SET2B} = 665Ω (0.1%) R_{BIAS2A}+R_{BIAS2B} = 665Ω (0.1%)	**12**	13.2	**15**	µA
	$IMON_{CSA2}$	$V_{RSEN-CSA2}$ = 76mV, V_{ISEN2N} = 4V to 55V, R_{SET2A}+R_{SET2B} = 665Ω (0.1%) R_{BIAS2A}+R_{BIAS2B} = 665Ω (0.1%)	**21**	22.8	**26**	µA
Fault Threshold at IMON/DE Pin		Selected LATCHOFF/HICCUP response	**1.9**	2.0	**2.1**	V
OC_AVG Hiccup Retry Delay				500		ms
Constant Current Limit Reference Accuracy	$VREF_{CC}$		**1.584**	1.6	**1.616**	V
PWM CONTROLLER						
Minimum UGATE ON Time	t_{MINON_UG}	UGATE pulse width, UG = OPEN, LG = OPEN	**240**	300	**360**	ns
Minimum UGATE OFF Time	t_{MINOFF_UG}	V_{COMP} = 3.5V, UG = OPEN, LG = OPEN		285		ns
Minimum LGATE ON Time	t_{MINON_LG}	V_{COMP} = 3.5V, UG = OPEN, LG = OPEN	**140**	175	**210**	ns

Electrical Specifications

Refer to the Block Diagram (page 6) and Typical Application Schematics (page 7). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V and V_{VCC} = 5.2V, EN = 5.0V, T_A = -40°C to +125°C. Typicals are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
GATE DRIVERS						
UG Source Resistance	R_{UGSRC}	50mA source current; V_{BOOT} - V_{PH} = 4.5V		1.2		Ω
UG Source Current	I_{UGSRC}	UG - PH = 2.5V; V_{BOOT} - V_{PH} = 4.5V		2.0		A
UG Sink Resistance	R_{UGPD}	100mA sink current; V_{BOOT} - V_{PH} = 4.5V		0.65		Ω
UG Sink Current	I_{UGPD}	UG - PH = 2.5V; V_{BOOT} - V_{PH} = 4.5V		3.0		A
LG Source Resistance	R_{LGSRC}	50mA source current		1.0		Ω
LG Source Current	I_{LGSRC}	LG - PGND = 2.5V		2.0		A
LG Sink Resistance	R_{LGPD}	100mA sink current		0.55		Ω
LG Sink Current	I_{LGPD}	LG - PGND = 2.5V		3.0		A
UG to PH Pull-Down Resistance				50		kΩ
LG to PGND Pull-Down Resistance				50		kΩ
BOOT-PH Refreshing Detection Threshold			**3.1**	3.3	**3.5**	V
BOOT-PH Refreshing Detection Threshold Hysteresis			**100**	150	**250**	mV
Dead-Time Delay - UG Falling to LG Rising	t_{DT1}	UG = OPEN, LG = OPEN	**45**	55	**65**	ns
Dead-Time Delay - LG Falling to UG Rising	t_{DT2}	UG = OPEN, LG = OPEN	**45**	55	**65**	ns
OUTPUT OVERVOLTAGE DETECTION/PROTECTION (NOTE: FB_OVP response is selectable to be LATCHOFF or HICCUP)						
FB Overvoltage Rising Trip Threshold	V_{FBOV_REF}	Percentage of Reference Point, VFB = 1.6V Selected LATCHOFF/HICCUP response.	**111**	115	**118**	%
FB Overvoltage Recovery Threshold			**108**	112	**115**	%
Overvoltage Threshold Hysteresis				3		%
FB Overvoltage Protection Delay		Overvoltage detection filter		1		µs
FB_OV Hiccup Retry Delay				500		ms
OUTPUT UNDERVOLTAGE DETECTION						
FB Undervoltage Falling Threshold	V_{FBUV_REF}	Percentage of reference point, VFB = 1.6V	**85**	87.5	**90**	%
FB Undervoltage Recovery Threshold			**88**	90.5	**93**	%
Undervoltage Hysteresis				3		%
POWER-GOOD MONITOR (OUTPUT OVERVOLTAGE, OUTPUT UNDERVOLTAGE, VIN OVERVOLTAGE)						
PGOOD Leakage Current		PGOOD HIGH, V_{PGOOD} = 5V			**1**	µA
PGOOD Low Voltage		PGOOD LOW, I_{PGOOD} = 0.5mA		0.20	**0.4**	V
PGOOD Rising Delay -1		From V_{SS} = 0.95*VREF to V_{SS} = $V_{SSCLAMP}$, C_{SS} = 15nF		5.6		ms
PGOOD Rising Delay -2		From V_{SS} = $V_{SSCLAMP}$ to PGOOD HIGH		0.5		ms
PGOOD Falling Delay		Blanking filter time before transition		10		us
HIC/LATCH Pin						
HIC/LATCH Input Pull-Down Current		$V_{HIC/LATCH}$ = 5V	**0.8**	1	**2**	µA
HIC/LATCH Input High Threshold			**2**			V
HIC/LATCH Input Low Threshold					**0.8**	V
OVER-TEMPERATURE PROTECTION						
Over-Temperature Threshold				160		°C
Over-Temperature Recovery Threshold				145		°C

NOTE:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance

All the performance curves are taken from the Evaluation Board (ISL78268EVAL1Z) unless otherwise noted.

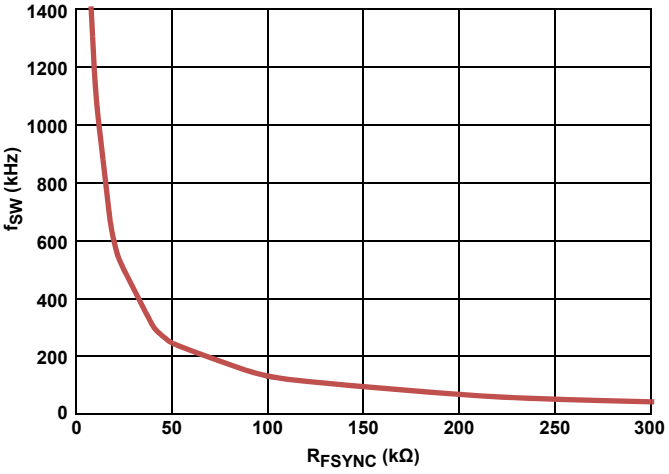


FIGURE 6. FREQUENCY SETTING (AT +25°C), V_{IN} = 36V

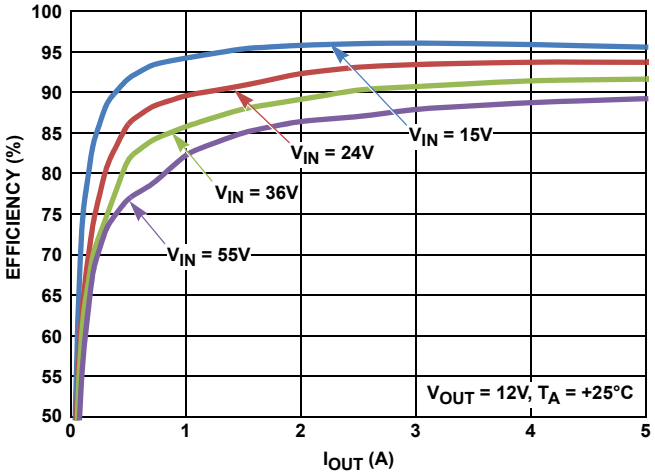


FIGURE 7. EFFICIENCY (AT +25°C): DE MODE, V_{OUT} = 12V, L = 4.7µH, f_{SW} = 300kΩ

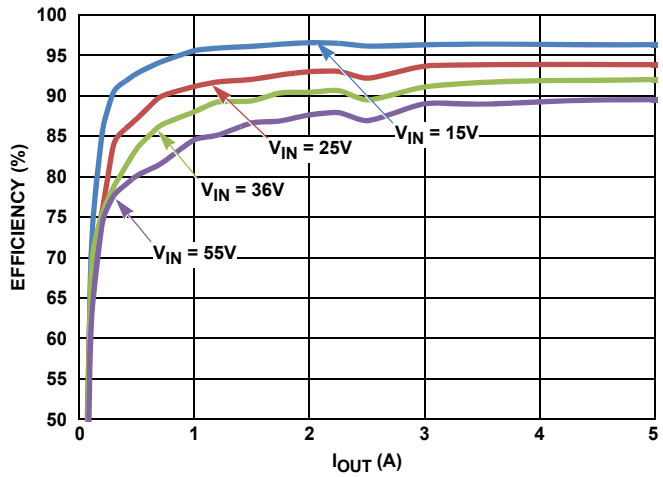


FIGURE 8. EFFICIENCY (AT +125°C): DE MODE, V_{OUT} = 12V, L = 4.7µH, f_{SW} = 300kΩ

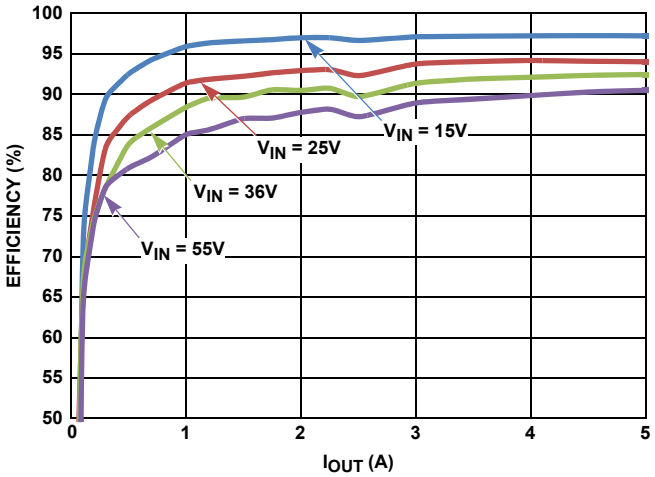


FIGURE 9. EFFICIENCY (AT -40°C), DE MODE, V_{OUT} = 12V, L = 4.7µH, f_{SW} = 300kΩ

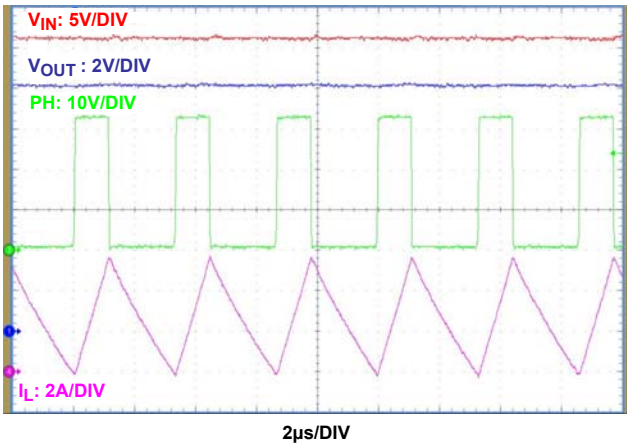


FIGURE 10. DE MODE: V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 2.5A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz (CONTINUOUS CONDUCTION OPERATION)

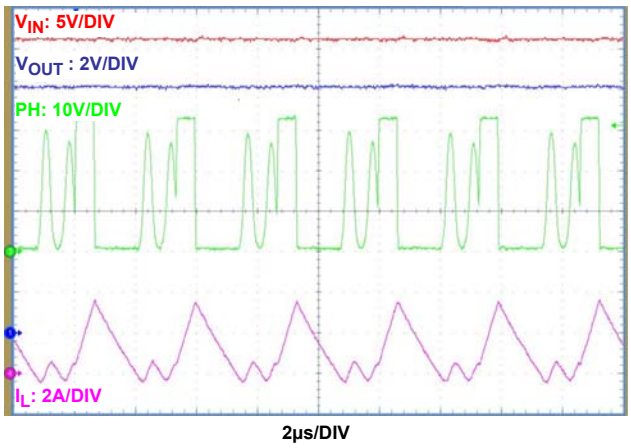


FIGURE 11. DE MODE: V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 1.0A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz (DISCONTINUOUS CONDUCTION OPERATION)

Typical Performance

All the performance curves are taken from the Evaluation Board (ISL78268EVAL1Z) unless otherwise noted. **(Continued)**

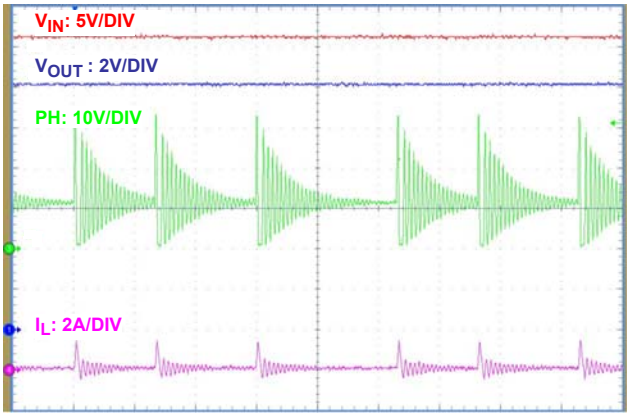


FIGURE 12. DE MODE: V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 30mA, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz (PULSE SKIP OPERATION)

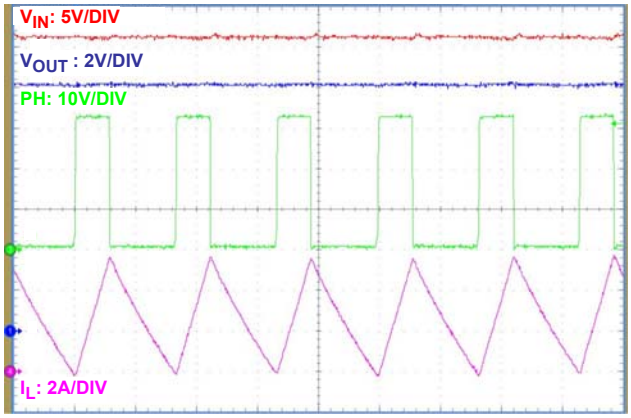


FIGURE 13. FORCED PWM MODE, V_{IN}=36V, V_{OUT} = 12V, I_{OUT} = 2.5A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

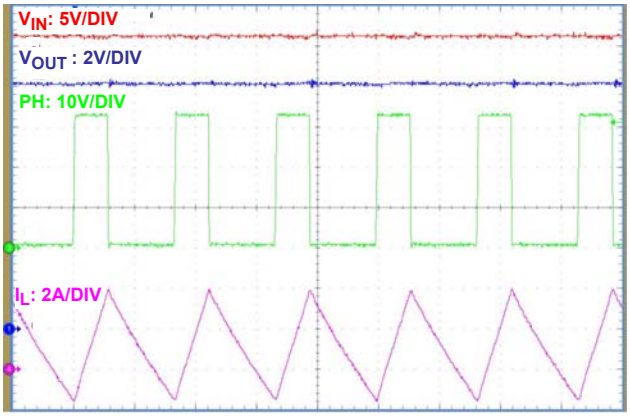


FIGURE 14. FORCED PWM MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 1.0A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

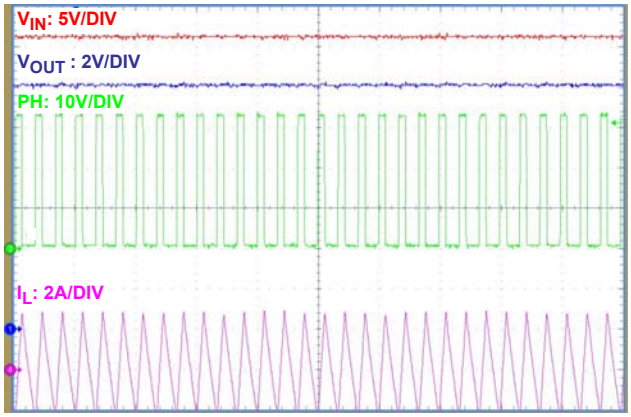


FIGURE 15. FORCED PWM MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 30mA, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

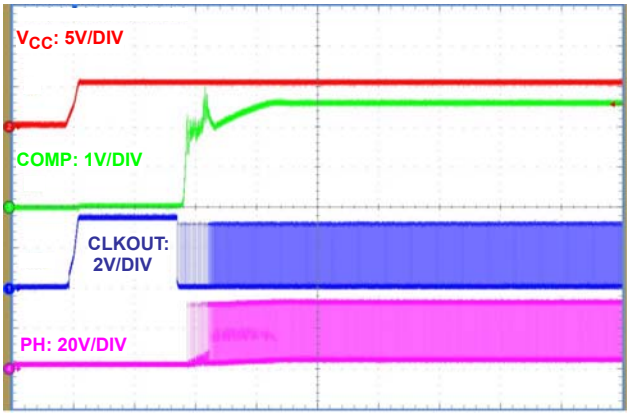


FIGURE 16. INITIALIZATION TO START-UP: DE MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 2.5A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

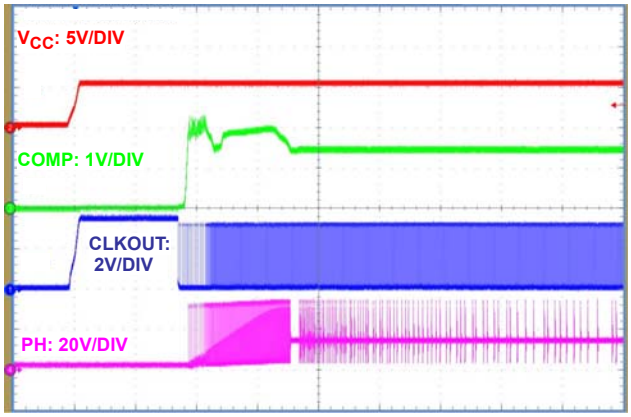


FIGURE 17. INITIALIZATION TO START-UP: DE MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 0A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

Typical Performance

All the performance curves are taken from the Evaluation Board (ISL78268EVAL1Z) unless otherwise noted. **(Continued)**

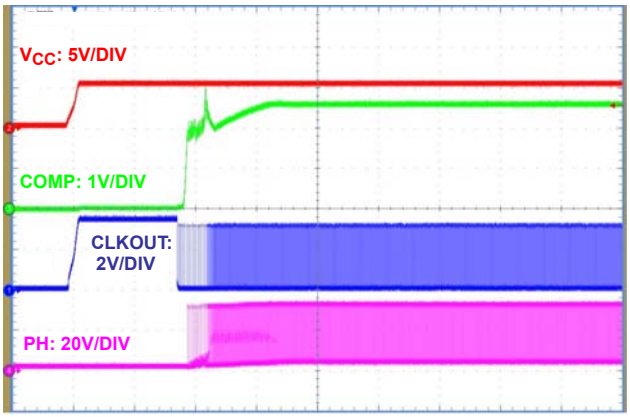


FIGURE 18. INITIALIZATION TO START-UP: FORCED-PWM MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 2.5A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

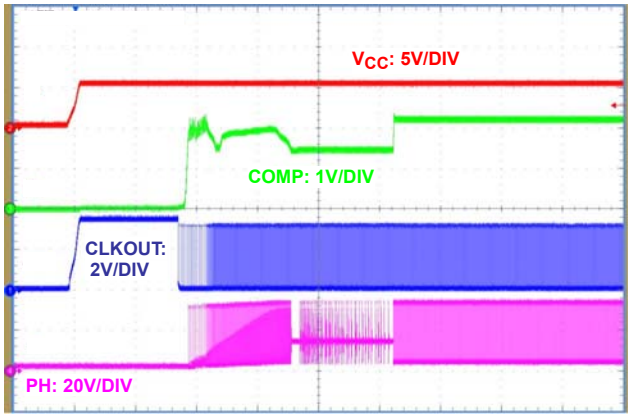


FIGURE 19. INITIALIZATION TO START-UP: FORCED-PWM MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 0A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

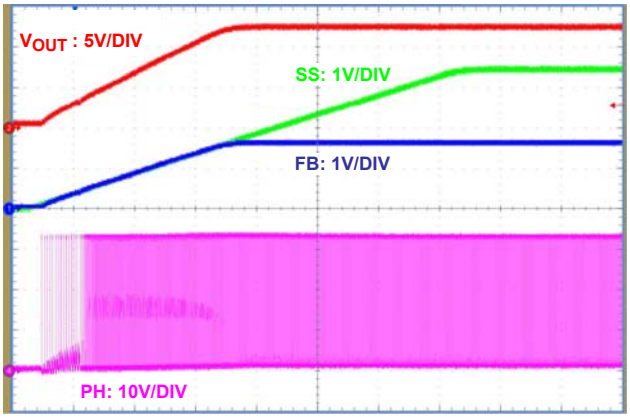


FIGURE 20. SOFT-START (NON-PREBIASED): DE MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 2.5A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

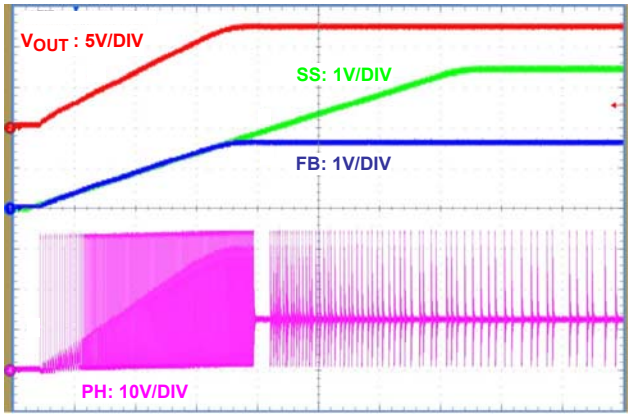


FIGURE 21. SOFT-START (NON-PREBIASED): DE MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 0A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

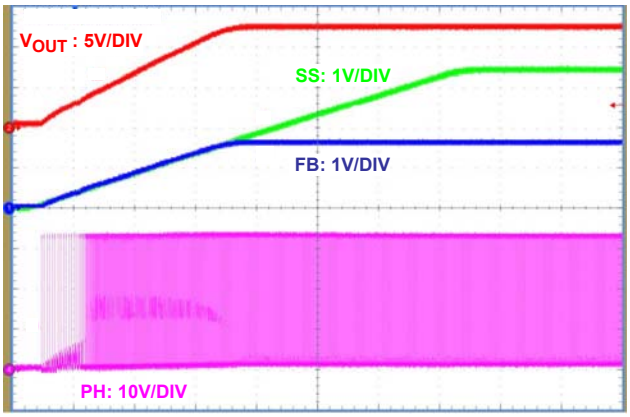


FIGURE 22. SOFT-START (NON-PREBIASED): FORCED-PWM MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 2.5A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

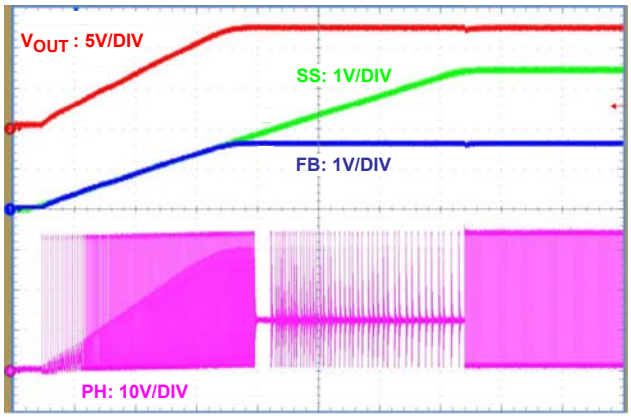


FIGURE 23. SOFT-START (NON-PREBIASED): FORCED-PWM MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 0A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

Typical Performance

All the performance curves are taken from the Evaluation Board (ISL78268EVAL1Z) unless otherwise noted. **(Continued)**

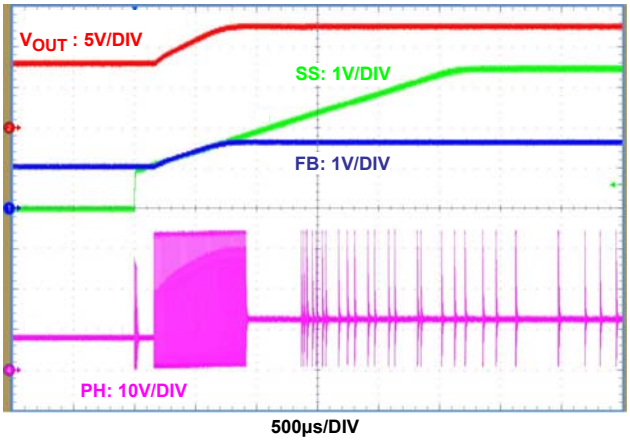


FIGURE 24. SOFT-START (PREBIASED): DE MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 0A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

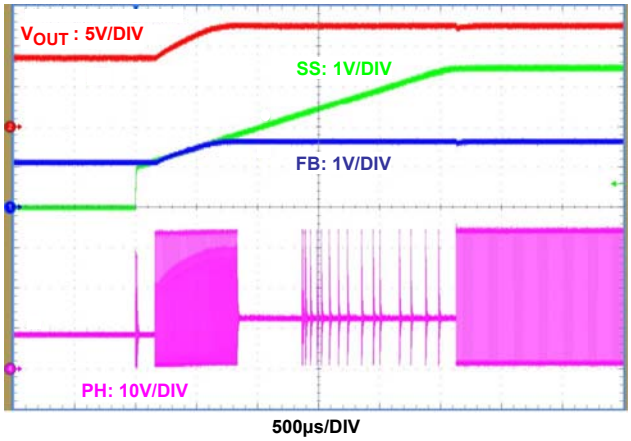


FIGURE 25. SOFT-START (PREBIASED): FORCED-PWM MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 0A, L = 4.7µH, C_{OUT} = 98µF, f_{SW} = 300kHz

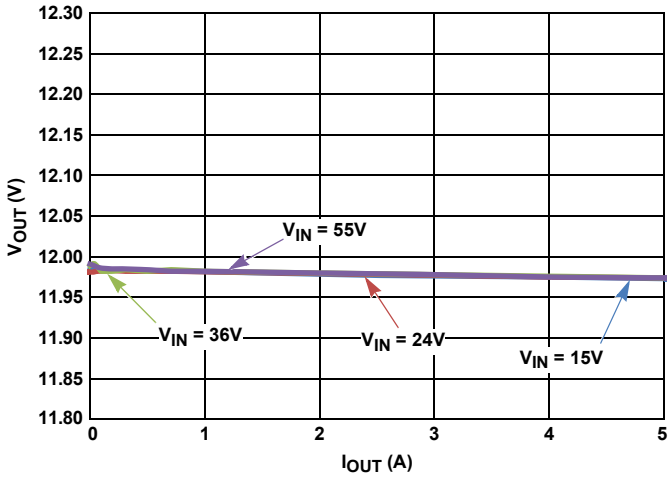


FIGURE 26. LOAD REGULATION

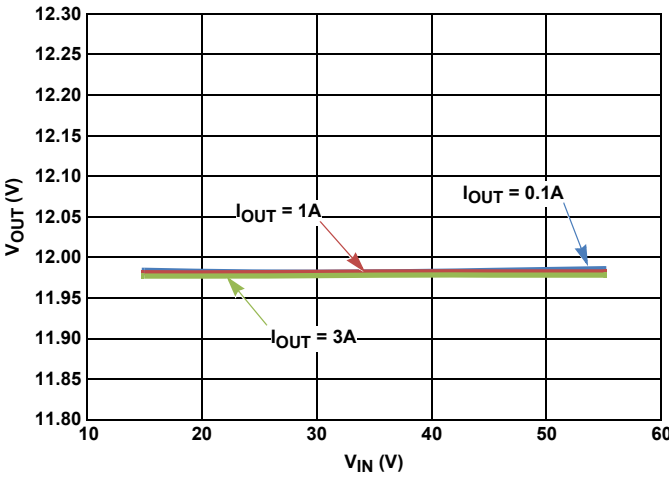


FIGURE 27. LINE REGULATION

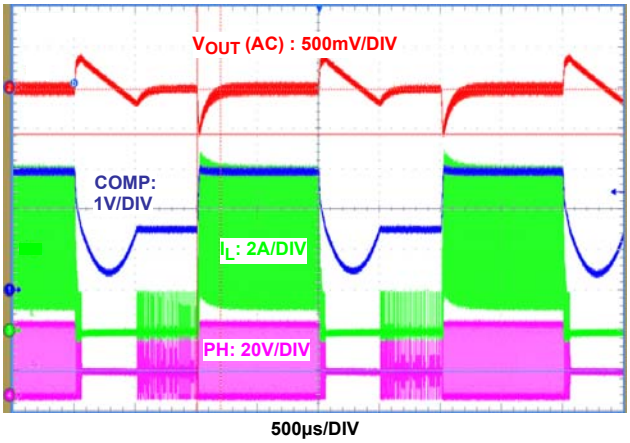


FIGURE 28. TRANSIENT RESPONSE: DE MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 0.1A TO 4.5A, L = 4.7µH, C_{OUT} = 98µF

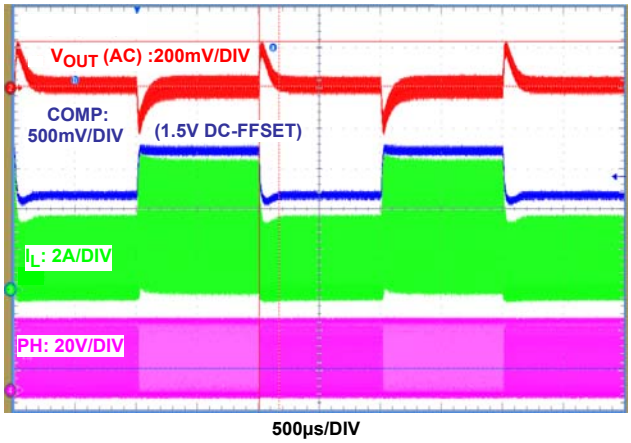


FIGURE 29. TRANSIENT RESPONSE: DE MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 1A TO 3A, L = 4.7µH, C_{OUT} = 98µF

Typical Performance

All the performance curves are taken from the Evaluation Board (ISL78268EVAL1Z) unless otherwise noted. **(Continued)**

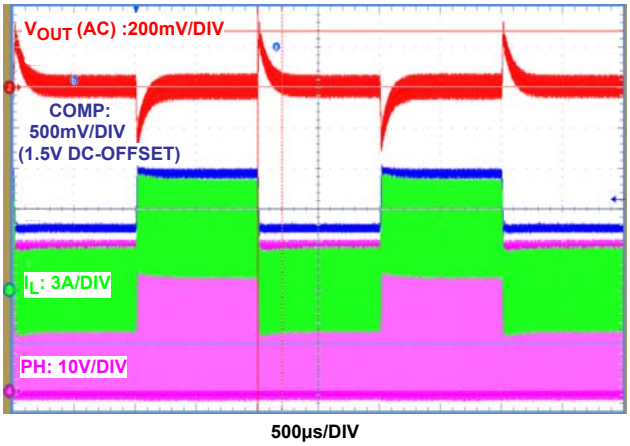


FIGURE 30. TRANSIENT RESPONSE: FORCED-PWM MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 0.1A TO 4.5A, L = 4.7µH, C_{OUT} = 98µF

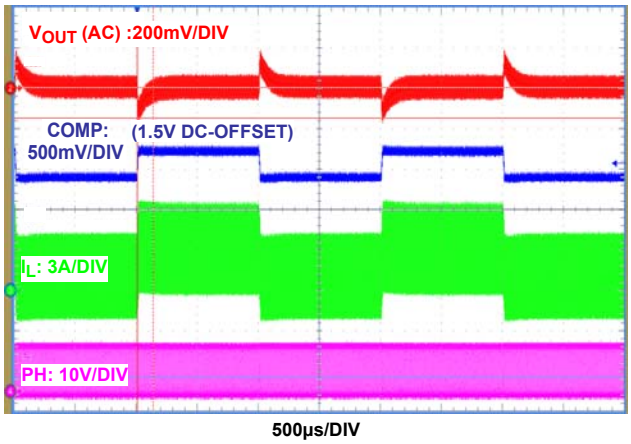


FIGURE 31. TRANSIENT RESPONSE: FORCED-PWM MODE, V_{IN} = 36V, V_{OUT} = 12V, I_{OUT} = 1A TO 3A, L = 4.7µH, C_{OUT} = 98µF

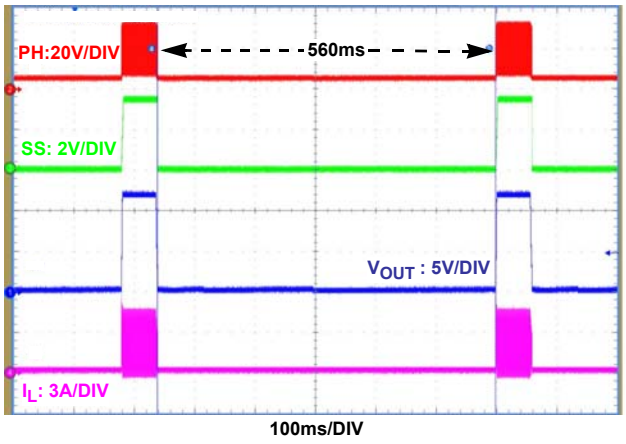


FIGURE 32. HICCUP: ACL, V_{IN} = 30V, V_{OUT} = 12V, R_{IMON} = 156kΩ

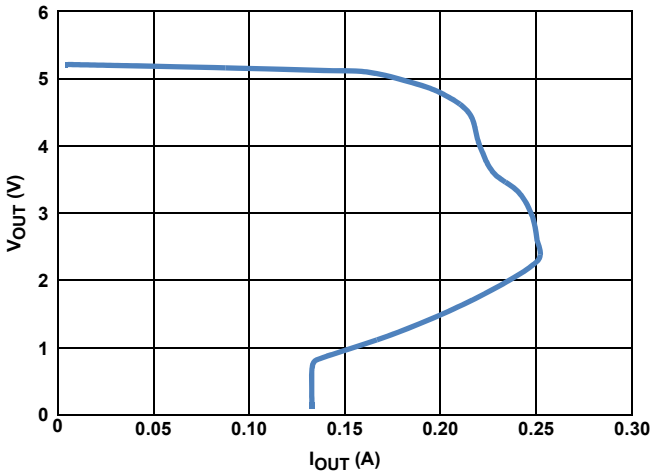


FIGURE 33. INTERNAL LDO LOAD REGULATION: V_{IN} = 36V, T_A = +25°C

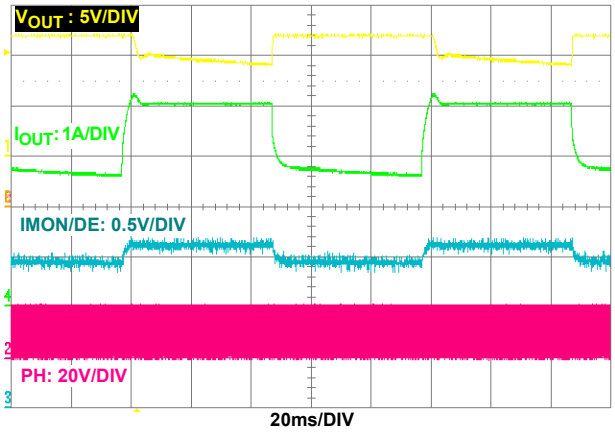


FIGURE 34. AVERAGE CONSTANT OUTPUT CURRENT CONTROL, V_{IN} = 20V, V_{OUT} (SETTING) = 12V, C_{IMON} = 1nF, R_{IMON} = 130kΩ, ACL = 4.05A, R_L = 5.0Ω TO 2.0Ω, F_{LOAD} = 10Hz, DUTY OF LOAD CHANGE = 50%

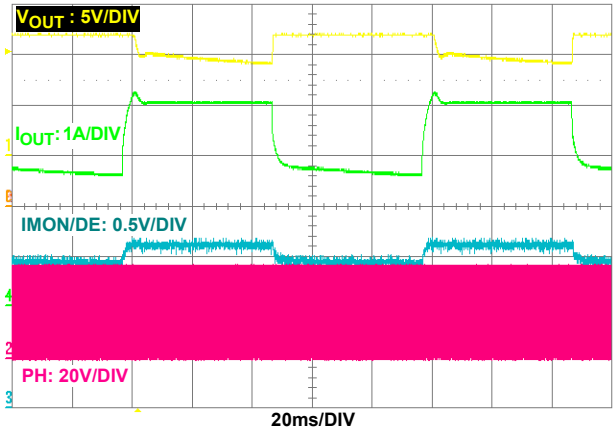


FIGURE 35. AVERAGE CONSTANT OUTPUT CURRENT CONTROL, V_{IN} = 36V, V_{OUT} (SETTING) = 12V, C_{IMON} = 1nF, R_{IMON} = 130kΩ, ACL = 4.05A, R_L = 5.0Ω TO 2.0Ω, F_{LOAD} = 10Hz, DUTY OF LOAD CHANGE = 50%

Typical Performance

All the performance curves are taken from the Evaluation Board (ISL78268EVAL1Z) unless otherwise noted. **(Continued)**

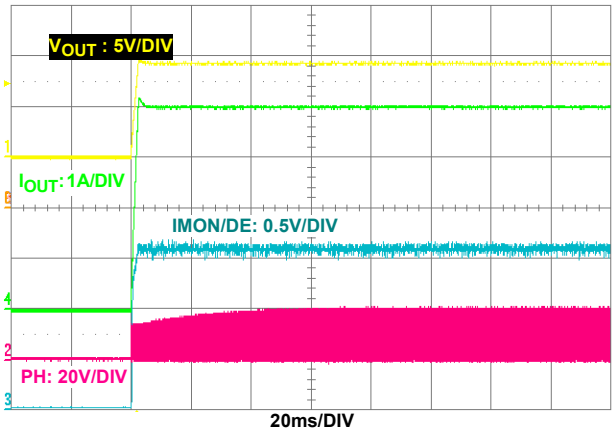


FIGURE 36. AVERAGE CONSTANT OUTPUT CURRENT CONTROL, V_{IN} = 20V, V_{OUT} (SETTING) = 12V, C_{IMON} = 1nF, R_{IMON} = 130kΩ, ACL = 4.05A, R_L = 2.3Ω, START-UP WITH FIXED R_L

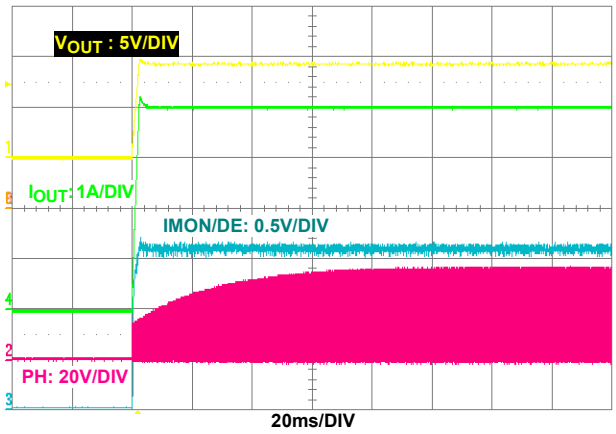


FIGURE 37. AVERAGE CONSTANT OUTPUT CURRENT CONTROL, V_{IN} = 36V, V_{OUT} (SETTING) = 12V, C_{IMON} = 1nF, R_{IMON} = 130kΩ, ACL = 4.05A, R_L = 2.3Ω, START-UP WITH FIXED R_L

Operation Description

The ISL78268 is an automotive graded (AEC-Q100 Grade-1) single-phase synchronous buck controller with integrated high/low side 2/3A MOSFET drivers. It supports a wide operating input voltage range of 5V to 55V and up to 60V at V_{IN} when not switching. The device also provides the features of selectable Diode Emulation mode for the higher efficiency operation in light load conditions, average constant output current controls, and several protection features such as input overvoltage protection, output overvoltage protection, cycle-by-cycle current limit and protections, and thermal protection. Details of the functions are described in the following.

Synchronous Buck

In order to improve the efficiency, the ISL78268 employs synchronous buck architecture. In a synchronous buck, the LG output drives the synchronous low-side MOSFET, which replaces the freewheeling diode and improves the power losses by the voltage drop of the freewheeling diode while the high-side MOSFET is off. The LG signal is complementary to the UG signal.

The UG signal is powered from a charge pump that generates a voltage between BOOT and PH. An external diode from PVCC to BOOT charges an external capacitor between BOOT and PH when LG is high and PH is low. The capacitor provides the power to drive UG high. BOOT rises with PH and maintains the voltage to drive UG as the bootstrap diode is reverse biased.

Adaptive Dead-Time Control

The UG and LG drivers are designed to have an adaptive dead-time algorithm that optimizes operation with varying MOSFET conditions. In this algorithm, the device detects the off timing of external MOSFETs which is turning off via the gate driver output voltage. The ISL78268 adds internally fixed 55ns dead-time before turning on the target gate driver. This algorithm helps to prevent shoot-through current at the switching of external MOSFETs and also optimizes the total dead-time to maximize the efficiency.

Operation Initialization and Soft-Start

Prior to the converter initialization, VIN and VCC need to be supplied within the valid voltage range and the EN pin needs to be biased to logic high. When these conditions are provided, the controller begins soft-start. Once the output voltage is within the proper window of output regulation, V_{PGOOD} is asserted logic high.

Figure 38 shows the ISL78268 internal start-up timing diagram from the power-up to soft-start and valid PGOOD assertion.

As shown on Figure 38, there are 5 time intervals before the soft-start is initialized, they are specified as $t_1$through t_5. After soft-start is initiated, there are 5 time intervals indicated as t_5 through t_{10}. The descriptions for each time interval are as follows:

t_1 - t_2: The internal enable comparator holds the ISL78268 in shutdown until the EN pin voltage (V_{EN}) rises above 1.2V (typ) at the time of t_1. During t_1 - t_2 the internal LDO output voltage at the PVCC pin (V_{PVCC}) will gradually increase until t_2 when it reaches the internal Power-On Reset (POR) rising threshold which is 4.5V(typ).

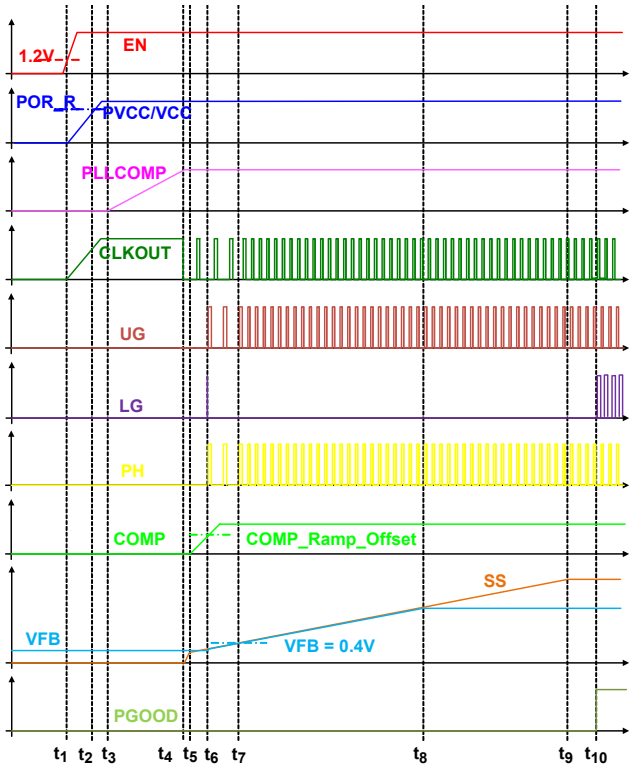


FIGURE 38. CIRCUIT INITIALIZATION AND SOFT-START

t_2 - t_3: During t_2 - t_3 time, the ISL78268 will go through a self-calibration process to determine the pin connections (HIC/LATCH, IMON/DE) for the operation mode selections. The time duration for t_2 - t_3 is typically 170µs.

t_3 - t_4: During this period, the ISL78268 will wait until the internal PLL circuit is locked to the preset oscillator frequency set by the resistor on FSYNC or the external clock at FSYNC. When PLL locking is achieved at t_4, the oscillator will generate output at the CLK_OUT pin. The time duration for t_3 - t_4 depends on PLL_COMP pin configuration. The PLL is compensated with a series resistor-capacitor R_{PLLCMP}, $C_{PLLCMP1}$ from the PLL_COMP pin to GND and a capacitor $C_{PLLCMP2}$ from PLL_COMP to GND. Typical values are R_{PLLCMP} = 3.24kΩ, $C_{PLLCMP1}$ = 6.8nF, $C_{PLLCMP2}$ = 1nF. With this PLL_COMP compensation, the time duration for t_3 - t_4 is around 0.8ms.

t_4 - t_5: After the PLL locks the frequency at t_4, the system is preparing to soft-start. The ISL78268's unique feature will prebias the V_{SS} based on V_{FB} voltage during this time. The duration time for t_4 - t_5 is around 50µs. During t_4 - t_5 drivers remain off.

t_5 - t_6: After t_5, the soft-start circuit starts to ramp up from the prebiased VFB. At the same time, the COMP pin voltage starts to ramp up also. The UG driver will be enabled at t_5. However, before t_6, COMP is still below the peak current mode control ramp offset, the drivers will not be switching. During soft-start period t_5 - t_{10}, the device will operate with Diode Emulation mode and keep LG driver off.

t_6 - t_7: If the FB voltage (VFB) is below 0.4V (typ), the device operates at fixed minimum frequency (50kHz (typ)) with minimum high-side MOSFET on-time. When VFB reaches

0.4V (typ), the switching frequency will change to the target frequency gradually and the high-side MOSFET on-time will be controlled by the PWM control loop. If the prebiased FB voltage is above 0.4V (typ), the device starts up with the target switching frequency. If FB voltage is >0.4V the time t_6 - t_7 is negligible.

t_6 - t_8: At t_6, COMP is above the peak current mode control ramp offset, the drivers starts switching. Output voltage ramps up while FB voltage is following SS ramp during this soft-start period. At t_8, output voltage reaches the regulation level and FB voltage reaches 1.6V (typ).

t_7 - t_{10}: SS pin voltage continues ramping up until it reaches SS clamp voltage 3.4V (typ) at t_9. The soft-start period will be completed at t_{10} which is 0.5ms (typ) after the t_9. When the soft-start completes, the device operates in the operation mode selected by the IMON/DE configuration. If the Forced PWM mode is selected, the device operates in full synchronous rectification. If the Diode Emulation Mode (DE Mode) is selected, the device will be able to operate in DE mode, i.e., turn-off low-side MOSFET when the inductor current reaches zero to prevent the negative current and improves the efficiency. At the end of soft-start period t_{10}, the PGOOD open-drain follows the COMP and inductor current ramp signal relations. Pin is released and will be pulled up by the external resistor.

Enable

To enable the device, the EN pin needs to be driven higher than 1.2V (typ.) by the external enable signal or resistor divider between VIN and GND. The EN pin has an internal 5MΩ (typ) pull-down resistor. Also, this pin internally has a 5.2V (typ) clamp circuit with 5kΩ (typ) resistor in series to prevent excess voltage applied to the internal circuits. When applying the EN signal using resistor divider from VIN, internal pull-down resistance needs to be considered. Also the resistor divider ratio needs to be adjusted as its EN pin input voltage may not exceed 5.2V.

To disable or reset all fault status, the EN pin needs to be driven lower than 1.1V (typ). When the EN pin is driven to low, the ISL78268 turns off all of the blocks to minimize the off-state quiescent current.

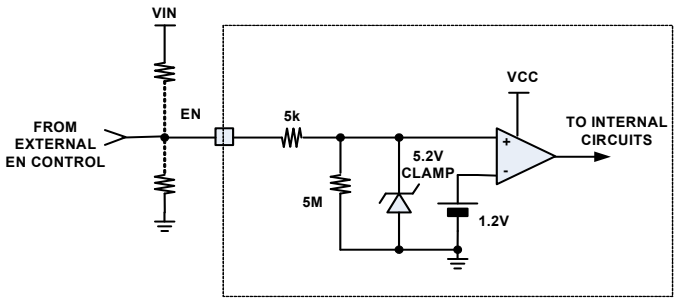


FIGURE 39. ENABLE BLOCK

Clock Generator and Synchronization

INTERNAL CLOCK FREQUENCY SETTING

The switching frequency is determined by the selection of the frequency-setting resistor, R_{FSYNC}, connected from the FSYNC pin to GND. Equation 1 and Figure 40 provide the relation between R_{FSYNC} and switching frequency. For stable operation of the device, it is recommended to set the f_{SW} between 50kHz to 1.1MHz.

$$R_{FSYNC} = 2.5x(10)^{10}x\left(\frac{0.5}{f_{SW}} - 5.0X10^{-8}\right) \quad \text{(EQ. 1)}$$

Where f_{SW} is the switching frequency of the device.

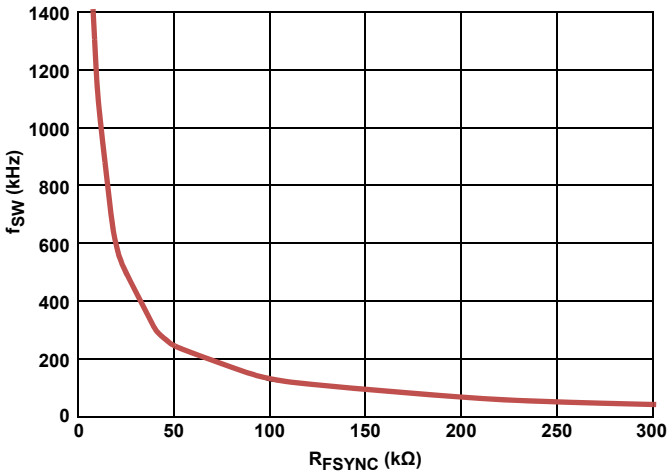


FIGURE 40. R_{FSYNC} vs f_{SW}

Figure 41 shows the block diagram of the Clock Generator block. The FSYNC pin is biased at 0.5V (typ). The 0.5V at FSYNC creates a constant current with R_{FSYNC}. The current is fed to the internal oscillator to generate the internal base clock. This internal base clock is reshaped with the Phase Lock Loop (PLL) circuitry and the output of PLL will be used as the main clock of the device.

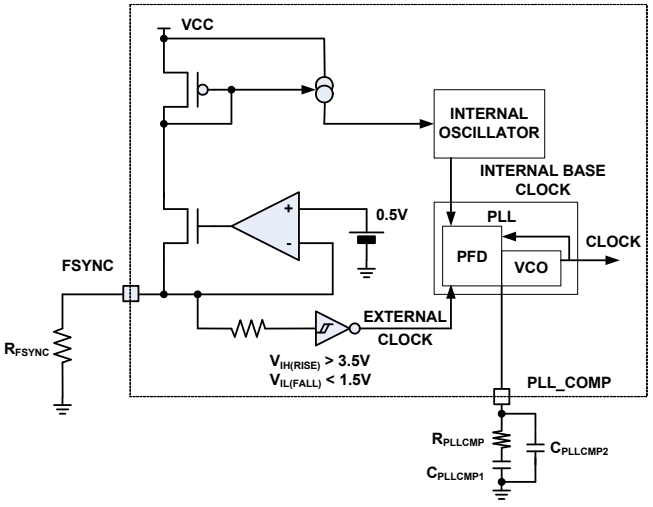


FIGURE 41. CLOCK GENERATOR AND EXTERNAL CLOCK SYNCHRONIZATION BLOCK

SYNCHRONIZATION WITH EXTERNAL CLOCK

The ISL78268 contains a PLL circuitry and has frequency synchronization capability by simply connecting the FSYNC pin to an external square pulse waveform.

The PLL block detects the rising edge of external clock and synchronizes it with the rising edge of UG. The delay time of UG rising from the external clock rising edge is 325ns (typ).

The FSYNC pin has special thresholds to detect the external clock. The input high level of external clock should be higher than 3.5V and low level should be lower than 1.5V.

When continuous external clock pulse is applied while operating with internal clock which is determined by R_{FSYNC}, this device synchronizes with the external clock gradually and continues its switching. However, when the external clock is removed for a certain period (~6ms), the device will stop its switching and restart from the initialization/soft-start process after about a 50ms interval.

The PLL is compensated with a series connected resistor and capacitor (R_{PLLCMP} and C_{PLLCMP}) from the PLL_COMP pin to GND and a capacitor ($C_{PLLCMP2}$) from PLL_COMP to GND. For stable operation, recommended to set R_{PLLCMP} = 3.24kΩ, $C_{PLLCMP1}$ = 6.8nF, $C_{PLLCMP2}$ = 1nF. The typical lock time for this case will be around 0.8ms.

The CLKOUT pin provides a square pulse waveform at the switching frequency. The amplitude is GND to VCC with 270ns (typ) pulse width, and the rising edge is 180° shifted from the rising edge of UG.

Soft-Start

Soft-start is implemented by an internal 5µA current source charging the soft-start capacitor (C_{SS}) at SS to GND. The voltage on the SS pin controls the reference voltage for the FB pin during soft-start. When starting up the system while the output voltage is remaining (prebiased), a prebias circuit charges the C_{SS} capacitor to the same voltage as FB voltage before soft-start begins. This allows more accurate correlation between the soft-start ramp time and the output voltage.

Assuming no prebiased output condition, the soft-start ramp time is:

$$t_{SS} = V_{REF}\frac{C_{SS}}{5\mu A} \quad \text{(EQ. 2)}$$

Where V_{REF} is the 1.6V reference.

Assuming no load condition, the average inductor current $I_{L\_softstart}$ to charge the output capacitors from 0V to final regulation voltage within soft-start time t_{SS} can be estimated as:

$$I_{Lsoftstart} = V_{OUT}\frac{C_{OUT}}{t_{SS}} \quad \text{(EQ. 3)}$$

If start-up with full load is required, the total inductor average current at the soft-start period is the sum of full load current and $I_{L\_softstart}$. Based on this consideration, enough soft-start time should be set to make sure overcurrent protection is not tripped.

At the beginning of soft-start, if the prebiased V_{FB} voltage is lower than 0.4V (typ), the device is forced to switch at 50kHz (typ) with minimum on-time of high-side MOSFET. When V_{FB} reaches 0.4V (typ) or higher, the device operates with normal switching frequency and on-time. If the prebiased VFB voltage is higher than 0.4V (typ) at the starting of soft-start, the device starts with normal switching frequency from the beginning.

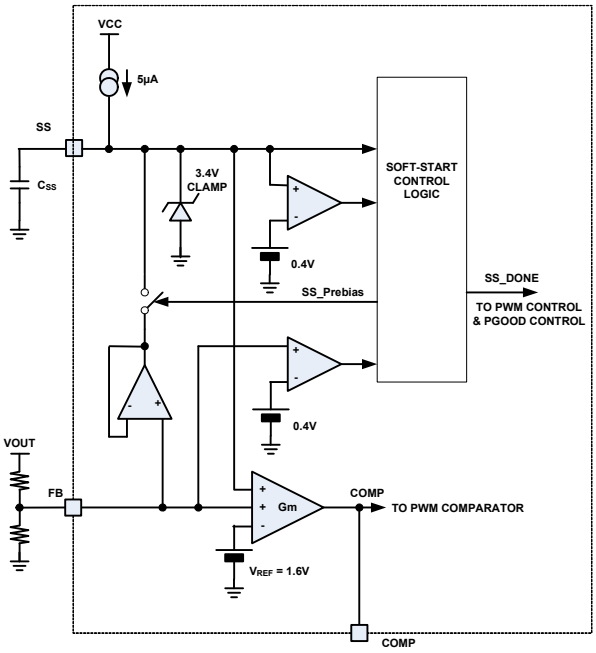


FIGURE 42. SOFT-START BLOCK

The soft-start period will be finished when the SS pin voltage reaches its clamp voltage (3.4V typ) with a 0.5ms (typ) additional interval. At the end of soft-start period, the pull-down of the PGOOD pin will be released and this pin will be pulled up by external resistor, which will be biased to VCC or external logic supply level.

While in soft-start period, the device operates in Diode Emulation mode to prevent undesired negative current at inductor from output. In this period, regardless of the configuration of IMON/DE pin, i.e., either Forced PWM mode or Diode Emulation mode is selected, only the high-side MOSFET will be switched and low-side MOSFET will be kept off.

Bootstrap for High-side NMOS Drive

To turn on the high-side MOSFET properly, the ISL78268 employs a bootstrap circuit using an external boot capacitor (C_{BOOT}) and diode (D_{BT}). At the time the high-side MOSFET turns off, to maintain the current on the inductor, the PH node will go down to GND level at low-side MOSFET turn on. While in this low-side MOSFET on period, the diode connected from PVCC to boot capacitor will be forward biased and charge up the boot capacitor. When the low-side MOSFET is turned off and the high-side MOSFET is turned on after dead-time, the PH node goes up to VIN level and the BOOT pin bias is VIN + PVCC - V_F to drive the high-side driver circuitry.

BOOT REFRESHING

In order to keep sufficient supply voltage for the high-side driver circuit operation, the ISL78268 has a boot-refreshing circuit. When the boot capacitor voltage becomes lower than 3.3V (typ), the low side transistor is forced to turn on with its minimum on time to charge the boot capacitor. The boot refreshing will occur at the beginning of soft-start and pulse skipping operation at very light load conditions.

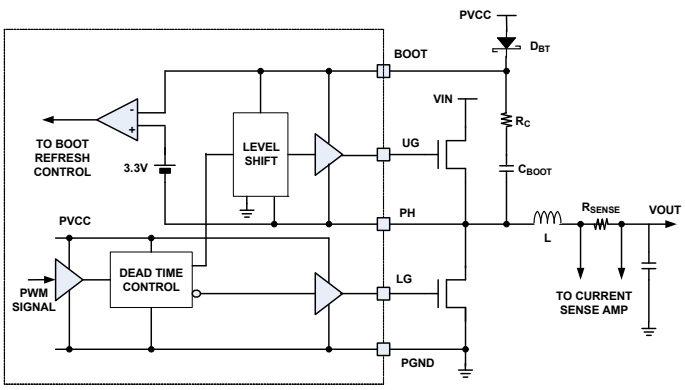


FIGURE 43. OUTPUT BOOT CONTROL

MINIMUM OFF-TIME CONSIDERATION

To ensure the charging of the boot capacitor, the device has internally fixed minimum off time (t_{minoff}) for the high-side MOSFET. Just after the high-side MOSFET turns off, the PH node goes down to GND level and boot capacitor will be charged from PVCC via an external diode (Schottky diode is recommended). However, when an NMOS with large Q_g is selected to support heavy load application, the internally fixed t_{minoff} may not be enough to charge the boot capacitor sufficiently. For this case, it is recommended to adjust the switching frequency or input voltage as the system has sufficient off time of high-side transistor.

PWM Operation

The switching cycle is defined as the time between UG pulse initiation signals. The cycle time of the pulse initiation signal is the inversion of the switching frequency set by the resistor between the FSYNC pin and ground.

The ISL78268 uses peak current mode control. The PWM operation is initialized by the clock from the oscillator. The high-side MOSFET is turned on (UG) by the clock at the beginning of a PWM cycle and the inductor current flows in the high-side MOSFET and ramps up. When the sum of the current sense signal (through I_{SEN1} current sense amplifier) and the slope compensation signal reaches the error amplifier output voltage, the PWM comparator is triggered and UG is turned off to shut down the high-side MOSFET. The high-side MOSFET stays off until the next clock signal comes for the next cycle.

After the high-side MOSFET is turned off, the low-side MOSFET turns on with the fixed dead-time. The off timing of low-side MOSFET is determined by either the next high-side on timing at next PWM cycle or when the inductor current become zero if the Diode Emulation mode is selected.

To prevent undesired shoot-through current at external high-side and low-side MOSFETs, the device has adaptive dead-time control and internally fixed dead-time. The internally fixed dead-time is typically 55ns, for both high-side to low side and low-side to high-side switching transition.

The output voltage is sensed by a resistor divider from V_{OUT} to the FB pin. The difference between the FB voltage and 1.6V (typ) reference is amplified and compensated to generate the error voltage signal at the COMP pin that is used for PWM generation circuits.

Current Sensing

The ISL78268 has two current sense amplifiers: one for high-side MOSFET peak current sensing for PWM control and overcurrent protections, and the other for output inductor current sensing for average current control and diode emulation timing control.

CURRENT SENSE AMPLIFIER 1 (CSA1)

The current-sense amplifier (CSA1) is used to sense the inductor current in the current-sense resistor placed in series with the high-side MOSFET. The sensed current information (I_{SEN1}) is used for peak current mode control and overcurrent protection. Peak current mode control is implemented using CSA1 in the PWM control loop as described in "PWM Operation".

The cycle-by-cycle peak current limit (OC1) is implemented by comparing I_{SEN1} with an 70µA threshold. At the peak current limit comparator threshold, the PWM pulse is terminated. During an overload condition when I_{SEN1} reaches 93µA (OC2 threshold), the IC enters into latch-off or hiccup mode, which is defined by the HIC/LATCH pin configuration. If latch-off mode is selected, the device stops switching when OC2 is tripped and will not restart until the EN or VIN is toggled. If Hiccup mode is selected, the PWM is disabled for 500ms (typ) before beginning a soft-start cycle. Three consecutive OC2 faults are required to enter hiccup or latch-off. OC2 hiccup or latch-off is enabled during soft-start and normal operating modes.

CURRENT SENSE AMPLIFIER 2 (CSA2)

The current-sense amplifier (CSA2) is used to sense the continuous (not pulsing as in R_{SEN1}) inductor current either by DCR sensing method or using a sense resistor in series with the inductor for more accurate sensing. The sensed current signal is used for three functions:

- Average constant current control
- Diode emulation
- Average OC protection

The ISEN2P voltage is also used to monitor the minimum output voltage. Under the overload condition (OC1) or under the average constant current control, if the voltage become lower than about 1.2V (typ), the device stops switching and enters Latch-off/ Hiccup mode.

If these three functions are not required in the application, CSA2 should be connected to VCC (or VIN).

SENSE RESISTOR CURRENT SENSING

A sense resistor can be placed in series with the inductor. As shown in Figure 44, the ISL78268 senses the voltage across the sense resistor. CSA1 is used to sense the high-side MOSFET's current. The sense resistor is placed between the input capacitors and the high-side MOSFET.

CSA2 is used to sense the inductor current. A sense resistor is placed between the inductor and the output capacitors.

The voltage on the ISEN(n)P and ISEN(n)N of the current sense amplifier are forced to be equal. The voltage across $R_{SET(n)}$ is equivalent to the voltage drop across the $R_{SEN(n)}$ resistor. The

resulting current into the ISEN(n)P pin is proportional (scaled) to the current in $R_{SEN(n)}$. Equation 4 is derived as:

$$I_{SEN(n)} = I_{R_{SEN(n)}} \cdot \frac{R_{SEN(n)}}{R_{SET(n)}} \quad \text{(EQ. 4)}$$

Where $R_{SET(n)}$ is the sum of $R_{SET(n)A}$ and $R_{SET(n)B}$ in Figure 44.

ISEN(n)P and ISEN(n)N have equal bias current (112µA typ) therefore, the resistors $R_{BIAS(n)}$ and $R_{SET(n)}$ should be matched to prevent offset.

To prevent noise injection from switching currents, it is recommended to place a filter capacitor in between the R_{SET} resistors. Typically, 220pF ceramic capacitor is used when the $R_{SET(n)}$ is 665Ω.

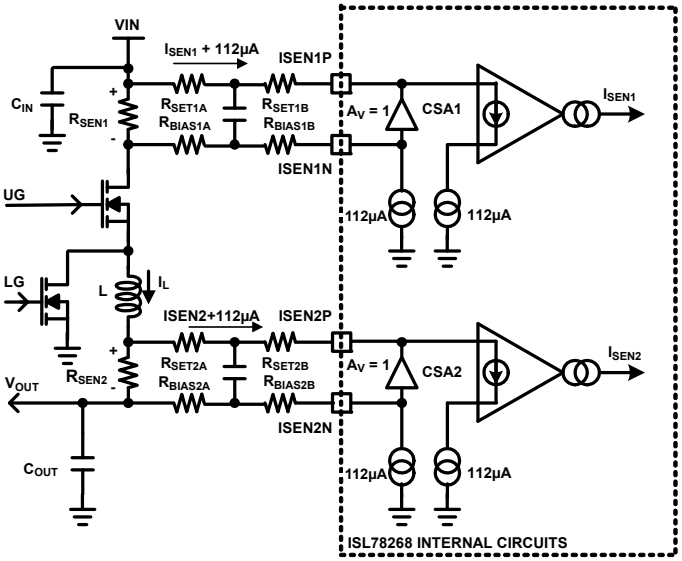


FIGURE 44. SENSE RESISTOR CURRENT SENSING

INDUCTOR DCR SENSING

An inductor has a distributed resistance as measured by the DCR (Direct Current Resistance) parameter.

The inductor DCR can be modeled as a lumped quantity, as shown in Figure 45, Equation 5 shows the S-domain equivalent voltage across the inductor V_L.

$$V_L = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 5)}$$

A simple R-C network across the inductor can extract the DCR voltage, as shown in Figure 45.

The voltage on the capacitor V_{CDCRS}, can be shown to be proportional to the channel current I_L, see Equation 6.

$$V_{CDCRS} = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{R_{DCRS} \times \left(\frac{1}{R_{SET}} + s \cdot C_{DCRS}\right) + 1} \quad \text{(EQ. 6)}$$

If the C_{DCRS} is selected so $2*\pi*f_{SW}*C_{DCRS}$ is much greater than $1/R_{SET}$, the $1/R_{SET}$ will be negligible. Also, if the R-C network components are selected such that the time constant ($R_{DCRS}*C_{DCRS}$) matches the inductor time constant (L/DCR), the voltage across the capacitor V_{CDCRS} is equal to the voltage drop across the DCR, i.e., proportional to the inductor current.

With the internal current sense amplifier, the capacitor voltage V_{CDCRS} is replicated across the sense resistor R_{SET2}. Therefore, the current flow into the ISEN2P pin is also proportional to the inductor current. Equation 7 shows the relation between sensed current I_{SEN2} and inductor current (I_L) when DCR sensing is used.

$$I_{SEN2} = I_L \cdot \frac{DCR}{R_{SET2}} \quad \text{(EQ. 7)}$$

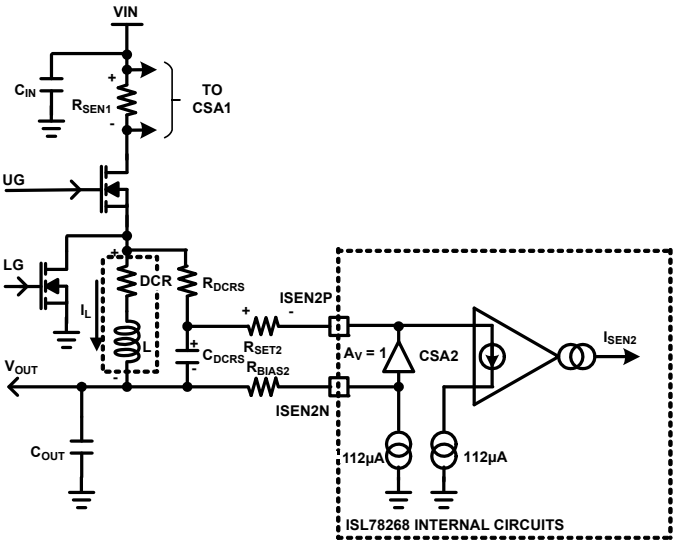


FIGURE 45. INDUCTOR DCR CURRENT SENSING

Adjustable Slope Compensation

A buck converter operating in peak current mode requires slope compensation when the duty cycle is larger than 50%. It is advisable to add slope compensation when the duty cycle is approximately 30% or more since a transient load step can push the duty cycle higher than the steady state level. When slope compensation is too low, the converter can suffer from subharmonic oscillation, which may result in noise emissions at half the switching frequency. On the other hand, overcompensation of the slope may reduce the phase margin. Therefore, proper design of the slope compensation is needed.

The ISL78268 features adjustable slope compensation by setting the resistor value R_{SLOPE} from the SLOPE pin to GND. Figure 46 shows the block diagram related to slope compensation.

For current mode control, in theory we need the compensation slope m_{SL} to be larger than 50% of the inductor current down ramp slope m_b.

Equation 8 shows the resistor value at SLOPE PIN to create a compensation ramp.

$$R_{SLOPE} = \frac{L \times 10^6 \times R_{SET}}{K \times V_{OUT} \times R_{SEN} \times 1.5} (\Omega) \quad \text{(EQ. 8)}$$

Where K is the selected gain of compensation slope over inductor down slope. For example, K = 1 gives the R_{SLOPE} value generating a compensation slope equal to inductor current down ramp slope. Theoretically, the K needs to be larger than 0.5 and in general, more than 1.0 is used in the actual application.

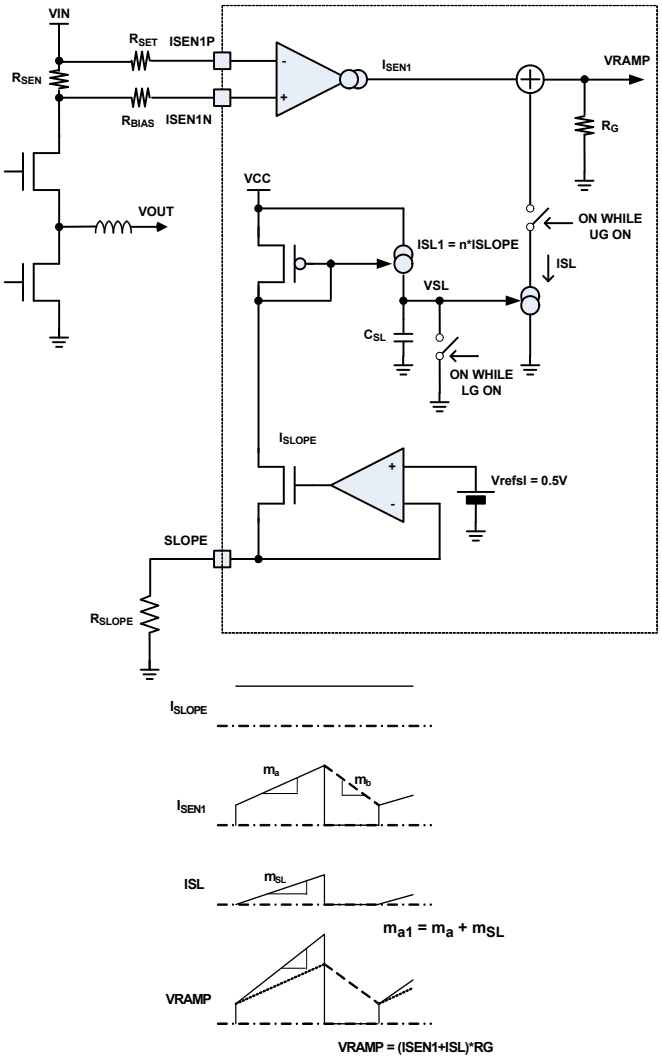


FIGURE 46. SLOPE COMPENSATION BLOCK

Light Load Efficiency Enhancement

For switching mode power supplies, the total loss is related to both the conduction loss and the switching loss. The conduction loss dominates at heavy load while the switching loss dominates at light load condition. The ISL78268 has the option to be set in cycle-by-cycle Diode Emulation mode and pulse skipping features to enhance the light load efficiency.

IMON/DE is used to select DE (Diode Emulation) mode. When the IMON/DE is connected to an external resistor or shorted to GND, the DE mode is selected. Also, if IMON/DE pin is pulled up to VCC level, the device operates in Forced PWM mode.

To achieve Diode Emulation mode, the current sense amplifier CSA2 is used to sense the output inductor current either by DCR sensing or an accurate current shunt resistor.

DIODE EMULATION AT LIGHT LOAD CONDITION

When DE mode is selected, if the inductor current reaches discontinuous conduction mode (DCM) operation, the ISL78268 controller will turn off the low-side MOSFET and enter into Diode Emulation mode.

By utilizing the cycle-by-cycle diode emulation scheme, negative current is prevented and the efficiency is improved from the smaller RMS current in the power stage.

While in soft-start period until the PGOOD pull-down is released, the low-side MOSFET is forced off (in either cases of DE mode or Forced PWM mode is selected).

PULSE SKIPPING AT DEEP LIGHT LOAD CONDITION

If the converter enters Diode Emulation mode and the load is further reduced, COMP voltage becomes lower than the minimum threshold and the device skips the pulses to increase the deep light load efficiency.

Average Constant Current Control

In normal PWM operation, the PWM pulse is terminated when the sensed peak current reaches the error amplifier control voltage. But some applications, such as charging a battery, may desire constant output current control instead of output voltage control. To support such requirements, ISL78268 provides the average constant current control loop to control the average current up to the FB regulated output voltage.

Average Constant Current control operates in the range of approximately 25% to 100% of targeted output voltage. This is due to the function described in the soft-start sequence (t_6-t_7) when the FB voltage (VFB) is below 0.4V and the device operates at 50kHz (typ) with minimum high-side MOSFET on time.

The IMON/DE pin serves to monitor the average current that is used for average constant current control and Average Overcurrent Protection (AVGOCP). The Current Sense Amplifier 2 (CSA2) output current, I_{SEN2}, which is representing the output current (see Figure 44 for R_{SEN} and R_{SET} positions) is sourcing out from this pin. Equation 9 describes the relation between output current (I_{OUT}) and IMON/DE pin current (I_{IMON}). An RC network should be connected between the IMON/DE pin and GND, such that the ripple current signal can be filtered out and converted to a voltage signal to represent the averaged output current. The time constant of the RC network should be on the order of 10 to 100 times slower than the voltage loop bandwidth so that the programmable current limit circuit does not interfere with the control loop stability. The IMON/DE pin voltage V_{IMON} can be calculated as Equation 10.

$$I_{IMON} = \left(I_{OUT} \cdot \frac{R_{SEN}}{R_{SET}} + 68 \times 10^{-6} \right) \cdot 0.125 \quad \text{(EQ. 9)}$$

$$V_{IMON} = I_{IMON} \cdot R_{IMON} \quad \text{(EQ. 10)}$$

When the IMON/DE pin voltage is at 1.6V (typ), the average constant output current control loop on the device limits the on time of high-side MOSFET to keep the output current constant. While the average constant output current control is working, the output voltage may become lower than preset output voltage because of the lowered duty cycle. Equation 11 shows the R_{IMON} for the desired average output current.

$$R_{IMON} = \frac{12.8}{I_{OUT} \cdot \frac{R_{SEN}}{R_{SET}} + 68 \times 10^{-6}} \quad \text{(EQ. 11)}$$

Fault Monitoring and Protection

The ISL78268 actively monitors input/output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to the load.

PGOOD SIGNAL

The Power-Good indicator pin (PGOOD pin) is provided for fault monitoring. The PGOOD pin is an open-drain logic output to indicate that the soft-start period is completed and the output voltage is within the specified range. An external pull-up resistor (10kΩ to 100kΩ) is required to be connected between PGOOD pin and VCC or external power supply (5.5V max). This pin is pulled low during soft-start. The PGOOD pin is released high after the voltage on SS pin reaches SS clamp voltage (3.4V typ) and after a 0.5ms (typ) delay. PGOOD will be pulled low with a 10µs (typ) blanking filter when output UV, or OV fault, or VIN OV fault occurs, or EN is pulled low. The PGOOD will be released high after the 0.5ms (typ) delay when the above faults are removed.

HICCUP/LATCH-OFF OPERATION

As a response to fault detection, either Hiccup or Latch-off mode can be selected by the configuration of the HIC/LATCH pin. When the HIC/LATCH pin is pulled high (VCC), the fault response will be Hiccup mode. When HIC/LATCH pin is pulled low (GND), the fault response will be in Latch-off mode.

In Hiccup mode, the device will stop switching when a fault condition is detected, and restart from soft-start after 500ms (typ). This operation will be repeated until fault conditions are completely removed.

In Latch-off mode, the device will stop switching when a fault condition is detected and be kept off even after fault conditions are removed. Either toggling the EN pin or cycling VIN below the POR threshold will restart the system.

INPUT OVERVOLTAGE PROTECTION

The ISL78268 features overvoltage (OV) fault protection for the input supply. When VIN is higher than 58V (typ), the UG and LG gate drivers are disabled and the PGOOD pin is pulled low. There is a 10µs (typ) transient filter to prevent noise spikes from triggering input OV. The input OV response can be selected as latch-off or hiccup.

The recovery from output overvoltage in hiccup or latch-off is the same as described in "Hiccup/Latch-off Operation". If the hiccup mode is selected, the input OV recovery threshold is below 55V (typ).

OUTPUT UNDERVOLTAGE DETECTION

The ISL78268 detects the output undervoltage condition. The output undervoltage threshold is set at 87.5% (typ) of the 1.6V FB reference voltage. When the FB voltage is below the undervoltage threshold for more than 10µs (typ), the PGOOD pin is pulled down. If the output voltage rises above the undervoltage recovery threshold of 90.5% (typ) of FB reference voltage, PGOOD is pulled up after 0.5ms (typ) delay. During an undervoltage condition, the device continues normal operation unless either OC2, AVGOCP, Input OVP, or thermal shutdown protection is triggered.

OUTPUT OVERVOLTAGE DETECTION/PROTECTION

The ISL78268 output overvoltage detection circuit is active after soft-start is completed. The output voltage is monitored at the FB pin and the output overvoltage trip point is set to 115% (typ) of the FB reference voltage. If the output overvoltage condition is longer than 10µs (typ) blanking time, the PGOOD pin is pulled down and the controller moves into hiccup or latch-off mode.

The recovery from output overvoltage in hiccup or latch-off is the same as described in "Hiccup/Latch-off Operation". If the hiccup mode is selected, the output OV recovery threshold is 112% (typ) of FB reference voltage.

CYCLE-BY-CYCLE PEAK OVERCURRENT LIMITING/PROTECTION

ISL78268 features cycle-by-cycle peak overcurrent protections by sensing the peak current at CSA1. The IC continuously compares the CSA1 output current (I_{SEN1} calculated from Equation 4), which is proportional to the current flowing at Current Sense Resistor1 (R_{SEN1}) with two overcurrent protection threshold, 70µA for OC1 and 93µA for OC2.

The OC1 and OC2 levels are defined as Equations 12 and 13.

$$I_{OC1} = 70 \times 10^{-6} \times \frac{R_{SET}}{R_{SEN}} \quad \text{(EQ. 12)}$$

$$I_{OC2} = 93 \times 10^{-6} \times \frac{R_{SET}}{R_{SEN}} \quad \text{(EQ. 13)}$$

If I_{SEN1} reaches OC1 threshold, the high-side MOSFET is turned off. This reduces the converter duty cycle which decreases the output voltage.

After OC1 protection has reduced the controller down to minimum duty cycle, if the output current increases to the OC2 threshold for three consecutive switching cycles, the controller disables the gate drivers and enters hiccup or latch-off mode.

The recovery from OC2 in hiccup or latch-off is the same as described in the "Hiccup/Latch-off Operation".

The OC1 cycle-by-cycle current limiting and OC2 protection are active during soft-start and normal operation period.

AVERAGE OVERCURRENT PROTECTION

When the average constant current control loop is active, the IC also provides average overcurrent protection.

When output current increases even the duty cycle becomes minimum by the average constant current control loop, the V_{IMON} voltage rises above 1.6V. If V_{IMON} reaches 2V (typ), the ISL78268 stops gate drivers and enters into the hiccup mode. This provides additional safety for the voltage regulator.

Equation 14 provides the R_{IMON} value for the desired average overcurrent protection level I_{OCPAVG}.

$$R_{IMON} = \frac{16}{I_{OCPAVG} \cdot \frac{R_{SEN}}{R_{SET}} + 68 \times 10^{-6}} \quad \text{(EQ. 14)}$$

The average overcurrent protection (2V REF at IMON/DE) will not be asserted until the soft-start period is completed.

NEGATIVE CURRENT LIMIT

When operating in Forced PWM mode operation in light load, the negative current from the output capacitor to GND flows by the turn on of the low-side MOSFET. The ISL78268 provides cycle-by-cycle negative current limit to prevent excess negative current. Equation 15 shows the peak negative current limit (I_{NEGLIM}) threshold.

$$I_{NEGLIM} = -50 \times 10^{-6} \times \frac{R_{SET}}{R_{SEN}} \quad \text{(EQ. 15)}$$

THERMAL PROTECTION

If the junction temperature reaches +160°C (typ), the ISL78268 switching will be disabled and enter into hiccup or latch-off mode. When hiccup mode is selected, a 15°C (typ) hysteresis insures that the device will not restart until the junction temperature drops below +145°C (typ) in Hiccup mode.

Internal 5.2V LDO

The ISL78268 has an internal LDO with input at VIN and a fixed 5.2V/100mA output at PVCC. A 4.7µF, 10V or higher X5R or X7R rated ceramic capacitor is recommended between PVCC to GND. The output of this LDO is mainly used as the bias supply of the internal circuitry. To provide a quiet power rail to the internal analog circuitry, it is recommended to place RC filter between PVCC and VCC. A 10Ω resistor between PVCC and VCC and at least 1µF ceramic capacitor from VCC to GND are recommended.

OUTPUT CURRENT LIMITATION OF INTERNAL LDO

The internal LDO tolerates an input supply range of VIN up to 55V (60V absolute maximum). However, the power losses at the LDO need to be considered, especially when the gate drivers are driving external MOSFETs with a large gate charge. At high V_{IN}, the LDO has significant power dissipation that may raise the junction temperature where the thermal shutdown occurs.

Figure 47 shows the relationship between maximum allowed LDO output current and input voltage. The curves are based on +39°C/W thermal resistance θ_{JA} of the package.

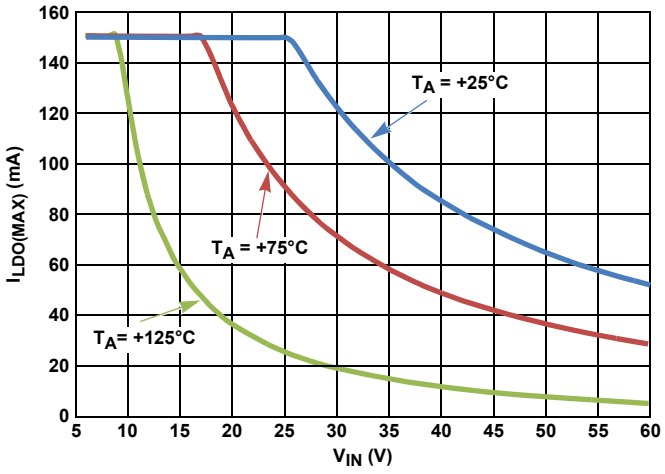


FIGURE 47. POWER DERATING CURVE

The maximum LDO current can be supplemented with an external PNP transistor as shown in Figure 48. The advantage is that the majority of the power dissipation can be moved from the ISL78268 to the external transistor. Choose R_S to be 68Ω so that the LDO delivers about 10mA when the external transistor begins to turn on. The external circuit increases the minimum input voltage to approximately 6.5V.

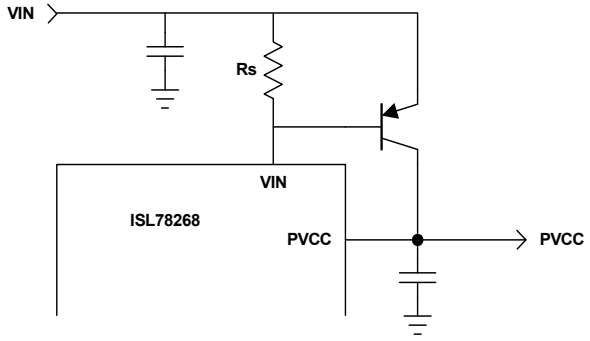


FIGURE 48. SUPPLEMENTING LDO CURRENT

Application Information

There are several ways to define the external components and parameters of buck regulators. This section shows one example of how to decide the parameters of the external components based on the typical application schematics shown in Figure 4 on page 8. In the actual application, the parameters may need to be adjusted and also a few more additional components may need to be added for the application specific noise, physical sizes, thermal, testing and/or other requirements.

Output Voltage Setting

The output voltage (V_{OUT}) of the regulator can be programmed by an external resistor divider set from V_{OUT} to FB and FB to GND. V_{OUT} can be defined as:

$$V_{out} = 1.6 \times \left(1 + \frac{R_{FB1}}{R_{FB0}}\right) \quad \text{(EQ. 16)}$$

In the actual application, the resistor value should be decided by considering the quiescent current requirement and loop response. Typically, between 10kΩ to 30kΩ will be used for the RFB0.

Switching Frequency

Switching frequency may be determined by considering several requirements such as system level response time, solution size, EMC/EMI limitation, power dissipation and efficiency, ripple noise level, minimum and maximum input voltage range, etc. Higher frequency may improve the transient response and help to minimize the solution size. However, this may increase the switching losses and EMC/EMI concerns. Thus, a balance of these parameters are needed when deciding the switching frequency.

Once the switching frequency is decided, the frequency setting resistor (R_{SYNC}) can be determined by Equation 1.

Output Inductor Selection

While the Buck Converter is operating in stable continuous conduction mode (CCM), the output voltage and on-time of the high-side transistor is determined by Equation 17:

$$V_{OUT} = VIN \cdot \frac{t_{ON}}{T} = VIN \cdot D \quad \text{(EQ. 17)}$$

Where T is the switching cycle ($1/f_{SW}$) and $D = t_{ON}/T$ is the on-duty of the high-side transistor.

Under this CCM condition, the inductor ripple current can be defined as Equation 18:

$$I_{L(P\text{-}P)} = t_{ON} \cdot \frac{VIN - V_{OUT}}{L} = t_{OFF} \cdot \frac{V_{OUT}}{L} \quad \text{(EQ. 18)}$$

From the previous equations, the inductor value will be determined as Equation 19:

$$L = \frac{VIN - V_{OUT}}{f_{SW}} \cdot \frac{V_{OUT}}{VIN} \quad \text{(EQ. 19)}$$

In general, once the inductor value is determined, the ripple current varies by the input voltage. At the maximum input voltage, the on-duty becomes minimum and the ripple current becomes maximum. So, the minimum inductor value can be estimated from Equation 20.

$$L_{min} = \frac{VIN_{max} - V_{out}}{f_{SW} \cdot \Delta IL_{max}} \cdot \frac{V_{OUT}}{VIN_{max}} \quad \text{(EQ. 20)}$$

In DC/DC converter design, this ripple current will be set around 20% to 50% of maximum DC output current. A reasonable starting point to adjust the inductor value will be around 30% of the maximum DC output current.

Increasing the value of inductor reduces the ripple current and thus ripple voltage. However, the large inductance value may reduce the converter's response time to a load transient. Also, this reduces the ramp signal and may cause a noise sensitivity issue.

Under stable operation, the peak current flow in the inductor will be the sum of output current and 1/2 of ripple current.

$$I_L = \frac{I_{L(P\text{-}P)}}{2} \cdot I_{OUT} \quad \text{(EQ. 21)}$$

This peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current may be observed at the start-up or heavy load transient. Therefore, the inductor's size needs to be determined with the consideration of these conditions. In addition, to avoid exceeding the inductor's saturation rating, it is recommended to set the OCP trip point between the maximum peak current and the inductor's saturation current rating.

Output Capacitor

To filter the inductor current ripples and to have sufficient transient response, an output capacitor is required.

The current mode control loop allows the usage of lower ESR ceramic capacitors and thus enables smaller board layout. Electrolytic and polymer capacitors may also be used.

However, additional consideration may be needed to use the ceramic capacitors. While the ceramic capacitor offers excellent overall performance and reliability, the actual capacitance may be considerably lower than the advertised value if used DC biased condition. The effective capacitance can be easily 50% lower than that of the rated value.

The following are equations for the required capacitance value to meet the desired ripple voltage level. Additional capacitance may be used to lower the ripple voltage and to improve transient response.

For the ceramic capacitor (low ESR):

$$V_{OUTripple} = \frac{\Delta I_L}{8 \cdot f_{SW} \cdot C_{OUT}} \quad \text{(EQ. 22)}$$

Where ΔI_L is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency and C_{OUT} is the output capacitor.

Required minimum output capacitance based on ripple current will be:

$$C_{OUTmin} = \frac{\Delta I_L}{8 \cdot f_{SW} \cdot V_{OUTmin}} \quad \text{(EQ. 23)}$$

If using electrolytic capacitors, the ESR will be the dominant portion of the ripple voltage.

$$V_{OUTripple} = \Delta I_L \cdot ESR \quad \text{(EQ. 24)}$$

So, to reduce the ripple voltage, reduce the ripple current with increasing the inductor value or use multiple capacitors in parallel to reduce the ESR.

The other factor which may affect the selection of the output capacitor will be the transient response. To estimate the capacitance value related to transient response, a good starting point is to determine the allowable overshoot in V_{OUT} if the load is suddenly reduced. In this case, energy stored in the inductor will be transferred to C_{OUT} and causing its voltage rise. Equation 25 determines the required output capacitor value in order to achieve a desired overshoot level relative to the regulated voltage.

$$C_{OUTtran} = \frac{I_{OUT}^2 \cdot L}{V_{OUT}^2 \cdot \left(\left(\frac{V_{OUTmax}}{Vout}\right)^2 - 1\right)} \quad \text{(EQ. 25)}$$

Where V_{OUTmax}/V_{OUT} is the relative maximum overshoot allowed during the removal of the load.

After calculating the required capacitance for both ripple and transient needs, choose the larger of the calculated values as the output capacitance. To keep enough capacitance over the biased voltage and temperature range, a good quality capacitor such as X7R or X5R is recommended.

Input Capacitor

Depending upon the system input power rail conditions, the aluminum electrolytic type capacitor is normally used to provide the stable input voltage and restrict the switching frequency pulse current in small areas over the input trace for better EMC performance. The input capacitor should be able to handle the RMS current from the switching power devices.

Ceramic capacitors must be used at the VIN pin of the IC and multiple ceramic capacitors including 1µF and 0.1µF are recommended.

Place these capacitors as close as possible to the IC.

Power MOSFET

The external MOSFETs that are driven by the ISL78268 controller need to be carefully selected to optimize the design of the synchronous buck regulator.

Since the ISL78268 input voltage can be up to 55V, the MOSFET's BVdss rating needs to have enough voltage margin against input voltage tolerance and PH node voltage transient during switching.

As the UG and LG gate drivers are 5V output, the MOSFET VGS need to be in this range.

The MOSFET should have low Total Gate Charge (Q_{gd}), low ON-resistance ($r_{DS(ON)}$) at VGS = 4.5V (less than 10mΩ is recommended) and small gate resistance (R_g <1.5Ω is recommended). It is recommended that the minimum VGS threshold should be higher than 1.2V but not exceeding 2.5V. This is because of the consideration of large gate pull-down current associated by gate-drain current at low side transistor due to the high speed transition of Phase node and limitation of maximum gate drive voltage, which is 5.2V (typ) for low-side MOSFET and lower than 4.5V (typ) due to diode drop of boot diode for high-side MOSFET.

Bootstrap Capacitor

The power required for high-side MOSFET drive is provided by the boot capacitor connected between BOOT and PH pins. The bootstrap capacitor can be chosen using Equation 26:

$$C_{BOOT} > \frac{Q_{gate}}{dV_{BOOT}} \quad \text{(EQ. 26)}$$

Where Q_{gate} is the total gate charge of the high-side MOSFET and dV_{BOOT} is the maximum droop voltage across the bootstrap capacitor while turning on the high-side MOSFET.

Though the maximum charging voltage across the bootstrap capacitor is PVCC minus the bootstrap diode drop (~4.5V), large excursions below GND by PH node requires at least 10V rating for this ceramic capacitor. To keep enough capacitance over the biased voltage and temperature range, a good quality capacitor such as X7R or X5R is recommended.

RESISTOR ON BOOTSTRAP CIRCUIT

In the actual application, sometimes a large ringing noise at the PH node and the boot node are observed. This noise is caused by energy stored in the body diode of the low-side MOSFET when it is turning off, parasitic PH node capacitance due to PCB routing, and the parasitic inductance. To reduce this noise, a resistor can be added between the BOOT pin and the bootstrap capacitor. A large resistor value will reduce the ringing noise at PH node but limits the charging of the bootstrap capacitor during the low-side MOSFET on-time, especially when the controller is operating at very high duty cycle.

Typically, up to 10Ω resistor is used for this purpose.

Loop Compensation Design

The ISL78268 uses constant frequency peak current mode control architecture with a Gm amp as the error amplifier. An external current sense resistor is required for the peak current sensing and overcurrent protection. Figures 49 and 50 show the conceptual schematics and control block diagram, respectively.

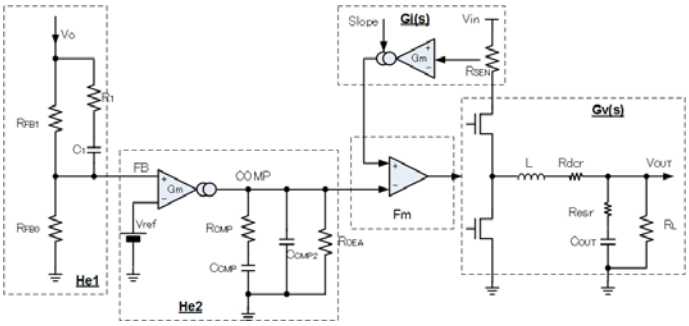


FIGURE 49. CONCEPTUAL BLOCK DIAGRAM OF PEAK CURRENT MODE CONTROLLED BUCK REGULATOR

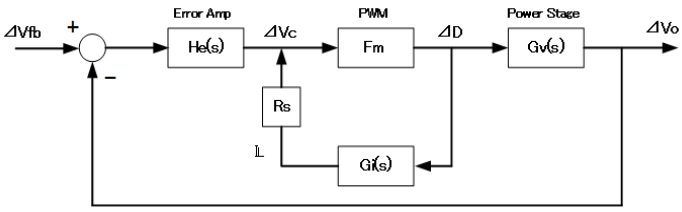


FIGURE 50. CONCEPTUAL CONTROL BLOCK DIAGRAM

The output stage consists of a power stage ($G_V(s)$) which converts the duty signal to output voltage and internal current loop stage which converts duty to sense current.

POWER STAGE TRANSFER FUNCTIONS

Transfer function at power stage ($G_V(s)$) can be expressed as Equation 27.

$$G_V(s) = VIN \cdot \left(1 + \frac{s}{\omega_{esr}}\right) \cdot \frac{1}{1 + \frac{s}{Q_p \cdot \omega_n} + \left(\frac{s}{\omega_n}\right)^2} \quad \text{(EQ. 27)}$$

Where,

$$\omega_{esr} = \frac{1}{C_{OUT} \cdot R_{esr}}$$

$$Q_p \approx R_{OUT} \cdot \sqrt{\frac{C_{OUT}}{L}}$$

$$\omega_n = \frac{1}{\sqrt{L \cdot C_{OUT}}}$$

INTERNAL CURRENT LOOP TRANSFER FUNCTIONS

Transfer function from control to inductor current ($G_i(s)$) is given by Equation 28.

$$G_i(S) = \frac{VIN}{R_{OUT}} \cdot \left(1 + \frac{s}{\omega_o}\right) \cdot \frac{1}{1 + \frac{s}{Q_p \times \omega_n} + \left(\frac{s}{\omega_n}\right)^2} \quad \text{(EQ. 28)}$$

Where,

$$\omega_o = \frac{1}{C_{OUT} \cdot R_{OUT}}$$

$$Q_p \approx R_{OUT} \cdot \sqrt{\frac{C_{OUT}}{L}}$$

$$\omega_n = \frac{1}{\sqrt{L \cdot C_{OUT}}}$$

PWM COMPARATOR GAIN Fm

The PWM comparator gain Fm for peak current mode control is given by Equation 29.

$$Fm = \frac{D}{V_{ramp}} = \frac{1}{(m_a + m_{SL}) \cdot T} \quad \text{(EQ. 29)}$$

Where m_{SL} is the slew rate of the slope compensation and m_a is the inductor current slew rate while high-side MOSFET is on and given as Equation 30.

$$I_a = R_S \cdot \frac{VIN - V_{OUT}}{L} \quad \text{(EQ. 30)}$$

Where R_S is the gain of the current sense amplifier.

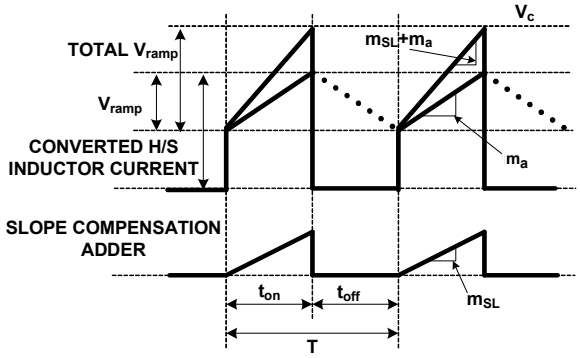


FIGURE 51. CONVERTED SENSE CURRENT WAVEFORM

TOTAL TRANSFER FUNCTION FROM PWM COMPARATOR TO POWER STAGE

The total transfer function from PWM to power stage including internal current sense loop is expressed as Equation 31 (assuming $F_m * G_i(s) * R_S >> 1$).

$$G_{T(s)} = \frac{F_m}{1 + F_m \cdot G_i(s) \cdot R_s} \cdot G_v(s) \approx \left(\frac{R_{out}}{R_s} \cdot \frac{1 + \frac{s}{\omega_{esr}}}{1 + \frac{s}{\omega_o}}\right) \quad \text{(EQ. 31)}$$

Equation 31 shows that the system is a single order system. Therefore, a simple Type-2 compensator can be used to stabilize the system. In the actual application, however, an extra phase margin will be provided by a Type-3 compensator.

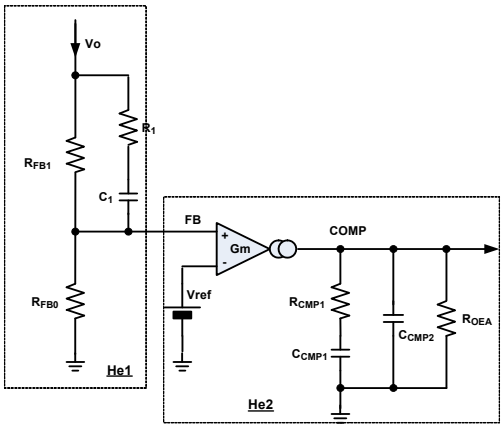


FIGURE 52. TYPE-3 COMPENSATOR

COMPENSATOR DESIGN

The transfer function at error amplifier and its compensation network will be expressed as Equation 32.

$$H_{e2}(s) = \frac{V_{COMP}}{V_{FB}} = g_m \cdot Z_{COMP} = \quad \text{(EQ. 32)}$$

$$g_m \frac{(1 + sR_{CMP}C_{CMP1})R_{OEA}}{1 + s[R_{CMP}C_{CMP1} + R_{EOA}(C_{CMP1} + C_{CMP2})] + C_{CMc2}C_{CMP1}R_{CMP}R_{OUT}s^2}$$

If $R_{OEA} >> R_{CMP}$, $C_{CMP1} >> C_{CMP2}$, and R_{OEA} = infinite, the equation can be simplified as shown in Equation 33:

$$H_{e2}(s) = g_m \cdot \frac{1 + s \cdot R_{CMP} \cdot C_{CMP1}}{s \cdot C_{CMP1} \cdot (1 + s \cdot R_{CMP} \cdot C_{CMP2})} = \frac{\omega_1}{s} \cdot \frac{1 + \frac{s}{\omega_{z2}}}{1 + \frac{s}{\omega_{p2}}} \quad \text{(EQ. 33)}$$

Where,

$$\omega_1 = \frac{g_m}{C_{CMP1}}$$

$$\omega_{z2} = \frac{1}{R_{CMP} \cdot C_{CMP1}}$$

$$\omega_{p2} = \frac{1}{R_{CMP} \cdot C_{CMP2}}$$

The transfer function at the feedback resistor network is:

$$H_{e1}(S) = \frac{R_{FB0}}{R_{FB0}+R_{FB1}} \cdot \frac{1+\frac{s}{\omega_{z1}}}{1+\frac{s}{\omega_{p1}}} \quad \text{(EQ. 34)}$$

Where,

$$\omega_{z1} = \frac{1}{C_1 \cdot (R_{FB1}+R_1)}$$

$$\omega_{p1} = \frac{1}{C_1 \cdot \frac{R_{FB1} \cdot R_{FB0} + R_{FB1} \cdot R_1 + R_{FB0} \cdot R_1}{R_{FB1}+R_{FB0}}}$$

The total transfer function with compensation network and gain stage will be expressed;

$$G_{open}(s) = G_T(s) \cdot H_{e1}(s) \cdot H_{e2}(s) \quad \text{(EQ. 35)}$$

$$G_{open}(s) = \left(\frac{R_o}{R_s} \cdot \frac{1+\frac{s}{\omega_{esr}}}{1+\frac{s}{\omega_o}}\right) \cdot \left(\frac{R_{FB0}}{R_{FB0}+R_{FB1}} \cdot \frac{1+\frac{s}{\omega_{z1}}}{1+\frac{s}{\omega_{p1}}}\right) \cdot \left(\frac{\omega_1}{s} \cdot \frac{1+\frac{s}{\omega_{z2}}}{1+\frac{s}{\omega_{p2}}}\right) \quad \text{(EQ. 36)}$$

From Equation 36, desired pole and zero locations can be determined as in Equations 37 through 42.

$$f_{po} = \frac{\omega_o}{2 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot R_{OUT}} \quad \text{(EQ. 37)}$$

$$f_{z1} = \frac{\omega_{z1}}{2 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot C_1 \cdot (R_{FB1}+R_1)} \quad \text{(EQ. 38)}$$

$$f_{z2} = \frac{\omega_{z2}}{2 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot C_{CMc1} \cdot R_{CMP}} \quad \text{(EQ. 39)}$$

$$f_{p1} = \frac{\omega_{p1}}{2 \cdot \pi} = \frac{R_{FB1}+R_{FB2}}{2\pi C_1 (R_{FB1} \cdot R_{FB0} + R_{FB1} \cdot R_1 + R_{FB0} \cdot R_1)} \quad \text{(EQ. 40)}$$

$$f_{p2} = \frac{\omega_{p2}}{2 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot C_{CMP2} \cdot R_{CMP}} \quad \text{(EQ. 41)}$$

$$f_{zesr} = \frac{\omega_{esr}}{2 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot R_{esr}} \quad \text{(EQ. 42)}$$

In general, set f_{z2} and f_{z1} close to the f_{po}. Set f_{p2} near the desired bandwidth. Set f_{p1} close to f_{zesr}.

VCC Input Filter

To provide a quiet power rail to the internal analog circuitry, it is recommended to place RC filter between PVCC and VCC. A 10Ω resistor between PVCC and VCC and at least 1µF ceramic capacitor from VCC to GND are recommended.

Current Sense Circuit

To set the current sense resistor, the voltage across the current sense resistor should be limited to less than 0.3V. In a typical application, it is recommended to set the voltage across the current sense resistor between 30mV to 100mV for the typical load current condition.

Layout Consideration

For DC/DC converter design, the PCB layout is a very important to ensure the desired performance.

1. Place the input ceramic capacitor as close as possible to the VIN pin and power ground connecting to the power MOSFET. Keep this loop (input ceramic capacitor, IC VIN pin and MOSFET) as small as possible to reduce voltage spikes induced by the trace parasitics.
2. Place the input aluminum capacitor close to IC VIN and ceramic capacitors.
3. Keep the phase node copper area small but large enough to handle the load current.
4. Place the output ceramic and aluminum capacitors as close as possible to the power stage components.
5. Place multiple vias under the thermal pad of the IC. The thermal pad should be connected to the ground copper plane with as large an area as possible in multiple layers to effectively reduce the thermal impedance.
6. Place the 4.7µF decoupling ceramic capacitor at the VCC pin and as close as possible to the IC. Put multiple vias close to the ground pad of this capacitor.
7. Keep the bootstrap capacitor as close as possible to the IC.
8. Keep the driver traces as short as possible and try to avoid using a via in the driver path to achieve the lowest impedance.
9. Place the current sense resistor as close as possible to the IC. Keep the traces of current sense lines symmetric to each other to avoid undesired switching noise injections.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
December 12, 2014	FN8657.3	Functional Pin Description Page 3, FSYNC description. Changed from: There is a 100ns delay from the FSYNC pin's.... To: There is a 325ns delay from the FSYNC pin's.... Page 4, PVCC description. Changed from: The PVCC operating range is 4V to 5.4V. To: The PVCC operating range is 4.75V to 5.5V. VCC description. Changed from: range of 4.7V to 5.5V, To: range of 4.75V to 5.5V, Typical Application Schematics Page 7, Left side changed from: HIC/LATCH:Connect to either Vcc for Latch-off mode or GND for Hiccup mode To: HIC/LATCH:Connect to either Vcc for Hiccup mode or GND for Latch-off mode Page 8, Left side changed from: HIC/LATCH:Connect to either Vcc for Latch-off mode or GND for Hiccup mode To: HIC/LATCH:Connect to either Vcc for Hiccup mode or GND for Latch-off mode Page 9, Left side changed from: HIC/LATCH:Connect to either Vcc for Latch-off mode or GND for Hiccup mode To: HIC/LATCH: Connect to either Vcc for Hiccup mode or GND for Latch-off mode Page 10, Electrical specification table, Test condition of Input Voltage range, changed from "For VIN = 5 the internal ... " to "For VIN = 5V, the internal ..." Elecrical Spec table, Page 11, Phase Lock Loop Locking Time Changed in Test Conditions: Cpllcmp2=_nF to: Cpllcmp2=1nF Page 20, Operation Description, 2nd sentence changed from: "such as input and output overvoltage protection, output overvoltage protection" to: "input overvoltage protection, output overvoltage protection" Page 22, SYNCHRONIZATION WITH EXTERNAL CLOCK, 2nd paragaph Changed from : The delay time of UG rising from the external clock rising edge is 100ns (typ). To: The delay time of UG rising from the external clock rising edge is 325ns (typ). Page 25, Figure 46 changed: "ma1 = Ma + mSL" to: "ma1 = ma + mSL" Page 30, EQ. 30 changed : mn=RS*..... to: ma=RS*..... Figure 51 changed: mb to: ma
August 1, 2014	FN8657.2	On page 1 in the Features section, updated the 5th bullet from “Low shutdown current, IQ<3µA” to “Low shutdown current, IQ<1µA”. In the “Block Diagram” on page 6, reversed the “+” and “-” Gm_Amp input polarity.
July 22, 2014	FN8657.1	Added Related Literature section on page 1 and ISL78268EVAL1Z information to the ordering information table on page 5
June 18, 2014	FN8657.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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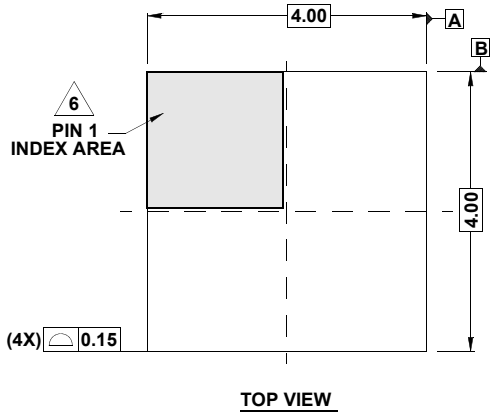
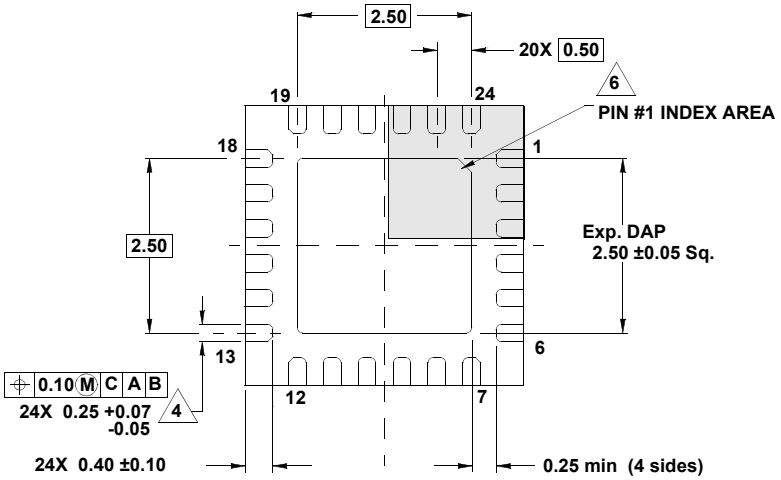
Package Outline Drawing

L24.4x4H

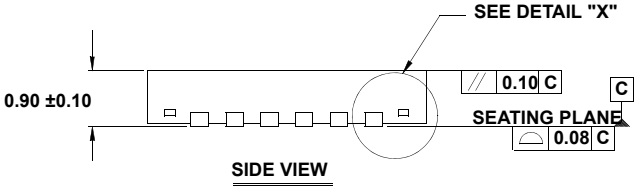
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 09/11



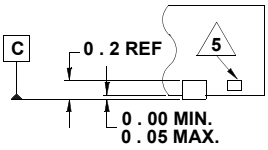
TOP VIEW



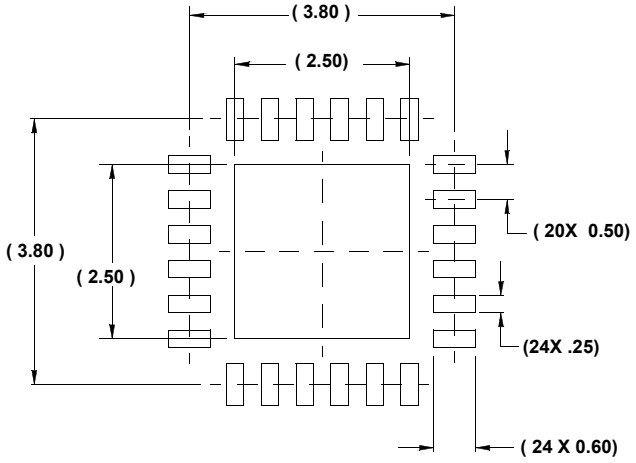
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-220 VGGD-8

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