THE DATASHEET OF

ISL8126IRZ-T

ISL8126

Dual/n-Phase Buck PWM Controller with Integrated Drivers

FN7892
Rev.2.00
January 29, 2015

The ISL8126 integrates two voltage-mode PWM leading-edge modulation control with input feed-forward synchronous buck PWM controllers to control dual independent voltage regulators or a 2-phase single output regulator. It also integrates current sharing control for the power module to operate in parallel, which offers high system flexibility.

The ISL8126 integrates an internal linear regulator, which generates IC's bias voltages for applications with only one single supply rail. The internal oscillator is adjustable from 150kHz to 1.5MHz, and is able to synchronize to an external clock signal for frequency synchronization and phase paralleling applications. Its PLL circuit can output a phase-shift-programmable clock signal for the system to be expanded to 3-, 4-, 6- and 12- phases with desired interleaving phase shift.

The ISL8126's Fault Spreading feature protects any channel from overloading/stressing due to system faults or phase failure. The undervoltage fault protection features are also designed to prevent a negative transient on the output voltage during falling down. This eliminates the Schottky diode that is used in some systems for protecting the load device from reversed output voltage damage.

Features

- Wide V_{IN} range operation: 3V to 26.5V
  - VCC operation from 3V to 5.60V
- Excellent output voltage regulation: 0.6V internal reference
- Frequency synchronization with programmable phase delay up to 12-phase applications
- Fault spreading capability for high system reliability
- Digital soft-start with precharged output start-up capability
- Dual independent channel enable inputs with precision voltage monitor and voltage feed-forward capability
  - Programmable input voltage POR and its hysteresis with a resistor divider at EN input
- Extensive circuit protection functions: output overvoltage, undervoltage, overcurrent protection, over-temperature and pre-power-on-reset overvoltage protection option

Applications

- Power supply for Datacom/Telecom and POL
- Paralleling power module
- Wide and narrow input voltage range buck regulators

Related Literature

- TB389 "PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages"
- AN1713, "ISL8126EVAL1Z Evaluation Board User Guide"

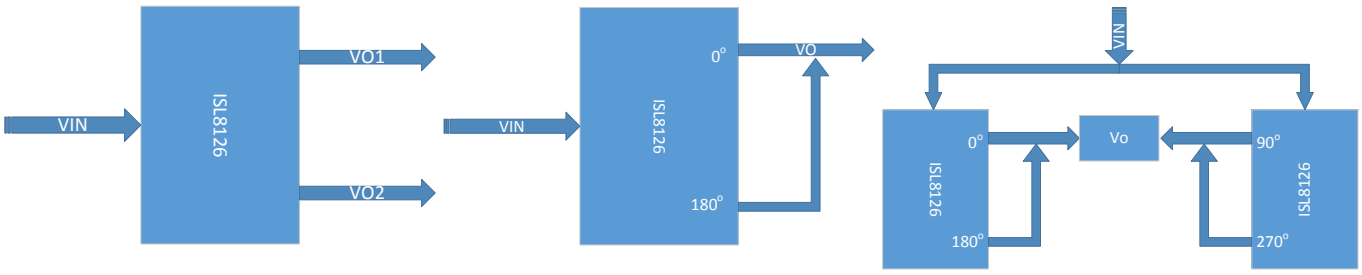

FIGURE 1. TYPICAL APPLICATION DIAGRAM

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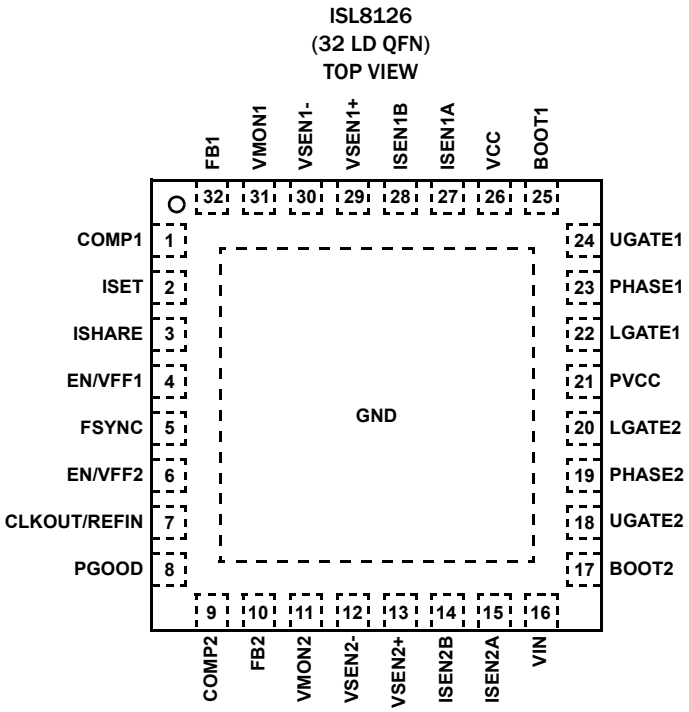
Pin Configuration



Functional Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 9	COMP1, COMP2	These pins are the error amplifier outputs. They should be connected to FB1, FB2 pins through desired compensation networks when both channels are operating independently. When VSEN1-, VSEN2- are pulled within 400mV of VCC, the corresponding error amplifier is disabled and its output (COMP pin) is high impedance. Thus, in multiphase operations, all other SLAVE phases' COMP pins can tie to the MASTER phase's COMP1 pin (1st phase), which modulates each phase's PWM pulse with a single voltage feedback loop. While the error amplifier is not disabled, an independent compensation network is required for each cascaded IC.
2	ISET	This pin along with ISHARE pin are used for multiple ISL8126 current sharing purposes. When in 2-phase mode (VSEN2- pulled within 400mV of VCC), this pin sources a current which is a combination of 15µA constant offset current, current correction current (more details on "Current Share Control in Multiphase Single Output with Shared COMP Voltage" on page 31), and the average of both sensed channel currents. When in Dual-output mode, this pin sources a current, which is a combination of 15µA constant offset current, current correction current and Channel 1's sensed current. The current sourced out from this pin and an external resistor (RISET) set the voltage at this pin (VISET). The RISET is recommended to be 10kΩ. A noise decoupling capacitor less than 100pF can be added in parallel with the 10kΩ RISET. In the single IC configuration (both 2-phase mode and dual-output mode), this pin can be tied to the ISHARE pin.
3	ISHARE	This pin is used for current sharing purposes and is configured to the current share bus representing all modules' average current. When in 2-phase mode (VSEN2- pulled within 400mV of VCC), this pin sources a current, which is a combination of 15µA constant offset current and the average of both sensed channel currents. When in Dual-output mode, this pin sources a current, which is a combination of 15µA constant offset current and Channel 1's sensed current. The share bus (ISHARE pins connected together) voltage (VISHARE) set by an external resistor (RISHARE) represents the average current level of all ISL8126 controller connected to the current share bus. The share bus impedance RISHARE should be set as RISET/NCTRL (RISET divided by number of ISL8126 in current sharing controllers). There is a 1.2V threshold for average overcurrent protection on this pin. VISHARE is compared with a 1.2V threshold for average overcurrent protections. When the fault condition on Channel 1 is detected or EN/VFF1 is pulled below its POR, ISHARE is internally pulled to VCC.

Functional Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
4, 6	EN/VFF1, EN/VFF2	These pins have triple functions. The voltage on EN/VFF_ pin is compared with a precision 0.8V threshold for system enable to initiate soft-start. With a voltage lower than the threshold, the corresponding channel can be disabled independently. By connecting these pins to the input rail through a voltage resistor divider, the input voltage can be monitored for UVLO (undervoltage lockout) function. The undervoltage lockout and its hysteresis levels can be programmed by these resistor dividers. The voltages on these pins are also fed into the controller to adjust the sawtooth amplitude of each channel independently to realize the feed-forward function. Furthermore, during fault (such as overvoltage, overcurrent, and over-temperature) conditions, these pins (EN/VFF_) are pulled low to communicate the information to other cascaded ICs.
5	FSYNC	The oscillator switching frequency is adjusted by placing a resistor (RFS) from this pin to GND. The internal oscillator will lock to an external frequency source if this pin is connected to a switching square pulse waveform, typically the CLKOUT signal from another ISL8126 or an external clock. The internal oscillator synchronizes with the leading edge of the input signal.
7	CLKOUT/REFIN	This pin has a dual function depending on the mode in which the chip is operating. It provides a clock signal to synchronize with other ISL8126(s) with its VSEN2- pulled within 400mV of VCC for multiphase (3-, 4-, 6-, 8-, 10-, or 12-phase) operation. When the VSEN2- pin is not within 400mV of VCC, ISL8126 is in dual mode (dual independent PWM output). The clockout signal of this pin is not available in this mode, but the ISL8126 can be synchronized to external clock. In dual mode, this pin works as the following two functions: 1. An external reference (0.6V target only) can be in place of the Channel 2's internal reference through this pin for DDR/tracking applications. 2. The ISL8126 operates as a dual-PWM controller for two independent regulators with selectable phase degree shift, which is programmed by the voltage level on REFIN (see "DDR and Dual Mode Operation" on page 36).
8	PGOOD	Provides an open drain Power-Good signal when both channels are within 9% of the nominal output regulation point with 4% hysteresis (13%/9%) and soft-start complete. PGOOD monitors the outputs (VMON1/2) of the internal differential amplifiers.
32, 10	FB1, FB2	These pins are the inverting inputs of the error amplifiers. These pins should be connected to VMON1, VMON2 with the compensation feedback network. No direct connection between FB and VMON pins is allowed. With VSEN2- pulled within 400mV of VCC, the corresponding error amplifier is disabled and the amplifier's output is high impedance. FB2 is one of the two pins to determine the relative phase relationship between the internal clock of both channels and the CLKOUT signal. See Table 1 on page 23.
31, 11	VMON1, VMON2	These pins are outputs of the differential amplifiers. They are connected internally to the OV/UV/PGOOD comparators. These pins should be connected to the FB1, FB2 pins by a standard feedback network when both channels are operating independently. When VSEN1-, VSEN2- are pulled within 400mV of VCC, the corresponding differential amplifier is disabled and its output (VMON pin) is high impedance. In such an event, the VMON pins can be used as additional monitors of the output voltage with a resistor divider to protect the system against single point of failure, which occurs in the system using the same resistor divider for both of the UV/OV comparator and output voltage feedback.
30, 12	VSEN1-, VSEN2-	These pins are the negative inputs of standard unity gain operational amplifier for differential remote sense for the corresponding regulator (Channels 1 and 2), and should be connected to the negative rail of the load. When VSEN1-, VSEN2- are pulled within 400mV of VCC, the corresponding error amplifier and differential amplifier are disabled and their outputs are high impedance. Both VSEN2+ and FB2 input signal levels determine the relative phases between the internal controllers as well as the CLKOUT signal (see Table 1 on page 23). When configured as multiple power modules (each module with independent voltage loop) operating in parallel, in order to implement the current sharing control, a resistor needs to be inserted between the VSEN1- pin and the output voltage negative sense point (between VSEN1- and lower voltage sense resistor), as shown in the "Typical Application Circuits" "Multiple Power Modules in Parallel with Current Sharing Control" on page 14. This introduces a correction voltage for the modules with lower load current to keep the current distribution balanced among modules. The module with the highest load current will automatically become the master module. The recommended value for the VSEN1- resistor is 100Ω and it should not be large in order to keep the unit gain amplifier input impedance compatibility. A capacitor is also recommended to place in parallel with the 100Ω.

Functional Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
29, 13	VSEN1+, VSEN2+	These pins are the positive inputs of the standard unity gain operational amplifier for differential remote sense for the corresponding channel (Channels 1 and 2), and should be connected to the positive rail of the load. These pins can also provide precision output voltage trimming capability by pulling a resistor from this pin to the positive rail of the load (trimming down) or the return (typical VSEN1-, VSEN2- pins) of the load (trimming up). By setting the resistor divider connected from the output voltage to the input of the differential amplifier, the desired output voltage can be programmed. To minimize the system accuracy error introduced by the input impedance of the differential amplifier, a resistor below 1kΩ is recommended to be used for the lower leg (ROS) of the feedback resistor divider. The typical input impedance of VSEN+ with respect to VSEN- is 500kΩ. With VSEN2- pulled within 400mV of VCC, the corresponding error amplifier is disabled and VSEN2+ is one of the two pins to determine the relative phase relationship between the internal clock of both channels and the CLKOUT signal. See Table 1 on page 23 for details.
28, 14	ISEN1B, ISEN2B	These pins are the inverting (-) inputs of the current sensing amplifiers to provide $r_{DS(ON)}$, DCR, or precision resistor current sensing together with the ISEN1A, ISEN2A pins. Refer to "2-Phase Operation with rDS(ON) Sensing" on page 9 for $r_{DS(ON)}$ sensing set up and "2-Phase Operation with DCR Sensing" on page 8 for DCR sensing set up.
27, 15	ISEN1A, ISEN2A	These pins are the non-inverting (+) inputs of the current sensing amplifiers to provide $r_{DS(ON)}$, DCR, or precision resistor current sensing together with the ISEN1B, ISEN2B pins.
16	VIN	This pin is the input of the internal linear regulator. It should be tied directly to the input rail. The internal linear device is protected against reverse bias generated by the remaining charge of the decoupling capacitor at PVCC when losing the input rail. When used with an external 3.3V to 5V supply, this pin can be tied directly to PVCC to bypass the internal LDO.
25, 17	BOOT1, BOOT2	These pins provide the bootstrap biases for the high-side drivers. Internal bootstrap diodes connected to the PVCC pin provide the necessary bootstrap charge. Its typical operational voltage range is 2.5V to 5.6V.
24, 18	UGATE1, UGATE2	These pins provide the gate signals to drive the high-side devices and should be connected to the MOSFETs' gates.
23, 19	PHASE1, PHASE2	Connect these pins to the source of the high-side MOSFETs and the drain of the low-side MOSFETs. These pins represent the return path for the high-side gate drives.
22, 20	LGATE1, LGATE2	These pins provide the drive for the low-side devices and should be connected to the MOSFETs' gates.
21	PVCC	This pin is the output of the internal series linear regulator. It provides the bias for both low-side and high-side drives. Its operational voltage range is 3V to 5.6V. A 10µF ceramic capacitor is required for decoupling PVCC to ground.
26	VCC	This pin provides bias power for the analog circuitry. An RC filter is recommended between the connection of this pin to a 3V to 5.6V bias (typically PVCC). R is suggested to be a 5Ω resistor. And in 3.3V applications, the R could be shorted to allow the low end input in concerns of the VCC falling threshold. The VCC decoupling capacitor is strongly recommended to be a low ESR ceramic capacitor. This pin can be powered either by the internal linear regulator or by an external voltage source.
EPAD	GND	The bottom pad is the signal and power ground plane. All voltage levels are referenced to this pad. This pad provides a return path for the low-side MOSFET drives and internal power circuitries as well as all analog signals. Connect this pad to the circuit ground with the shortest possible path (more than 5 to 6 vias to the internal ground plane, placed on the soldering pad are recommended).

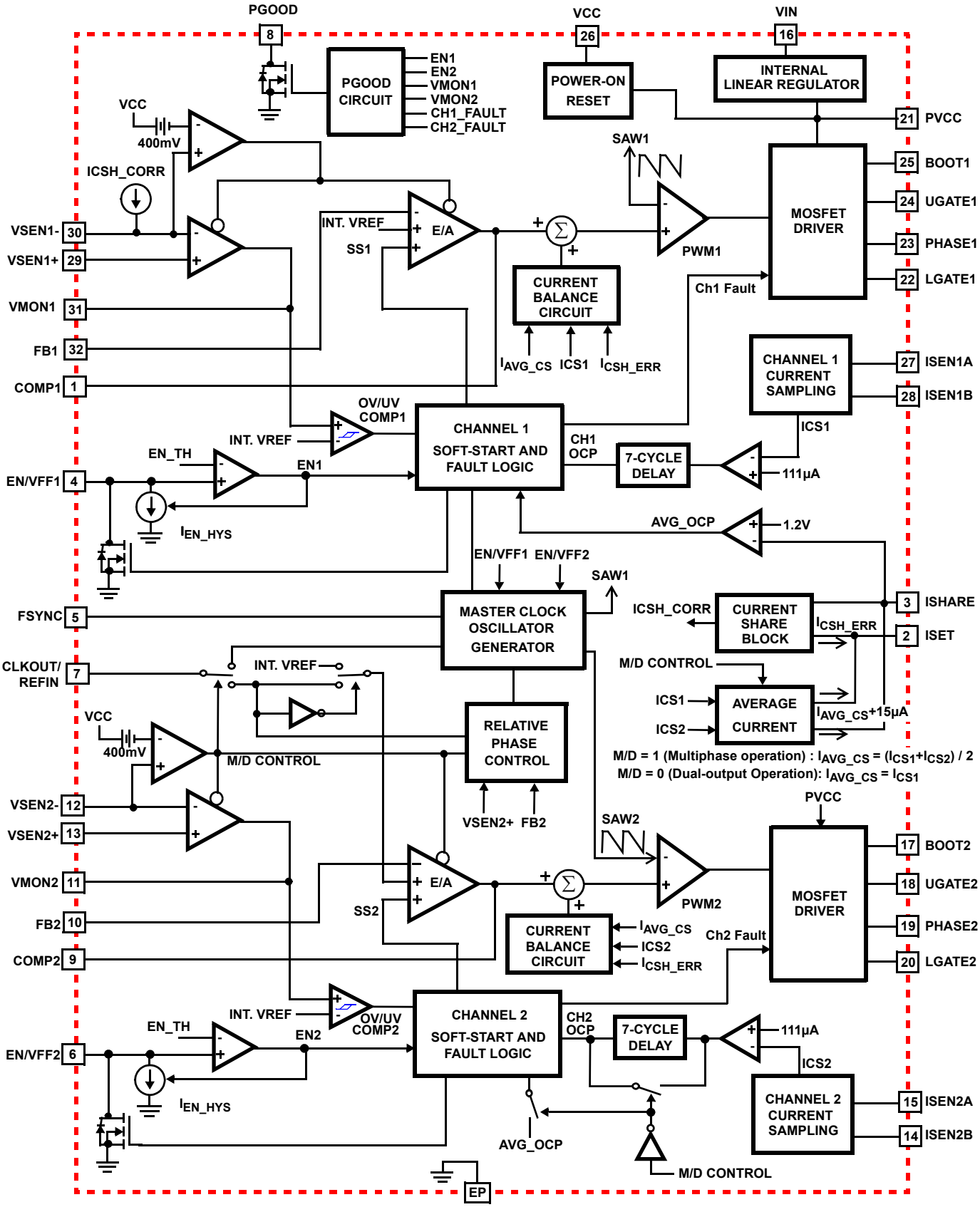
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL8126CRZ	ISL8126 CRZ	0 to +70	32 Ld 5x5 QFN	L32.5x5B
ISL8126IRZ	ISL8126 IRZ	-40 to +85	32 Ld 5x5 QFN	L32.5x5B
ISL8126EVAL1Z	Evaluation Board			

NOTES:

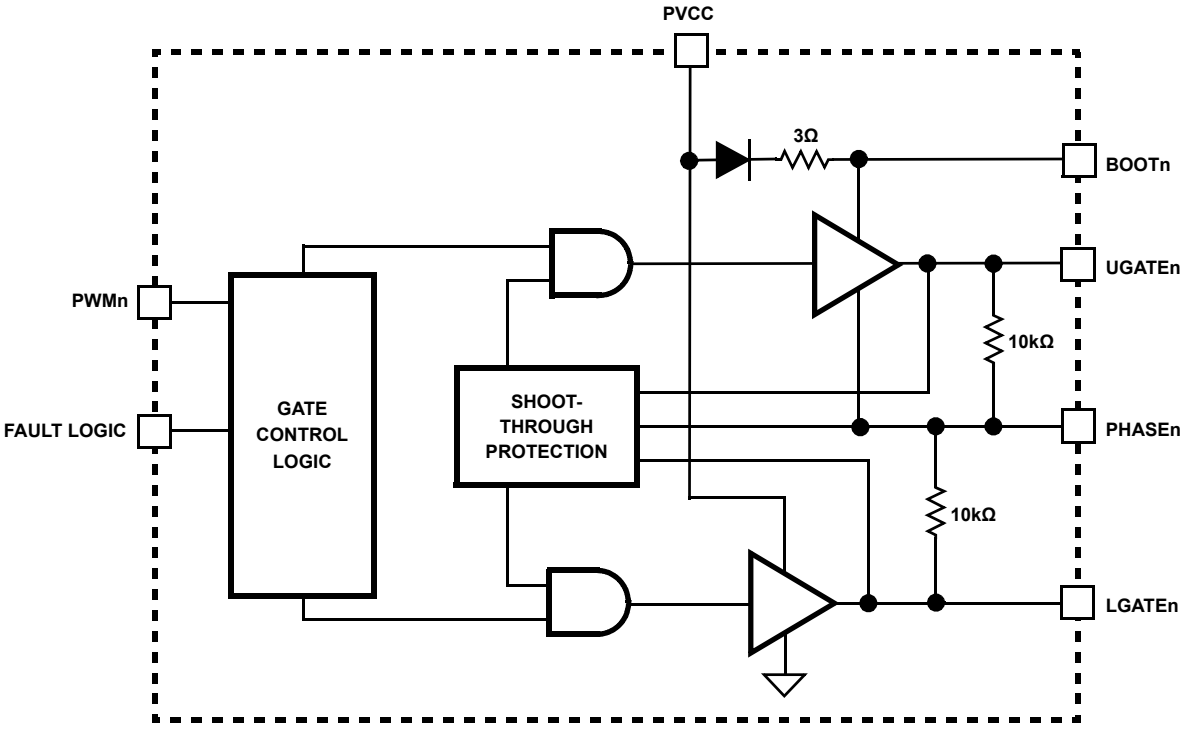
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8126. For more information on MSL please see techbrief TB363.

Controller Block Diagram



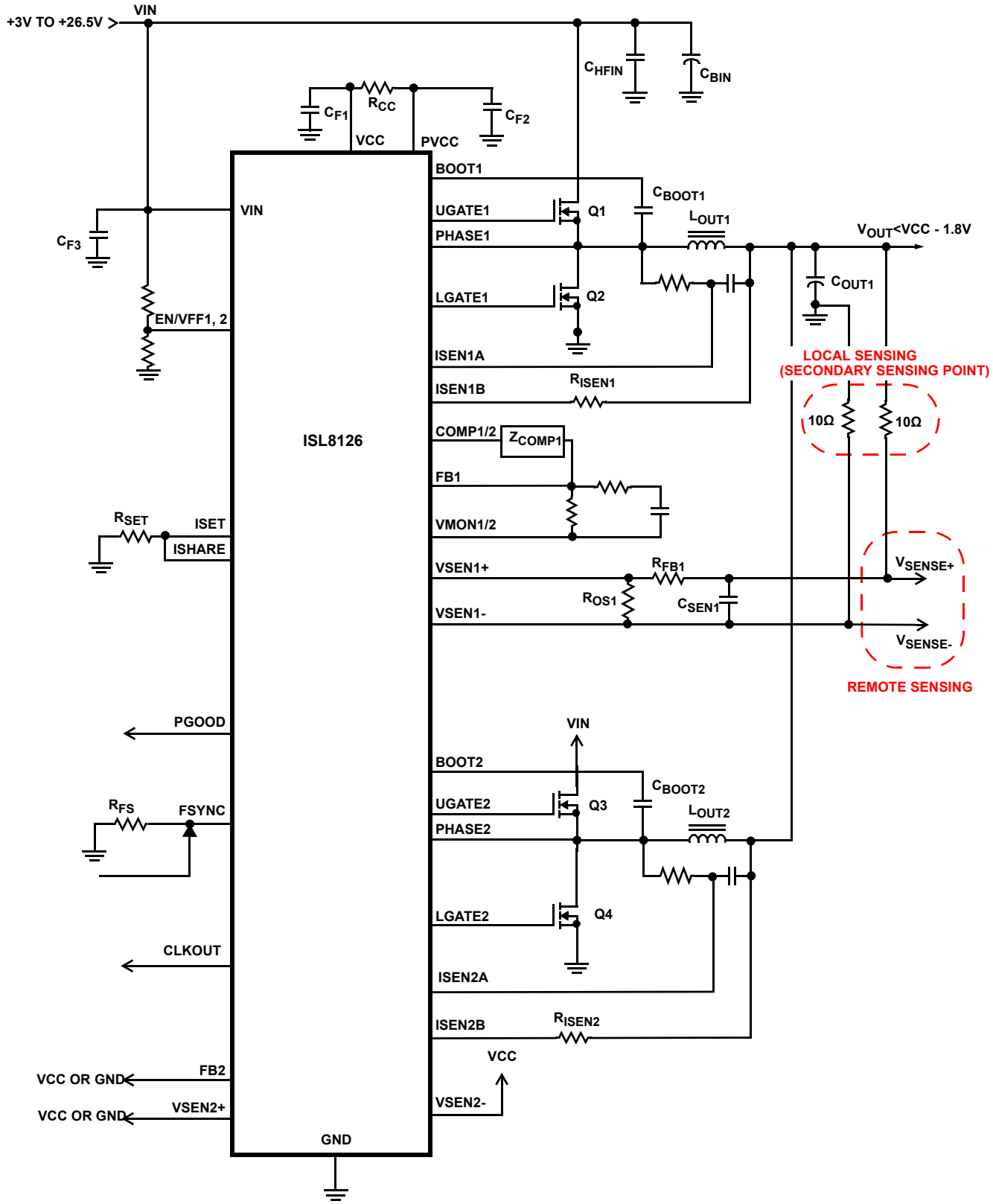
Integrated Driver Block Diagram

Channels 1 and 2 Gate Drive



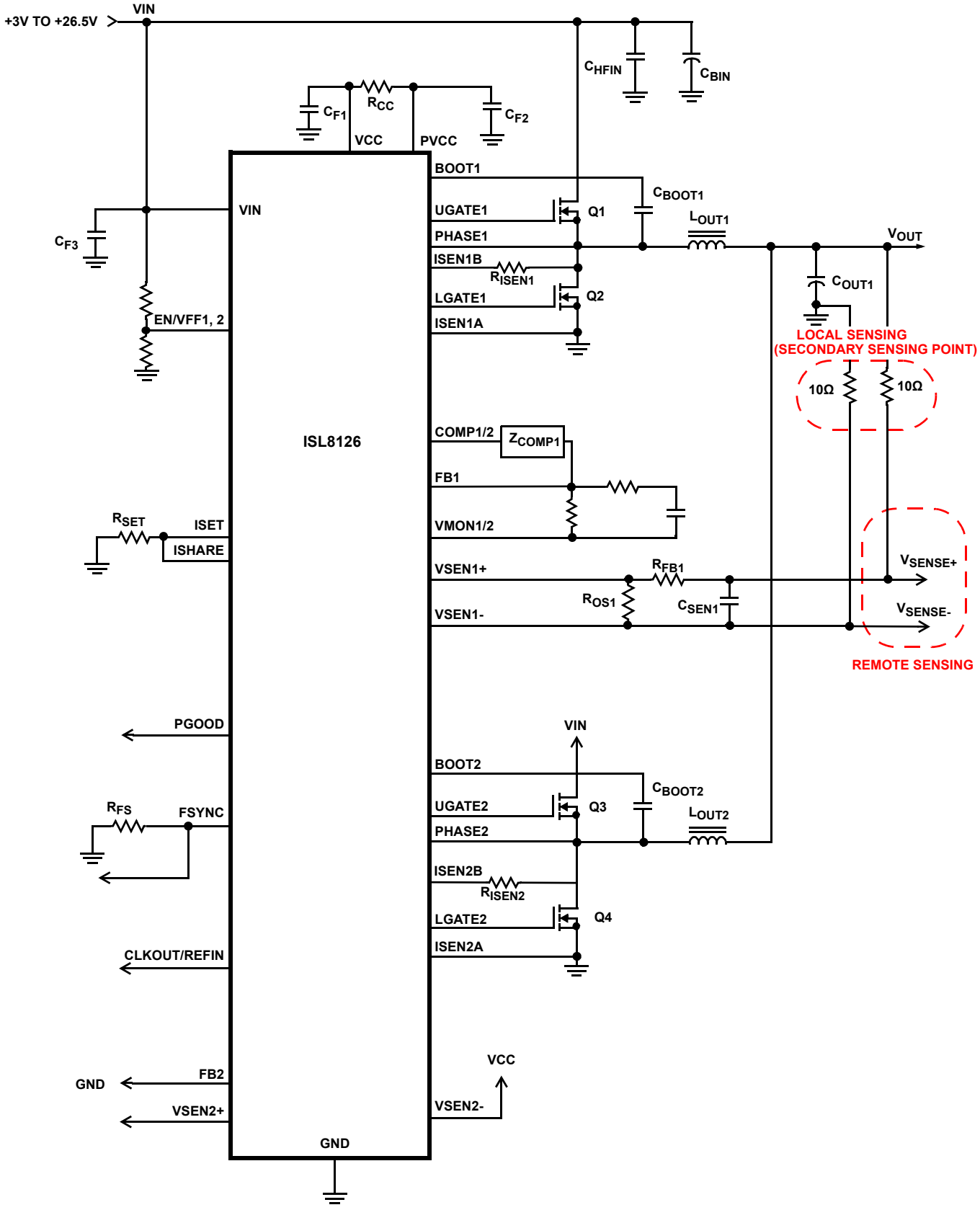
Typical Application Circuits

2-Phase Operation with DCR Sensing



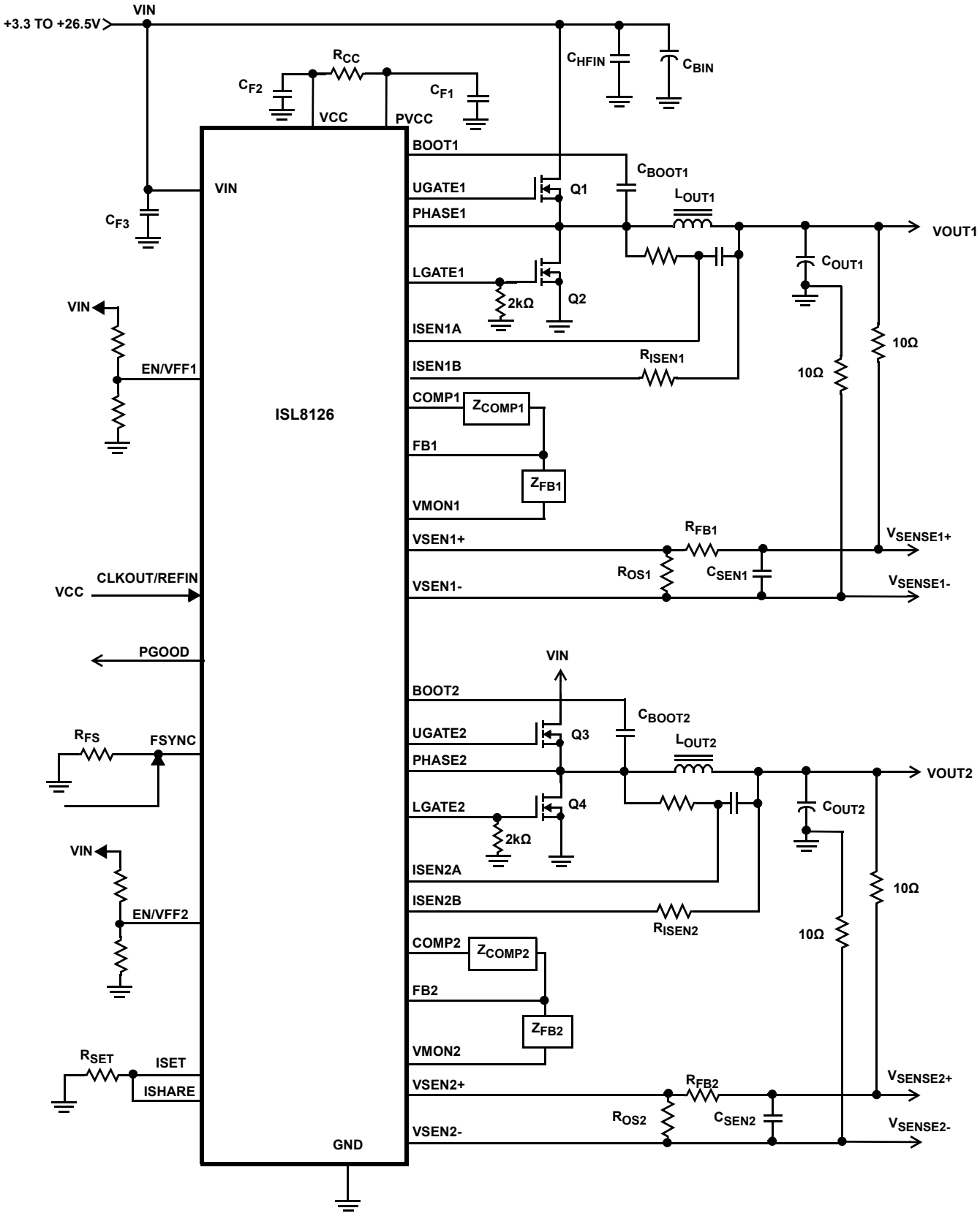
Typical Application Circuits (Continued)

2-Phase Operation with $r_{DS(ON)}$ Sensing



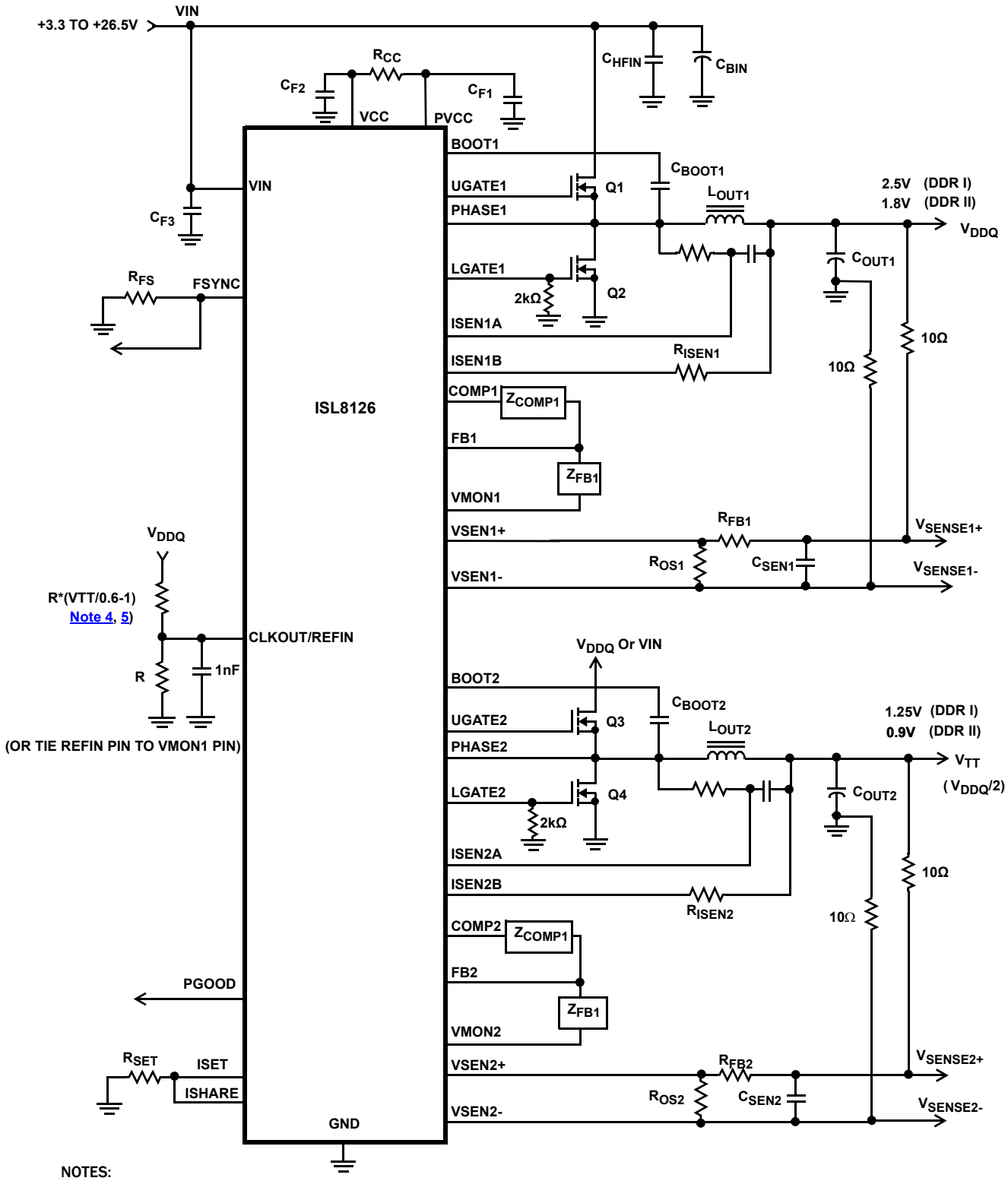
Typical Application Circuits (Continued)

Dual Regulators with DCR Sensing and Remote Sense



Typical Application Circuits (Continued)

Double Data Rate I or II

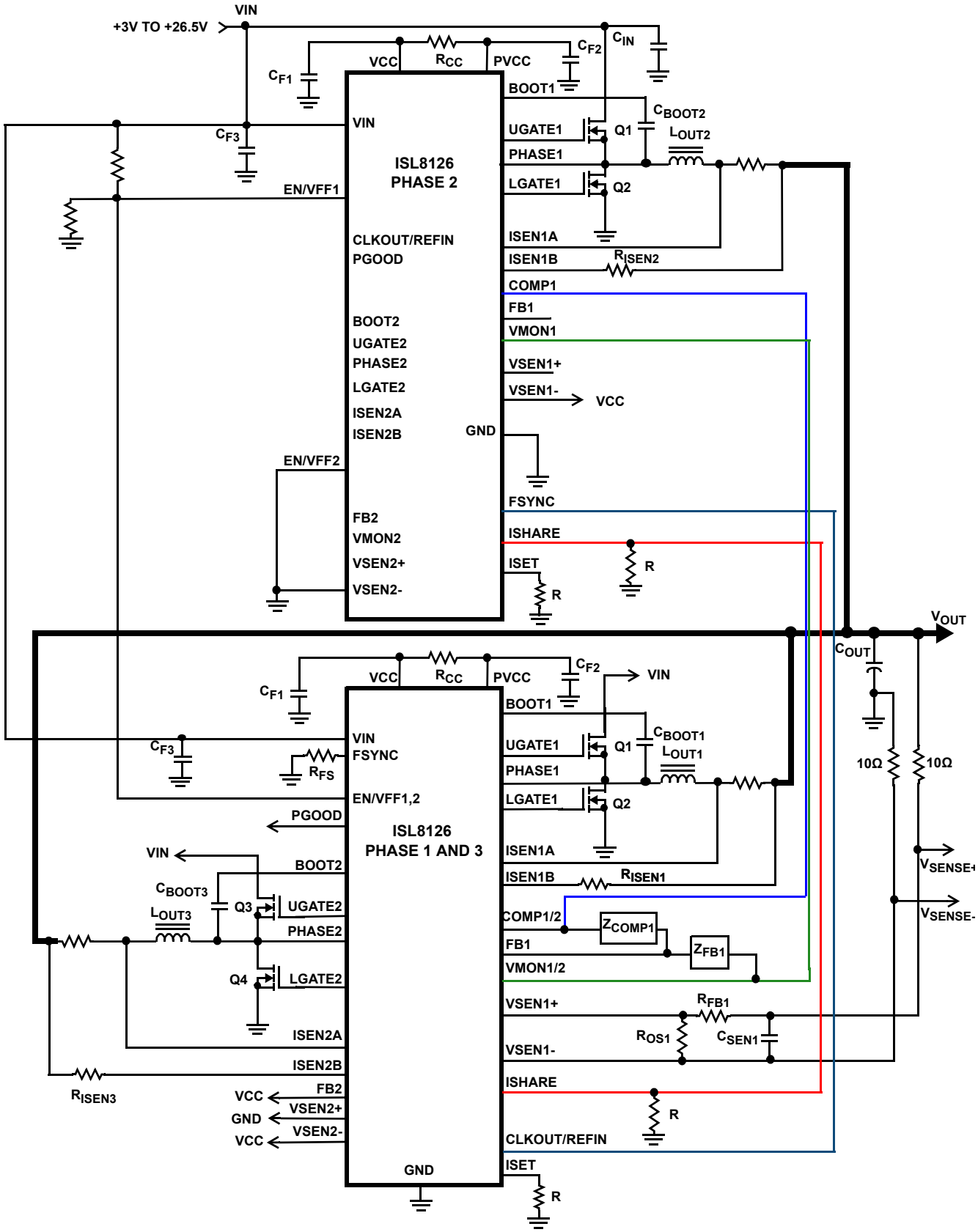


NOTES:

4. Setting the upper resistor to be a little higher than R*(VDDQ/0.7 - 1) will set the final REFIN voltage (stead state voltage after soft-start) derived from the VDDQ to be a little higher than internal 0.6V reference. In this way, the VTT final voltage will use the internal 0.6V reference after soft-start. The other way is to add more delay at EN/VFF1 pin to have Channel 2 tracking VDDQ (check the "DDR and Dual Mode Operation" on page 36 for more details).
5. Another way to set REFIN voltage is to connect VMON1 directly to the REFIN pin.

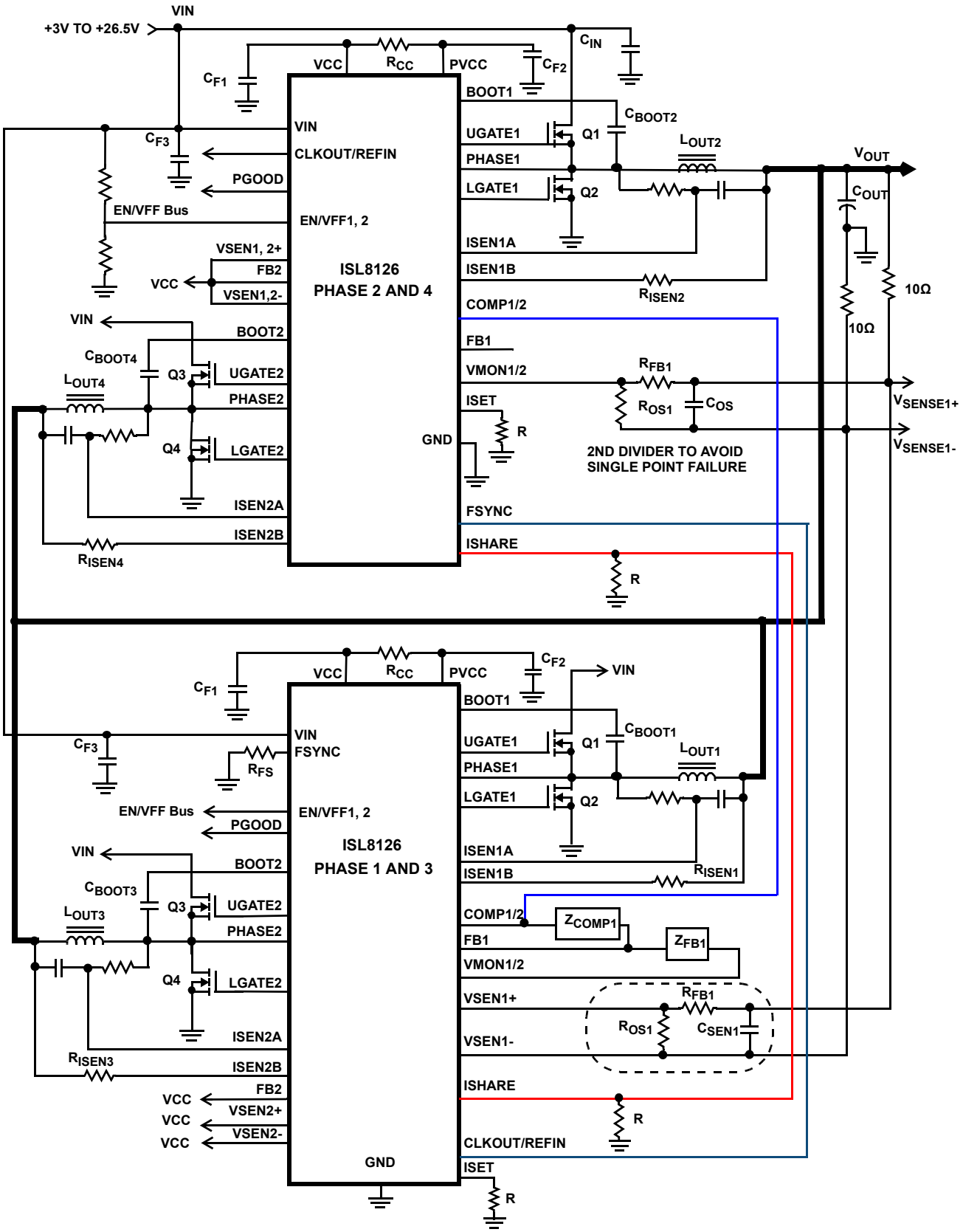
Typical Application Circuits (Continued)

3-Phase Regulator with Precision Resistor Sensing



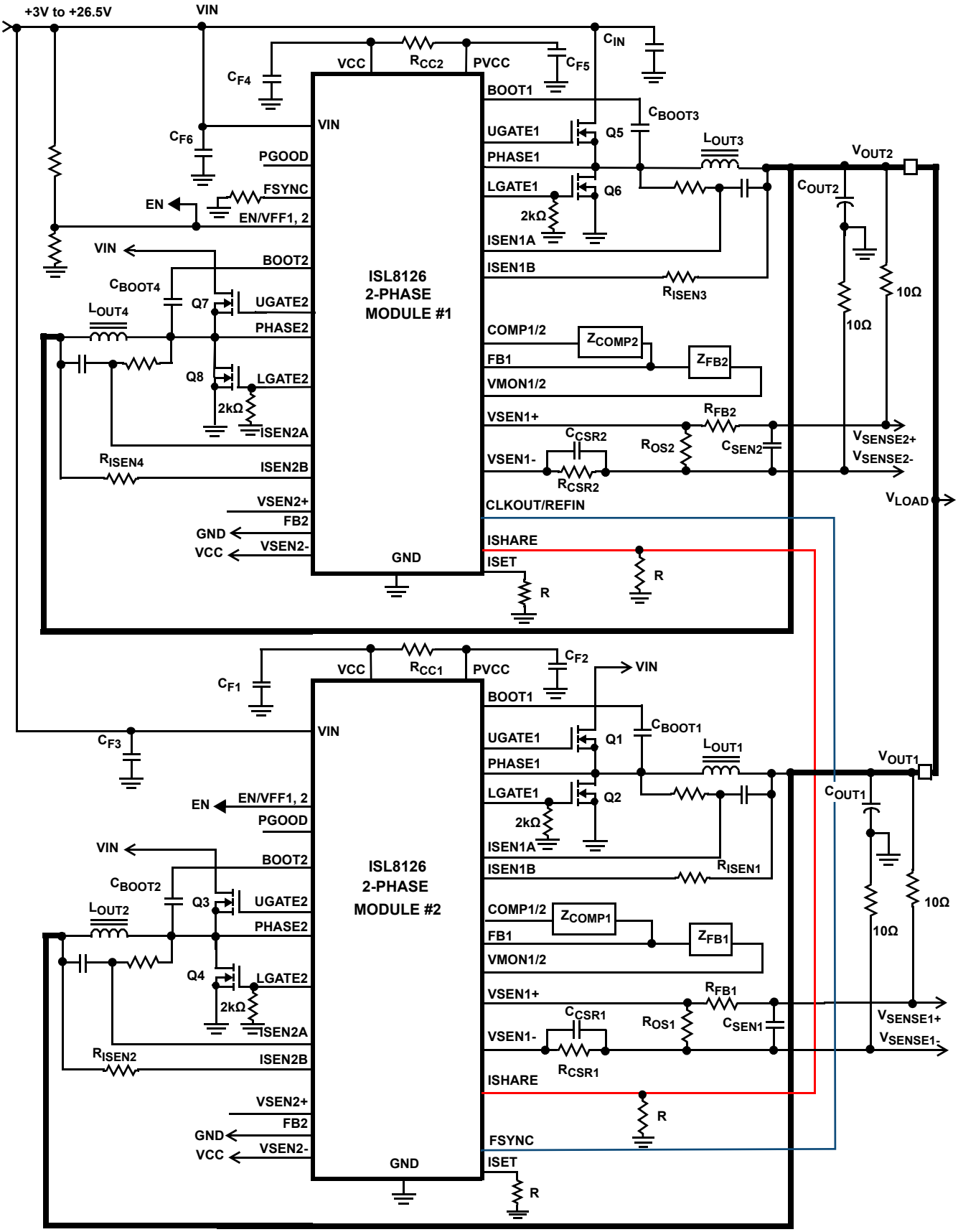
Typical Application Circuits (Continued)

4-Phase Operation with DCR Sensing



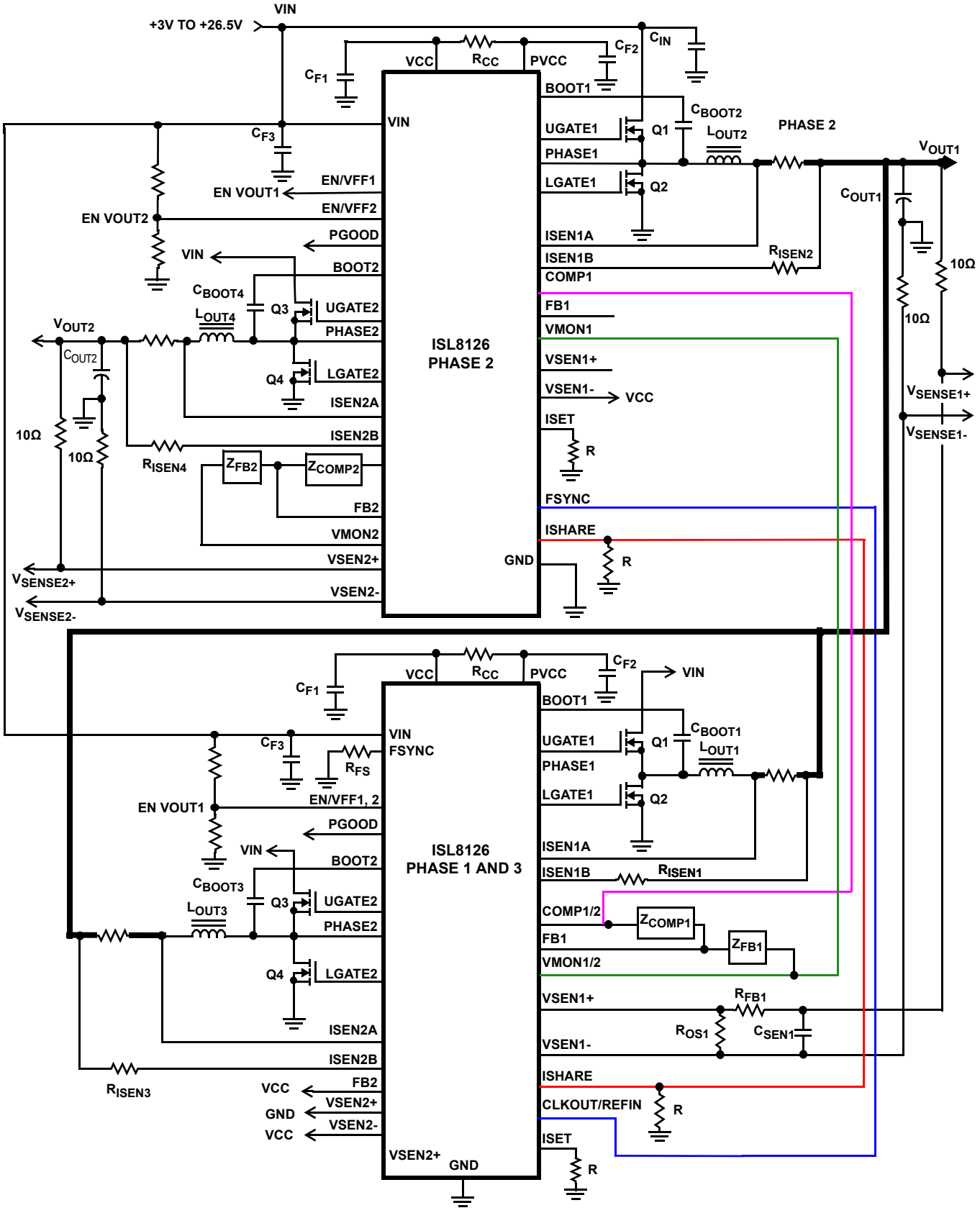
Typical Application Circuits (Continued)

Multiple Power Modules in Parallel with Current Sharing Control



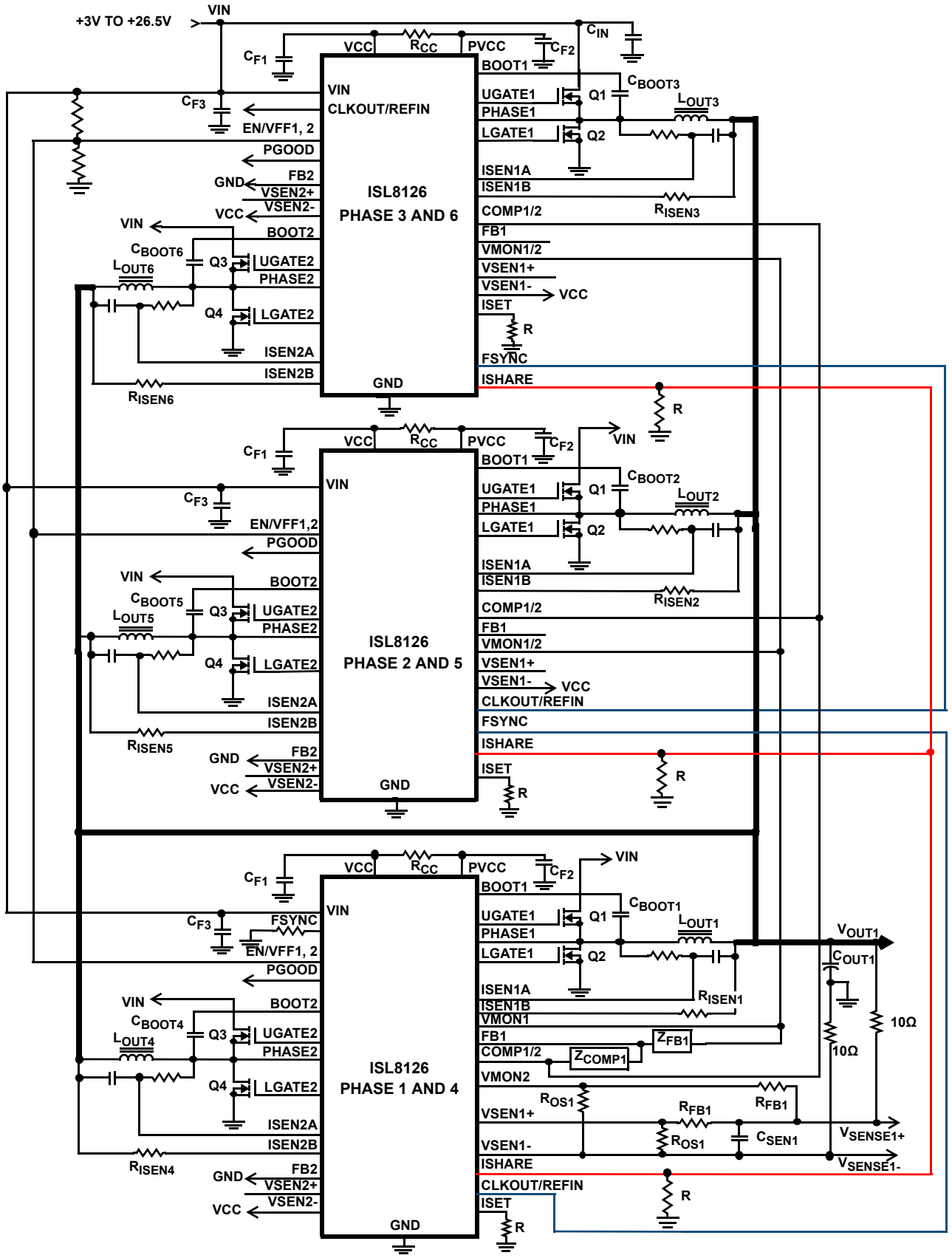
Typical Application Circuits (Continued)

3-Phase Regulator with Resistor Sensing and 1-Phase Regulator



Typical Application Circuits (Continued)

6-Phase Operation with DCR Sensing



Absolute Maximum Ratings

Input Voltage, VIN . . . . . -0.3V to +28V
Driver Bias Voltage, PVCC . . . . . -0.3V to +6.0V
Signal Bias Voltage, VCC . . . . . -0.3V to +6.5V
BOOT/UGATE Voltage, V_{BOOT} . . . . . -0.3V to +35V
Phase Voltage, V_{PHASE} . . . . . V_{BOOT} - 7V to V_{BOOT} + 0.3V
BOOT to PHASE Voltage, V_{BOOT} - V_{PHASE} . . . . . -0.3V to VCC +0.3V
Input, Output or I/O Voltage . . . . . -0.3V to VCC +0.3V
ESD Rating
- Human Body Model (Tested per JESD22-A114F) 3kV
- Machine Model (Tested per JESD22-A115C) 200V
- Charged Device Model (Tested per JESD22-C101D) 1kV

Latch Up (Tested per JESD-78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical Notes 6, 7)	θ_{JA}(°C/W)	θ_{JC}(°C/W)
32 Ld QFN Package	31	3

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Input Voltage, VIN . . . . . 3V to 26.5V
Driver Bias Voltage, PVCC . . . . . 3V to 5.6V
Signal Bias Voltage, VCC . . . . . 3V to 5.6V
Boot to Phase Voltage (Overcharged), V_{BOOT} - V_{PHASE} . . . . . <6V
Temperature
- ISL8126CRZ (Commercial) . . . . . 0°C to +70°C
- ISL8126IRZ (Industrial) . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
7. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C (Industrial) or 0°C to +70°C (Commercial).**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
VCC SUPPLY CURRENT						
Nominal Supply VIN Current	I_{Q_VIN}	V_{IN} = 20V; VCC = PVCC; f_{SW} = 500kHz; UGATE, LGATE = open	**11**	15	**22**	mA
Nominal Supply VIN Current	I_{Q_VIN}	V_{IN} = 3.3V; VCC = PVCC; f_{SW} = 500kHz; UGATE, LGATE = open	**7**	12	**14**	mA
Shutdown Supply PVCC Current	I_{PVCC}	EN = 0V, PVCC = 5V	**0.5**	1	**2.0**	mA
Shutdown Supply VCC Current	I_{VCC}	EN = 0V, VCC = 3V	**5**	10	**12**	mA
INTERNAL LINEAR REGULATOR						
Current Limit Threshold	I_{PVCC}	V_{IN} = 6V; PVCC = 4V		320		mA
Saturated Equivalent Impedance (Note 8)	R_{LDO}	P-Channel MOSFET (V_{IN} = 5V)		1		Ω
PVCC Voltage Level	PVCC	I_{PVCC} = 0mA; V_{IN} = 12V	**5.15**	5.40	**5.60**	V
POWER-ON RESET						
Rising VCC Threshold				2.85	**2.97**	V
Falling VCC Threshold				2.65	**2.75**	V
Rising PVCC Threshold				2.85	**2.97**	V
Falling PVCC Threshold				2.65	**2.75**	V
System Soft-start Delay (Note 8)	t_{SS_DLY}	After PLL, VCC, and PVCC PORs, and EN(s) above their thresholds		192		Cycles
ENABLE						
Turn-On Threshold Voltage			**0.75**	0.8	**0.86**	V
Hysteresis Sink Current	I_{EN_HYS}	0°C < T_A < +85°C	24	30	35	µA
		-40°C < T_A < +85°C	21	30	35	µA

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C (Industrial) or 0°C to +70°C (Commercial). (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Undervoltage Lockout Hysteresis (Note 8)	V_{EN_HYS}	V_{EN_RTH} = 10.6V; V_{EN_FTH} = 9V R_{UP} = 53.6kΩ, R_{DOWN} = 5.23kΩ		1.6		V
Sink Current	I_{EN_SINK}	V_{ENFF} = 1V	**15.4**			mA
Sink Impedance	R_{EN_SINK}	V_{ENFF} = 1V			**64**	Ω
OSCILLATOR						
Oscillator Frequency Range			**150**		**1500**	kHz
Oscillator Frequency		R_{FS} = 100k, (Figure 29)	**344**	377	**406**	kHz
Total Variation		VCC = 5V; -40°C < T_A < +85°C	-9		+9	%
Peak-to-Peak Ramp Amplitude	ΔV_{RAMP}	VCC = 5V, V_{EN} = 0.8V		1		V_{P-P}
Linear Gain of Ramp Over V_{EN}	G_{RAMP}	$G_{RAMP} = \Delta V_{RAMP}/V_{EN}$		1.25		
Ramp Peak Voltage	V_{RAMP_PEAK}	V_{EN} = VCC		VCC - 1.4		V
Peak-to-Peak Ramp Amplitude	ΔV_{RAMP}	V_{EN} = VCC = 5.4V, R_{UP} = 2k		3		V_{P-P}
Peak-to-Peak Ramp Amplitude	ΔV_{RAMP}	V_{EN} = VCC = 3V; R_{UP} = 2k		0.6		V_{P-P}
Ramp Amplitude Upon Disable	ΔV_{RAMP}	V_{EN} = 0V; VCC = 3.5V to 5.5V		1		V_{P-P}
Ramp Amplitude Upon Disable	ΔV_{RAMP}	V_{EN} = 0V; VCC < 3.4V		VCC - 2.4		V_{P-P}
Ramp DC Offset	V_{RAMP_OS}			1		V
FREQUENCY SYNCHRONIZATION AND PHASE LOCK LOOP						
Synchronization Frequency		VCC = 5V	**150**		**1500**	kHz
PLL Locking Time		VCC = 5.4V (2.97V); F_{SW} = 400kHz;		105		µs
Input Signal Duty Cycle Range (Note 8)			**10**		**90**	%
PWM						
Minimum PWM OFF Time	t_{MIN_OFF}		**310**	345	**410**	ns
Current Sampling Blanking Time (Note 8)	$t_{BLANKING}$			175		ns
REFERENCE						
Channel 1 Reference Voltage (Include Error and Differential Amplifiers' Offsets)	V_{REF1}	0°C < T_A < +70°C		0.6		V
			-0.6		0.6	%
		-40°C < T_A < +85°C		0.6		V
			-0.75		0.75	%
Channel 2 Reference Voltage (Include Error and Differential Amplifiers' Offsets)	V_{REF2}	0°C < T_A < +70°C		0.6		V
			-0.75		0.75	%
		-40°C < T_A < +85°C		0.6		V
			-0.8		0.8	%
ERROR AMPLIFIER						
DC Gain (Note 8)		R_L = 10k, C_L = 100pF, at COMP Pin		98		dB
Unity Gain-Bandwidth (Note 8)	UGBW_EA	R_L = 10k, C_L = 100pF, at COMP Pin		80		MHz
Input Common Mode Range (Note 8)			**-0.2**		**VCC - 1.8**	V
Output Voltage Swing		VCC = 5V	**0.85**		**VCC - 1.0**	V

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C (Industrial) or 0°C to +70°C (Commercial). (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Slew Rate (Note 8)	SR_EA	R_L = 10k, C_L = 100pF, at COMP Pin		20		V/µs
Input Current (Note 8)	I_{FB}	Positive Direction Into the FB pin		100		nA
Output Sink Current	I_{COMP}			3		mA
Output Source Current	I_{COMP}			6		mA
Disable Threshold (Note 8)	V_{VSEN-}			VCC - 0.4		V
DIFFERENTIAL AMPLIFIER						
DC Gain (Note 8)	UG_DA	Unity Gain Amplifier		0		dB
Unity Gain Bandwidth (Note 8)	UGBW_DA			5		MHz
Maximum Source Current for Current Sharing (See "Typical Application Circuit on page 14)	I_{VSEN1-}	VSEN1- Source Current for Current Sharing when parallel multiple modules each of which has its own voltage loop		350		µA
Output Voltage Swing (Note 8)			**0**		**VCC - 1.8**	V
Input Common Mode Range (Note 8)			**-0.2**		**VCC - 1.8**	V
Disable Threshold (Note 8)	V_{VSEN-}	V_{MON1}, V_{MON2} = tri-state		VCC - 0.4		V
VSEN+ Pin Input Current	I_{VSEN+}		**0.2**	1.16	**2.5**	µA
Input Impedance	$R_{VSEN+\_to\_VSEN-}$	V_{VSEN+}/I_{VSEN+}, V_{VSEN+} = 0.6V		-500		kΩ
GATE DRIVERS						
Upper Drive Source Resistance	R_{UGATE}	45mA Source Current		1.0		Ω
Upper Drive Sink Resistance	R_{UGATE}	45mA Sink Current		1.0		Ω
Lower Drive Source Resistance	R_{LGATE}	45mA Source Current		1.0		Ω
Lower Drive Sink Resistance	R_{LGATE}	45mA Sink Current		0.4		Ω
OVERCURRENT PROTECTION						
Channel Overcurrent Limit (Note 8)	I_{SOURCE}	VCC = 2.97V to 5.6V		111		µA
Channel Overcurrent Limit	I_{SOURCE}	VCC = 5V; 0°C < T_A < +70°C	**94**	111	**129**	µA
		VCC = 5V; -40°C < T_A < +85°C	**89**	111	**129**	µA
Share Pin OC Threshold	V_{OC_ISHARE}	comparator offset included	**1.16**	1.20	**1.22**	V
CURRENT SHARE						
Internal Balance Accuracy (Note 8)		VCC = 2.97V and 5.6V, 1% Resistor Sense, 10mV Signal		±5		%
Internal Balance Accuracy (Note 8)		VCC = 4.5V and 5.6V, 1% Resistor Sense, 10mV Signal		±5		%
External Current Share Accuracy (Note 8)		VCC = 2.97V and 5.6V, 1% Resistor Sense, 10mV Signal		±10		%
POWER-GOOD MONITOR						
Undervoltage Falling Trip Point	V_{UVF}	Percentage Below Reference Point	**-15**	-13	**-11**	%
Undervoltage Rising Hysteresis	V_{UVR_HYS}	Percentage Above UV Trip Point		4		%
Overvoltage Rising Trip Point	V_{OVR}	Percentage Above Reference Point	**11**	13	**15**	%
Overvoltage Falling Hysteresis	V_{OVF_HYS}	Percentage below OV Trip Point		4		%

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C (Industrial) or 0°C to +70°C (Commercial). (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
PGOOD Low Output Voltage		I_{PGOOD} = 2mA			**0.35**	V
Sinking Impedance		I_{PGOOD} = 2mA			**70**	Ω
Maximum Sinking Current (Note 8)		V_{PGOOD} <0.8V		10		mA
OVERVOLTAGE PROTECTION						
OV Latching Trip Point		EN/FF= UGATE = LATCH Low, LGATE = High	**118**	120	**122**	%
OV Non-Latching Trip Point (Note 8)		EN/FF = Low, UGATE = Low, LGATE = High		113		%
LGATE Release Trip Point		EN/FF = Low/HIGH, UGATE = Low, LGATE = Low		87		%
OVER-TEMPERATURE PROTECTION						
Over-Temperature Trip (Note 8)				150		°C
Over-Temperature Release Threshold (Note 8)				125		°C

NOTES:

8. Limits should be considered typical and are not production tested.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

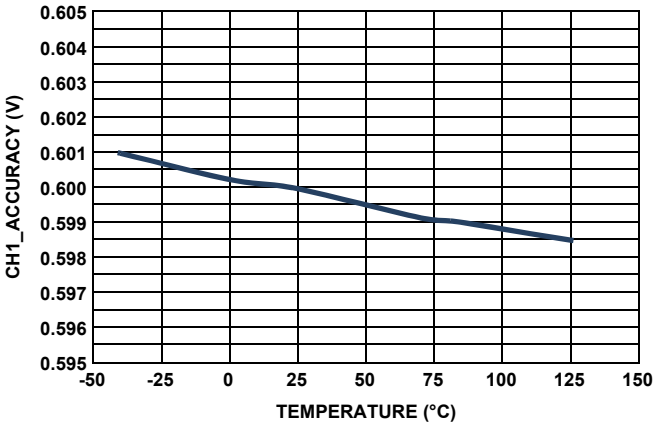


FIGURE 2. CHANNEL 1 ACCURACY vs TEMPERATURE

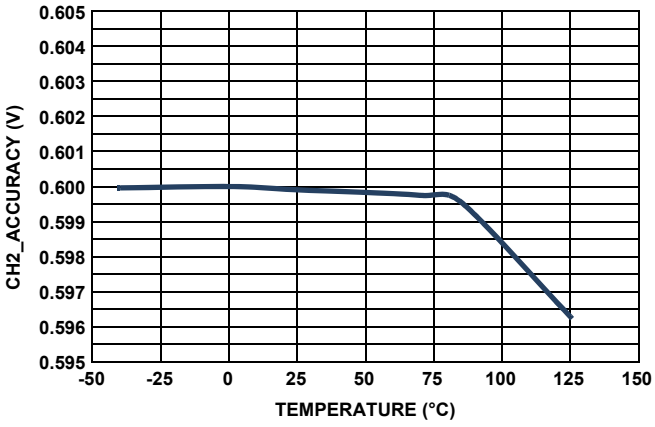


FIGURE 3. CHANNEL 2 ACCURACY vs TEMPERATURE

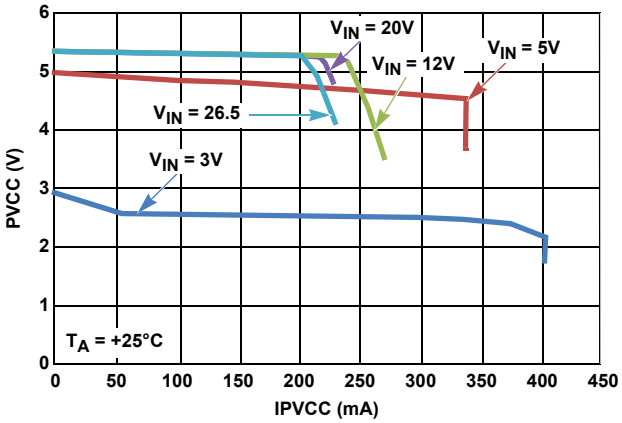


FIGURE 4. PVCC V-I CURVE AT +25°C

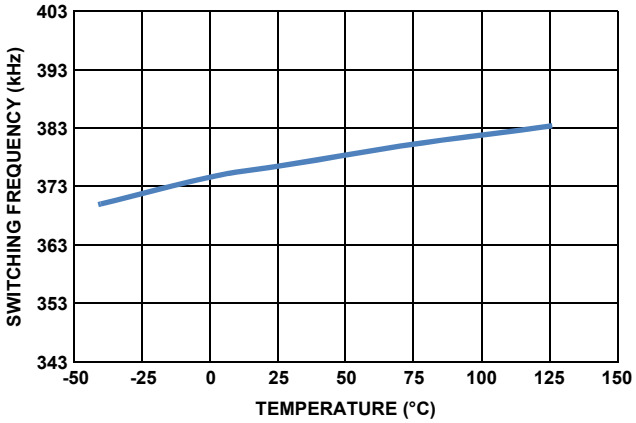


FIGURE 5. SWITCHING FREQUENCY vs TEMPERATURE

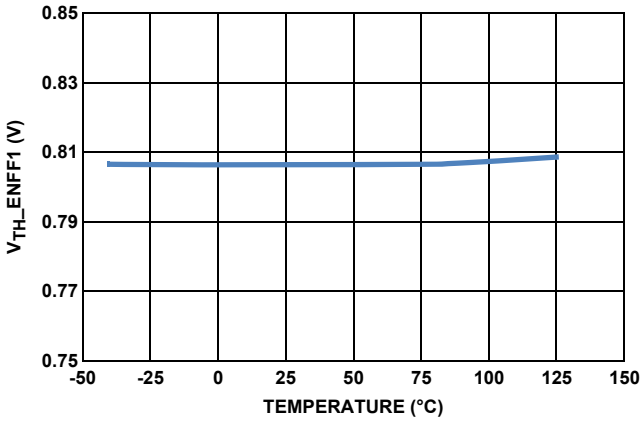


FIGURE 6. $V_{EN/VFF1}$ ENABLE THRESHOLD vs TEMPERATURE

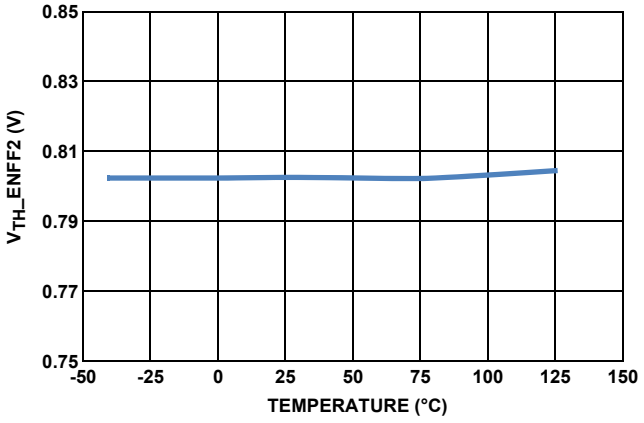


FIGURE 7. $V_{EN/VFF2}$ ENABLE THRESHOLD vs TEMPERATURE

Typical Performance Curves (Continued)

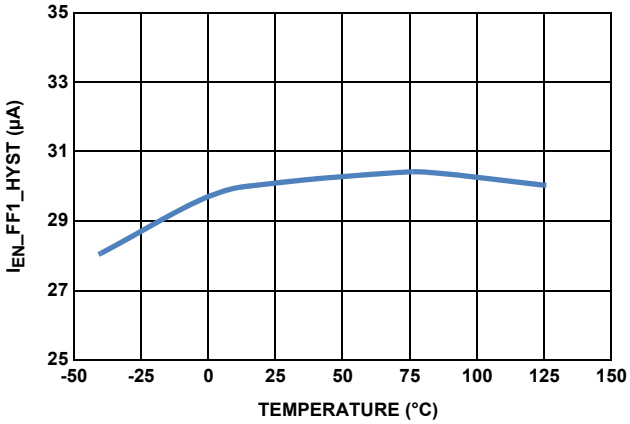


FIGURE 8. EN/VFF1 HYSTERESIS CURRENT vs TEMPERATURE

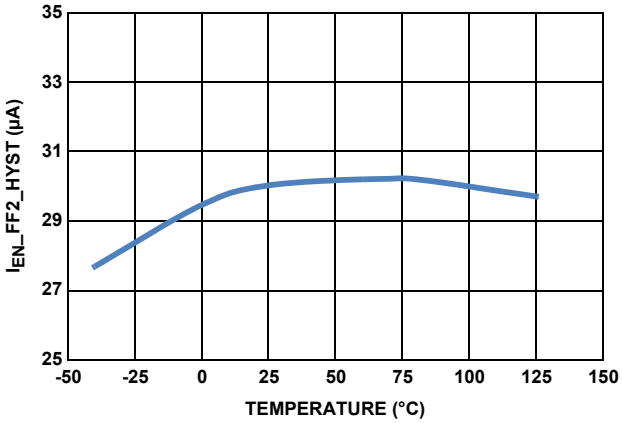


FIGURE 9. EN/VFF2 HYSTERESIS CURRENT vs TEMPERATURE

Modes of Operation

There are 9 typical operation modes depending upon the signal levels on EN/VFF1, EN/VFF2, VSEN2+, VSEN2-, FB2, and CLKOUT/REFIN.

MODE 1: The IC is completely disabled when EN/VFF1 and EN/VFF2 are pulled below 0.8V.

MODE 2: With EN/VFF1 pulled low and EN/VFF2 pulled >0.8V (Mode 2A), or EN/VFF1 pulled >0.8V and EN/VFF2 pulled low (Mode 2B), the ISL8126 operates as a single phase regulator. When EN/VFF1 is pulled low, the ISHARE pin is pulled to VCC internally. Upon EN/VFF1 >0.8V, there will be current sourcing out from the ISHARE pin, which represents the Channel 1 current plus 15µA offset current.

MODE 3: When VSEN2- is used as a negative sense line, both channels' phase shift depends upon the voltage level of CLKOUT/REFIN. When the CLKOUT/REFIN pin is within 29% to 45% of VCC, Channel 2 delays 0° over Channel 1 (Mode 3A); when within 45% to 62% of VCC, there is a 90° delay (Mode 3B); when greater than 62% to VCC, there is a 180° delay (Mode 3C). Refer to the "DDR and Dual Mode Operation" on page 36.

MODE 4: When VSEN2- is used as a negative remote sense line, and CLKOUT/REFIN is connected to an external voltage ramp lower than the internal soft-start ramp and lower than 0.6V, the external ramp signal will replace Channel 2's internal soft-start ramp to be tracked at start-up, controller operating in DDR mode. The controller will use the lowest voltage among the internal 0.6V reference, the external voltage in CLKOUT/REFIN pin and the soft-start ramp signal. Channel 1 is delayed 60° behind Channel 2. Refer to the "DDR and Dual Mode Operation" on page 36.

MODE 5: With VSEN2- pulled within 400mV of VCC, FB2 pulled to ground and VSEN2+ pulled either to VCC or GND, the internal channels are 180° out-of-phase and operate in 2-phase single output (Mode 5A). The CLKOUT/REFIN pin also signals out clock with 60° phase shift (rising edge) relative to the Channel 1's clock signal (falling edge of PWM) for 6-phase operation with two other ISL8126s (Mode 5B). When the share pins are not connected to each other for the three ICs in sync, two of which can operate in Mode 5A. The 3rd IC can be operated in Mode 3 to generate 3 independent outputs (Mode 5C), or the 3rd IC can also be operated in Mode 4 to generate 4 independent outputs (Mode 5D).

MODE 6: With VSEN2- pulled within 400mV of VCC, FB2 pulled to VCC and VSEN2+ pulled to GND, the internal channels (as 1st and 3rd Phase, respectively) are 240° out-of-phase. The CLKOUT/REFIN pin signals out 120° relative phases to the falling edge of Channel 1's clock signal to synchronize with the second ISL8126's Channel 1 (as 2nd Phase). This allows 3-phase single output configuration to be constructed using two ISL8126s.

MODE 7: With VSEN2- pulled within 400mV of VCC and both of FB2 and VSEN2+ pulled to VCC, the internal channel is 180° out-of-phase. The CLKOUT/REFIN pin signals out (rising edge) 90° relative phase to the Channel 1's clock signal (falling edge of PWM) to synchronize with another ISL8126, which can operate at Mode 3, 4, 5A, or 7A. A 4-phase single output converter can be constructed with two ISL8126s operating in Mode 5A or 7A (Mode 7A). If the share bus is not connected between ICs, each IC could generate an independent output (Mode 7B). When the second ISL8126 operates as two independent regulators (Mode 3) or in DDR mode (Mode 4), then a three independent output system is generated (Mode 7C). Both ICs can also be constructed as a 3-phase converter (0°, 90°, and 180°, not an equal phase shift for 3-phase) with a single phase regulator (270°).

MODE 8: The output CLKOUT signal allows expansion for 12-phase operation with the cascaded sequencing, as shown in Table 1. No external clock is required in this mode for the desired phase shift.

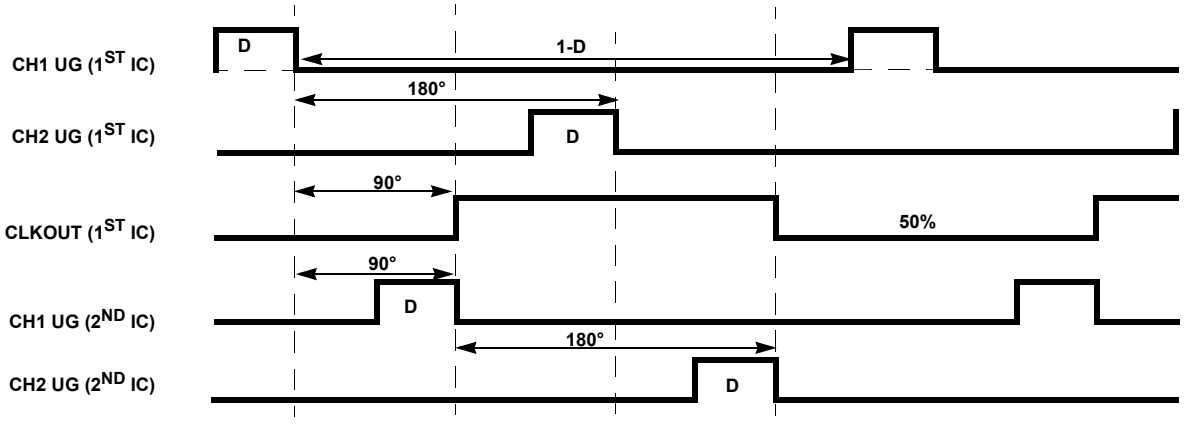
MODE 9: With an external clock, the part can be expanded for 5, 7, 8, 9 10 and 11 phase single output operation with the desired phase shift.

TABLE 1.

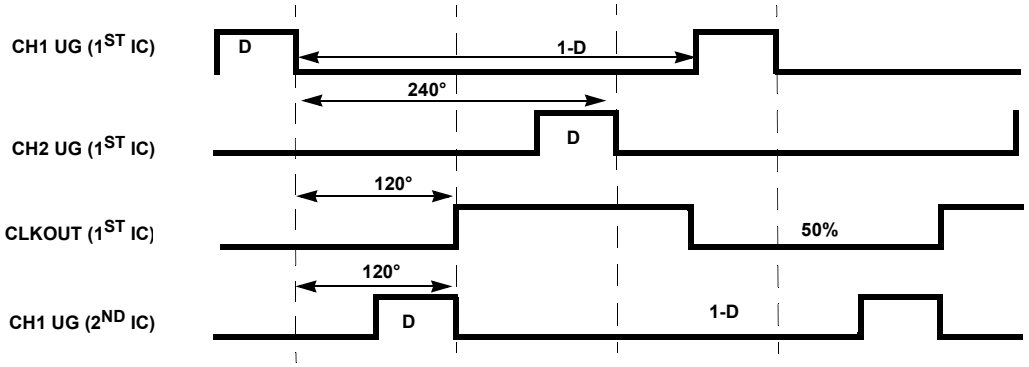
1ST IC (I = INPUT; O = OUTPUT; I/O = INPUT AND OUTPUT, BIDIRECTION)									MODES OF OPE	
MODE	EN/ VFF1	EN/ VFF2	VSEN2- (I)	FB2 (I)	VSEN2+ (I)	CLKOUT/REFIN WRT 1ST (I or O)	ISHARE (I/O) REPRESENTS WHICH CHANNEL(S) CURRENT	2ND CHANNEL WRT 1ST (O) (Note 10)	OPERATION MODE of 2ND IC	OP
1	<0.8V	<0.8V	-	-	-	-	-	-	-	
2A	<0.8V	>0.8V	ACTIVE	ACTIVE	ACTIVE	-	N/A	-	-	
2B	>0.8V	<0.8V	-	-	-	-	1ST CHANNEL	-	-	
3A	>0.8V	>0.8V	<VCC -0.4V	ACTIVE	ACTIVE	29% to 45% of VCC (I)	1ST CHANNEL	0°	-	
3B	>0.8V	>0.8V	<VCC -0.4V	ACTIVE	ACTIVE	45% to 62% of VCC (I)	1ST CHANNEL	90°	-	
3C	>0.8V	>0.8V	<VCC -0.4V	ACTIVE	ACTIVE	> 62% of VCC (I)	1ST CHANNEL	180°	-	
4	>0.8V	>0.8V	<VCC-0.4V	ACTIVE	ACTIVE	< 29% of VCC (I)	1ST CHANNEL	-60°	-	
5A	Note 11	Note 11	VCC	GND	VCC/GND	60°	Average of Channel 1 & 2	180°	-	
5B	Note 11	Note 11	VCC	GND	VCC/GND	60°	Average of Channel 1 and 2	180°	5A	
5C	Note 11	Note 11	VCC	GND	VCC/GND	60°	Average of Channel 1 and 2	180°	5A	
5D	Note 11	Note 11	VCC	GND	VCC/GND	60°	Average of Channel 1 and 2	180°	5A	
6	Note 11	Note 11	VCC	VCC	GND	120°	Average of Channel 1 and 2	240°	2B	
7A	Note 11	Note 11	VCC	VCC	VCC	90°	Average of Channel 1 and 2	180°	5A or 7A	
7B	Note 11	Note 11	VCC	VCC	VCC	90°	Average of Channel 1 and 2	180°	5A or 7A	
7C	Note 11	Note 11	VCC	VCC	VCC	90°	Average of Channel 1 and 2	180°	3, 4	
8	Note 11	Note 11	Cascaded IC Operation MODEs 5A+5A+7A+5A+5A+5A/7A, No External Clock Required							
9	Note 11	Note 11	External Clock or External Logic Circuits Required for Equal Phase Interval							

NOTES:

10. "**2ND CHANNEL WRT 1ST**" is referred to as "channel 2 lag channel 1 by the degrees specified by the number in the corresponding table cells". For example, 90 means channel 2 lags channel 1 by 90°; -60° with **2ND CHANNEL WRT 1ST** means channel 2 leads channel 1 by 60°.
11. All EN/VFF pins are tied together.



4 PHASE TIMING DIAGRAM (MODE 7A)



CH2 UG (2ND IC, OFF, EN/VFF2 = 0)

3-PHASE TIMING DIAGRAM (MODE 6)

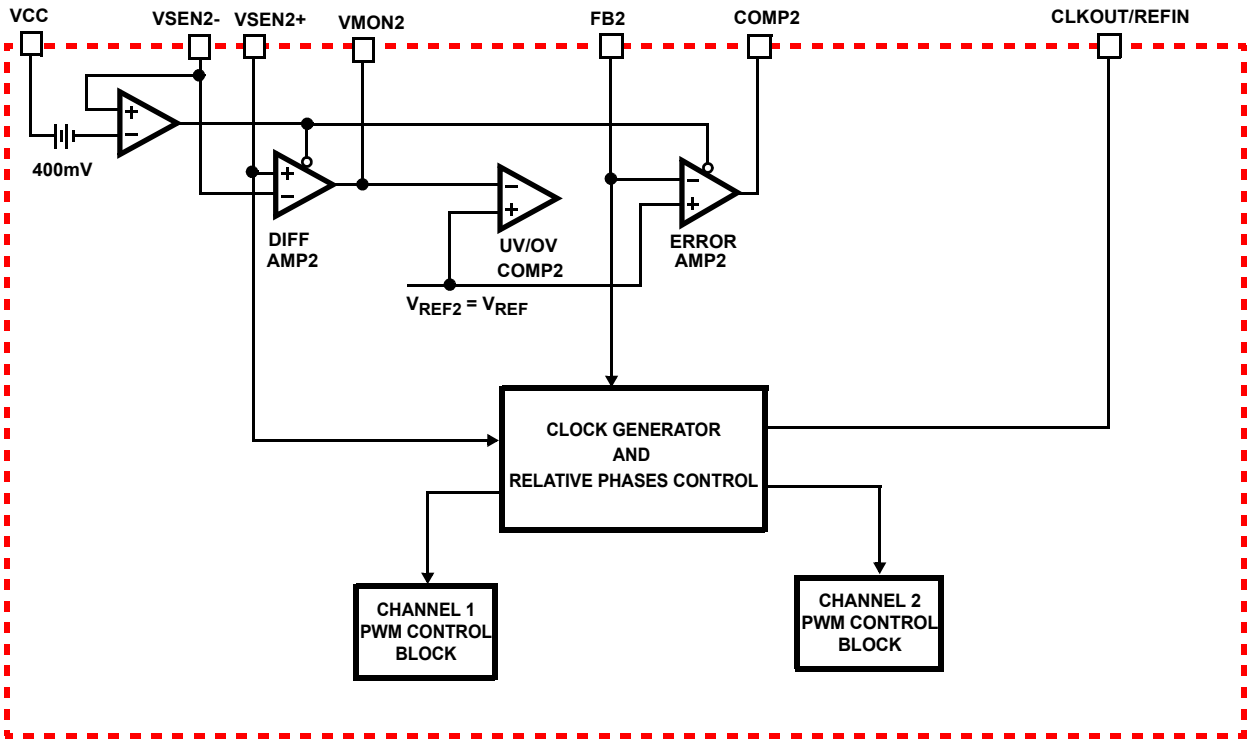


FIGURE 10. SIMPLIFIED RELATIVE PHASES CONTROL

Functional Description

Initialization

Initially, the ISL8126 Power-On Reset (POR) circuits continually monitor the bias voltages (PVCC and VCC) and the voltage at the EN/VFF pin. The POR function initiates soft-start operation 192 clock cycles after the following conditions are met:

- VCC and PVCC voltages exceed their POR thresholds.
- PLL locking time has expired.
- EN/VFF pin voltage is pulled to be above 0.8V.
- For Channel 1 only, ISHARE voltage must fall below 70% (typical) of VCC.

ISHARE is also pulled to VCC when Channel1 detects fault conditions or EN/VFF1 is below its POR threshold. ISHARE is released from VCC after EN/VFF1's voltage higher than its POR threshold for 16 switching cycles; therefore, there is 176 cycles delay from ISHARE falls to 0.7*VCC to the beginning of soft-start.

During shutdown or fault conditions, the soft-start is reset quickly while UGATE and LGATE change states immediately (<100ns) upon the input drop below falling POR. The soft-start initialization circuit is shown in Figure 11.

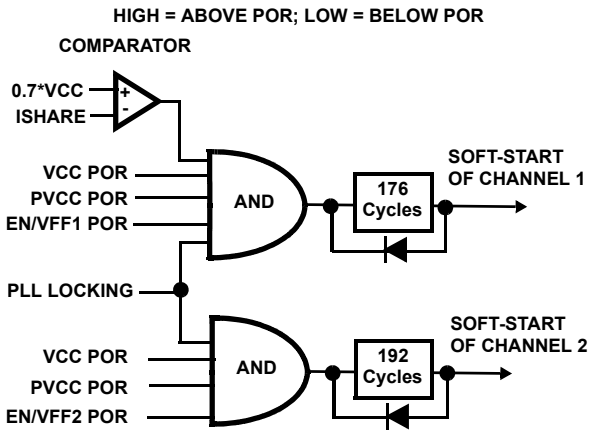


FIGURE 11. SOFT-START INITIALIZATION LOGIC

The EN/VFF pin can be used as a voltage monitor and to set desired hysteresis with an internal 30µA sinking current going through an external resistor divider. The sinking current is disengaged after the system is enabled. This feature is especially designed for applications that require higher input rail POR for better undervoltage protection. For example, in single-phase 12V input applications, R_{UP} = 53.6k and R_{DOWN} = 5.23k will set the turn-on threshold (V_{EN_RTH}) to 10.6V and turn-off threshold (V_{EN_FTH}) to 9V, with 1.6V hysteresis (V_{EN_HYS}).

There is an internal transistor, which will pull down the EN/VFF pin under fault conditions. The multiphase system can immediately turn off all ICs under fault conditions of one or more phases by pulling all EN/VFF pins low. Thus, no bouncing occurs among channels at fault and no single phase could carry all current and be overstressed. The pull-up resistor (R_{UP}) should be scaled to sink no more than 5mA current to the EN/VFF pin. Essentially, the EN/FF pins cannot be directly connected to VCC.

Voltage Feed-forward

Other than used as a voltage monitor described in the previous section, the voltages applied to the EN/VFF pins are also fed to adjust the amplitude of each channel's individual sawtooth. This helps to maintain a constant gain ($G_M = VIN \cdot D_{MAX}/\Delta V_{RAMP}$) contributed by the modulator and the input voltage to achieve optimum loop response over a wide input voltage range. The amplitude of each channel's sawtooth is set to 1.25x the corresponding EN/VFF voltage upon its enable (above 0.8V). The sawtooth ramp offset voltage is 1V, and the peak of the sawtooth is limited to VCC - 1.4V. This allows a maximum peak-to-peak amplitude of sawtooth ramp to be VCC - 2.4V. A constant voltage (0.8V) is fed into the ramp generator to maintain a minimum peak-to-peak ramp.

With VCC = 5.4V, the ramp has an allowable maximum peak-to-peak voltage of 3V and minimum of 1V. Therefore, the feed-forward voltage effective range is typically 3x.

A 192 cycle delay is added after the system reaches its rising POR and prior to the soft-start. The RC timing at the EN/VFF pin should be sufficiently small to ensure that the input bus reaches its static state and the internal ramp circuitry stabilizes before soft-start. A large RC could cause the internal ramp amplitude not to synchronize with the input bus voltage during output start-up or when recovering from faults. It is recommended to use open-drain or open collector to gate this pin for any system delay, as shown in Figure 12.

$$R_{UP} = \frac{V_{EN\_HYS}}{N \times I_{EN\_HYS}} \qquad R_{DOWN} = \frac{R_{UP} \bullet V_{EN\_REF}}{V_{EN\_FTH} - V_{EN\_REF}}$$

where N is number of EN/VFF pins connected together

$$V_{EN\_FTH} = V_{EN\_RTH} - V_{EN\_HYS}$$

$$\Delta V_{RAMP} = \max(V_{CC\_FF} \times G_{RAMP}, VCC - 1.4V - V_{RAMP\_OFFSET})$$

$$V_{CC\_FF} = \max(0.8V, V_{ENFF})$$

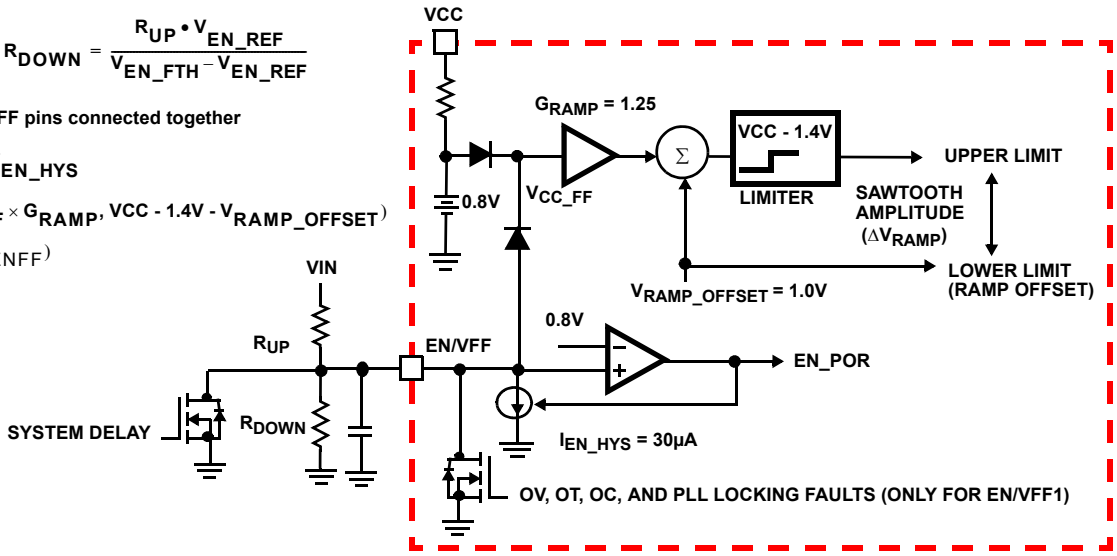


FIGURE 12. SIMPLIFIED ENABLE AND VOLTAGE FEED-FORWARD CIRCUIT

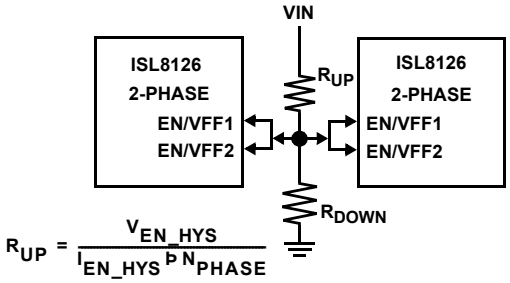


FIGURE 13. TYPICAL 4-PHASE WITH FAULT HANDSHAKE

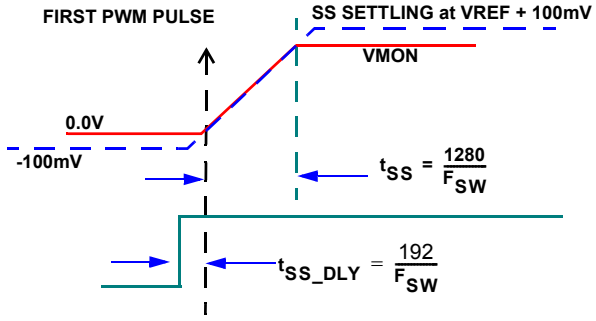


FIGURE 14. SOFT-START WITH VOUT = 0V

Soft-start

The ISL8126 has two independent digital soft-start circuitry with fixed 1280 switching cycles. Refer to Figure 14. The full soft-start time from 0V to the target value can be estimated using Equation 1.

$$t_{SS} = \frac{1280}{f_{SW}} \qquad \text{(EQ. 1)}$$

The ISL8126 has the ability to work under a precharged output (see Figure 15). The output voltage would not be yanked down during precharged start-up. If the precharged output voltage is greater than the final target level but lowered to 120% setpoint, the switching will not start until the FB voltage reduces to the internal soft-start signal or the end of the soft-start is declared (see Figure 16).

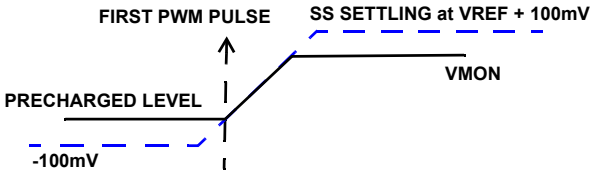


FIGURE 15. SOFT-START WITH OUTPUT PRE-CHAREGED LEVEL < FINAL TARGET LEVEL

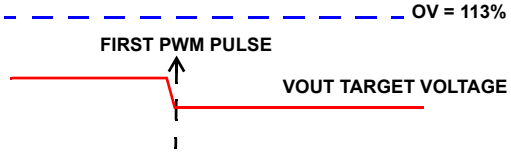


FIGURE 16. SOFT-START WITH VOUT BELOW 0V BUT ABOVE FINAL TARGET VOLTAGE

Power-Good

Both channels share the same PGOOD output. Either of the channels indicating out-of-regulation will pull down the PGOOD pin. The Power-Good comparators monitor the voltages on the VMON pins. The trip points are shown in Figure 17. States of both EN/VFF1 and EN/VFF2 have impact on the PGOOD signal. If one of the VMON pins' voltage is out of the threshold window, PGOOD will not pull low until the fault presents for three consecutive clock cycles.

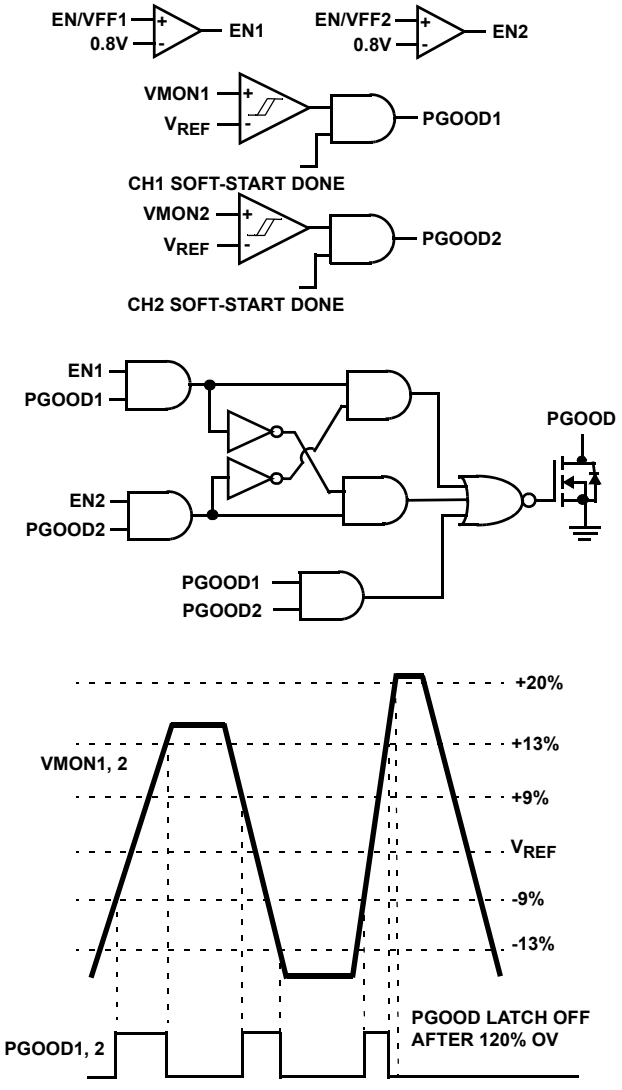


FIGURE 17. POWER-GOOD THRESHOLD WINDOW

Overvoltage and Undervoltage Protection

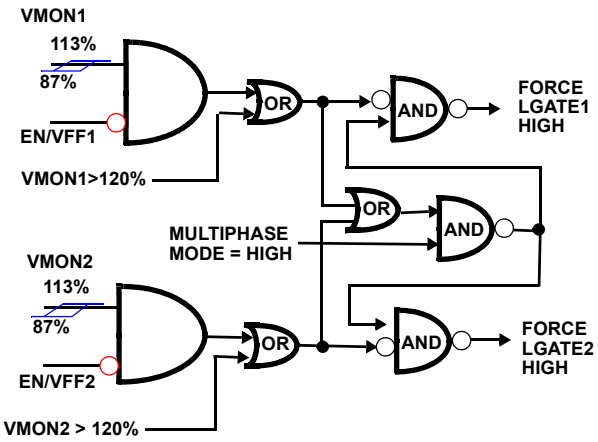


FIGURE 18. FORCE LGATE HIGH LOGIC

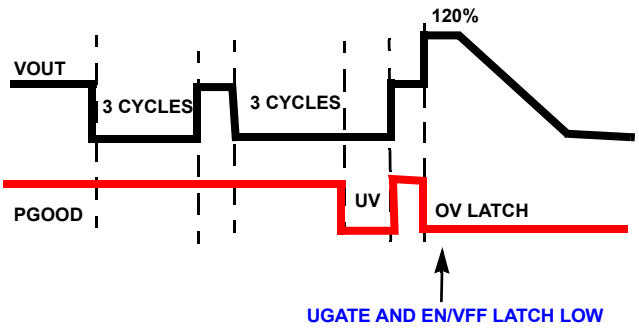


FIGURE 19. PGOOD TIMING UNDER UV AND OV

The Overvoltage (OV) and Undervoltage (UV) protection circuitry monitor the voltage on the VMON pins.

OV protection is active upon VCC POR. An OV condition (>120%) would latch IC off (the high-side MOSFET to latch off permanently; the low-side MOSFET turns on immediately at the time of OV trip and then turns off after the VMON drops below 87%). The EN/VFF and PGOOD are also latched low at OV event. The latch condition can be reset only by recycling VCC. In Dual/DDR mode, each channel is responsible for its own OV event with the corresponding VMON as the monitor. In multiphase mode, both channels respond simultaneously when either triggers an OV event.

There is another non-latch OV protection (113% of target level). At the condition of EN/VFF low and the output over 113% OV, the lower side MOSFET will turn on until the output drops below 87%. This is to protect the overall power trains in case of only one channel of a multiphase system detecting OV. The low-side MOSFET always turns on at the conditions of EN/VFF = LOW and the output voltage above 113% (all VMON pins and EN/VFF pins are tied together) and turns off after the output drops below 87%. Thus, in a high phase count application (Multiphase Mode), all cascaded ICs can latch off simultaneously via the EN/VFF pins (EN/VFF pins are tied together in multiphase mode), and each IC shares the same sink current to reduce the stress and eliminate the bouncing among phases.

The UV functionality is not enabled until the end of soft-start. In a UV event, if the output drops below -13% of the target level due to

some reason (cases when EN/VFF is not pulled low) other than OV, OC, OT, and PLL faults, the lower MOSFETs will be turned on for ~345ns for each switching cycle to avoid high negative voltage ringing until the UN condition is removed.

PRE-POR Overvoltage Protection (PRE-POR-OVP)

When both the VCC and PVCC are below PORs (not including EN POR), the UGATE is low and LGATE is floating (high impedance). EN/VFF has no control on LGATE when VCC and PVCC are below their PORs. When VCC and PVCC are above their PORs, the LGATE would not be floating but toggling with its PWM pulses. An internal 10kΩ resistor, connected in between PHASE and LGATE nodes, implements the PRE-POR-OVP circuit. The output of the converter that is equal to phase node voltage via output inductors is then effectively clamped to the low-side MOSFET's gate threshold voltage, which provides some protection to the load if the upper MOSFET(s) is shorted during start-up, shutdown, or normal operations. For complete protection, the low-side MOSFET should have a gate threshold that is much smaller than the maximum voltage rating of the load.

The PRE-POR-OVP works against prebiased start-up when precharged output voltage is higher than the threshold of the low-side MOSFET, however, it can be disabled by placing a resistor from LGATE to ground. The resistor value can be estimated from Equation 2.

$$R < \frac{10k}{\frac{V_{pre-biased(max)}}{V_{th(min)}} - 1} \quad \text{(EQ. 2)}$$

The resistor value should be as large as possible to minimize power dissipation, while providing sufficient margin for the internal 10kΩ and MOSFET's Vth tolerances. For example, a 2kΩ resistor is recommended for applications using logic-level MOSFET with the maximum prebiased voltage less than 5V.

Over-Temperature Protection (OTP)

When the junction temperature of the IC is greater than +150°C (typically), both EN/VFF pins pull low to inform other cascaded channels via their EN/VFF pins. All connected EN/VFFs stay low and release after the IC's junction temperature drops below +125°C (typically), with a +25°C hysteresis (typical).

INDUCTOR CURRENT SENSING

The ISL8126 supports inductor DCR sensing, MOSFET's $r_{DS(ON)}$ sensing, or resistive sensing techniques. The circuits shown in Figures 20, 21, and 22 represent one channel of the controller. This circuitry is identical for both channels.

Note that the common mode input voltage range of the current sense amplifiers is VCC - 1.8V. Therefore, the $r_{DS(ON)}$ sensing must be used for applications with output voltage greater than VCC - 1.8V. For example, when VCC = 5.4V, the inductor DCR and the resistive sensing configurations can be used for output voltage less than 3V. For higher output voltage, $r_{DS(ON)}$ sensing configuration must be used.

INDUCTOR DCR SENSING

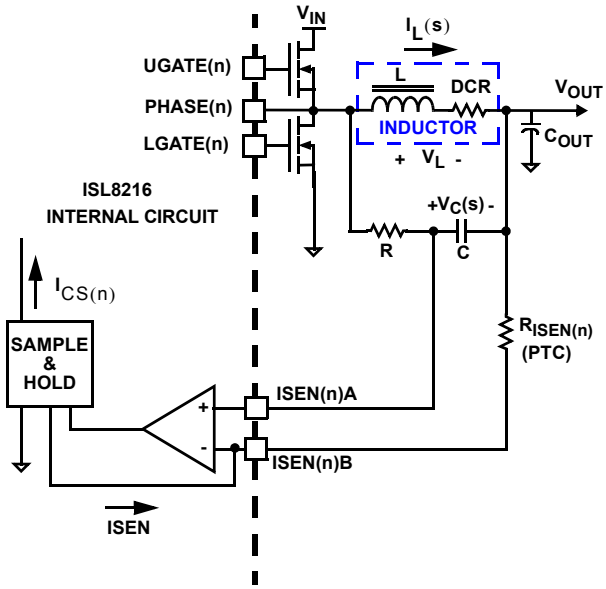


FIGURE 20. DCR SENSING CONFIGURATION

An inductor's winding is characteristic of a distributed resistance as measured by the DCR (Direct Current Resistance) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 20. The inductor current, I_L; will also pass through the DCR. Equation 3 shows the s-domain equivalent voltage across the inductor V_L.

$$V_L = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 3)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 20. The voltage on the capacitor V_C, can be shown to be proportional to the inductor current I_L, see Equation 4.

$$V_C = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 4)}$$

If the R-C network components are selected such that the RC time constant (= R*C) matches the inductor time constant (= L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR, i.e. proportional to the inductor current. The value of R should be as small as feasible for best signal-to-noise ratio. Make sure the resistor package size is appropriate for the power dissipated and include this loss in efficiency calculations. In calculating the minimum value of R, the average voltage across C (which is the average $I_L DCR$ product) is small and can be neglected. Therefore, the minimum value of R may be approximated using Equation 5.

$$R_{min} = \frac{D \cdot (V_{IN-max} - V_{OUT})^2 + (1 - D) \cdot V_{OUT}^2}{k \cdot P_{R-pkg} \cdot \delta_P} \quad \text{(EQ. 5)}$$

Where $P_{R\text{-}pkg}$ is the maximum power dissipation specification for the resistor package and δ_P is the derating factor for the same parameter (eg.: $P_{R\text{-}pkg}$ = 0.063W for 0402 package, δ_P = 80% at +85°C). k is the margin factor, also to limit

temperature raise in the resistor package, recommend using 0.4. Once R_{min} has been calculated, solve for the maximum value of C using Equation 6:

$$C_{max} = \frac{L}{R_{min} \cdot DCR} \quad \text{(EQ. 6)}$$

and choose the next-lowest readily available value. Then substitute the chosen value into the same equation and recalculate the value of R. Choose the 1% resistor standard value closest to this recalculated value of R. For example, when V_{IN_MAX} = 14.4V, V_{OUT} = 2.5V, L = 1µH and DCR = 1.5mΩ, with 0402 package Equation 5 yields R_{MIN} of 1476Ω and Equation 6 yields C_{MAX} of 0.45µF. By choosing 0.39µF and recalculating the resistor it yields 1.69kΩ.

With the internal low-offset current amplifier, the capacitor voltage V_C is replicated across the sense resistor R_{ISEN}. Therefore, the current out of ISEN(n)B pin, I_{SEN}, is proportional to the inductor current. After 175ns blanking period with respect to the falling edge of the PWM pulse of each channel, the I_{SEN} current is filtered and sampled for 175ns. The sampling current I_{CS} then can be derived as shown by Equation 7:

$$ICS = \frac{\left(I_L + \frac{V_{OUT}}{L} \bullet \left(\frac{1-D}{2f_{SW}} - t_{MIN\_OFF}\right)\right) \bullet DCR}{R_{ISEN}} \quad \text{(EQ. 7)}$$

Where I_L is the inductor DC current, f_{SW} is the switching frequency, and t_{MIN_OFF} is 350ns.

RESISTIVE SENSING

For accurate current sense, a dedicated current-sense resistor RSENSE in series with the output inductor can serve as the current sense element (see Figure 21). This technique is more accurate, but reduces overall converter efficiency due to the additional power loss on the current sense element RSENSE.

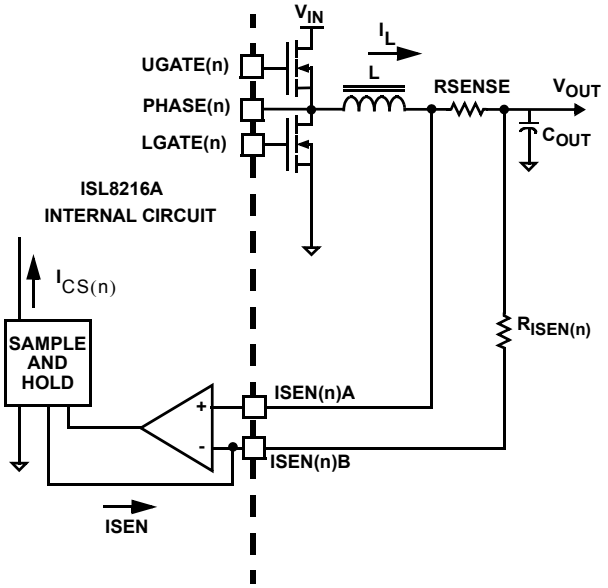


FIGURE 21. SENSE RESISTOR IN SERIES WITH INDUCTOR

Equation 8 shows the sampling current, I_{CS}, when using sensing resistor.

$$ICS = \frac{\left(IL + \frac{V_{OUT}}{L} \bullet \left(\frac{1-D}{2F_{SW}} - t_{MIN\_OFF}\right)\right) \bullet RSENSE}{R_{ISEN}} \quad \text{(EQ. 8)}$$

Similar to DCR current sensing approach, the resistive sensing approach can be used with output voltage less than VCC - 1.8V.

MOSFET $r_{DS(ON)}$ SENSING

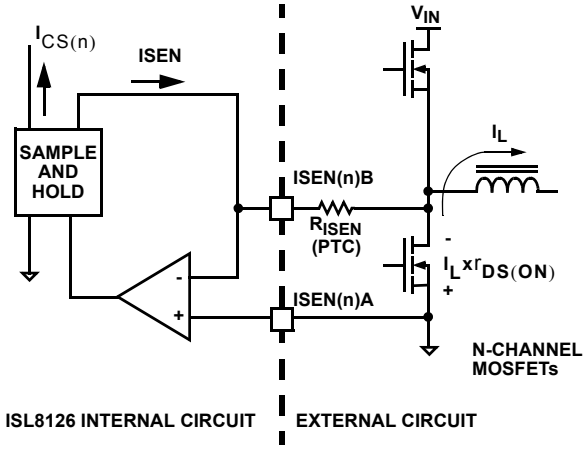


FIGURE 22. MOSFET $r_{DS(ON)}$ CURRENT-SENSING CIRCUIT

The controller can also sense the channel load current by sampling the voltage across the synchronous MOSFET $r_{DS(ON)}$ (see Figure 22). The amplifier is ground-reference by connecting the ISEN(n)A pin to the source of the synchronous MOSFET. ISEN(n)B pin is connected to the synchronous MOSFET'S drain through the current sense resistor R_{ISEN}. The voltage across R_{ISEN} is equivalent to the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET while it is conducting. The resulting current out of the ISEN(n)B pin is proportional to the channel current I_L.

Equation 9 shows the sampling current, I_{CS}, when using MOSFET $r_{DS(ON)}$ sensing.

$$I_{CS} = \frac{\left(I_L + \frac{V_{OUT}}{L} \bullet \left(\frac{1-D}{2F_{SW}} - t_{MIN\_OFF}\right)\right) \bullet r_{DS(ON)}}{R_{ISEN}} \quad \text{(EQ. 9)}$$

Both inductor DCR and MOSFET $r_{DS(ON)}$ value will increase as the temperature increases. Therefore, the sensed current will increase as the temperature of the current sense element increases. In order to compensate the temperature effect on the sensed current signal, a Positive Temperature Coefficient (PTC) resistor can be selected for the sense resistor R_{ISEN}.

Overcurrent Protection

For overload and hard short condition, the overcurrent protection reduces the regulator RMS output current much less than full load by putting the controller into hiccup mode. A delay time, equal to 3 soft-start intervals, is inserted to allow the disturbance to be cleared out. After the delay time, the controller then initiates a soft-start interval. If the output voltage comes up and returns to the regulation, PGOOD transitions high. If the OC trip is

exceeded during the soft-start interval, the controller pulls EN/VFF low again. The PGOOD signal will remain low and the soft-start interval will be allowed to expire. Another soft-start interval will be initiated after the delay interval. If an overcurrent trip occurs again, this same cycle repeats until the fault is removed.

The OCP function is enabled at start-up. The ISL8126 monitors 2 signals: sampled channel current, ICS, and ISHARE voltage for overcurrent protection.

CHANNEL CURRENT OCP

Each sampled channel current, I_{CS}, is compared to 111µA (typ.) for the OCP trip point. The channel overcurrent trip point can be set by using R_{ISEN} value such that the overcurrent trip point corresponds to the channel sensing current, ICS, of 111µA. For DCR current sensing, Equation 7, and $r_{DS(ON)}$ current sensing, Equation 9, the R_{ISEN} can be estimated from Equations 10 and 11, respectively.

$$R_{ISEN} = \frac{\left(IOC + \frac{V_{OUT}}{L} \bullet \left(\frac{1-D}{2F_{SW}} - t_{MIN\_OFF}\right)\right) \bullet DCR}{111\mu A} \quad \text{(EQ. 10)}$$

$$R_{ISEN} = \frac{\left(IOC + \frac{V_{OUT}}{L} \bullet \left(\frac{1-D}{2F_{SW}} - t_{MIN\_OFF}\right)\right) \bullet r_{DS(ON)}}{111\mu A} \quad \text{(EQ. 11)}$$

Without temperature compensation, the OCP trip point should be evaluated based on the DCR or MOSFET $r_{DS(ON)}$ values at the maximum device's temperature.

While configured as multiphase operation (VSEN2- > VCC - 400mV), the channel OCP has 7 clock cycles delay before entering hiccup mode.

In dual-output operation, the 7-clock cycle delay on Channel 2 is bypassed so the circuit responds to over current condition immediately. In this mode, the 7-clock cycle delay in Channel1 is still active. The fast OCP response on Channel1 will be rely on the OCP on ISHARE pin where the voltage on this pin represents the Channel1 current.

During soft-start period with VMON1 less than 0.4V, the OCP threshold on the sampled channel current, ICS, of both channels are increased to 222µA (typ.) to compensate the in-rush current.

ISHARE OCP

Refer to the "Controller Block Diagram" on page 6, ISHARE pin sources out a current IAVG_CS with 15µA offset. In the 2-phase mode, IAVG_CS is the average of both Channels 1 and 2 sampled currents as calculated in Equation 12.

$$IAVG\_CS = \frac{ICS1 + ICS2}{2} \quad \text{(EQ. 12)}$$

While in the dual-output mode, IAVG_CS is a copy of Channel1's sampled current.

In multiphase operation, the VISHARE represents the average current of all ISL8126 and compares with the ISHARE pin precision 1.2V threshold to determine the overcurrent condition. At the same time, each channel has an additional overcurrent trip point at 111µA with 7-cycle delay for channel overcurrent protection. This scheme helps protect against loss of channel(s) in multiphase mode so that no single channel could carry excessive current in such event. With R_{ISHARE} = 10kΩ, It would make the channel current OCP and ISHARE OCP trip at the same over current level; (111µA + 15µA) x 10kΩ = 1.26V.

Note that it is not necessary for the R_{ISHARE} to be scaled to trip at the same level as the 111µA OCP comparator if the application allows. For instance, when Channel 1 operates independently, the OC trip set by 1.2V comparator can be lower than 111µA trip point.

To set the ISHARE OCP in the multiphase configuration, the R_{ISEN} must be determined first by using Equations 10 or 11. The IOC is the overcurrent for each phase, which is approximately IOC_total/number of phases. Upon determining R_{ISET}, Equations 7, 8, 9, and 11 can be used to determine ISHARE OCP, as shown in Equation 13.

$$R_{ISHARE} = \frac{1.2V}{N_{CNTL}} \cdot \sum_{i=1} (I_{AVG\_CS} + 15\mu A)_i \quad \text{(EQ. 13)}$$

$$R_{ISET} = R_{ISHARE} \cdot N_{CNTL}$$

where N_{CNTL} is the number of the ISL8126 controllers in parallel or multiphase operations.

For the R_{ISEN} chosen for OCP setting, the final value is usually higher than the number calculated from Equation 9. The PCB and inductor pad soldering resistance would affect the total impedance a lot especially at low DCR applications.

Current Sharing Loop

When the ISL8126 operates in 2-phase mode (VSEN2- is pulled within VCC - 400mV), the current control loop keeps Channel 1 and Channel 2 currents in balance. The sensed currents from both channels are combined to create an average current reference (IAVG), which represents average current of both channel currents. The signal IAVG is then subtracted from the individual sensed current (ICS1 or ICS2) to produce a current correction signal for each channel. The block diagram of current sharing control circuit is shown in Figure 23.

When both channels operate independently, the average function is disabled, and the current correction block of Channel 2 is also disabled. The I_{AVG_CS} is Channel 1 sensed current I_{CS1}. Channel 1 makes any necessary current correction by comparing the voltages at ISET and ISHARE pins (for 3-phase, two ISL8126s configuration).

When the share bus does not connect to other ICs, the ISET and ISHARE pins can be shorted together and grounded via a single resistor to ensure zero share error.

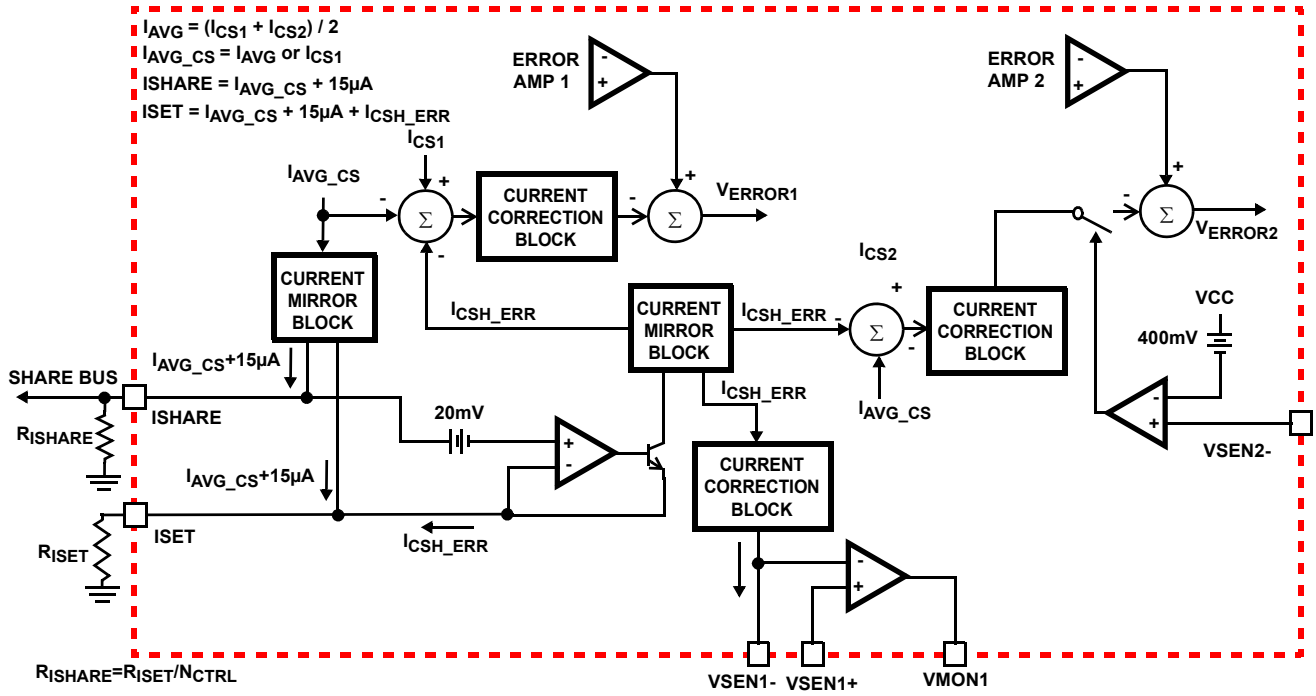


FIGURE 23. SIMPLIFIED CURRENT SHARE AND INTERNAL BALANCE IMPLEMENTATION

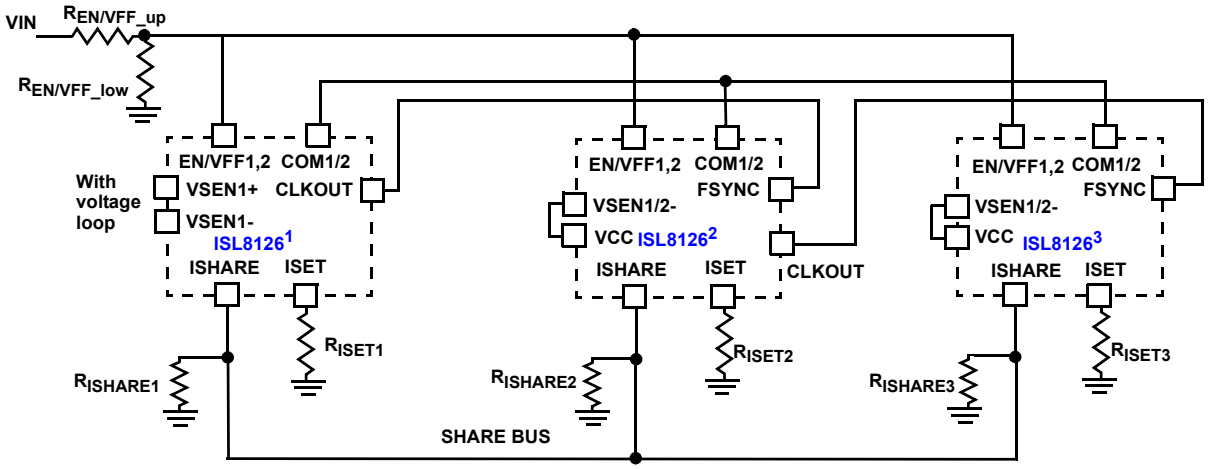
Current Share Control in Multiphase Single Output with Shared COMP Voltage

In multiphase/multi-IC implementation with one single error amplifier for the voltage loop, all COMP pins must be tied together. Therefore, all other channels' error amplifiers that are not used in voltage loop should be disabled with their corresponding VSEN- pulled to VCC, as shown in Figure 24.

For current sharing purposes, all ISHARE pins must also be tied together. The share bus (VISHARE) represents the average current of all ISL8126s connected to the same ISHARE bus. The ISHARE pin sources a copy of the IAVG_CS with 15µA offset (IAVG_CS equals to IAVG or ICS1 depending upon the configuration). The ISET pin sources out a copy of IAVG_CS, ICSH_ERR and 15µA offset. ICSH_ERR on the ISET pin makes the voltage at the ISET pin track the voltage at the ISHARE pin with 20mV offset. Thus, ICSH_ERR represents the difference of an individual ISL8126 current to the average current (ISHARE). The current share error signal (ICSH_ERR) is then fed into the current correction block to adjust each channel's PWM pulse accordingly.

If one single external resistor is used as RISHARE connecting the ISHARE bus to ground for all the ICs in parallel, RISHARE should be set equal to RISET/NCTRL (where NCNTL is the number of the ISL8126 controllers in parallel or multiphase operations), and the share bus voltage (VISHARE) set by the RISHARE, represents the average current of all channels. RISHARE can also be set by putting one resistor in each IC's ISHARE pin and using the same value with RISET (RISHARE = RISET), which results in the total equivalent resistance value as RISET/NCTRL.

The current share function provides at least 10% overall accuracy between ICs, 5% within the IC when using a 1% resistor to sense a 10mV signal. The current share bus works for up to 12-phase.



$R_{ISHARE\_} = R_{ISET\_}$

FIGURE 24. SIMPLIFIED 6-PHASE SINGLE OUTPUT IMPLEMENTATION

Current Share Control Loop in Multi-Module with Independent Voltage Loop

The power module controlled by ISL8126 with its own voltage loop can be paralleled to supply one common output load with its integrated Master-Slave current sharing control, as shown in the "Typical Application Circuits" on page 14. A resistor R_{CSR} and a capacitor C_{CSR} need to be inserted between VSEN1- pin and the lower resistor of the voltage sense resistor divider for each module. With this resistor, the correction current sourcing from the VSEN1- pin will create a voltage offset to maintain even current sharing among modules. The recommended value for the VSEN1- resistor R_{CSR} is 100Ω and it should not be large in order to keep the unity gain amplifier input pin impedance compatibility. The maximum source current from the VSEN1- pin is 350µA, which is combined with R_{CSR} to determine the current sharing regulation range. The generated correction voltage on R_{CSR} is suggested to be within 5% of VREF (0.6V) to avoid fault triggering of UV/OV and PGOOD during dynamic events. The value for C_{CSR} can be estimated from Equation 14.

$$C_{CSR} = \frac{35}{R_{CSR} \times F_{SW}} \quad \text{(EQ. 14)}$$

Where F_{SW} is switching frequency.

It is recommended to have 3 analog signals: CLKOUT-SYNC, ISHARE, and EN/VFF for communication among the paralleled modules. All the modules are synchronized and the phase shift can also be configured to optimal to reduce the input current ripple by interleaving effects. The connections of these three wires allows the system to be started at the same time and achieve good current balance in start-up without overcurrent trip.

Internal Series Linear and Power Dissipation

The VIN pin is connected to PVCC with an internal series linear regulator. The internal linear regulator's input (VIN) can range between 3V to 26.5V. PVCC pin is the output of the internal linear regulator and it provides power for both the internal MOSFET drivers. The PVCC and VIN pins should have the recommended bypass ceramic capacitors (10µF) connected to GND for proper operation. PVCC can be used to bias the IC analog circuitry, VCC, by connecting VCC to PVCC pin. The VCC pin should be connected to the PVCC pin with an RC filter to prevent high frequency driver switching noise into the analog circuitry. When the VIN drops below 5.0V, the pass element will saturate; PVCC will track VIN with a dropout of the linear regulator. When used with an external supply less than 5V, the PVCC pin is recommended to be tied directly to VIN.

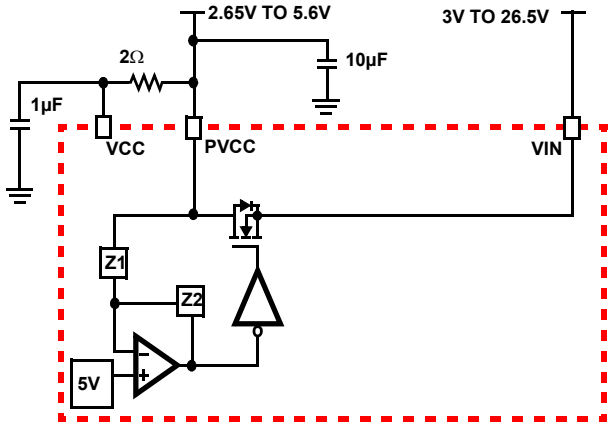


FIGURE 25. INTERNAL REGULATOR IMPLEMENTATION

The LDO is capable of supplying 250mA with regulated 5.4V output. In 3.3V input applications, when the VIN pin voltage is 3V, the LDO can still supply 150mA while maintaining LDO output voltage higher than VCC falling threshold to keep the IC operating. Figure 4 shows the typical V-I curve of the internal LDO. Note that the power dissipation in the device should not be exceeded the package thermal limit. The power dissipation inside the IC can be estimated with Equations 15 and 16.

Where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage ($V_{GS1}$and V_{GS2}) in the corresponding MOSFET datasheet; I_{Q_VIN} is the driver's total quiescent current with no load at drive outputs; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively.

$$P_{IC} = (VIN - PVCC) \cdot I_{VIN} + P_{DR} \quad \text{(EQ. 15)}$$

$$I_{VIN} = \left(\frac{Q_{G1} \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet N_{Q2}}{V_{GS2}}\right) \bullet PVCC \bullet F_{SW} + I_{Q\_VIN}$$

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} \quad \text{(EQ. 16)}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet PVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet PVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$R_{EXT2} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

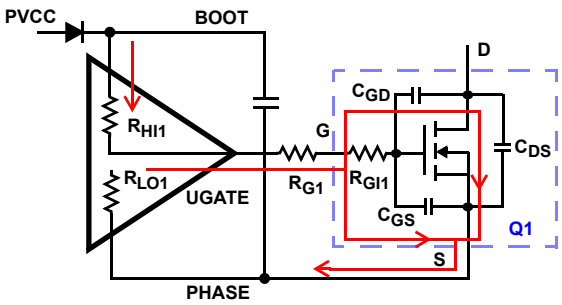


FIGURE 26. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

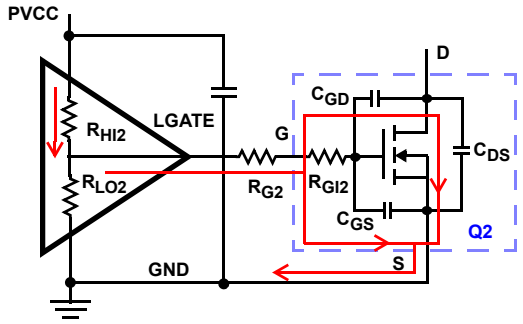


FIGURE 27. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

It is recommended that the operating junction temperature of the IC to be less that +135°C. This limits the maximum power dissipation inside the IC. Equations 15 and 16 and θ_{JA} can be used to estimate the maximum total gate change, Q_{g_total}. The power dissipation inside the IC should be evaluated at the maximum ambient temperature. In addition, the total gate change and the operating switching frequency should not load the internal LDO beyond the current limit threshold. Figure 28 provides the guideline of the allowed maximum gate charge.

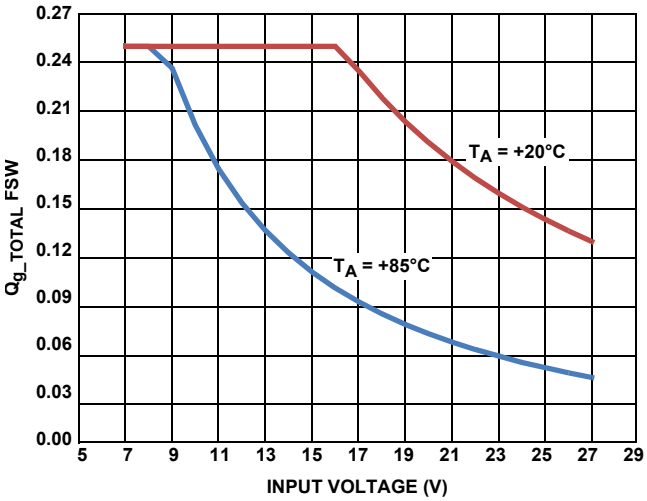


FIGURE 28. ALLOWED MAXIMUM GATE CHARGE vs INPUT VOLTAGE

To keep the IC within its operating temperature range, an external power resistor could be used in series with the VIN pin to bring the heat out of the IC, or and external LDO could be used when necessary.

Oscillator

The Oscillator is a sawtooth waveform, providing for leading edge modulation with 350ns minimum PWM off-time. The oscillator (Sawtooth) waveform has a DC offset of 1.0V. Each channel's peak-to-peak of the ramp amplitude is set proportional to the voltage applied, which is corresponding the EN/VFF pin. See "Voltage Feed-forward" on page 25.

Frequency Synchronization and Phase Lock Loop

The FSYNC pin has two primary capabilities: fixed frequency operation and synchronized frequency operation. By connecting a resistor (R_{FSYNC}) to GND from the FSYNC pin, the switching frequency can be set at any frequency between 150kHz and 1.5MHz. The value of R_{FSYNC} can be estimated using Equation 17. The frequency setting curve shown in Figure 29 is also provided to assist in selecting the correct value for R_{FSYNC}.

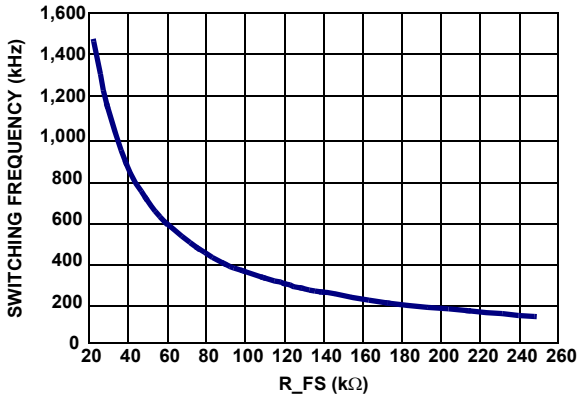


FIGURE 29. R_{FS} vs SWITCHING FREQUENCY

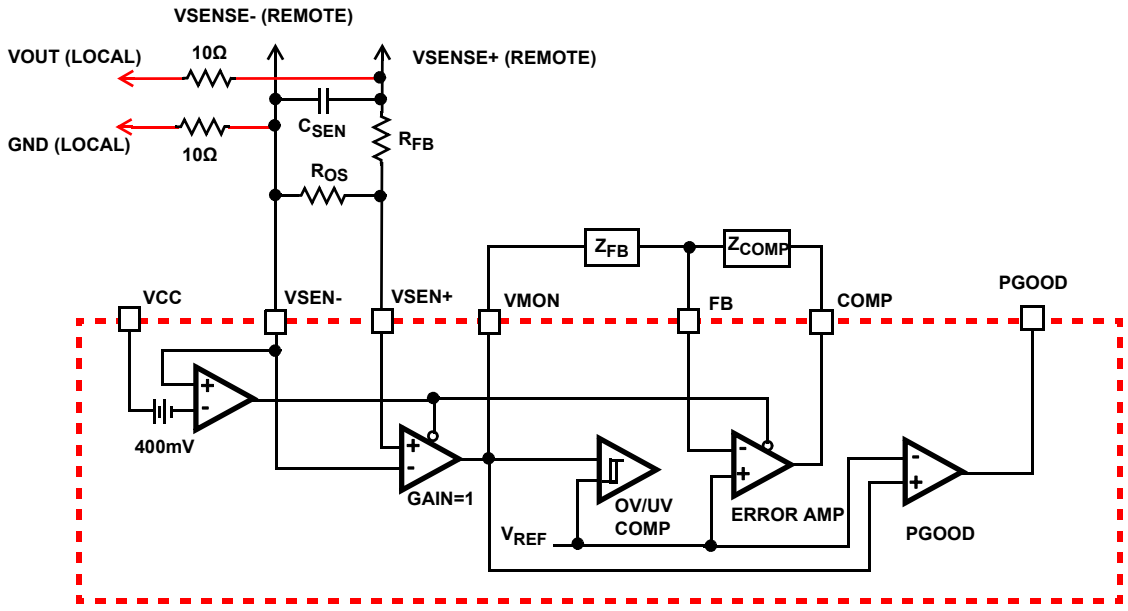


FIGURE 30. SIMPLIFIED REMOTE SENSING IMPLEMENTATION

$$R_{FSYNC}[k\Omega] = 4.671\times10^{4}\cdot f_{SW}[kHz]^{-1.04} \quad \text{(EQ. 17)}$$

By connecting the FSYNC pin to an external square pulse waveform (such as the CLOCK signal, typically 50% duty cycle from another ISL8126), the ISL8126 will synchronize its switching frequency to the fundamental frequency of the input waveform. The maximum voltage to the FSYNC pin is VCC + 0.3V. The Frequency Synchronization feature will synchronize the leading edge of CLKOUT signal with the falling edge of Channel 1's PWM clock signal. The CLKOUT is not available until the PLL locks.

The locking time is typically 130µs for f_{SW} = 500kHz. EN/VFF1 is pulled down internally until the FSYNC stabilized and the PLL is in locking. The PLL circuits control only EN/VFF1, and control the delay time of Channel 2's soft-start. Therefore, it is recommended to connect all EN/VFF pins together in multiphase configuration.

The loss of a synchronization signal for 13 clock cycles causes the IC to be disabled until the PLL returns locking, at which point a soft-start cycle is initiated and normal operation resumes. Holding FSYNC low will disable the IC.

Differential Amplifier for Remote Sensing

The differential remote sense buffers help compensate the droop due to load on the positive and negative rails and maintain the high system accuracy of ±0.6%. They have precision unity gain resistor matching networks, which has a ultra low offset of 1mV.

The output of the remote sense buffer is connected directly to the internal OV/UV comparator. As a result, a resistor divider should be placed on the input of the buffer for proper regulation, as shown in Figure 30. The VMON pin should be connected to the FB pin by a standard feedback network. The output voltage can be set by using Equation 18:

$$V_{OUT} = V_{ref}\cdot\left(1+\frac{R_{FB}}{R_{OS}}\right) \quad \text{(EQ. 18)}$$

To optimize system accuracy, it is highly recommended to include this impedance into calculation and use resistor with resistance as low as possible for the lower leg (R_{OS}) of the feedback resistor divider. Note that any RC filter at the inputs of the differential amplifier will contribute as a pole to the overall loop compensation.

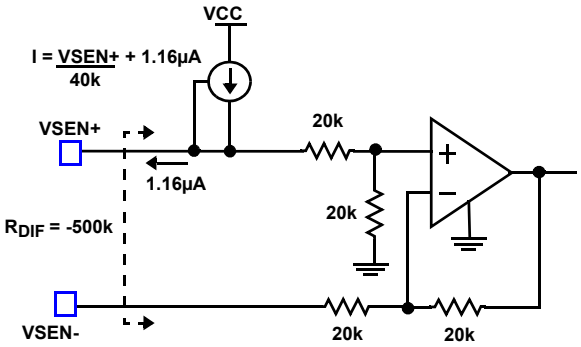


FIGURE 31. EQUIVALENT DIFFERENTIAL AMPLIFIER

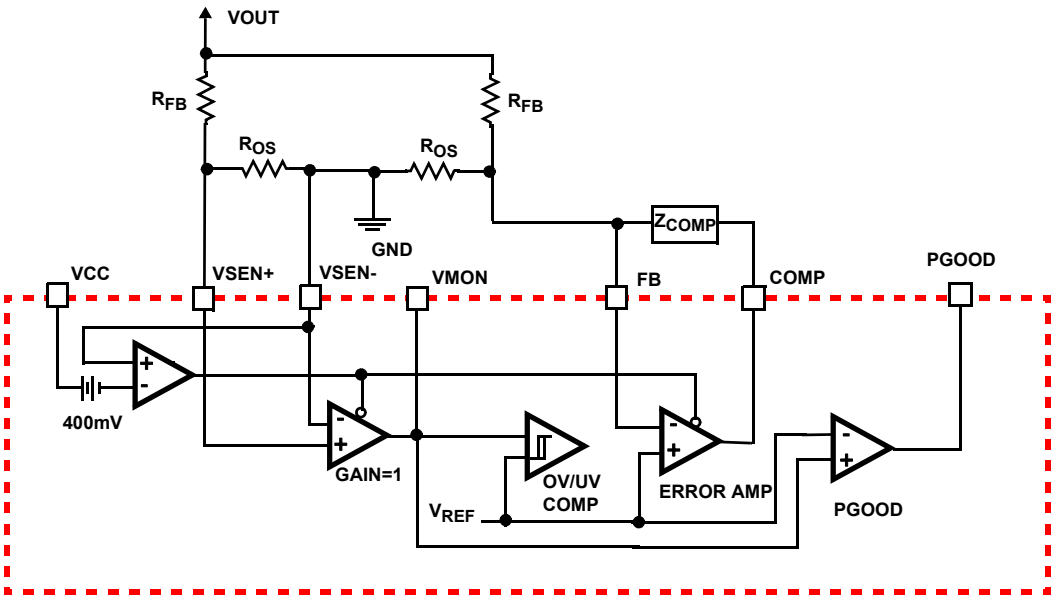


FIGURE 32. DUAL OUTPUT VOLTAGE SENSE FOR SINGLE POINT OF FAILURE PROTECTION

As some applications will not need the differential remote sense, the output of the remote sense buffer can be disabled and be placed in high impedance by pulling VSEN- within 400mV of VCC. Thus, the VMON pin can be used as an additional monitor of the output voltage with a resistor divider to protect the system against single point of failure, which occurs in the system using the same resistor divider for the UV/OV comparator and the output regulation. The resistor divider ratio should be the same as the one for the output regulation so that the correct voltage information is provided to the OV/UV comparator. Figure 32 shows the differential sense amplifier can be directly used as a monitor without pulling VSEN- high.

Internal Reference and System Accuracy

The internal reference is set to 0.6V. Including bandgap variation and offset of differential and error amplifiers, it has an accuracy of ±0.6% over commercial temperature range, and 0.9% over industrial temperature range. While the remote sense is not used, its offset (V_{OS_DA}) should be included in the tolerance calculation. Equations 19 and 20 show the worst case of system accuracy calculation. V_{OS_DA} should set to zero when the differential amplifier is in the loop, the differential amplifier's input impedance (R_{DIF}) is typically -600kΩ with a tolerance of 20% (RDIF%) and can be neglected when R_{OS} is less than 100Ω. To set a precision setpoint, R_{OS} can be scaled by two paralleled resistors.

Figure 33 shows the tolerance of various output voltage regulation for 1%, 0.5%, and 0.1% feedback resistor dividers. Note that the farther the output voltage setpoint away from the internal reference voltage, the larger the tolerance; the lower the resistor tolerance (R%), the tighter the regulation.

$$\%min = (Vref \cdot (1 - Ref\%) - V_{OS\_DA}) \cdot \left(1 + \frac{R_{FB} \cdot (1 - R\%)}{R_{OSMAX}}\right) \quad \text{(EQ. 19)}$$

$$R_{OSMAX} = \frac{1}{\frac{1}{R_{OS} \cdot (1 + R\%)} + \frac{1}{R_{DIF} \cdot (1 + R_{DIF}\%)}}$$

$$\%max = (Vref \cdot (1 - Ref\%) - V_{OS\_DA}) \cdot \left(1 + \frac{R_{FB} \cdot (1 - R\%)}{R_{OSMIN}}\right) \quad \text{(EQ. 20)}$$

$$R_{OSMIN} = \frac{1}{\frac{1}{R_{OS} \cdot (1 - R\%)} + \frac{1}{R_{DIF} \cdot (1 - R_{DIF}\%)}}$$

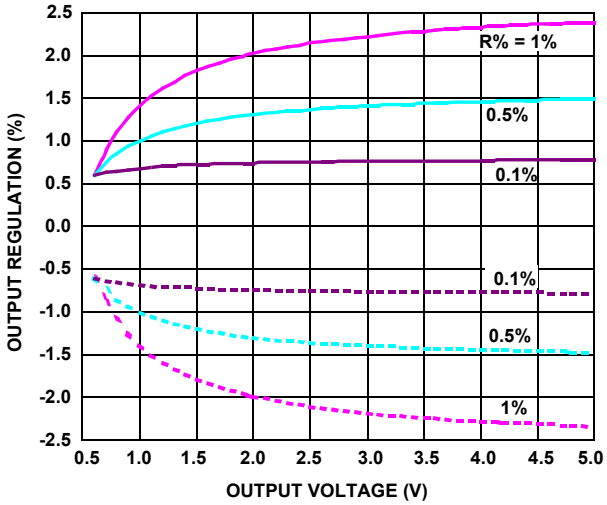


FIGURE 33. OUTPUT REGULATION WITH DIFFERENT RESISTOR TOLERANCE FOR Ref% = ±0.6%

DDR and Dual Mode Operation

When ISL8126 is used in dual-output mode, the CLKOUT/REFIN pin is an input signal pin. If the CLKOUT/REFIN is less than 29% of VCC, an external soft-start ramp (0.6V) can be in parallel with Channel 2s internal soft-start ramp for DDR/tracking applications (DDR Mode).

The output voltage (typical VTT output) of Channel 2 tracks with the input voltage (typical VDDQ*(1+k) from Channel 1) at the CLKOUT/REFIN pin. As for the external input signal and internal reference signal (ramp and 0.6V), the one with the lowest voltage will be the one to be used as the reference compared with the FB signal. So in DDR configuration, VTT channel should start-up later after its internal soft-start ramp, in which way, the VTT will track the voltage on REFIN pin derived from VDDQ. This can be achieved by adding more filtering at EN/VFF1 compared with EN/VFF2.

Since the UV/OV comparator uses the same internal reference 0.6V to guarantee UV/OV and Precharged start-up functions of Channel 2, the target voltage derived from Channel 1 (VDDQ) should be scaled close to 0.6V, and it is suggested to be slightly above (+2%) 0.6V with an external resistor divider, which will have Channel 2 use the internal 0.6V reference after soft-start. Any capacitive load at the REFIN pin should not slow down the ramping of this input 150mV lower than the Channel 2's internal ramp. Otherwise, the UV protection could be fault triggered prior to the end of the soft-start. The start-up of Channel 2 can be delayed to avoid such a situation from happening, if high capacitive load presents at REFIN pin for noise decoupling. During shutdown, Channel 2 will follow Channel 1 until both channels drops below 87%, at which point both channels enter UV protection zone. Depending on the loading, Channel 1 might drop faster than Channel 2. To solve this race condition, Channel 2 can either power up from Channel 1 or bridge the Channel 1 output with a high current Schottky diode. If the system requires to shutdown both channels when either has a fault, tying EN/VFF1 and EN/VFF2 will do the job. In DDR mode, Channel 1 delays 60° over Channel 2.

In Dual mode, depending upon the resistor divider level of REFIN from VCC, the ISL8126 operates as a dual-PWM controller for two independent regulators with a phase shift, as shown in Table 2. The phase shift is latched as VCC raises above POR and cannot be changed on the fly.

TABLE 2.

MODE	DECODING REFIN RANGE	PHASE FOR CHANNEL 2 WRT CHANNEL 1	REQUIRED REFIN
DDR	<29% of VCC	-60°	0.6V
Dual	29% to 45% of VCC	0°	37% VCC
Dual	45% to 62% of VCC	90°	53% VCC
Dual	62% to VCC	180°	VCC

Layout Considerations

MOSFETs switch very fast and efficiently. The speed at which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component selection, layout, and placement

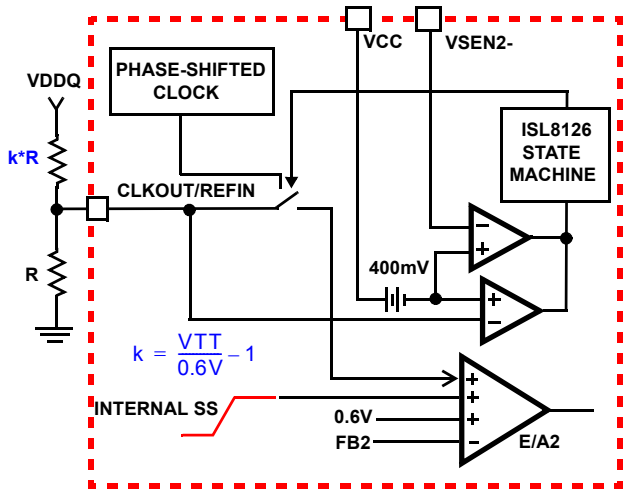


FIGURE 34. SIMPLIFIED DDR IMPLEMENTATION

minimizes these voltage spikes. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET was carrying current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using a ISL8126 controller. The power components are the most critical because they switch large amounts of energy. Next, are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first, which include the MOSFETs, input and output capacitors, and the inductors. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each. Symmetrical layout allows heat to be dissipated equally across all power trains. Equidistant placement of the controller to the power trains (it controls through the integrated drivers), helps keep the gate drive traces equally short, resulting in equal trace impedances and similar drive capability of all sets of MOSFETs.

When placing the MOSFETs, try to keep the source of the upper FETs and the drain of the lower FETs as close as thermally possible. Input high-frequency capacitors, C_{HF}, should be placed close to the drain of the upper FETs and the source of the lower FETs. Input bulk capacitors, C_{BULK}, case size typically limits following the same rule as the high-frequency input capacitors. Place the input bulk capacitors as close to the drain of the upper FETs as possible and minimize the distance to the source of the lower FETs.

Locate the output inductors and output capacitors between the MOSFETs and the load. The high-frequency output decoupling capacitors (ceramic) should be placed as close as practicable to the decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND next or on the capacitor solder pad.

The critical small components include the bypass capacitors (C_{FILTER}) for VCC and PVCC, and many of the components surrounding the controller including the feedback network and current sense components. Locate the VCC/PVCC bypass capacitors as close to the ISL8126 as possible. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up.

A multilayer printed circuit board is recommended. Dedicate one solid layer, usually the one underneath the component side of the board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to output inductors short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

Routing UGATE, LGATE and PHASE Traces

Great attention should be paid to routing the UGATE, LGATE, and PHASE traces since they drive the power train MOSFETs using short, high current pulses. It is important to size them as large and as short as possible to reduce their overall impedance and inductance. They should be sized to carry at least one ampere of current (0.02” to 0.05”). Going between layers with vias should also be avoided, but if so, use two vias for interconnection when possible.

Extra care should be given to the LGATE traces in particular since keeping their impedance and inductance low helps to significantly reduce the possibility of shoot-through. It is also important to route each channels UGATE and PHASE traces in as close proximity as possible to reduce their inductances.

Current Sense Component Placement and Trace Routing

One of the most critical aspects of the ISL8126 regulator layout is the placement of the inductor DCR current sense components and traces. The R-C current sense components must be placed as close to their respective ISENA and ISENB pins on the ISL8126 as possible.

The sense traces that connect the R-C sense components to each side of the output inductors should be routed away from the noisy switching components. These traces should be routed side by side, and they should be very thin traces. It is important to route these traces as far away from any other noisy traces or planes as possible. These traces should pick up as little noise as possible. These traces should also originate from the geometric center of the inductor pin pads and that location should be the single point of contact the trace makes with its respective net.

General PowerPAD Design Considerations

The following is an example of how to use vias to remove heat from the IC.

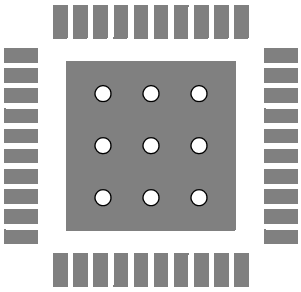


FIGURE 35. PCB VIA PATTERN

It is recommended to fill the thermal pad area with vias. A typical via array fills the thermal pad foot print such that their centers are 3x the radius apart from each other. Keep the vias small but not so small that their inside diameter prevents solder wicking through during reflow.

Connect all vias to the ground plane. It is important the vias have a low thermal resistance for efficient heat transfer. It is important to have a complete connection of the plated-through hole to each plane.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
January 29, 2015	FN7892.2	Removed mention of ISL8126A and Table of key differences on page 1. Added regulator graphics on page 1. Updated Products verbiage to About Intersil verbiage.
May 10, 2012	FN7892.1	“Multiple Power Modules in Parallel with Current Sharing Control” on page 14. Changed the CLKOUT/REFIN pin to FSYNC pin with resistor to GND. Figure 17 on page 27. Changed the OR gate (PGOOD1 and PGOOD2 as input) to AND gate.
September 7, 2011	FN7892.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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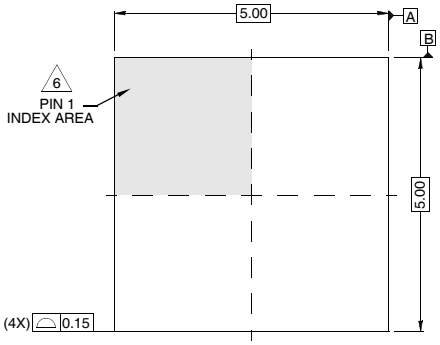
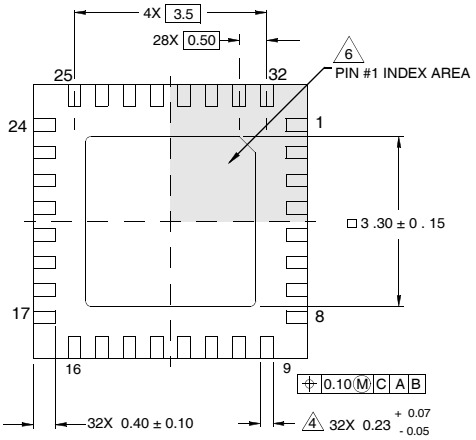
Package Outline Drawing

L32.5x5B

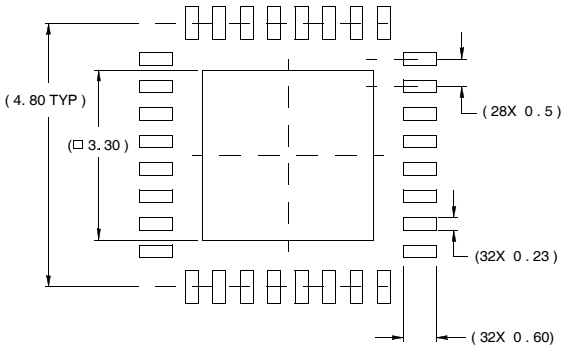
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 5/10



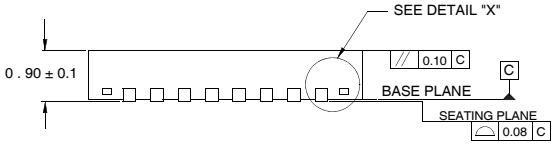
TOP VIEW



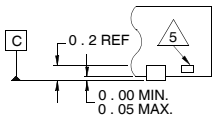
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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