WINSOURCE ELECTRONICS

THE DATASHEET OF

ISL85001IRZ

ISL85001

1A Standard Buck PWM Regulator

FN6769
Rev.3.00
Apr 14, 2017

The ISL85001 is a high-performance, simple output controller that provides a single, high frequency power solution for a variety of point-of-load applications. The ISL85001 integrates a 1A standard buck PWM controller and switching MOSFET.

The PWM controller in the ISL85001 drives an internal switching N-channel power MOSFET and requires an external Schottky diode to generate an output voltage from 0.6V to 19V. The integrated power switch is optimized for excellent thermal performance for up to 1A of output current. The standard buck input voltage range supports a fixed 5V or variable 5.5V to 25V range. The PWM regulator switches at a fixed frequency of 500kHz and utilizes simple voltage mode control with input voltage feed-forward to provide flexibility in component selection and minimize solution size. Protection features include overcurrent, undervoltage and thermal overload protection integrated into the IC. The ISL85001 power-good signal output indicates loss of regulation on the PWM output.

ISL85001 is available in a small 4mmx3mm Dual Flat No-Lead (DFN) package.

Related Literature

- For a full list of related documents, visit our website
  - ISL85001 product page

Features

- Standard buck controller with integrated switching power MOSFET
- Integrated boot diode
- Input voltage range
  - Fixed 5V ±10%
  - Variable 5.5V to 25V
- PWM output voltage adjustable from 0.6V to 19V with continuous output current up to 1A
- ±1% VFB tolerance
- Voltage mode control with voltage feed-forward
- Fixed 500kHz switching frequency
- Externally adjustable soft-start time
- Output undervoltage protection
- Enable inputs
- PGOOD output
- Overcurrent protection
- Thermal overload protection
- Internal 5V LDO regulator
- Pb-free (RoHS compliant)

Applications

- General purpose
- WLAN Cards-PCMCIA, Cardbus32, MiniPCI cards-compact flash cards
- Hand-held instruments
- LCD panel
- Set-top box

Typical Application Schematic

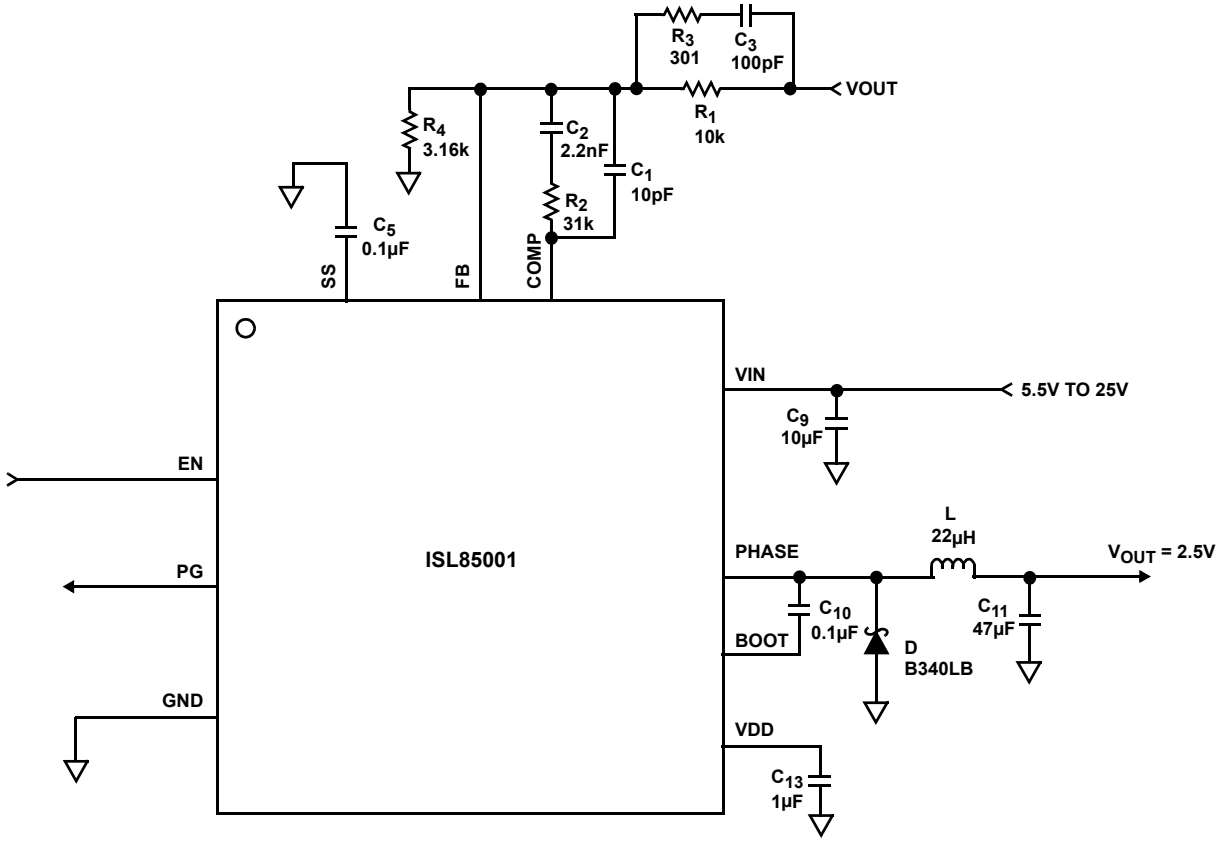


FIGURE 1. V_{IN} RANGE FROM 5.5V TO 25V

Functional Block Diagram

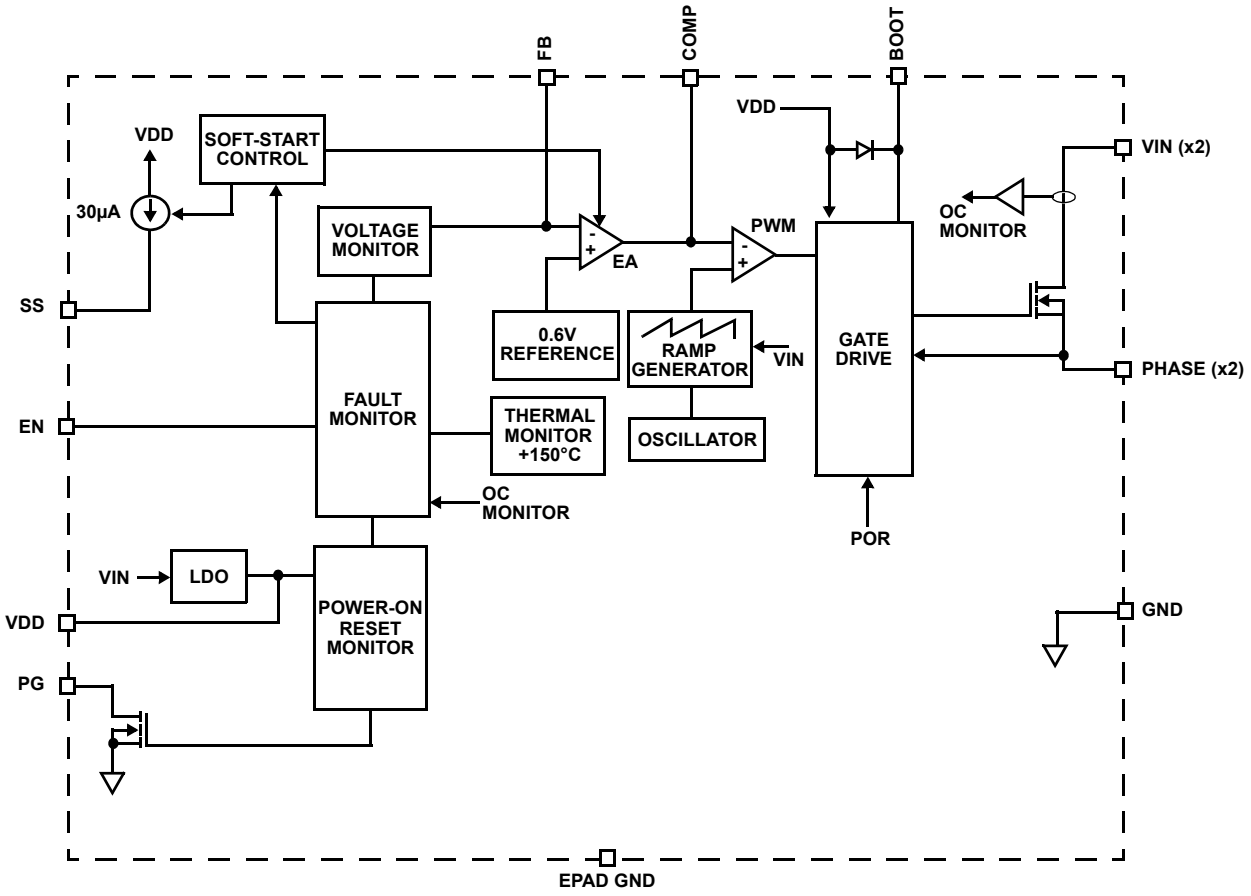
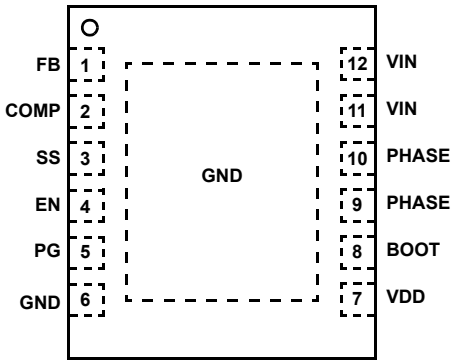


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

Pin Configuration

ISL85001
(12 LD 4x3 DFN)
TOP VIEW



Pin Descriptions

SYMBOL	PIN NUMBER	DESCRIPTION
FB	1	The standard buck regulator employs a single voltage control loop. FB is the negative input to the voltage loop error amplifier. COMP is the output of the error amplifier. The output voltage is set by an external resistor divider connected to FB. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. Connecting an AC network across COMP and FB provides loop compensation to the amplifier. In addition, the PWM regulator power-good and undervoltage protection circuitry use FB to monitor the regulator output voltage.
COMP	2	
SS	3	Program pin for soft-start duration. A regulated 30µA pull-up current source charges a capacitor connected from the pin to GND. The output voltage of the converter follows the ramping voltage on the SS pin.
EN	4	PWM controller enable input. The PWM converter output is held off when the pin is pulled to ground. When the voltage on this pin rises above 1.7V, the chip is enabled.
PG	5	PWM converter power-good output. Open drain logic output that is pulled to ground when the output voltage is outside regulation limits. Connect a 100kΩ resistor from this pin to VDD. Pin is low when the buck regulator output voltage is not within 10% of the respective nominal voltage, or during the soft-start interval. Pin is high impedance when the output is within regulation.
GND	6	Ground connect for the IC and thermal relief for the package. The exposed pad must be connected to GND and soldered to the PCB. All voltage levels are measured with respect to this pin.
VDD	7	Internal 5V linear regulator output provides bias to all the internal control logic. The ISL85001 may be powered directly from a 5V (±10%) supply at this pin. When used as a 5V supply input, this pin must be externally connected to VIN. The VDD pin must always be decoupled to GND with a ceramic bypass capacitor (minimum 1µF) located close to the pin.
BOOT	8	Floating bootstrap supply pin for the power MOSFET gate driver. The bootstrap capacitor provides the necessary charge to turn and hold on the internal N-channel MOSFET. Connect an external capacitor from this pin to PHASE.
PHASE	9, 10	Switch node connections to internal power MOSFET source, external output inductor and external diode cathode.
VIN	11, 12	The input supply for the PWM regulator power stage and the source for the internal linear regulator that provides bias for the IC. Place a ceramic capacitor from VIN to GND, close to the IC for decoupling (typical 10µF).

TABLE 1. INPUT SUPPLY CONFIGURATION

INPUT	PIN CONFIGURATION
5.5V to 25V	Connect the input supply to the VIN pin only. The VDD pin will provide a 5V output from the internal linear regulator.
5V ±10%	Connect the input supply to the VIN and VDD pins.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL85001IRZ	501Z	-40 to +85	12 Ld DFN	L12.4x3
ISL85001EVAL1Z	Evaluation Board			

NOTES:

1. Add “-T” suffix for 6k unit tape and reel option. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL85001. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings

VIN . . . . . -0.3V to 26V
BOOT to GND . . . . . -0.3V to 33V
BOOT to PHASE . . . . . -0.03V to 6V
VDD, FB, EN, COMP, PG, SS . . . . . -0.3V to 6V

Recommended Operating Conditions

VIN Supply Voltage Range . . . . . 4.5V to 25V
Load Current Range . . . . . 0A to 1A
Ambient Temperature Range . . . . . -40°C to +85°

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 4, 5)	39	3

Ambient Temperature Range . . . . . -40°C to +85°C
Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Typical specifications are measured at the following conditions: T_A = -40°C to +85°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
SUPPLY VOLTAGE						
V_{IN} Voltage Range	V_{IN}		5.5	-	25	V
		VIN connected to VDD	4.5	5.0	5.5	V
V_{IN} Operating Supply Current	I_{OP}	(Note 6)	-	2.0	2.5	mA
V_{IN} Shutdown Supply Current	I_{SD}	V_{IN} = 15V, EN = GND	-	80	100	µA
POWER-ON RESET						
VDD POR Threshold		Rising Edge	4.00	4.15	4.30	V
		Hysteresis	-	275	-	mV
INTERNAL V_{DD} LDO						
V_{DD} Output Voltage Range		V_{IN} = 5.5V to 25V, I_{VDD} = 0mA to 30mA	4.50	5.00	5.50	V
REFERENCE						
Reference Voltage	V_{FB}	V_{IN} = 5.5V to 25V, I_{REF} = 0	0.594	0.600	0.606	V
STANDARD BUCK PWM REGULATOR						
FB Line Regulation		I_{OUT} = 0mA, V_{IN} = 5.5V to 25V	-0.05	-	0.05	%
FB Leakage Current		V_{FB} = 0.6V	-50	0	50	nA
OSCILLATOR AND PWM MODULATOR						
Nominal Switching Frequency	f_{SW}		450	500	550	kHz
Modulator Gain	A_{MOD}	V_{IN} = 12V (A_{MOD} = 8/V_{IN})	0.65	0.75	0.95	V/V
Peak-to-Peak Sawtooth Amplitude	V_{RAMP}	V_{IN} = 12V (V_{P-P} = V_{IN}/8)	-	1.3	-	V
PWM Ramp Offset Voltage	V_{OFFSET}		0.75	0.80	0.85	V
Maximum Duty Cycle	DCmax	COMP > 4V	80	-	-	%
ERROR AMPLIFIER						
Open-Loop Gain			-	88	-	dB
Gain Bandwidth Product	GBWP		-	15	-	MHz
Slew Rate	SR	COMP = 10pF	-	5	-	V/µs

Electrical Specifications

Typical specifications are measured at the following conditions: T_A = -40°C to +85°C. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
ENABLE SECTION						
EN Threshold		Rising Edge	1.2	1.7	2.2	V
		Hysteresis	-	400	-	mV
EN Logic Input Current			-1	-	1	µA
FAULT PROTECTION						
Thermal Shutdown Temperature	T_{SD}	Rising Threshold	-	150	-	°C
	T_{HYS}	Hysteresis	-	15	-	°C
PWM UV Trip Level	V_{UV}	Referred to Nominal V_{OUT}	70	75	80	%
PWM UVP Propagation Delay			-	270	-	ns
PWM OCP Threshold		V_{IN} = V_{DD} = 5V, (Note 7)	1.37	1.70	2.17	A
OCP Blanking Time			-	100	-	ns
POWER-GOOD						
PG Trip Level Referred to Nominal V_{OUT}		Lower level, falling edge, with typically 15mV hysteresis	85	88	91	%
		Upper level, rising edge, with typically 15mV hysteresis	108	112	116	%
PG Propagation Delay			-	9	-	µs
PG Low Voltage		I_{SINK} = 4mA	-	0.05	0.30	V
PG Leakage Current		V_{PG} = 5.5V, V_{FB} = 0.6V, V_{DD} = 5.5V	-1	-	1	µA
SOFT-START SECTION						
Soft-Start Threshold to Enable Buck			0.9	1.0	1.1	V
Soft-Start Threshold to Enable PG			2.5	3.0	3.5	V
Soft-Start Voltage High			-	3.45	-	V
Soft-Start Charging Current			20	30	40	µA
Soft-Start Pull-Down		V_{SS} = 3.0V	-	25	-	mA
POWER MOSFET						
$r_{DS(ON)}$		I_{OUT} = 100mA, Die Resistance	-	120	200	mΩ

NOTES:

6. Test Condition: V_{IN} = 15V, FB forced above regulation point (0.6V), no switching, and power MOSFET gate charging current not included.
7. Excluding the blanking time.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 12V, EN = V_{DD}, L = 22µH, C_9 = 10µF, C_{11} = 47µF, I_{OUT} = 0A to 1A. See "VIN" on page 4.

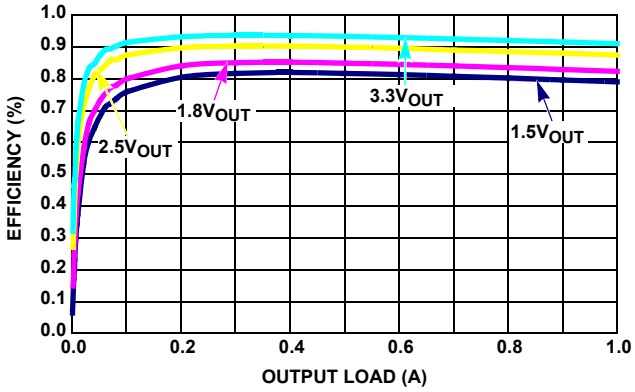


FIGURE 3. EFFICIENCY vs LOAD, 500kHz, $5V_{IN}$

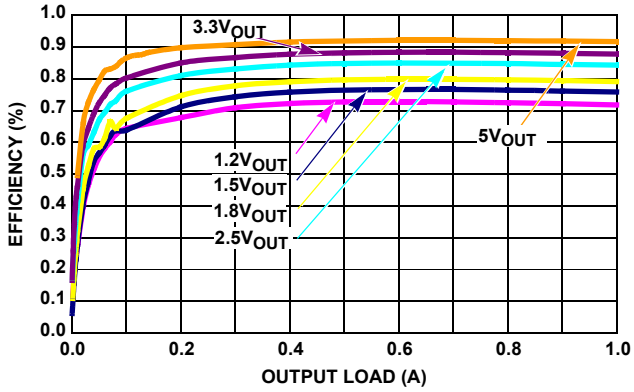


FIGURE 4. EFFICIENCY vs LOAD, 500kHz, $12V_{IN}$

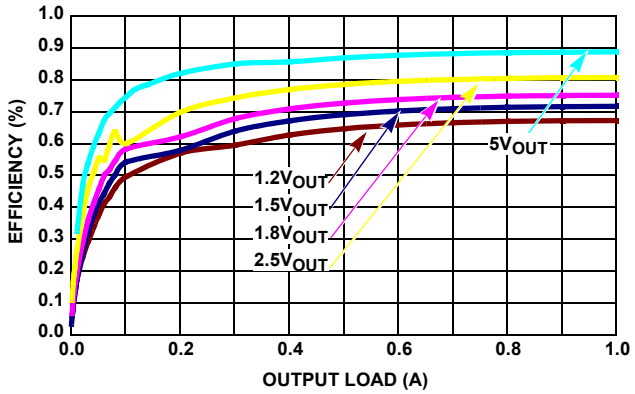


FIGURE 5. EFFICIENCY vs LOAD, 500kHz, $25V_{IN}$

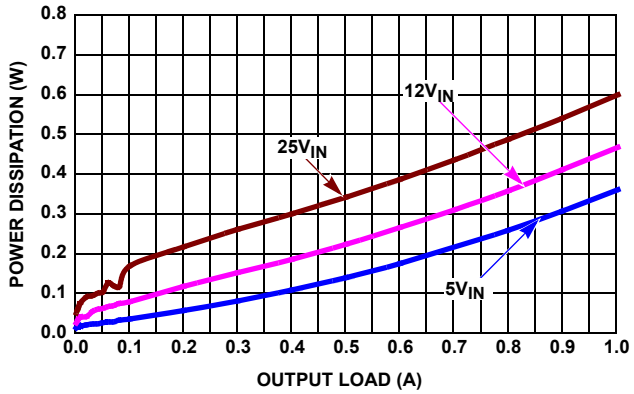


FIGURE 6. POWER DISSIPATION vs LOAD, 500kHz, $2.5V_{OUT}$

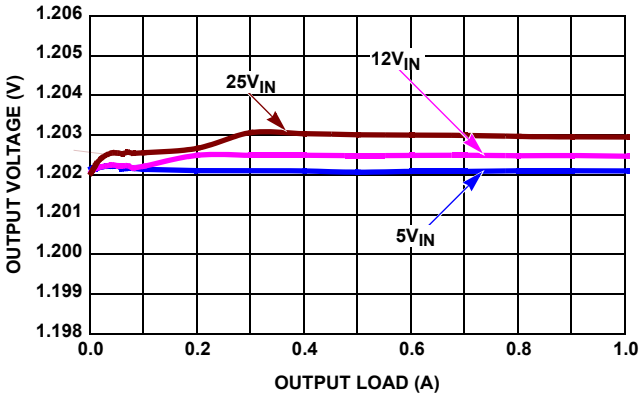


FIGURE 7. V_{OUT} REGULATION vs LOAD, 500kHz, $1.2V_{OUT}$

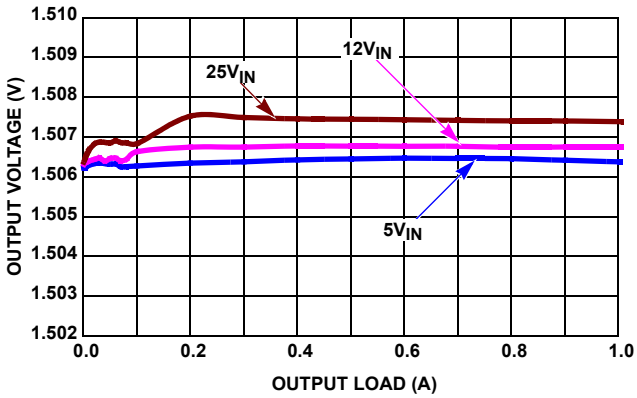


FIGURE 8. V_{OUT} REGULATION vs LOAD, 500kHz, $1.5V_{OUT}$

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 12V, EN = V_{DD}, L = 22µH, C_9 = 10µF, C_{11} = 47µF, I_{OUT} = 0A to 1A. See "VIN" on page 4. **(Continued)**

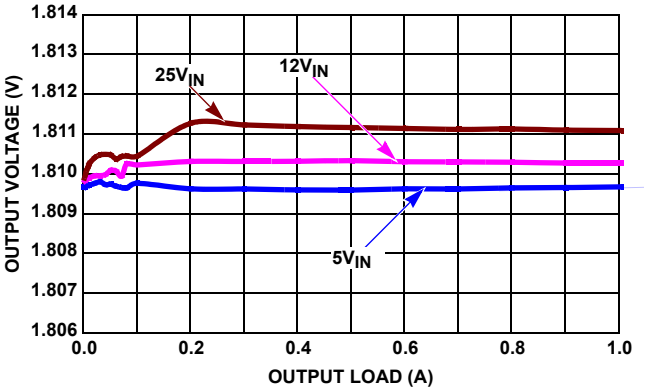


FIGURE 9. V_{OUT} REGULATION vs LOAD, 500kHz, 1.8V_{OUT}

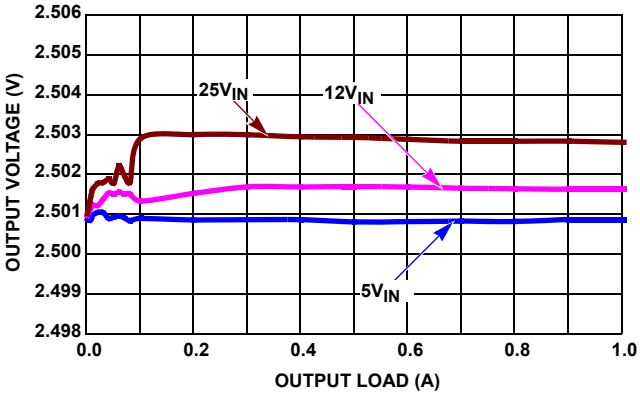


FIGURE 10. V_{OUT} REGULATION vs LOAD, 500kHz, 2.5V_{OUT}

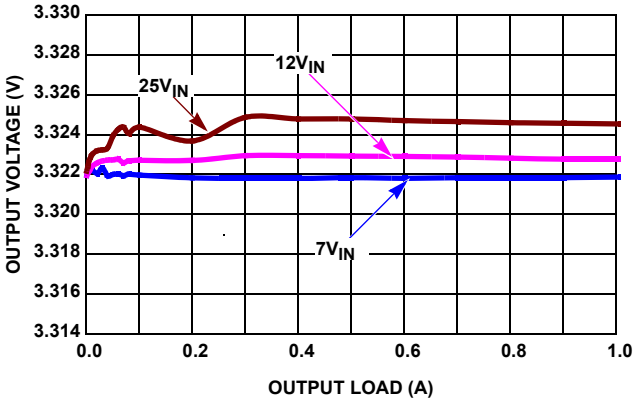


FIGURE 11. V_{OUT} REGULATION vs LOAD, 500kHz, 3.3V_{OUT}

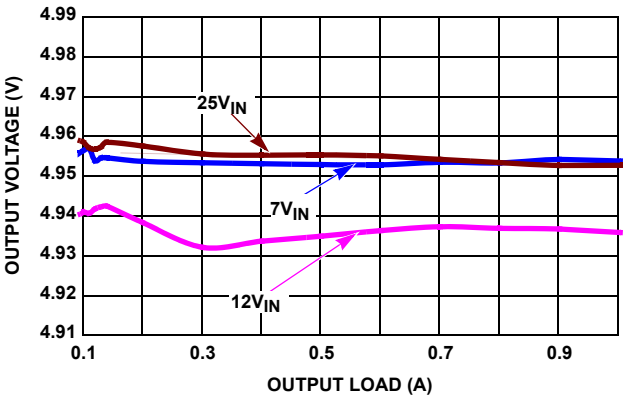


FIGURE 12. V_{OUT} REGULATION vs LOAD, 500kHz, 5V_{OUT}

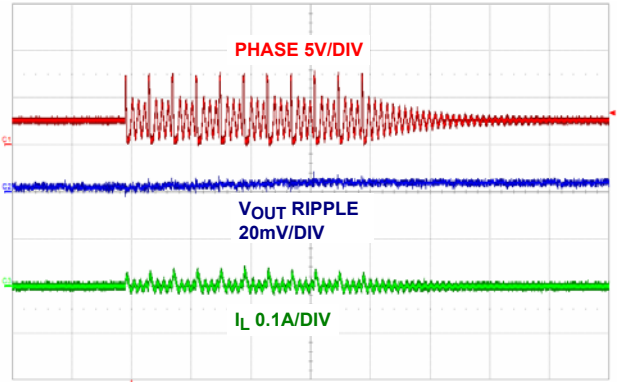


FIGURE 13. STEADY STATE OPERATION AT NO LOAD (5µs/DIV)

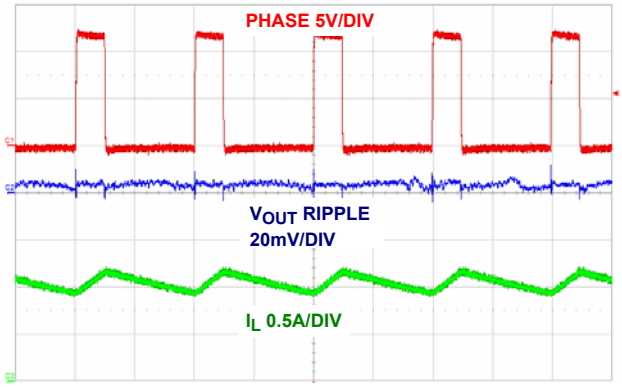


FIGURE 14. STEADY STATE OPERATION AT FULL LOAD (1µs/DIV)

Typical Performance Curves Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 12V, EN = V_{DD}, L = 22µH, C_9 = 10µF, C_{11} = 47µF, I_{OUT} = 0A to 1A. See "VIN" on page 4. **(Continued)**

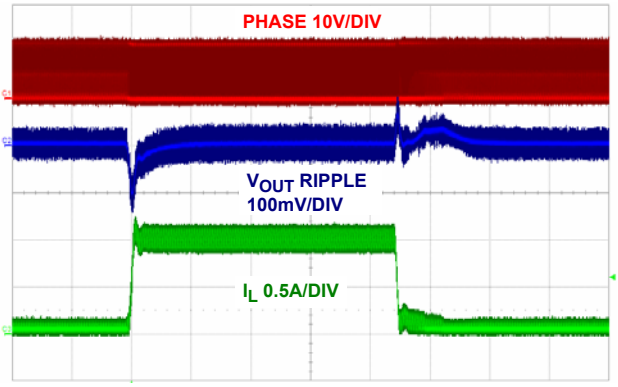


FIGURE 15. LOAD TRANSIENT (200µs/DIV)

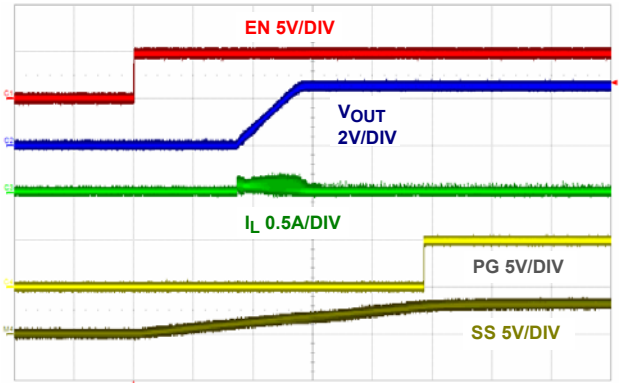


FIGURE 16. SOFT-START AT NO LOAD (2ms/DIV)

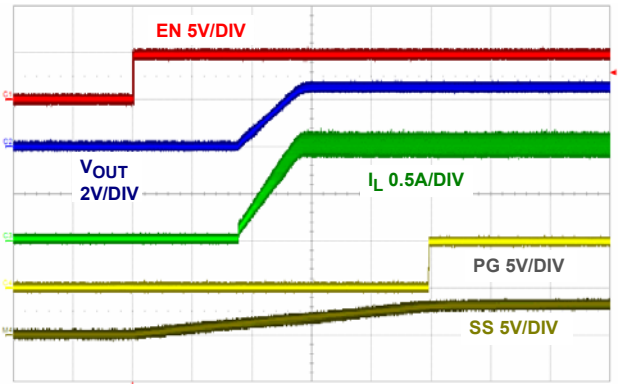


FIGURE 17. SOFT-START AT FULL LOAD (2ms/DIV)

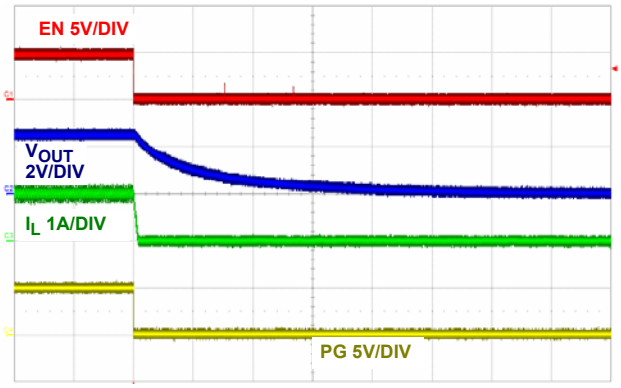


FIGURE 18. SHUTDOWN CIRCUIT (100µs/DIV)

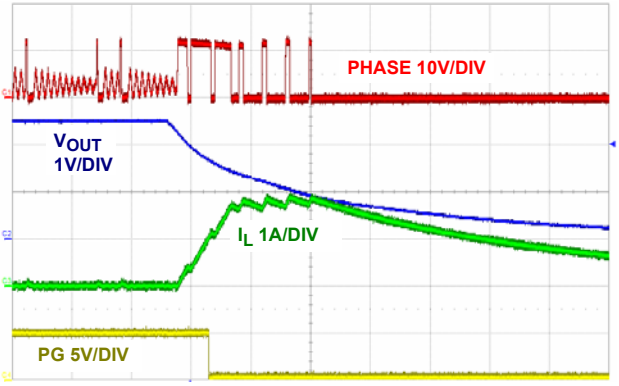


FIGURE 19. OUTPUT SHORT-CIRCUIT (5µs/DIV)

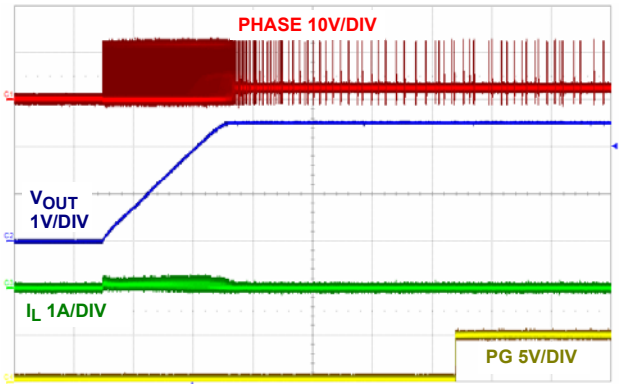


FIGURE 20. OUTPUT SHORT-CIRCUIT RECOVERY (1ms/DIV)

Detailed Description

The ISL85001 combines a standard buck PWM controller with an integrated switching MOSFET. The buck controller drives an internal N-channel MOSFET and requires an external diode to deliver load current up to 1A. A Schottky diode is recommended for improved efficiency and performance over a standard diode. The standard buck regulator can operate from either an unregulated DC source, such as a battery, with a voltage ranging from +5.5V to +25V, or from a regulated system rail of +5V. When operating from +5.5V or greater, the controller is biased from an internal +5V LDO voltage regulator. The converter output is regulated down to 0.6V from either input source. These features make the ISL85001 ideally suited for FPGA and wireless chipset power applications.

The PWM control loop uses a single output voltage loop with input voltage feed-forward, which simplifies feedback loop compensation and rejects input voltage variation. External feedback loop compensation allows flexibility in output filter component selection. The regulator switches at a fixed 500kHz.

The buck regulator is equipped with a lossless current limit scheme. The current limit in the buck regulator is achieved by monitoring the drain-to-source voltage drop of the internal switching power MOSFET. The current limit threshold is internally set at 1.7A. The part also features undervoltage protection by latching the switching MOSFET driver to the OFF-state during an overcurrent, when the output voltage is lower than 75% of the regulated output. This helps minimize power dissipation during a short-circuit condition. Due to only the switching power MOSFET integration, there is no overvoltage protection feature for this part.

+5V Internal Bias Supply (VDD)

Voltage applied to the VIN pin with respect to GND is regulated to +5V DC by an internal LDO regulator. The output of the LDO, VDD, is the bias voltage used by all the internal control and protection circuitry. The VDD pin requires a ceramic capacitor connected to GND. The capacitor serves to stabilize the LDO and to decouple load transients.

The input voltage range for the ISL85001 is specified as +5.5V to +25V or +5V ±10%. In the case of an unregulated supply case, the power supply is connected to VIN only. Once enabled, the linear regulator will turn-on and rise to +5V on VDD. In the +5V supply case, the VDD and VIN pins must be tied together to bypass the LDO. The external decoupling capacitor is still required in this mode.

Operation Initialization

The power-on reset circuit and enable inputs prevent false start-up of the PWM regulator output. Once all the input criteria are met, the controller soft-starts the output voltage to the programmed level.

Power-On Reset and Undervoltage Lockout

The PWM portion of the ISL85001 automatically initializes upon receipt of input power. The Power-On Reset (POR) function continually monitors the VDD voltage. While below the POR thresholds, the controller inhibits switching off the internal power MOSFET. Once exceeded, the controller initializes the internal soft-start circuitry. If either input supply drops below their falling POR threshold during soft-start or operation, the buck regulator latches off.

Enable and Disable

All internal power devices are held in a high-impedance state, which ensures they remain off while in shutdown mode. Typically, the enable input for a specific output is toggled high after the input supply to that regulator is active and the internal LDO has exceeded its POR threshold.

The EN pin enables the buck controller portion of the ISL85001. When the voltage on the EN pin exceeds the POR rising threshold, the controller initiates the soft-start function for the PWM regulator. If the voltage on the EN pin drops below the POR falling threshold, the buck regulator shuts down.

Pulling the EN pin low simultaneously puts the output into shutdown mode and supply current drops to 100µA typical.

Soft-Start

Once the input supply latch and enable threshold are met, the soft-start function is initialized. The soft-start circuitry begins sourcing 30µA, from an internal current source, which charges the external soft-start capacitor. The voltage on SS begins ramping linearly from ground until the voltage across the soft-start capacitor reaches 3.0V. This linear ramp is applied to the noninverting input of the internal error amplifier and overrides the nominal 0.6V reference. The output voltage reaches its regulation value when the soft-start capacitor voltage reaches 1.6V. Connect a capacitor from the SS pin to ground. This capacitor (along with an internal 30µA current source) sets the soft-start interval of the converter, t_{SS}.

$$C_{SS}[\mu F] = 50 \cdot t_{SS}[s] \quad \text{(EQ. 1)}$$

Upon disable, the SS pin voltage will discharge to zero voltage.

Power-Good

PG is an open-drain output of a window comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. After the soft-start period terminates, PG becomes high impedance as long as the output voltage is within ±12% of the nominal regulation voltage set by FB. When VOUT drops 12% below or rises 12% above the nominal regulation voltage, the ISL85001 pulls PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. For logic level output voltages, connect an external pull-up resistor between PG and VDD. A 100kΩ resistor works well in most applications.

Output Voltage Selection

The regulator output voltages can be programmed using external resistor dividers that scale the voltage feedback relative to the internal reference voltage. The scaled voltage is fed back to the inverting input of the error amplifier; refer to Figure 21.

The output voltage programming resistor, R_4, will depend on the value chosen for the feedback resistor, R_1, and the desired output

voltage, V_{OUT}, of the regulator; see Equation 2. The value for the feedback resistor is typically between 1kΩ and 10kΩ.

$$R_4 = \frac{R_1 \cdot 0.6V}{V_{OUT} - 0.6V} \quad \text{(EQ. 2)}$$

If the output voltage desired is 0.6V, then R_P is left unpopulated.

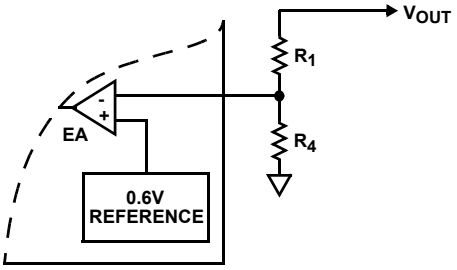


FIGURE 21. EXTERNAL RESISTOR DIVIDER

The buck output can be programmed as high as 19V. Proper heatsinking must be provided to insure that the junction temperature does not exceed +125°C.

When the output is set greater than 2.7V, it is recommended to preload at least 10mA and make sure that the input rise time is much faster than the V_{OUT1} rise time. This allows the BOOT capacitor adequate time to charge for proper operation.

Protection Features

The ISL85001 limits current in the power devices to limit on-chip power dissipation. Overcurrent limits on the regulator protect the internal power device from excessive thermal damage. Undervoltage protection circuitry on the buck regulator provides a second layer of protection for the internal power device under high current condition.

Buck Regulator Overcurrent Protection

During the PWM on-time, the current through the internal switching MOSFET is sampled and scaled through an internal pilot device. The sampled current is compared to a nominal 1.7A overcurrent limit. If the sampled current exceeds the overcurrent limit reference level, an internal overcurrent fault counter is set to 1 and an internal flag is set. The internal power MOSFET is immediately turned off and will not be turned on again until the next switching cycle.

The protection circuitry continues to monitor the current and turns off the internal MOSFET as described. If the overcurrent condition persists for eight sequential clock cycles, the overcurrent fault counter overflows, indicating an overcurrent fault condition exists. The regulator is shut down and power-good goes low. If the overcurrent condition clears prior to the counter reaching four consecutive cycles, the internal flag and counter are reset.

The protection circuitry attempts to recover from the overcurrent condition after waiting 4 soft-start cycles. The internal overcurrent flag and counter are reset. A normal soft-start cycle is attempted and normal operation continues if the fault condition has cleared. If the overcurrent fault counter overflows during soft-start, the converter shuts down and this hiccup mode operation repeats.

There is 100ns blanking time for noise immunity. It is recommended to operate the duty cycle higher than the blanking time to insure proper overcurrent protection.

Undervoltage Protection

If the voltage detected on the buck regulator FB pin falls 25% below the internal reference voltage, the undervoltage fault condition flag is set. The regulator is shut down. The controller enters a recovery mode similar to the overcurrent hiccup mode. No action is taken for 4 soft-start cycles and the internal undervoltage counter and fault condition flag are reset. A normal soft-start cycle is attempted and normal operation continues if the fault condition has cleared. If the undervoltage counter overflows during soft-start, the converter is shut down and this hiccup mode operation repeats.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ISL85001. There is a sensor on the chip to monitor the junction temperature of the internal LDO and PWM switching power N-channel MOSFET. When the junction temperature (T_J) of the sensor exceeds +150°C, the thermal sensor sends a signal to the fault monitor.

The fault monitor commands the buck regulator to shut down. The buck regulator soft-starts turn on again after the IC's junction temperature cools by 20°C. The buck regulator experiences hiccup mode operation during continuous thermal overload conditions. For continuous operation, do not exceed the +125°C junction temperature rating.

Application Guidelines

Operating Frequency

The ISL85001 operates at a fixed switching frequency of 500kHz.

Buck Regulator Output Capacitor Selection

An output capacitor is required to filter the inductor current and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Embedded processor systems are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equation 3:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{f_{SW} \cdot L} \cdot \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \cdot ESR \qquad \text{(EQ. 3)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL85001 will provide either 0% or 80% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equation 4 gives the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \cdot I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \cdot I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 4)}$$

Where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check Equation 4 at the minimum and maximum output levels for the worst case response time.

Rectifier Selection

Current circulates from ground to the junction of the MOSFET and the inductor when the high-side switch is off. As a consequence, the polarity of the switching node is negative with respect to ground. This voltage is approximately -0.5V (a Schottky diode drop) during the off-time. The rectifier's rated reverse breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor. The power dissipation is shown in Equation 5:

$$P_D[W] = I_{OUT} \cdot V_D \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad \text{(EQ. 5)}$$

Where V_D is the voltage of the Schottky diode = 0.5V to 0.7V

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the switching MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFET VIN pins (switching MOSFET drain) and the Schottky diode anode.

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a conservative guideline. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current required by the regulator may be closely approximated through Equation 6:

$$I_{RMS\_MAX} = \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left[\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right) \cdot I_{OUTMAX}^2 + \frac{1}{12} \cdot \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \cdot \frac{V_{OUT}}{L \cdot f_{SW}}\right)^2\right]} \qquad \text{(EQ. 6)}$$

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

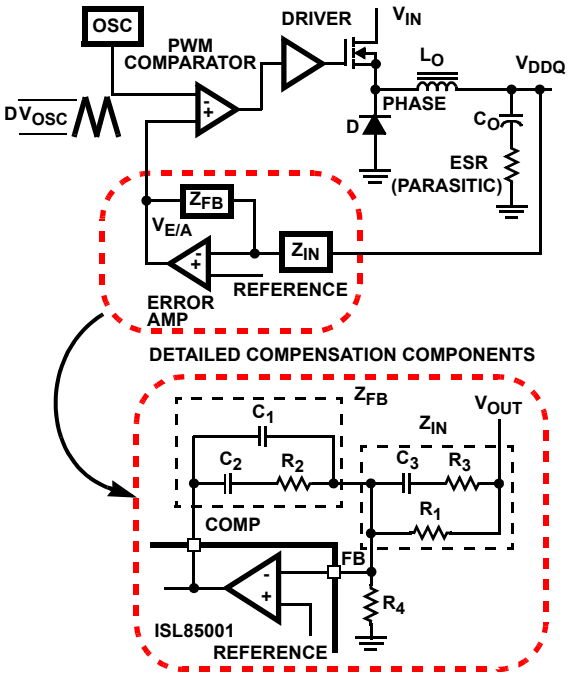


FIGURE 22. VOLTAGE MODE BUCK CONVERTER COMPENSATION DESIGN AND OUTPUT VOLTAGE SELECTION

Feedback Compensation

Figure 22 on page 13 highlights the voltage mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a Pulse-Width Modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L_O \cdot C_O}} \qquad F_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C_O} \qquad \text{(EQ. 7)}$$

The compensation network consists of the error amplifier (internal to the ISL85001) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide an open loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the open loop phase at f_{0dB} and 180°. Equation 8 relates the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 23. Use the following guidelines for locating the poles and zeros of the compensation network:

1. Pick gain (R_2/R_1) for desired converter bandwidth.
2. Place 1ST zero below filter's double pole (~75% F_{LC}).
3. Place 2ND zero at filter's double pole.
4. Place 1ST pole at the ESR zero.
5. Place 2ND pole at half the switching frequency.
6. Check gain against error amplifier's open-loop gain.
7. Estimate phase margin - repeat if necessary.

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \cdot R_2 \cdot C_2} \qquad F_{P1} = \frac{1}{2\pi \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)} \qquad \text{(EQ. 8)}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R_1 + R_3) \cdot C_3} \qquad F_{P2} = \frac{1}{2\pi \cdot R_3 \cdot C_3}$$

Figure 23 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual modulator gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 23. Using the previously mentioned guidelines should give a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The open loop gain is constructed on the graph of Figure 21 by adding the modulator gain (in dB) to the compensation gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

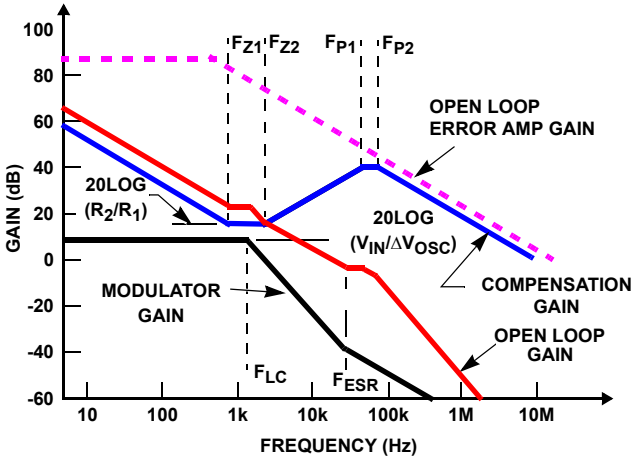


FIGURE 23. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin.

A more detailed explanation of voltage mode control of a buck regulator can be found in TB417, entitled "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators."

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently between 100kHz and 600kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes.

As an example, consider the turn-off transition of the upper MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the Schottky diode. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components and short, wide traces minimizes the magnitude of voltage spikes.

There are two sets of critical components in the ISL85001 switching converter. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. Next are the small signal components, which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 24 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the phase terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

In order to dissipate heat generated by the internal LDO and MOSFET, the ground pad, Pin 13, should be connected to the internal ground plane through at least four vias. This allows the heat to move away from the IC and also ties the pad to the ground plane through a low impedance path.

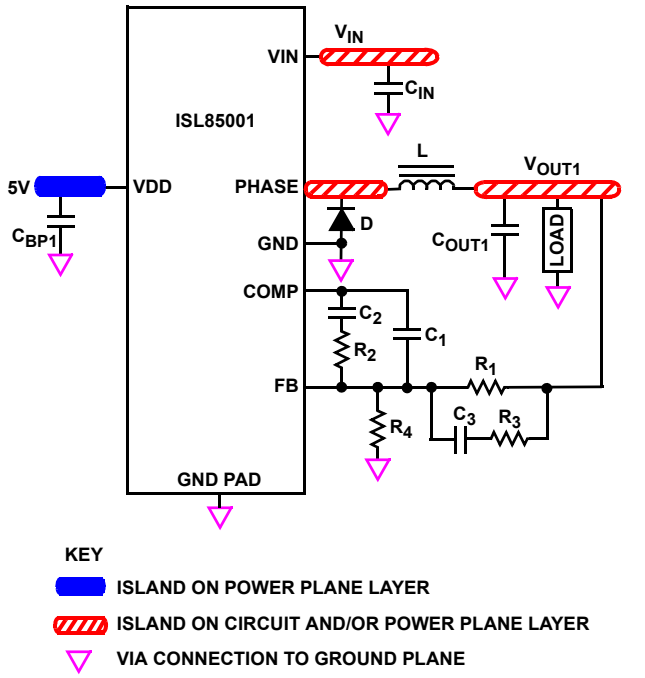


FIGURE 24. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

The switching components should be placed close to the ISL85001 first. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between the upper and Schottky diode and the load.

The critical small signal components include any bypass capacitors, feedback components and compensation components. Place the PWM converter compensation components close to the FB and COMP pins. The feedback resistors should be located as close as possible to the FB pin with vias tied straight to the ground plane as required.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
April 14, 2017	FN6769.3	Updated Related Literature section on page 1. Updated Figure 2 on page 3 by removing the VDD label next to power-on reset monitor. Added Evaluation Board to Ordering Information table on page 4. Updated Note 1 to include the unit amount for the tape and reel option. Updated 70% to 75% in the third paragraph under Detailed Description section. Replaced all of the 'x' in the formulas with the '·'. Updated Equation 6 on page 12. Updated POD to the latest revision, changes are as follows: Tiebar Note 5 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
May 16, 2012	FN6769.2	Converted to new datasheet template. Added "Related Literature" to page 1. Added MSL note to "Ordering Information" on page 4. Updated Tape & Reel note in "Ordering Information" on page 4 to new standard "Add "-T*" suffix for tape and reel." The "*" covers all possible tape and reel options. Removed incorrect note 4 reference from "Absolute Maximum Ratings" on page 5. Added "Revision History" and "Products" on page 16. Updated "Package Outline Drawing" on page 17. Added land pattern. Removed table and added dimensions to drawing.
March 17, 2009	FN6769.1	Changed "Note 5" to "Note 6" in "V_{IN} Operating Supply Current" on page 5
November 17, 2008	FN6769.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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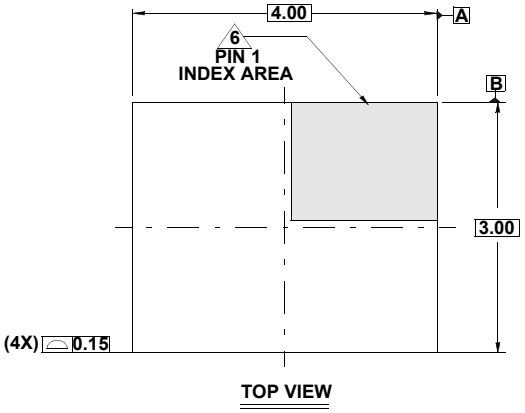
Package Outline Drawing

For the most recent package outline drawing, see L12.4x3.

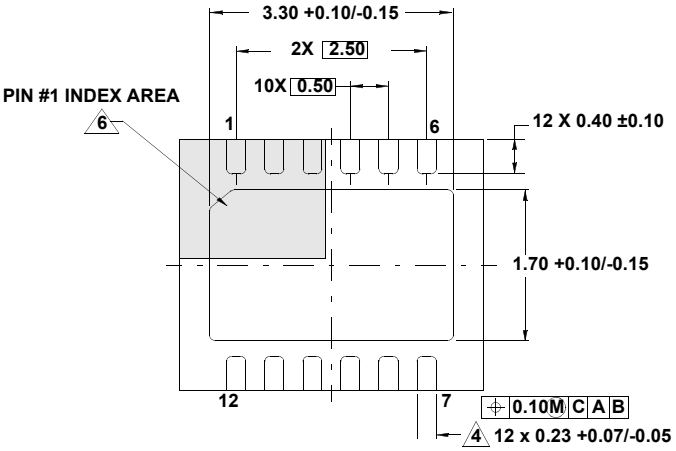
L12.4x3

12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

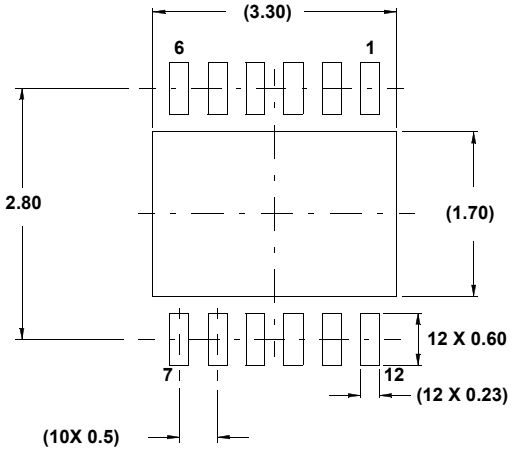
Rev 3, 3/15



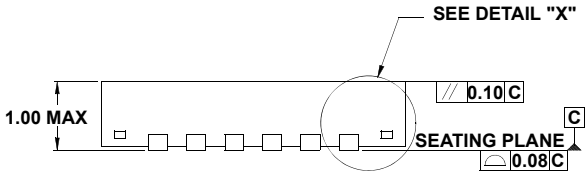
TOP VIEW



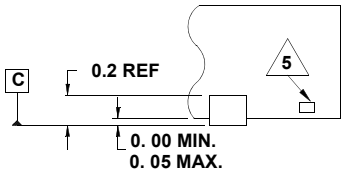
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 V4030D-4 issue E.

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