THE DATASHEET OF

LT3682IDD#TRPBF

1A Micropower Step-Down Switching Regulator

FEATURES

- **Wide Input Range:**
  - **Operation from 3.6V to 36V**
  - **Overvoltage Lockout Protects Circuits through 60V Transients**
- **1A Output Current**
- **Low Ripple Burst Mode® Operation**
  - **I_Q = 75µA at 12V_{IN} to 3.3V_{OUT}**
  - **Output Ripple < 15mV_{P-P}**
- **Adjustable Switching Frequency: 250kHz to 2.2MHz**
- **Short-Circuit Protected**
- **Synchronizable Between 300kHz and 2.2MHz**
- 0.8V Feedback Reference Voltage
- Output Voltage 0.8V to 20V
- Soft-Start Capability
- Power Good Flag
- Small 12-Pin Thermally Enhanced 3mm × 3mm DFN Package

APPLICATIONS

- Automotive Battery Regulation
- Automotive Entertainment Systems
- Industrial Supplies
- Power for Portable Products
- Distributed Supply Regulation

DESCRIPTION

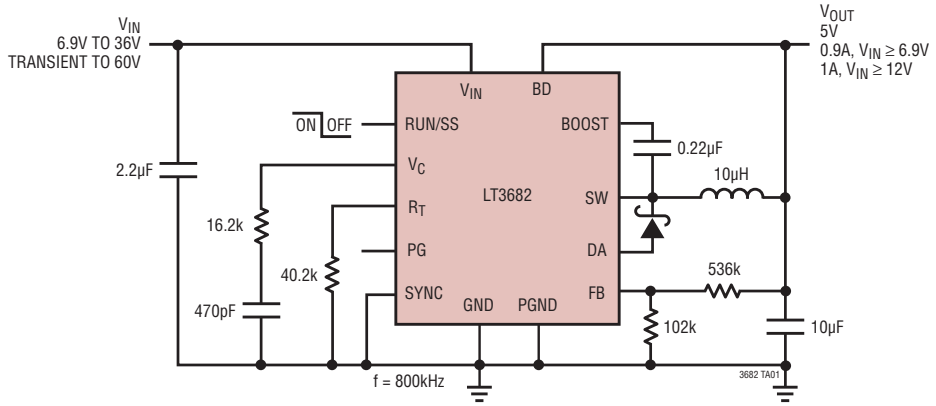
The LT®3682 is an adjustable frequency (250kHz to 2.2MHz) monolithic buck switching regulator that accepts input voltages up to 36V. A high efficiency 0.5Ω switch is included on the device along with a boost diode and the necessary oscillator, control, and logic circuitry. Current mode topology is used for fast transient response and good loop stability. A SYNC pin allows the user to synchronize the part to an external clock, and to choose between Low Ripple Burst Mode operation and standard PWM operation.

The Low Ripple Burst Mode maintains high efficiency at low output currents while keeping output ripple below 15mV in typical applications. Shutdown reduces input supply current to less than 1µA while a resistor and capacitor on the RUN/SS pin provide a controlled output voltage ramp (soft-start). A power good flag signals when V_{OUT} reaches 90% of the programmed output voltage. Protection circuitry senses the current in the power switch and external Schottky catch diode to protect the LT3682 against short-circuit conditions. Frequency foldback and thermal shutdown provide additional protection.

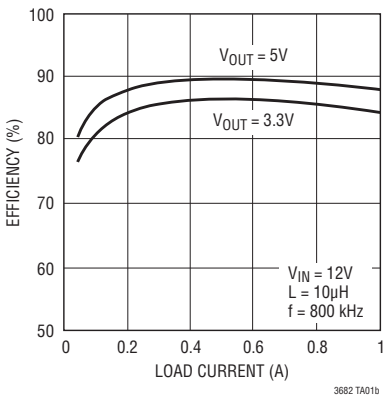
The LT3682 is available in a 12-Pin 3mm × 3mm DFN with exposed pad for low thermal resistance.

TYPICAL APPLICATION

5V Step-Down Converter



Efficiency

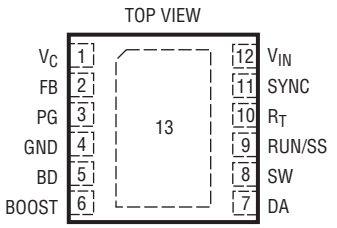


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, RUN/SS Voltage (Note 2) 60V
BOOST Pin Voltage 50V
BOOST Pin Above SW Pin 30V
FB, R_T, V_C Voltage 5V
SYNC 20V
BD and PG Voltage 30V
Operating Junction Temperature Range (Notes 3 and 6)
LT3682E .....–40°C to 125°C
LT3682I .....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN

θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3682EDD#PBF	LT3682EDD#TRPBF	LFDW	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3682IDD#PBF	LT3682IDD#TRPBF	LFDW	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 10V, V_{RUN}/SS = 10V, V_{BD} = 3.3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage	V_{BD} = 3.3V V_{BD} < 3.0V	● ●		3.4 3.4	3.6 4.3	V V
V_{IN} Overvoltage Lockout		●	36	39	41	V
Quiescent Current from V_{IN}	$V_{RUN/SS}$ = 0.2V $V_{RUN/SS}$ = 10V, V_{BD} = 3.3V, Not Switching $V_{RUN/SS}$ = 10V, V_{BD} = 0V, Not Switching	 ● 		0.01 35 90	0.5 60 160	µA µA µA
Quiescent Current from BD Pin	$V_{RUN/SS}$ = 0.2V $V_{RUN/SS}$ = 10V, V_{BD} = 3.3V, Not Switching $V_{RUN/SS}$ = 10V, V_{BD} = 0V, Not Switching	 ● 		0.01 55 0	0.5 100 5	µA µA µA
Minimum BD Pin Voltage				2.8	3	V
Feedback Voltage		 ●	792 780	800 800	808 812	mV mV
FB Pin Bias Current (Note 4)	FB Pin Voltage = 800mV	●		5	80	nA
FB Voltage Line Regulation	3.6V < V_{IN} < 36V			0.001	0.005	%/V
Error Amp g_m	I_{VC} = ±1.5µA			430		µS
Error Amp Voltage Gain				1300		V/V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 10V, V_{RUN}/SS = 10V, V_{BD} = 3.3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_C Source Current				50		µA
V_C Sink Current				50		µA
V_C Pin to Switch Current Gain				1.25		A/V
V_C Switching Threshold			0.5	0.6	0.7	V
V_C Clamp Voltage				2		V
Switching Frequency	R_{RT} = 8.06kΩ R_{RT} = 29.4kΩ R_{RT} = 158kΩ		1.98 0.9 225	2.2 1 250	2.42 1.1 275	MHz MHz kHz
Minimum Switch Off-Time		●		130	210	ns
Switch Current Limit (Note 7)	SYNC = 0V SYNC = 3.3V or Clocked		1.45 1.18	1.7 1.4	2 1.66	A A
Switch V_{CESAT}	I_{SW} = 1A			460		mV
DA Pin Current to Stop OSC			1.25	1.6	1.95	A
Switch Leakage Current	V_{SW} = 0V, V_{IN} = 60V			0.01	1	µA
Boost Schottky Diode Voltage Drop	I_{BSD} = 50mA			720	850	mV
Boost Schottky Diode Reverse Leakage	V_{SW} = 10V, V_{BD} = 0			0.1	1	µA
Minimum Boost Voltage (Note 5)		●		1.7	2.5	V
BOOST Pin Current	I_{SW} = 0.5A			10.5	17.5	mA
RUN/SS Pin Current	$V_{RUN/SS}$ = 10V			12	20	µA
RUN/SS Input Voltage High			2.5			V
RUN/SS Input Voltage Low					0.2	V
PG Leakage Current	V_{PG} = 5V			0.1	1	µA
PG Sink Current	V_{PG} = 0.4V	●	100	1000		µA
PG Threshold as % of V_{FB}	Measured at FB pin. FB Pin Voltage Rising		88%	90%	92%	V
PG Threshold Hysteresis	Measured at FB Pin			12		mV
SYNC Threshold Voltage			300	550	800	mV
SYNC Input Frequency			0.3		2.2	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect the device reliability and lifetime.

Note 2: Absolute Maximum Voltage at V_{IN} and RUN/SS pins is 60V for nonrepetitive 1 second transients, and 36V for continuous operation.

Note 3: The LT3682E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3682I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 4: Bias current flows out of the FB pin.

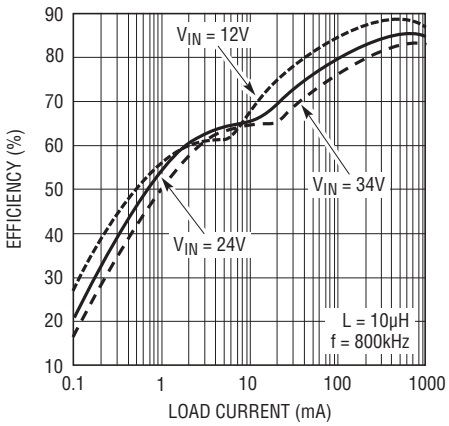
Note 5: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the switch.

Note 6: This IC includes over-temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

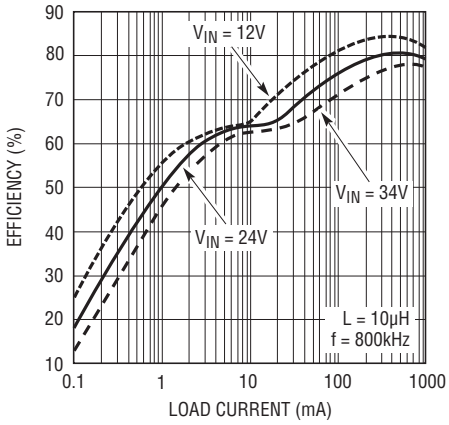
Note 7: Current limit guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

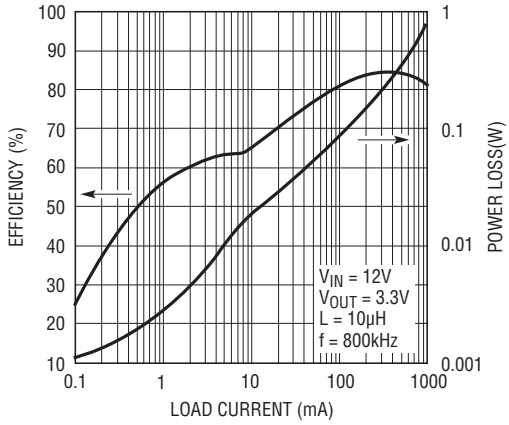
Efficiency (V_{OUT} = 5V, SYNC = 0V)



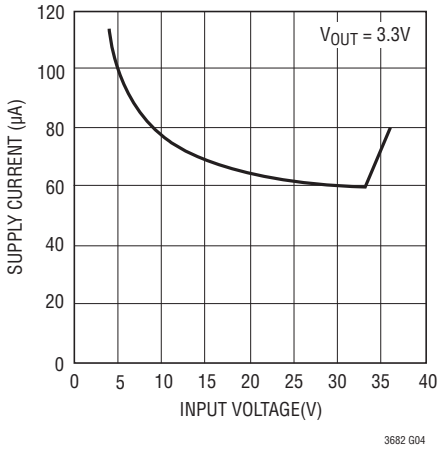
Efficiency (V_{OUT} = 3.3V, SYNC = 0V)



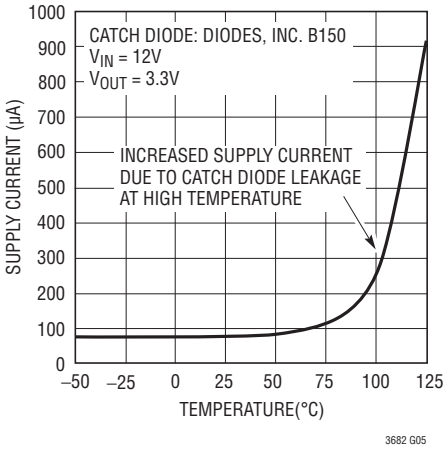
Efficiency (V_{OUT} = 3.3V, SYNC = 0V)



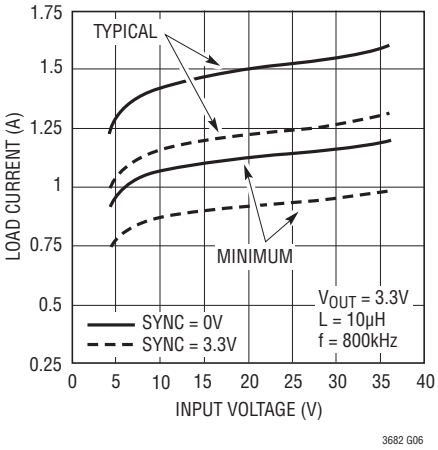
No Load Supply Current



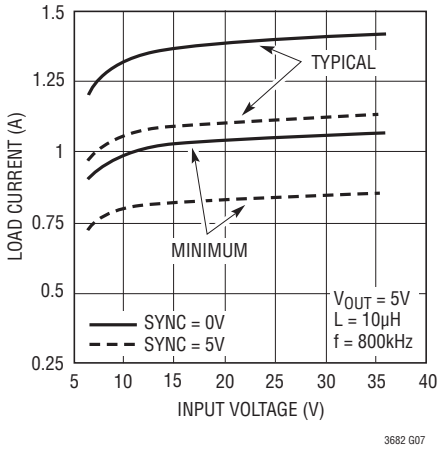
No Load Supply Current



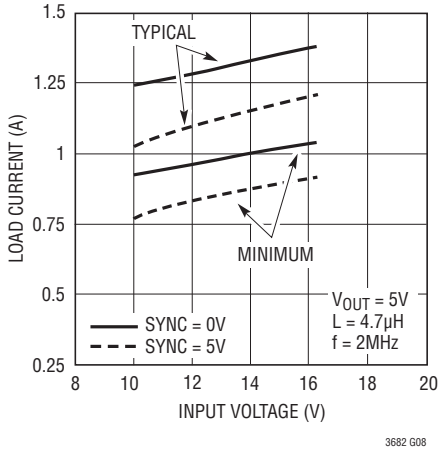
Maximum Load Current



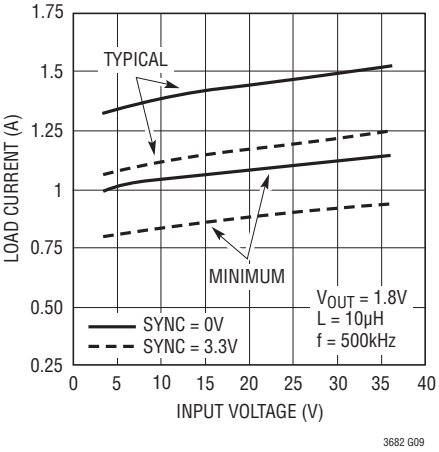
Maximum Load Current



Maximum Load Current

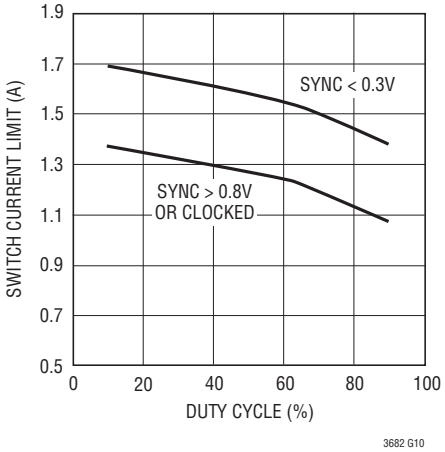


Maximum Load Current



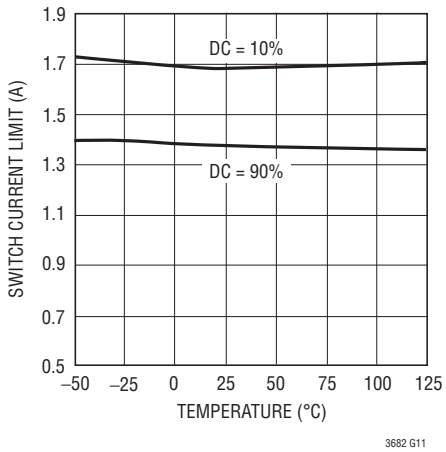
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Switch Current Limit



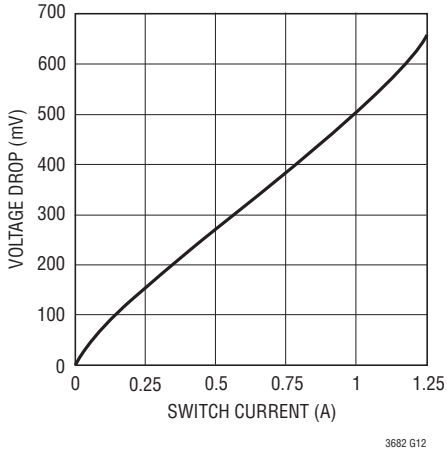
3682 G10

Switch Current Limit (SYNC Pin Grounded)



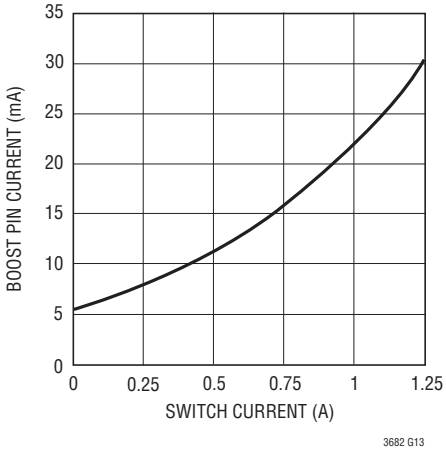
3682 G11

Switch Voltage Drop



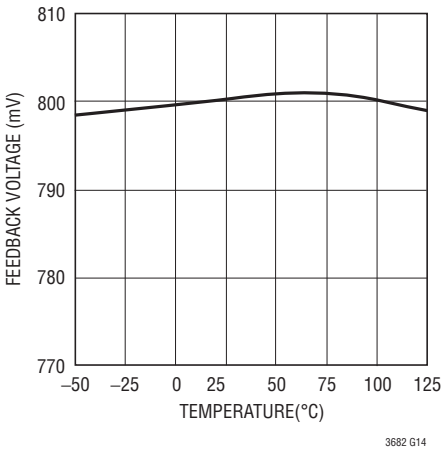
3682 G12

Boost Pin Current



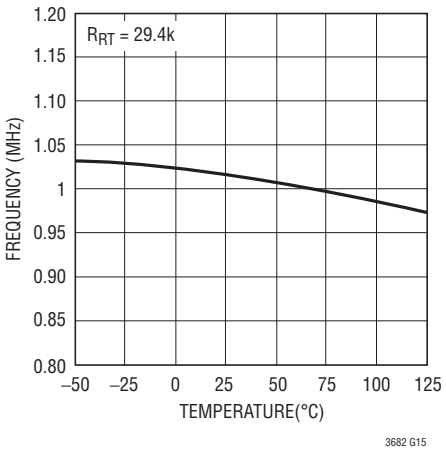
3682 G13

Feedback Voltage



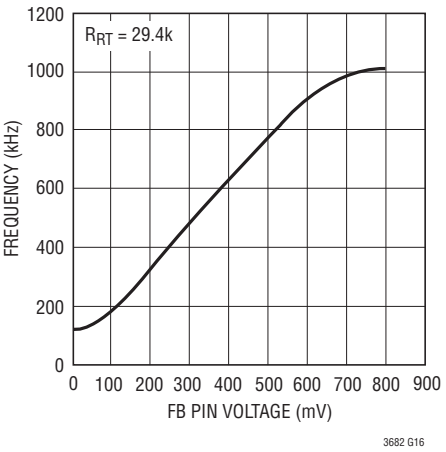
3682 G14

Switching Frequency



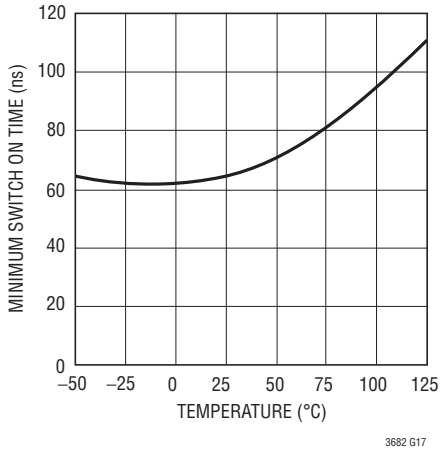
3682 G15

Frequency Foldback



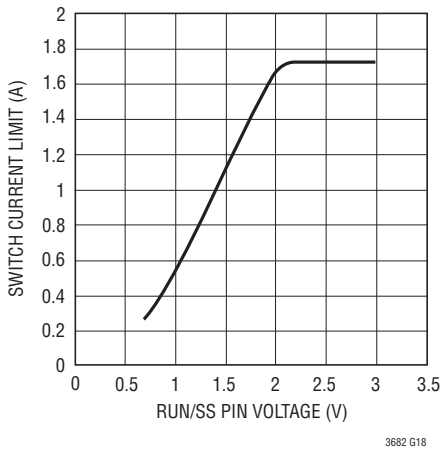
3682 G16

Minimum Switch On-Time



3682 G17

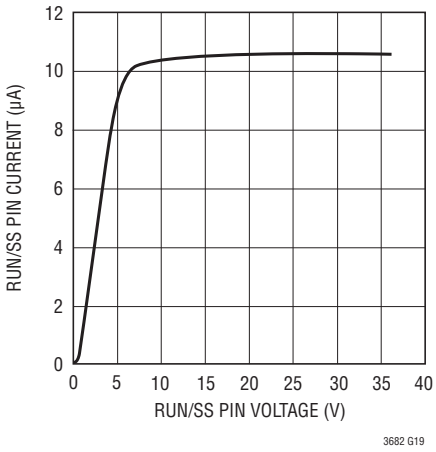
Soft-Start



3682 G18

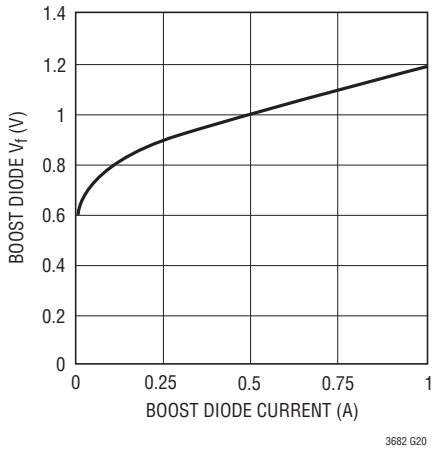
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

RUN/SS Pin Current



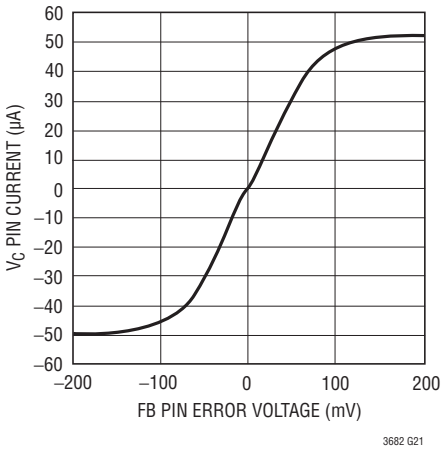
3682 G19

Boost Diode Forward Voltage



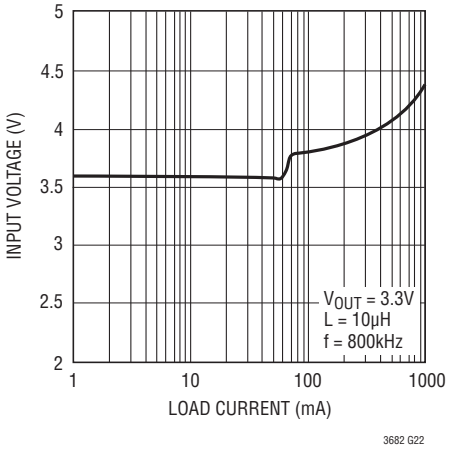
3682 G20

Error Amplifier Output Current



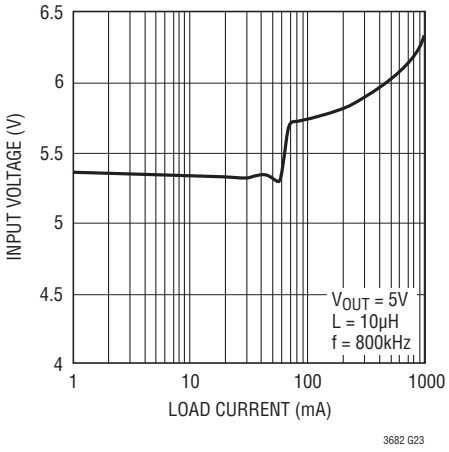
3682 G21

Minimum Input Voltage



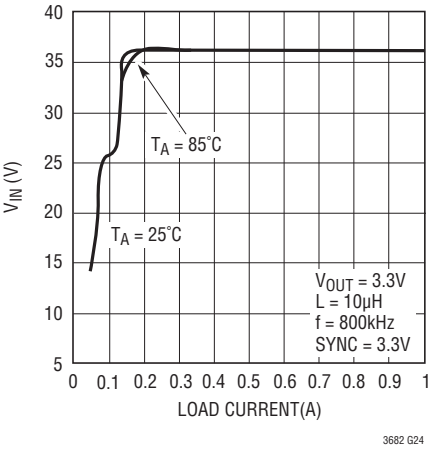
3682 G22

Minimum Input Voltage



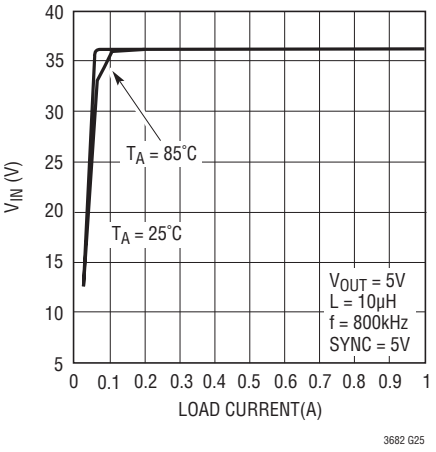
3682 G23

Maximum V_{IN} for Full Frequency



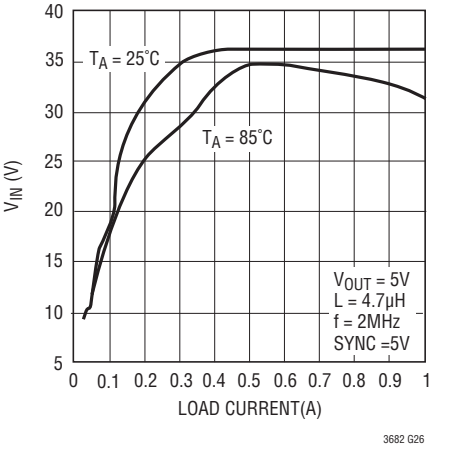
3682 G24

Maximum V_{IN} for Full Frequency



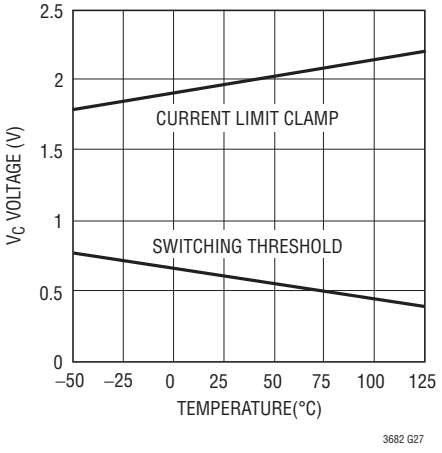
3682 G25

Maximum V_{IN} for Full Frequency



3682 G26

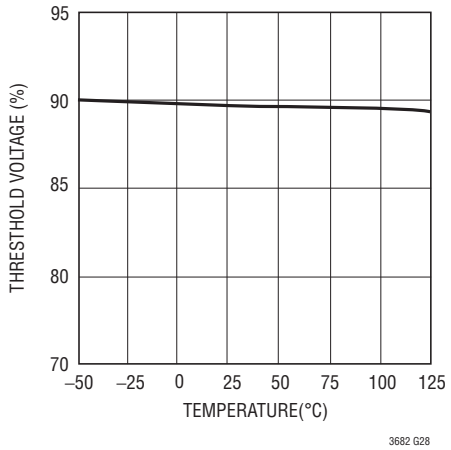
V_C Voltages



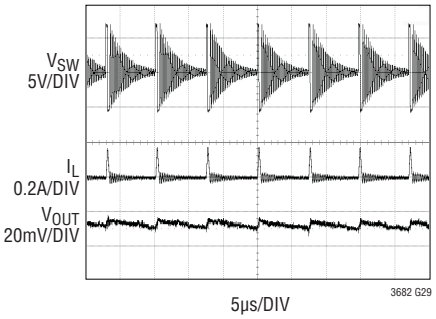
3682 G27

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Power Good Threshold

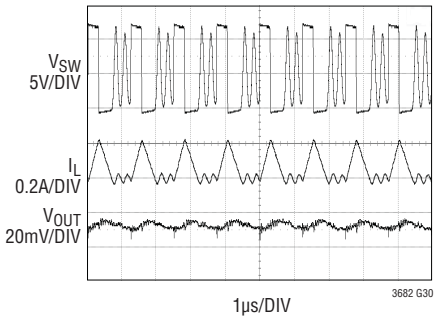


Switching Waveforms; Burst Mode



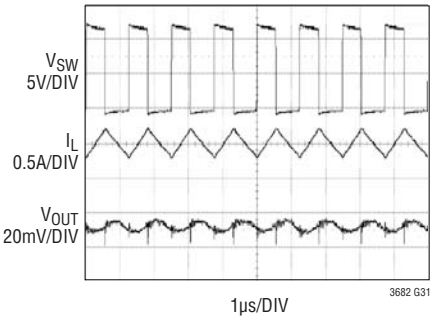
V_{IN} = 12V; FRONT PAGE APPLICATION
I_{LOAD} = 5mA

Switching Waveforms; Transition from Burst Mode to Full Frequency



V_{IN} = 12V; FRONT PAGE APPLICATION
I_{LOAD} = 55mA

Switching Waveforms; Full Frequency Continuous Operation



V_{IN} = 12V; FRONT PAGE APPLICATION
I_{LOAD} = 500mA

PIN FUNCTIONS

V_C (Pin 1): The V_C pin is the output of the internal error amplifier. The voltage on this pin controls the peak switch current. Tie an RC network from this pin to ground to compensate the control loop.

FB (Pin 2): The LT3682 regulates the FB pin to 0.8V. Connect the feedback resistor divider tap to this pin.

PG (Pin 3): The PG pin is the open collector output of an internal comparator. PG remains low until the FB pin is within 10% of the final regulation voltage. PG output is valid when V_{IN} is above the minimum input voltage and RUN/SS is high.

GND (Pin 4): The GND pin is the ground of all the internal circuitry. Tie directly to the local GND plane.

BD (Pin 5): This pin connects to the anode of the boost Schottky diode. BD also supplies current to the LT3682's internal regulator.

BOOST (Pin 6): This pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch. Connect a capacitor (typically 0.22µF) between BOOST and SW.

DA (Pin 7): Connect the anode of the catch diode (D1 in Block Diagram) to this pin. Internal circuitry senses the current through the catch diode providing frequency foldback in extreme situations.

SW (Pin 8): The SW pin is the output of the internal power switch. Connect this pin to the inductor, catch diode and boost capacitor.

RUN/SS (Pin 9): The RUN/SS pin is used to put the LT3682 in shutdown mode. Tie to ground to shut down the LT3682. Tie to 2.5V or more for normal operation. RUN/SS also provides a soft-start function; see the Applications Information section for more information.

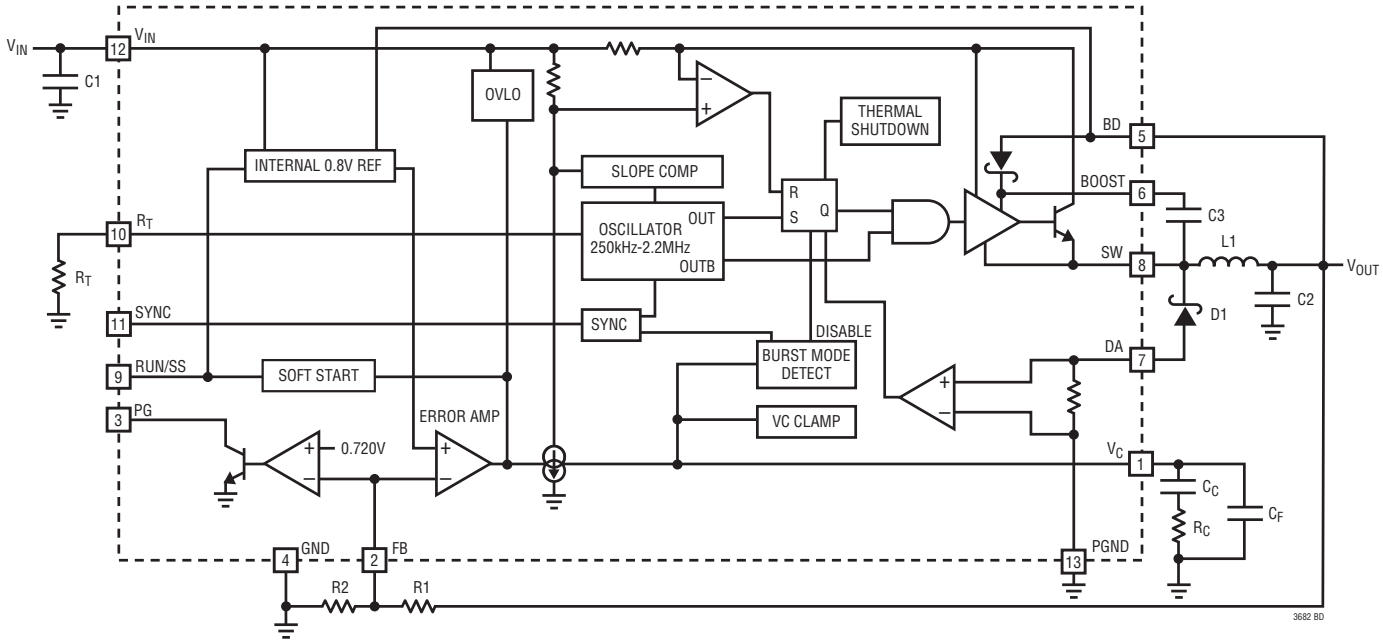
R_T (Pin 10): Oscillator Resistor Input. Connect a resistor from this pin to ground to set the switching frequency.

SYNC (Pin 11): This is the external clock synchronization input. Ground this pin for low ripple Burst Mode operation at low output loads. Tie to 0.8V or more for pulse skipping mode operation. Tie to a clock source for synchronization. Clock edges should have rise and fall times faster than 1µs. Note that the maximum load current depends on which mode is chosen. See the Applications Information section for more information.

V_{IN} (Pin 12): The V_{IN} pin supplies current to the LT3682's internal regulator and to the internal power switch. This pin must be locally bypassed.

Exposed Pad (Pin 13): PGND. This is the power ground used by the catch diode (D1) when its anode is connected to the DA pin. The exposed pad must be soldered to the PCB.

BLOCK DIAGRAM



OPERATION

The LT3682 is a constant frequency, current mode step-down regulator. An oscillator, with frequency set by R_T, enables an RS flip-flop, turning on the internal power switch. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at V_C. An error amplifier measures the output voltage through an external resistor divider tied to the FB pin and servos the V_C pin. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. An active clamp on the V_C pin provides current limit. The V_C pin is also clamped to the voltage on the RUN/SS pin; soft-start is implemented by generating a voltage ramp at the RUN/SS pin using an external resistor and capacitor.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the BD pin is connected to an external voltage higher than 3V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN/SS pin is used to place the LT3682 in shutdown, disconnecting the output and reducing the input current to less than 1µA.

The switch driver operates from either the input or from the BOOST pin. An external capacitor and the internal boost diode are used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation.

To further optimize efficiency, the LT3682 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 75µA in a typical application.

The oscillator reduces the LT3682's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during startup and overload conditions.

Internal circuitry monitors the current flowing through the catch diode via the DA pin and delays the generation of new switch pulses if this current is too high (above 1.6A nominal). This mechanism also protects the part during short-circuit and overload conditions by keeping the current through the inductor under control.

The LT3682 contains a power good comparator which trips when the FB pin is at 90% of its regulated value. The PG output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. Power good is valid when the LT3682 is enabled and V_{IN} is above the minimum input voltage.

The LT3682 has an overvoltage protection feature which disables switching action when the V_{IN} goes above 39V typical (36V minimum) during transients. When switching is disabled, the LT3682 can safely sustain transient input voltages up to 60V.

APPLICATIONS INFORMATION

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

Setting the Switching Frequency

The LT3682 uses a constant frequency PWM architecture that can be programmed to switch from 250kHz to 2.2MHz by using a resistor tied from the R_T pin to ground. A table showing the necessary R_T value for a desired switching frequency is in Figure 1.

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.25	158
0.3	127
0.4	90.9
0.5	71.5
0.6	57.6
0.7	47.5
0.8	40.2
0.9	34
1.0	29.4
1.2	22.6
1.4	18.2
1.6	14.7
1.8	12.1
2.0	9.76
2.2	8.06

Figure 1. Switching Frequency vs. R_T Value

Operating Frequency Tradeoffs

Selection of the operating frequency is a tradeoff between efficiency, component size, minimum dropout voltage, and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, lower maximum input voltage, and higher dropout voltage. The highest acceptable switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_D}{t_{ON(MIN)}(V_{IN} - V_{SW} + V_D)}$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.5V) and V_{SW} is the internal switch drop (~0.5V at max load). This equation shows that slower switching frequency is necessary to safely accommodate high V_{IN}/V_{OUT} ratio. Also, as shown in the Input Voltage Range section, lower frequency allows a lower dropout voltage. Input voltage range depends on the switching frequency because the LT3682 switch has finite minimum on and off times. An internal timer forces the switch to be off for at least $t_{OFF(MIN)}$ per cycle; This timer has a maximum value of 210ns over temp. On the other hand, delays associated with turning off the power switch dictate the minimum on time $t_{ON(MIN)}$ before the switch can be turned off; $t_{ON(MIN)}$ has a maximum value of 150ns over temp. The minimum and maximum duty cycles that can be achieved taking minimum on and off times into account are:

$$DC_{MIN} = f_{SW} t_{ON(MIN)}$$

$$DC_{MAX} = 1 - f_{SW} t_{OFF(MIN)}$$

where f_{SW} is the switching frequency, the $t_{ON(MIN)}$ is the minimum switch on time (150ns), and the $t_{OFF(MIN)}$ is the minimum switch off time (210ns). These equations show that duty cycle range increases when switching frequency is decreased.

A good choice of switching frequency should allow adequate input voltage range (see Input Voltage Range section) and keep the inductor and capacitor values small.

Input Voltage Range

The minimum input voltage is determined by either the LT3682's minimum operating voltage of ~3.6V (V_{BD} > 3V) or by its maximum duty cycle (see equation in Operating

APPLICATIONS INFORMATION

Frequency Tradeoffs section). The minimum input voltage due to duty cycle is:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_D}{1 - f_{SW} t_{OFF(MIN)}} - V_D + V_{SW}$$

where $V_{IN(MIN)}$ is the minimum input voltage, and $t_{OFF(MIN)}$ is the minimum switch off time (210ns). Note that higher switching frequency will increase the minimum input voltage. If a lower dropout voltage is desired, a lower switching frequency should be used.

The maximum input voltage for LT3682 applications depends on switching frequency, the Absolute Maximum Ratings of the V_{IN} and BOOST pins, and the operating mode. The LT3682 can operate from continuous input voltages up to 36V. Input voltage transients of up to 60V are also safely withstood. However, note that while V_{IN}>V_{OVLO} (39V typical), the LT3682 will stop switching, allowing the output to fall out of regulation.

For a given application where the switching frequency and the output voltage are already fixed, the maximum input voltage that guarantees optimum output voltage ripple for that application can be found by applying the following expression:

$$V_{IN(MAX)} = \frac{V_D + V_{OUT}}{f_{SW} t_{ON(MIN)}} - V_D + V_{SW}$$

where $V_{IN(MAX)}$ is the maximum operating input voltage, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.5V), V_{SW} is the internal switch drop (~0.5V at max load), f_{SW} is the switching frequency (set by R_T), and $t_{ON(MIN)}$ is the minimum switch on time (~150ns). Note that a higher switching frequency will reduce the maximum operating input voltage. Conversely, a lower switching frequency will be necessary to achieve optimum operation at high input voltages.

Special attention must be paid when the output is in start-up, short-circuit, or other overload conditions. In these cases, the LT3682 tries to bring the output in regulation by driving lots of current into the output load. During these events, the inductor peak current might easily reach and even exceed the maximum current limit of the LT3682, especially in those cases where the switch already operates at minimum on time. The circuitry monitoring the current through the catch diode via the DA pin prevents the switch from turning on again if the inductor valley current is above 1.6A nominal. In these cases, the inductor peak current is therefore the maximum current limit of the LT3682 plus the additional current overshoot during the turn off delay due to minimum on time:

$$I_{L(PEAK)} = 2A + \frac{V_{IN(MAX)} - V_{OUTOL}}{L} \bullet t_{ON(MIN)}$$

where $I_{L(PEAK)}$ is the peak inductor current, $V_{IN(MAX)}$ is the maximum expected input voltage, L is the inductor value, $t_{ON(MIN)}$ is the minimum on time and V_{OUTOL} is the output voltage under the overload condition. The part is robust enough to survive prolonged operation under these conditions as long as the peak inductor current does not exceed 3.5A. Inductor current saturation and excessive junction temperature may further limit performance.

If the output is in regulation and no short-circuit, startup, or overload events are expected, then input voltage transients of up to V_{OVLO} are acceptable regardless of the switching frequency. In this case, the LT3682 may enter pulse skipping operation where some switching pulses are skipped to maintain output regulation. In this mode the output voltage ripple and inductor current ripple will be higher than in normal operation.

Input voltage transients above V_{OVLO} and up to 60V can be tolerated. However, since the part will stop switching during these transients, the output will fall out of regulation and the output capacitor may eventually be completely discharged. This case must be treated then as a start-up condition as soon as V_{IN} returns to values below V_{OVLO} and the part starts switching again.

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = (V_{OUT} + V_D) \bullet \frac{1.8}{f_{SW}}$$

APPLICATIONS INFORMATION

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.5V) and L is the inductor value in µH.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be about 30% higher. To keep the efficiency high, the series resistance (DCR) should be less than 0.1Ω, and the core material should be intended for high frequency applications. Table 1 lists several vendors and suitable types.

For robust operation in fault conditions (start-up or short circuit) and high input voltage (>30V), the saturation current should be chosen high enough to ensure that the inductor peak current does not exceed 3.5A. For example, an application running from an input voltage of 36V using a 10µH inductor with a saturation current of 2.5A will tolerate the mentioned fault conditions.

The optimum inductor for a given application may differ from the one indicated by this simple design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. If your load is lower than the maximum load current, then you can relax the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that if the inductance differs from the simple rule above, then the maximum load current will depend on input voltage. In addition, low inductance may result in discontinuous mode operation, which further reduces maximum load current. For details of maximum output current and discontinuous mode operation, see Linear Technology's Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillations:

$$L_{MIN} = (V_{OUT} + V_D) \bullet \frac{1.2}{f_{SW}}$$

The current in the inductor is a triangle wave with an average value equal to the load current. The peak inductor and switch current is:

$$I_{SW(PEAK)} = I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

where $I_{L(PEAK)}$ is the peak inductor current, $I_{OUT(MAX)}$ is the maximum output load current, and ΔI_L is the inductor ripple current. The LT3682 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3682 will deliver depends on the switch current limit, the inductor value and the input and output voltages.

When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = \frac{(1-DC) \bullet (V_{OUT} + V_D)}{L \bullet f_{SW}}$$

where f_{SW} is the switching frequency of the LT3682, DC is the duty cycle and L is the value of the inductor.

To maintain output regulation, the inductor peak current must be less than the LT3682's switch current limit I_{LIM}. If SYNC pin is grounded I_{LIM} is at least 1.45A at low duty cycles and decreases to 1.1A at DC = 90%. If SYNC pin is tied to 0.8V or more or if it is tied to a clock source for synchronization I_{LIM} is at least 1.18A at low duty cycles and decreases to 0.85A at DC = 90%. The maximum output current is also a function of the chosen inductor value and can be approximated by the following expressions depending on the SYNC pin configuration:

For SYNC pin grounded:

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} = 1.45A \bullet (1 - 0.24 \bullet DC) - \frac{\Delta I_L}{2}$$

APPLICATIONS INFORMATION

For SYNC pin tied to 0.8V or more, or tied to a clock source for synchronization:

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} = 1.18A \bullet (1 - 0.29 \bullet DC) - \frac{\Delta I_L}{2}$$

Choosing an inductor value so that the ripple current is small will allow a maximum output current near the switch current limit.

Table 1. Inductor Vendors

VENDOR	URL	PART SERIES	TYPE
Murata	www.murata.com	LQH55D	Open
TDK	www.componenttdk.com	SLF7045 SLF10145	Shielded Shielded
Toko	www.toko.com	D62CB D63CB D73C D75F	Shielded Shielded Shielded Open
Coilcraft	www.coilcraft.com	MSS7341 MSS1038	Shielded Shielded
Sumida	www.sumida.com	CR54 CDRH74 CDRH6D38 CR75	Open Shielded Shielded Open

One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors, and choose one to meet cost or space goals. Then use these equations to check that the LT3682 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when I_{OUT} is less than $\Delta I_L/2$.

Input Capacitor

Bypass the input of the LT3682 circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 2.2µF to 10µF ceramic capacitor is adequate to bypass the LT3682 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a lower performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3682 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 2.2µF capacitor is capable of this task, but only if it is placed close to the LT3682 (see the PCB Layout section for more information). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3682. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LT3682 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3682's voltage rating. For details see Application Note 88.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3682 to produce the DC output. In this role it determines the output ripple, and low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3682's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{50}{V_{OUT} f_{SW}}$$

where f_{SW} is in MHz, and C_{OUT} is the recommended output capacitance in µF. Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value capacitor if the compensation network is also adjusted to maintain the loop bandwidth. A lower value of output capacitor can be used to save space and cost but transient performance will suffer. See the Frequency Compensation section to choose an appropriate compensation network.

APPLICATIONS INFORMATION

Table 2. Capacitor Vendors

VENDOR	PHONE	URL	PART SERIES	COMMENTS
Panasonic	(714) 373-7366	www.panasonic.com	Ceramic, Polymer, Tantalum	EEF Series
Kemet	(864) 963-6300	www.kemet.com	Ceramic, Tantalum	T494, T495
Sanyo	(408)749-9714	www.sanyovideo.com	Ceramic, Polymer, Tantalum	POSCAP
Murata	(408)436-1300	www.murata.com	Ceramic	
AVX		www.avxcorp.com	Ceramic, Tantalum	TPS Series
Taiyo Yuden	(864)963-6300	www.taiyo-yuden.com	Ceramic	

When choosing a capacitor, look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor, or one with a higher voltage rating, may be required. High performance tantalum or electrolytic capacitors can be used for the output capacitor. Low ESR is important, so choose one that is intended for use in switching regulators. The ESR should be specified by the supplier, and should be 0.05Ω or less. Such a capacitor will be larger than a ceramic capacitor and will have a larger capacitance, because the capacitor must be large to achieve low ESR. Table 2 lists several capacitor vendors.

Diode Selection

The catch diode (D1 from block diagram) conducts current only during switch off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT} \bullet (1 - DC)$$

where DC is the duty cycle. The only reason to consider a diode with larger current rating than necessary for nominal operation is for the case of shorted or overloaded output conditions. For the worst case of shorted output the diode average current will then increase to a value that depends on the following internal parameters: switch current limit, catch diode (DA pin) current threshold and minimum on-time. The worst case (taking maximum values for the above mentioned parameters) is given by the following expression:

$$I_{D(AVG)MAX} = 2A + \frac{1}{2} \bullet \frac{V_{IN}}{L} \bullet 150ns$$

Peak reverse voltage is equal to the regulator input voltage if it is below the overvoltage protection threshold. This feature keeps the switch off for V_{IN} > OVLO (41V maximum). For inputs up to the maximum operating voltage of 36V, use a diode with a reverse voltage rating greater than the input voltage. If transients at the input of up to 60V are expected, use a diode with a reverse voltage rating only higher than the maximum OVLO of 41V. Table 3 lists several Schottky diodes and their manufacturers. If operating at high ambient temperatures, consider using a Schottky with low reverse leakage.

Audible Noise

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can sometimes cause problems when used with the LT3682 due to their piezoelectric nature. When in Burst Mode operation, the LT3682's switching frequency depends on the load current, and at very light loads the LT3682 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT3682 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

APPLICATIONS INFORMATION

Table 3. Schottky Diodes

PART NUMBER	V_R (V)	I_{AVE} (A)	V_F at 1A (mV)	V_F at 2A (mV)
On Semiconducor				
MBR0520L	20	0.5		
MBR0540	40	0.5	620	
MBRM120E	20	1	530	595
MBRM140	40	1	550	
Diodes Inc.				
B0530W	30	0.5		
B0540W	40	0.5	620	
B120	20	1	500	
B130	30	1	500	
B140	40	1	500	
B150	50	1	700	
B220	20	2		500
B230	30	2		500
B140HB	40	1		
DFLS240L	40	2		500
DFLS140	40	1.1	510	
B240	40	2		500
Central Semiconductor				
CMSH1 – 40M	40	1	500	
CMSH1 – 60M	60	1	700	
CMSH1 – 40ML	40	1	400	
CMSH2 – 40M	40	2		550
CMSH2 – 60M	60	2		700
CMSH2 – 40L	40	2		400
CMSH2 – 40	40	2		500
CMSH2 – 60	60	2		700

Frequency Compensation

The LT3682 uses current mode control to regulate the output. This simplifies loop compensation. In particular, the LT3682 does not require the ESR of the output capacitor for stability, so you are free to use ceramic capacitors to achieve low output ripple and small circuit size. Frequency compensation is provided by the components tied to the V_C pin, as shown in Figure 2. Generally a capacitor (C_C) and a resistor (R_C) in series to ground are used. In addition, there may be a lower value capacitor in parallel. This capacitor (C_F) is used to filter noise at the switching frequency, and is required only if a phase-lead capacitor (C_{PL}) is used or if the output capacitor has high ESR.

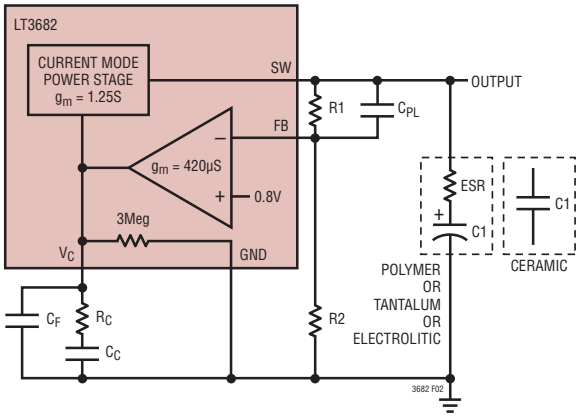


Figure 2. Model for Loop Response

Loop compensation determines the stability and transient performance. Optimizing the design of the compensation network depends on the application and type of output capacitor. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load. Figure 2 shows an equivalent circuit for the LT3682 control loop. The error amplifier is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C pin. Note that the output capacitor integrates this current, and that the

APPLICATIONS INFORMATION

capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. In most cases a zero is required and comes from either the output capacitor ESR or from a resistor R_C in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (C_{PL}) across the feedback divider may improve the transient response. Figure 3 shows the transient response when the load current is stepped from 300mA to 650mA and back to 300mA.

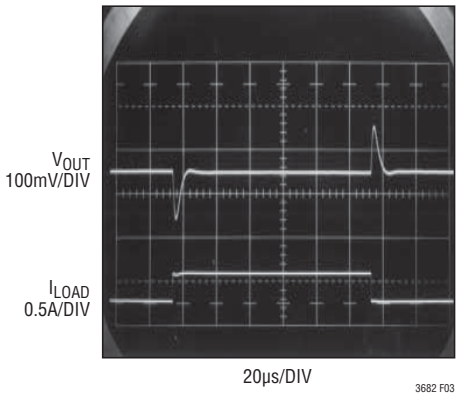


Figure 3. Transient Load Response of the LT3682. 3.3V_{OUT} Typical Application with V_{IN} = 12V as the Load Current is Stepped from 300mA to 650mA.

Low Ripple Burst Mode and Pulse-Skip Mode

The LT3682 is capable of operating in either Low Ripple Burst Mode or Pulse-Skip Mode which are selected using the SYNC pin. See the Synchronization section for more information.

To enhance efficiency at light loads, the LT3682 can be operated in Low Ripple Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LT3682 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. Because the LT3682 delivers power to the output with single, low current pulses, the output ripple is kept below 15mV for a typical application. In addition, V_{IN} and BD quiescent currents are reduced to typically 35µA and 55µA respectively during the sleep time. As the load current decreases towards a no load condition, the percentage of time that the LT3682 operates in sleep mode increases and the average input current is greatly reduced resulting in high efficiency even at very low loads. (See Figure 4). At higher output loads (above about 70mA for the front page application) the LT3682 will be running at the frequency programmed by the R_T resistor, and will be operating in standard PWM mode. The transition between PWM and Low Ripple Burst Mode is seamless, and will not disturb the output voltage.

If low quiescent current is not required, tie SYNC high to select pulse-skip mode. The benefit of this mode is that the LT3682 will enter full frequency standard PWM operation at a lower output load current than when in Burst Mode. The front page application circuit will switch at full frequency at output loads higher than about 30mA. The maximum load current that the LT3682 can supply is reduced when SYNC is high.

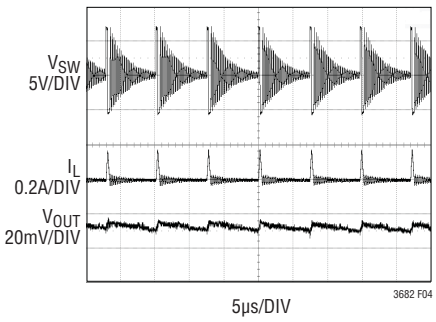


Figure 4. Burst Mode Operation

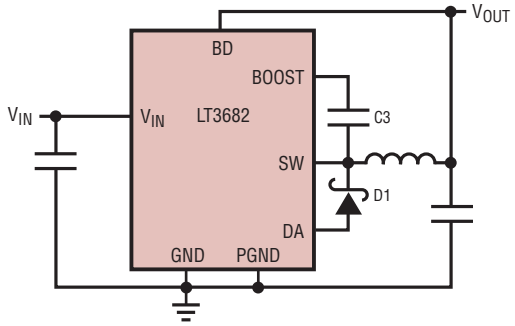
APPLICATIONS INFORMATION

BOOST and BD Pin Considerations

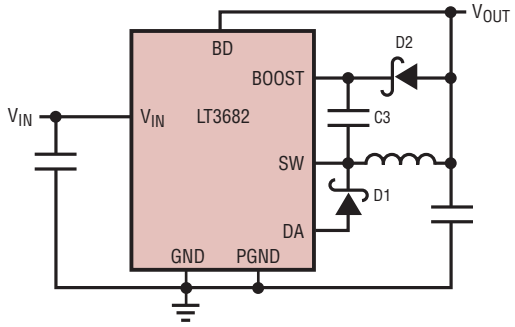
Capacitor C3 and the internal boost Schottky diode (see the Block Diagram) are used to generate a boost voltage that is higher than the input voltage. In most cases a 0.22µF capacitor will work well. Figure 5 shows three ways to arrange the boost circuit. The BOOST pin must be more than 2.3V above the SW pin for best efficiency. For outputs of between 3V and 8V, the standard circuit (Figure 5a) is best. For outputs between 2.8V and 3V, use a 1µF boost capacitor. A 2.5V output presents a special case because it is marginally adequate to support the boosted drive stage while using the internal boost diode. For reliable BOOST pin operation with 2.5V outputs use a good external Schottky diode (such as the ON Semi MBR0540), and a 1µF boost capacitor (see Figure 5b). For lower output voltages the boost diode can be tied to the input (Figure 5c), or to another supply greater than 2.8V. Keep in mind that a minimum input voltage of 4.3V is required if the voltage at the BD pin is smaller than 3V. Tying BD to V_{IN} reduces the maximum input voltage to 25V. The circuit in Figure 5a is more efficient because the BOOST pin current and BD pin quiescent current come from a lower voltage source. You must also be sure that the maximum voltage ratings of the BOOST and BD pins are not exceeded.

As mentioned, a minimum of 2.5V across the BOOST capacitor is required for proper operation of the internal BOOST circuitry to provide the base current for the power NPN switch. For BD pin voltages higher than 3V, the excess voltage across the BOOST capacitor does not bring an increase in performance but dissipates additional power in the internal BOOST circuitry instead. The BOOST circuitry tolerates reasonable amounts of power, however excessive power dissipation on this circuitry may impair reliability. For reliable operation, use no more than 8V on the BD pin for the circuit in Figure 5a. For higher output voltages, make sure that there is no more than 8V at the BD pin either by connecting it to another available supply higher than 3V or by using a Zener diode between V_{OUT} and BD to maintain the BD pin voltage between 3V and 8V.

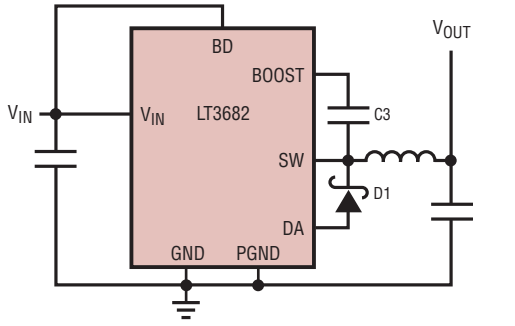
The minimum operating voltage of an LT3682 application is limited by the minimum input voltage and by the maximum duty cycle as outlined previously. For proper startup, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or the LT3682 is turned on with its RUN/SS pin when the output



(5a) For V_{OUT} > 2.8V; $V_{IN(MIN)}$ = 4.3V if V_{OUT} < 3V



(5b) For 2.5V < V_{OUT} < 2.8V; $V_{IN(MIN)}$ = 4.3V



(5c) For V_{OUT} < 2.5V; $V_{IN(MAX)}$ = 25V

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Figure 5. Three Circuits For Generating The Boost Voltage

APPLICATIONS INFORMATION

is already in regulation, then the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. Figure 6 shows a plot of minimum load to start and to run as a function of input voltage. In many cases the discharged output capacitor will present a load to the switcher, which will allow it to start. The plots show the worst-case situation where V_{IN} is ramping very slowly. For lower start-up voltage, the boost diode can be tied to V_{IN}; however, this restricts the input range to one-half of the absolute maximum rating of the BOOST pin. At light loads, the inductor current becomes discontinuous and the effective duty cycle can be very high. This reduces the minimum input voltage to approximately 300mV above V_{OUT}. At higher load currents, the inductor current is continuous and the duty cycle is limited by the maximum duty cycle of the LT3682, requiring a higher input voltage to maintain regulation.

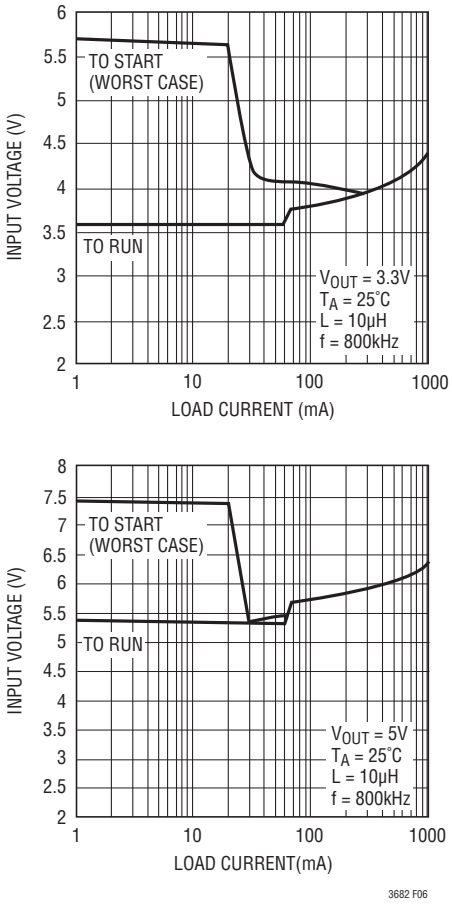


Figure 6. The Minimum Input Voltage Depends on Output Voltage, Load Current and Boost Circuit

Soft-Start

The RUN/SS pin can be used to soft-start the LT3682, reducing the maximum input current during start-up. The RUN/SS pin is driven through an external RC network to create a voltage ramp at this pin. Figure 7 shows the startup and shut-down waveforms with the soft-start circuit. By choosing a large RC time constant, the peak start-up current can be reduced to the current that is required to regulate the output, with no overshoot. Choose the value of the resistor so that it can supply 20µA when the RUN/SS pin reaches 2.5V.

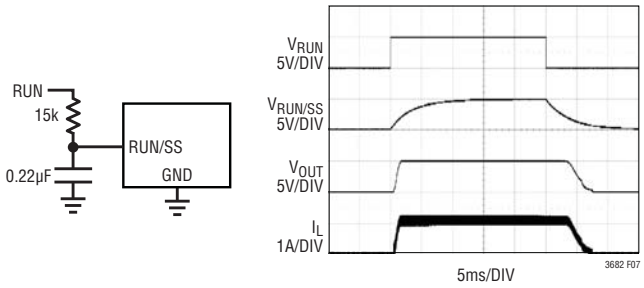


Figure 7. To Soft-Start the LT3682, Add a Resistor and Capacitor to the RUN/SS Pin

APPLICATIONS INFORMATION

Synchronization

To select Low Ripple Burst Mode operation, tie the SYNC pin below 0.3V (this can be ground or a logic output).

Synchronizing the LT3682 oscillator to an external frequency can be done by connecting a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.3V and peaks that are above 0.8V (up to 6V).

The LT3682 will not enter Burst Mode at low output loads while synchronized to an external clock, but instead will skip pulses to maintain regulation.

The maximum load current that the part can supply is reduced when a clock signal is applied to SYNC.

The LT3682 may be synchronized over a 300kHz to 2.2MHz range. The R_T resistor should be chosen to set the LT3682 switching frequency 20% below the lowest synchronization input. For example, if the synchronization signal will be 360kHz, the R_T should be chosen for 300kHz. To assure reliable and safe operation the LT3682 will only synchronize when the output voltage is near regulation as indicated by the PG flag. It is therefore necessary to choose a large enough inductor value to supply the required output current at the frequency set by the R_T resistor. See the Inductor Selection section for more information. It is also important to note that slope compensation is set by the R_T value: to avoid subharmonics, calculate the minimum inductor value using the frequency determined by R_T.

Shorted and Reversed Input Protection

If the inductor is chosen so that it won't saturate excessively, the LT3682 will tolerate a shorted output. When operating in short-circuit condition, the LT3682 will reduce its frequency until the valley current is at a typical value of 1.6A (see Figure 8). There is another situation to consider in systems where the output will be held high when the input to the LT3682 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LT3682's output. If the V_{IN} pin is allowed to float and the RUN/SS pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT3682's internal circuitry will pull its quiescent current through its SW pin. This is fine if your system can tolerate a few mA in this state. If you ground the RUN/SS pin, the SW pin current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LT3682 can pull large currents from the output through the SW pin and the V_{IN} pin. Figure 9 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

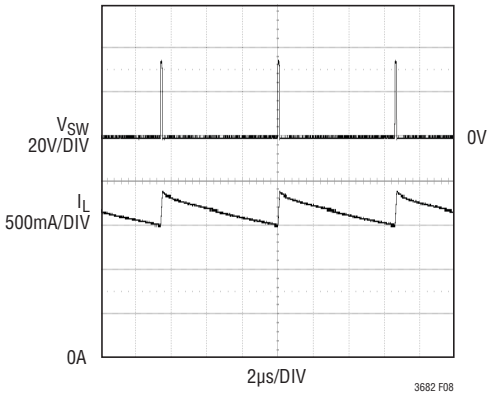


Figure 8. The LT3682 Reduces its Frequency to Protect Against Shorted Output with 36V Input

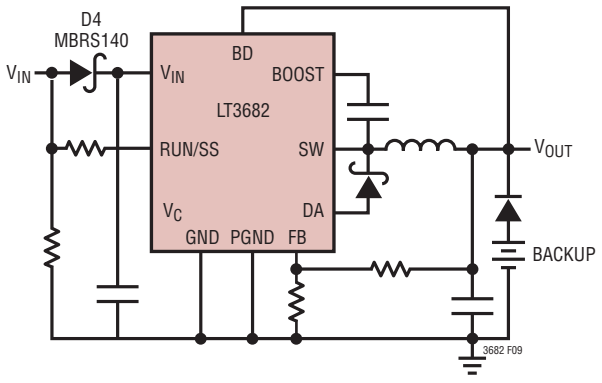


Figure 9. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LT3682 Runs Only When the Input is Present

APPLICATIONS INFORMATION

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 10 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT3682's V_{IN}, SW and PGND pins, the catch diode and the input capacitor (C_{IN}). The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor (C_{OUT}), should be placed on the same side of the circuit board, and their connections should be made on that layer. All connections to GND should be made at a common star ground point or directly to a local, unbroken ground plane below these components. The SW and BOOST nodes should be laid out carefully to avoid interference. If the part is synchronized externally using the SYNC pin, care must be taken laying out this signal to avoid interference with sensitive nodes, especially V_C, FB, and R_T. Finally, keep the FB, R_T, and V_C nodes small so that the ground traces will shield them from the SW and BOOST nodes. The exposed pad Pin 13 on the bottom of the package acts as a heat sink and must be soldered to the ground node. To keep thermal resistance low, extend the ground plane as much as possible and add thermal vias under and near the LT3682 to any additional ground planes within the circuit board and on the bottom side. Keep in mind that the thermal design must keep the junctions of the IC below the specified absolute maximum temperature of 125°C.

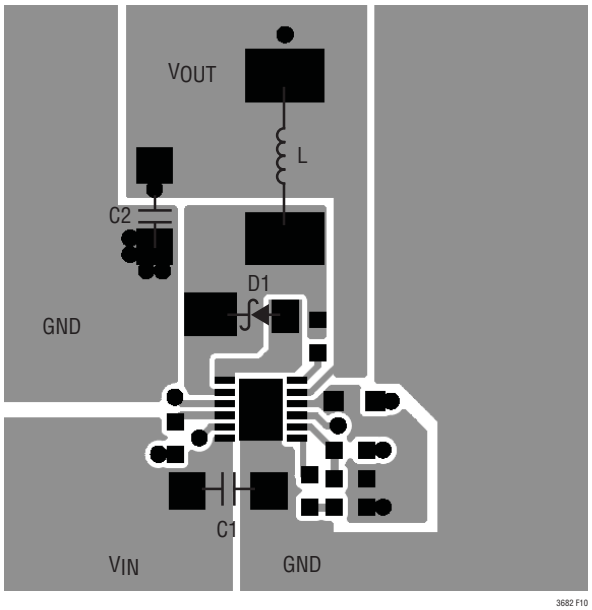


Figure 10. A Good PCB Layout Ensures Proper, Low EMI Operation

High Temperature Considerations

The PCB must provide heat sinking to keep the LT3682 cool. The exposed pad on the bottom of the package must be soldered to a copper area, which in turn should be tied to large copper layers below with thermal vias; these layers will spread the heat dissipated by the LT3682. Place additional vias to reduce thermal resistance further. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to θ_{JA} = 35°C/W or less. With 100 LFPM airflow, this resistance can fall by another 25%. Further increases in airflow will lead to lower thermal resistance. Because of the large output current capability of the LT3682, it is possible to dissipate enough heat to raise the junction temperature beyond the absolute maximum of 125°C. When operating at high ambient temperatures, the maximum load current should be derated as the ambient temperature approaches these maximums. If the junction temperature reaches the thermal shutdown threshold, the part will stop switching to prevent internal damage due to overheating.

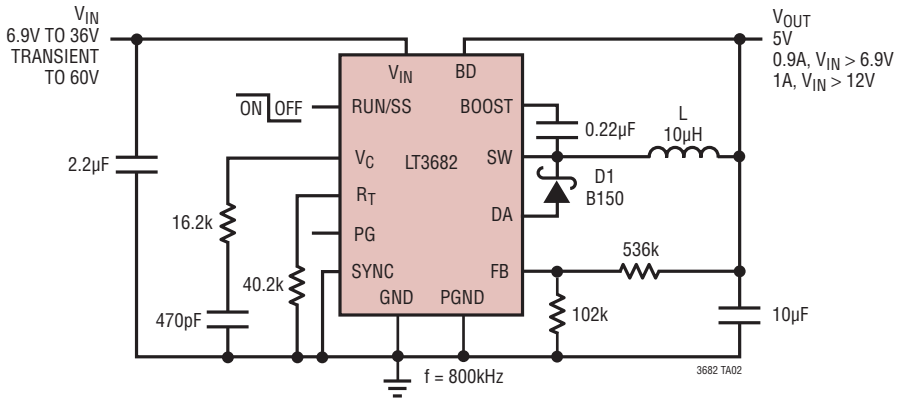
Power dissipation within the LT3682 can be estimated by calculating the total power loss from an efficiency measurement. The die temperature is calculated by multiplying the LT3682 power dissipation by the thermal resistance from junction to ambient.

Other Linear Technology Publications

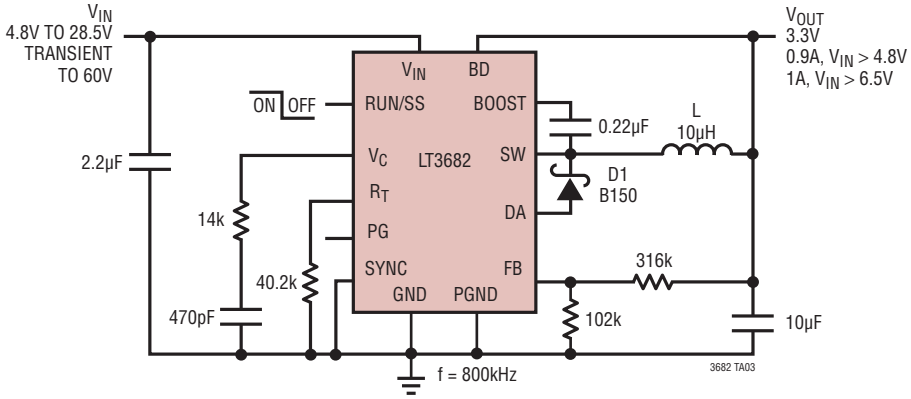
Application Notes 19, 35 and 44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note 318 shows how to generate a bipolar output supply using a buck regulator.

TYPICAL APPLICATIONS

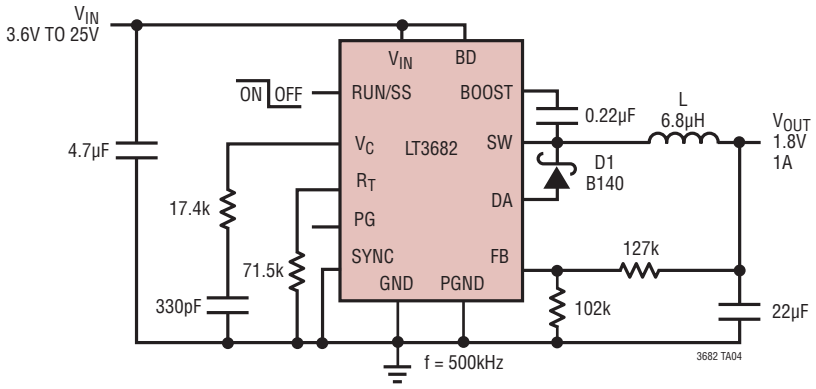
5V Step-Down Converter



3.3V Step-Down Converter

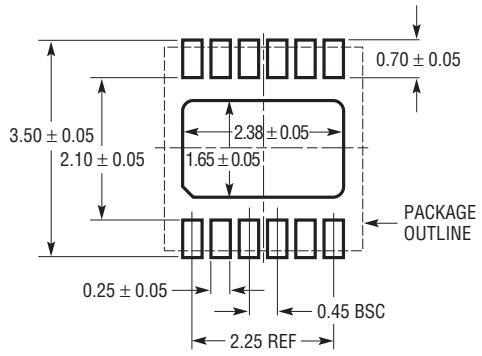


1.8V Step-Down Converter

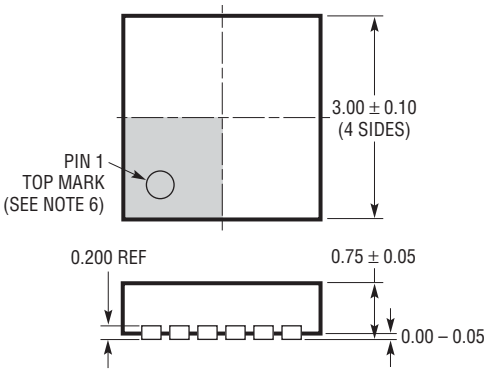


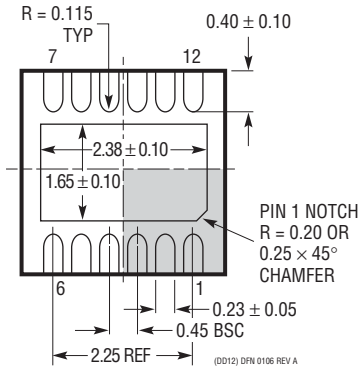
PACKAGE DESCRIPTION

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



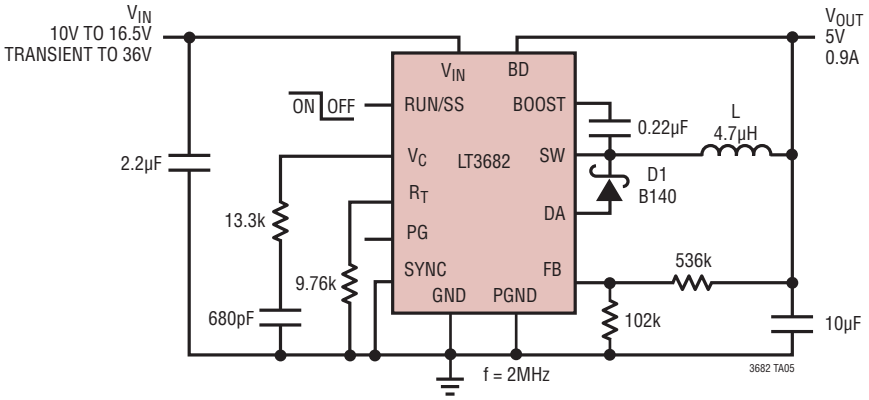


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATIONS

5V, 2MHz Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1766	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 5.5V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5mA, I_{SD} = 25µA, TSSOP16E Package
LT1767	25V, 1.2A (I_{OUT}), 1.2MHz High Efficiency Step-Down DC/DC Converter	V_{IN} = 3V to 25V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 1mA, I_{SD} < 6µA, MS8E Package
LT1933	500mA (I_{OUT}), 500kHz Step-Down DC/DC Converter	V_{IN} = 3.6V to 36V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 1.6mA, I_{SD} < 1µA, ThinSOT™ Package
LT1936	36V, 1.4A (I_{OUT}), 500kHz High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 36V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 1.9mA, I_{SD} < 1µA, MS8E Package
LT1940	Dual 25A, 1.4A (I_{OUT}), 1.1MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 25V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 3.8mA, I_{SD} < 30µA, TSSOP16E Package
LT1976/LT1967	60V, 1.2A (I_{OUT}), 200kHz/500kHz, High Efficiency Step-Down DC/DC Converters with Burst Mode Operation	V_{IN} = 3.3V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 100µA, I_{SD} < 1µA, TSSOP16E Package
LT3434/LT3435	60V, 2.4A (I_{OUT}), 200kHz/500kHz, High Efficiency Step-Down DC/DC Converters with Burst Mode Operation	V_{IN} = 3.3V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 100µA, I_{SD} < 1µA, TSSOP16 Package
LT3437	60V, 400mA (I_{OUT}), Micropower Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} = 3.3V to 60V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 100µA, I_{SD} < 1µA, 3mm × 3mm DFN10 and TSSOP16E Packages
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} = 3.6V to 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 3mm DFN10 and MSOP10E Packages
LT3481	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} = 3.6V to 34V, $V_{OUT(MIN)}$ = 1.26V, I_Q = 50µA, I_{SD} < 1µA, 3mm × 3mm DFN10 and MSOP10E Packages
LT3493	36V, 1.4A (I_{OUT}), 750kHz High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.9mA, I_{SD} < 1µA, 2mm × 3mm DFN8 and MSOP8E Packages
LT3505	36V with Transient Protection to 40V, 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 34V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 2mA, I_{SD} = 2µA, 3mm × 3mm DFN6 Package
LT3508	36V with Transient Protection to 40V, Dual 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.7V to 37V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 4.6mA, I_{SD} = 1µA, 4mm × 4mm QFN24 and TSSOP16E Packages
LT3684	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 34V, $V_{OUT(MIN)}$ = 1.26V, I_Q = 850mA, I_{SD} < 1µA, 3mm × 3mm DFN10 and MSOP10E Packages
LT3685	36V with Transient Protection to 60V, Dual 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} = 3.6V to 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70mA, I_{SD} < 1µA, 3mm × 3mm DFN10 and MSOP10E Packages

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- Shortage Management
- Alternative Solution
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