THE DATASHEET OF

LTC2953IDD-2#TRPBF

Push Button On/Off Controller with Voltage Monitoring

FEATURES

- **Wide Operating Voltage Range: 2.7V to 27V**
- **Push Button Control of System Power**
- **Low Supply Current: 14µA**
- **Power Fail Comparator Generates Warning**
- **UVLO Comparator Gracefully Latches Power Off**
- **Adjustable Supply Monitor with 200ms Reset**
- Adjustable Power Down Timer
- Low Leakage EN Output (LTC2953-1) Allows DC/DC Converter Control
- High Voltage $\overline{EN}$ Output (LTC2953-2) Allows Circuit Breaker Control
- Simple Interface Allows Orderly System Power Up and Power Down
- ±1.5% Threshold Tolerances
- ±10kV ESD HBM on $\overline{PB}$ Input
- 12-Pin 3mm × 3mm DFN

APPLICATIONS

- Push Button Power Path Control
- Battery Power Supervisor
- Portable Instrumentation, PDA
- Blade Servers
- Desktop and Notebook Computers

DESCRIPTION

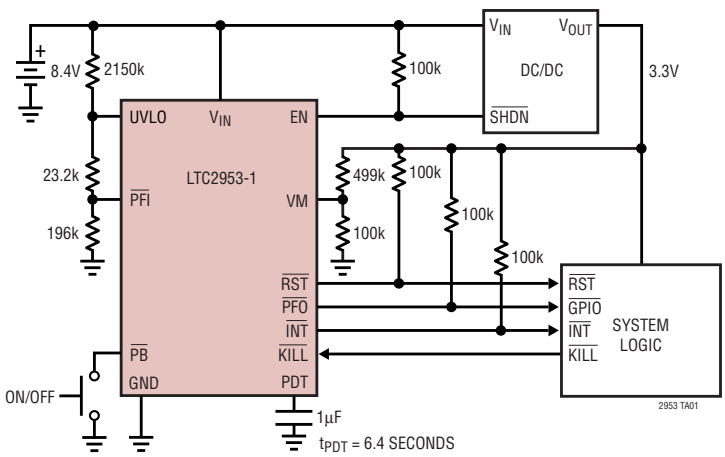
The LTC®2953 is a push button On/Off controller that manages system power via a push button interface. An enable output toggles system power while an interrupt output provides debounced push button status. The interrupt output can be used in menu driven applications to request a system power down.

The LTC2953 also features input and output power supply monitors. An uncommitted power fail comparator provides real time input monitor information, while a de-glitched under voltage lockout comparator gracefully initiates a system power down. The under voltage lockout comparator prevents the system from powering from a low power supply.

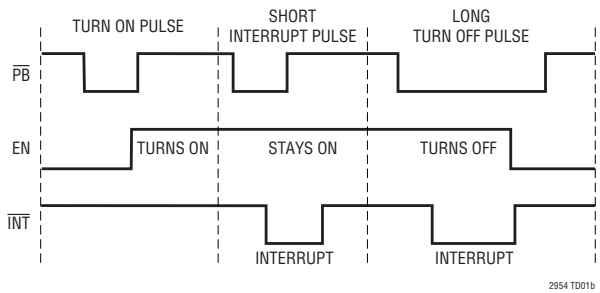
The adjustable supply monitor input is compared against an accurate internal 0.5V reference. The reset output remains low until the supply monitor input has been in compliance for 200ms.

The LTC2953 operates over a wide 2.7V to 27V input voltage range and draws only 14µA of current. Two versions of the part accommodate either positive or negative enable polarities.

TYPICAL APPLICATION



Push Button On/Off Control with Interrupt

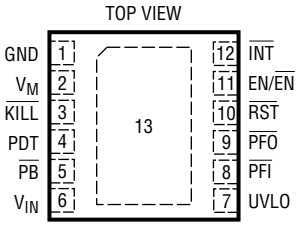


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{IN}) ..... –0.3V to 33V
Input Voltages
  $\overline{PB}$, $\overline{PFI}$, UVLO..... –6V to 33V
  VM..... –0.3V to 20V
  $\overline{KILL}$..... –0.3V to 10V
  PDT..... –0.3V to 2.7V
Output Voltages
  EN/$\overline{EN}$, $\overline{PFO}$..... –0.3V to 50V
  $\overline{RST}$, $\overline{INT}$ ..... –0.3V to 10V
Operating Temperature Range
  LTC2953C ..... 0°C to 70°C
  LTC2953I ..... –40°C to 85°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) PCB GROUND CONNECTION OPTIONAL

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2953CDD-1#PBF	LTC2953CDD-1#TRPBF	LCWT	12-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2953CDD-2#PBF	LTC2953CDD-2#TRPBF	LCQT	12-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2953IDD-1#PBF	LTC2953IDD-1#TRPBF	LCWT	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2953IDD-2#PBF	LTC2953IDD-2#TRPBF	LCQT	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 2.7V to 27V, unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Pin (V_{IN})							
V_{IN}	Supply Voltage Range	Steady State Operation	●	2.7		27	V
I_{IN}	V_{IN} Supply Current	V_{IN} = 2.7V to 27V	●		14	26	µA
V_{UVL}	V_{IN} Undervoltage Lockout	V_{IN} Falling	●	2.2	2.3	2.5	V
Push Button, Enable ($\overline{PB}$, EN/$\overline{EN}$)							
$V_{PB(MIN, MAX)}$	$\overline{PB}$ Operating Voltage Range	Single-Ended	●	–1		27	V
I_{PB}	$\overline{PB}$ Input Current	2.5V < V_{PB} < 27V	●			±1	µA
		V_{PB} = 1V	●	–1	–6	–12	µA
		V_{PB} = 0.6V	●	–3	–9	–15	µA
$V_{PB(VTH)}$	$\overline{PB}$ Input Threshold	$\overline{PB}$ Falling	●	0.6	0.8	1	V
$V_{PB(VOC)}$	$\overline{PB}$ Open Circuit Voltage	I_{PB} = –1µA	●	1	1.6	2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 2.7V to 27V, unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{EN(LKG)}$	EN/$\overline{EN}$ Leakage Current	$V_{EN/\overline{EN}}$ = 1V, Sink Current Off $V_{EN/\overline{EN}}$ = 40V, Sink Current Off	● ●			±0.1 ±1	µA µA
$V_{EN(VOL)}$	EN/$\overline{EN}$ Voltage Output Low	$I_{EN/\overline{EN}}$ = 500µA	●		0.11	0.4	V
$t_{EN,\ Lock\ Out}$	EN/$\overline{EN}$ Lock Out Time (Note 3)	Enable Released → Enable Asserted	●	52	64	82	ms
On/Off Timing Pins ($\overline{PB}$, UVLO, PDT, $\overline{INT}$)							
$t_{DB,\ ON}$	Turn On Debounce Time	$\overline{PB}$ Falling → Enable Asserted	●	26	32	41	ms
$I_{PDT(PU)}$	PDT Pull Up Current	V_{PDT} = 0V	●	–2.4	–3	–3.6	µA
$I_{PDT(PD)}$	PDT Pull Down Current	V_{PDT} = 1.3V	●	2.4	3	3.6	µA
$t_{DB,\ OFF}$	Turn Off Interrupt Debounce Time	$\overline{PB}$, UVLO Falling → $\overline{INT}$ Falling	●	26	32	41	ms
$t_{PD,\ Min}$	Internal $\overline{PB}$ Power Down Delay Time (Note 4)	$\overline{PB}$, UVLO Falling → Enable Released PDT Open	●	52	64	82	ms
t_{PDT}	Additional Adjustable $\overline{PB}$ Power Down Delay Time	C_{PDT} = 1500pF	●	9	11.5	13.5	ms
$t_{INT,\ Min}$	Minimum $\overline{INT}$ Pulse Width	$\overline{INT}$ Asserted → $\overline{INT}$ Released	●	26	32	41	ms
$t_{INT,\ Max}$	Maximum $\overline{INT}$ Pulse Width	C_{PDT} = 1500pF, $\overline{INT}$ Asserted → $\overline{INT}$ Released	●	35	43.5	54.5	ms
µP Handshake Pins ($\overline{KILL}$, $\overline{INT}$)							
$V_{KILL(TH)}$	$\overline{KILL}$ Input Threshold Voltage	$\overline{KILL}$ Falling	●	0.57	0.6	0.63	V
$V_{KILL(HYST)}$	$\overline{KILL}$ Input Threshold Hysteresis		●	10	30	50	mV
$t_{KILL(PW)}$	$\overline{KILL}$ Minimum Pulse Width		●	30			µs
$t_{KILL(PD)}$	$\overline{KILL}$ Propagation Delay	$\overline{KILL}$ Falling → Enable Released	●			30	µs
$t_{KILL,\ ON\ BLANK}$	$\overline{KILL}$ Turn On Blanking (Note 5)	$\overline{KILL}$ = Low, Enable Asserted → Enable Released	●	400	512	650	ms
$I_{KILL(LKG)}$	$\overline{KILL}$ Leakage Current	V_{KILL} = 0.6V	●			±0.1	µA
$I_{INT(LKG)}$	$\overline{INT}$ Leakage Current	V_{INT} = 3V	●			±0.1	µA
$V_{INT(VOL)}$	$\overline{INT}$ Output Voltage Low	I_{INT} = 3mA	●		0.11	0.4	V
Power Fail and Voltage Monitor Pins ($\overline{PFI}$, $\overline{PFO}$, UVLO, VM, $\overline{RST}$)							
$V_{PFI(TH)}$	$\overline{PFI}$ Input Threshold Voltage	Falling	●	492	500	508	mV
$V_{UVLO(TH)}$	UVLO Input Threshold Voltage	Falling	●	492	500	508	mV
$VM_{(TH)}$	Adjustable Reset Threshold	Falling/Rising	●	492	500	508	mV
ΔV_{TH}	$\overline{PFI}$-UVLO Threshold Mismatch		●	–5	0	5	mV
$V_{PFI(HYST)}$	$\overline{PFI}$ Input Hysteresis		●	2	4	10	mV
$V_{UVLO(HYST)}$	UVLO Input Hysteresis		●	30	50	70	mV
$V_{PFO(VOL)}$	$\overline{PFO}$ Output Voltage Low	I_{PFO} = 500µA	●		0.11	0.4	V
$V_{RST(VOL)}$	$\overline{RST}$ Output Voltage Low	I = 3mA	●		0.11	0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 2.7V to 27V, unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{PFI(LKG)}$	$\overline{PFI}$ Leakage Current	V_{PFI} = 0.5V V_{PFI} = 27V	●		2	±10 ±1	nA µA
$I_{PFO(LKG)}$	$\overline{PFO}$ Leakage Current	V_{PFO} = 1V V_{PFO} = 40V	●		2	±10 ±1	nA µA
$I_{UVLO(LKG)}$	UVLO Leakage Current	V_{UVLO} = 0.5V V_{UVLO} = 27V	●		2	±10 ±1	nA µA
$I_{VM(LKG)}$	VM Input Leakage Current	VM = 0.5V	●		2	±10	nA
$I_{RST(LKG)}$	$\overline{RST}$ Output Leakage Current	V_{RST} = 3V	●			±0.1	µA
t_{PFI}	$\overline{PFI}$ Delay to $\overline{PFO}$		●	40	100	200	µs
t_{RST}	Reset Timeout Period		●	140	200	260	ms
t_{uv}	VM Under Voltage Detect to $\overline{RST}$	VM Less Than $VM_{(TH)}$ By More Than 1%			250		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

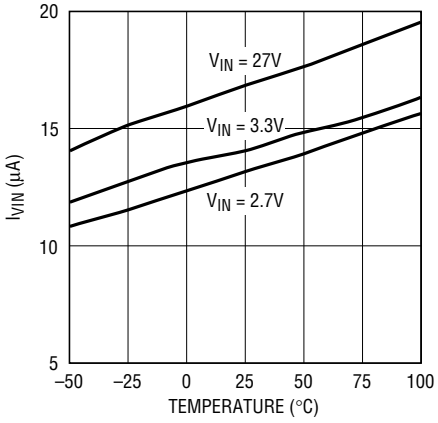
Note 3: The Enable Lock Out time is designed to allow an application to properly power down such that the next power up sequence starts from a consistent powered down configuration. $\overline{PB}$ is ignored during this lock out time. This time delay does not include $t_{DB, ON}$.

Note 4: To manually force a release of the EN/$\overline{EN}$ pin, either $\overline{PB}$ or UVLO must be held low for at least $t_{PD, Min}$ (internal default power down timer) + t_{PDT} (adjustable by placing external capacitor at PDT pin).

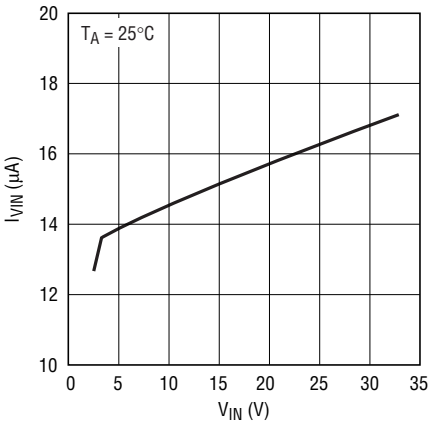
Note 5: The $\overline{KILL}$ turn on blanking timer period ($t_{KILL, ON BLANK}$) is the waiting period immediately after enable output is asserted. This blanking time allows sufficient time for the DC/DC converter and the µP to perform power up tasks. The $\overline{KILL}$, $\overline{PB}$ and UVLO inputs are ignored during this period. If $\overline{KILL}$ remains low at the end of this blanking period, the enable output is released, thus turning off system power.

TYPICAL PERFORMANCE CHARACTERISTICS

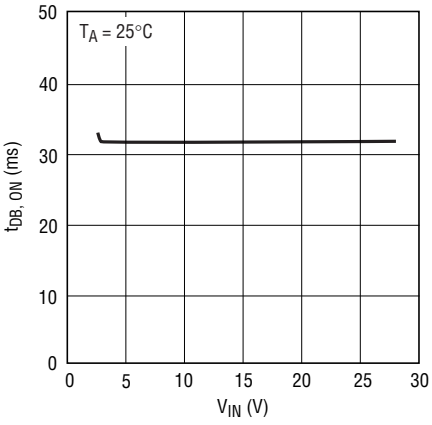
Supply Current vs Temperature



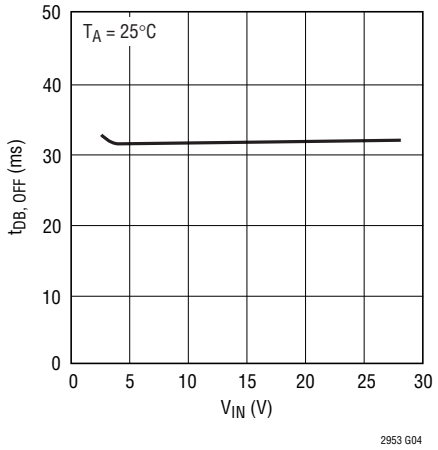
Supply Current vs Supply Voltage



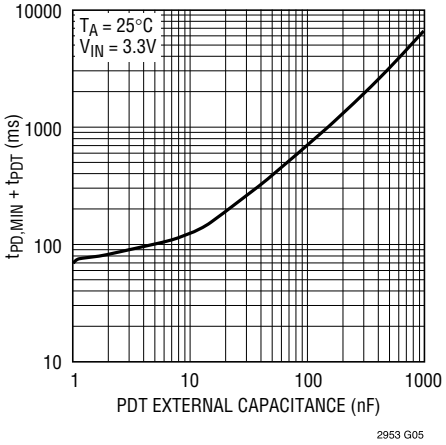
Turn On Debounce Time ($t_{DB, ON}$) vs V_{IN}



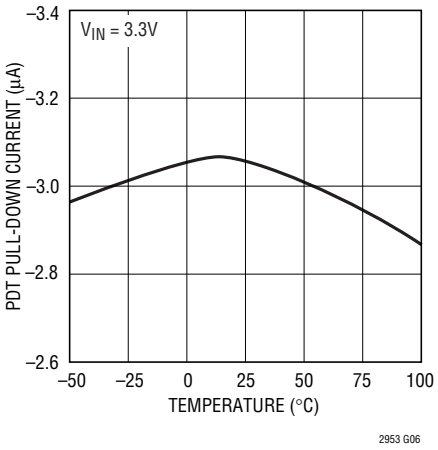
Turn Off Interrupt Debounce Time ($t_{DB, OFF}$) vs V_{IN}



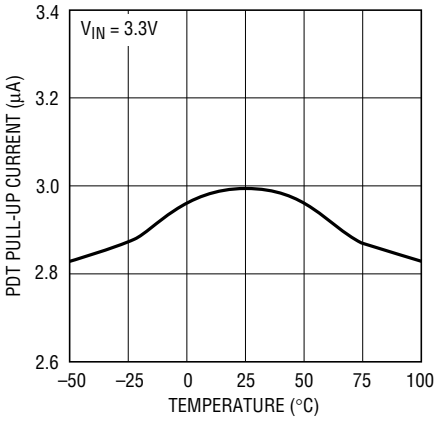
Forced Power Down Delay Time ($t_{PD, MIN}$ + t_{PDT}) vs PDT External Capacitance



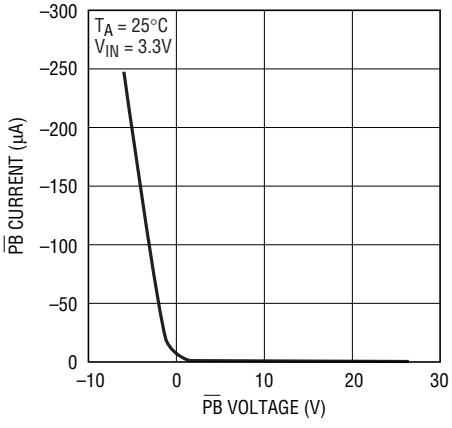
PDT Pull-Down Current vs Temperature



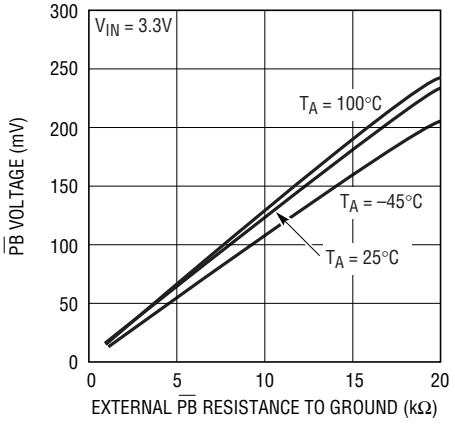
PDT Pull-Up Current vs Temperature



$\overline{PB}$ Current vs $\overline{PB}$ Voltage

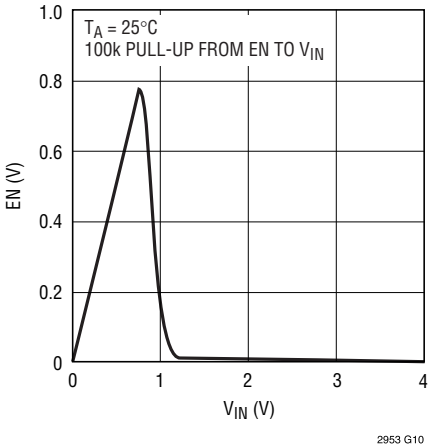


$\overline{PB}$ Voltage vs External $\overline{PB}$ Resistance to Ground

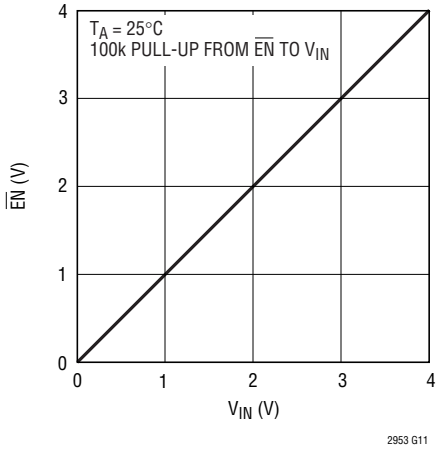


TYPICAL PERFORMANCE CHARACTERISTICS

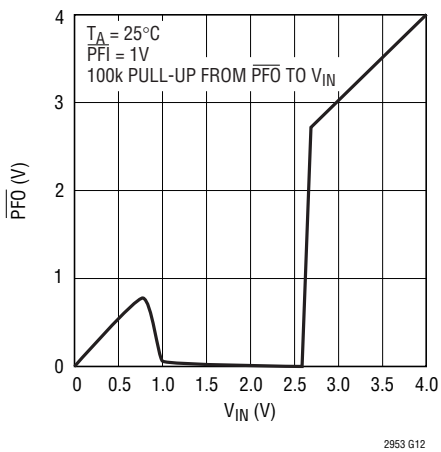
EN (LTC2953-1) Voltage vs V_{IN}



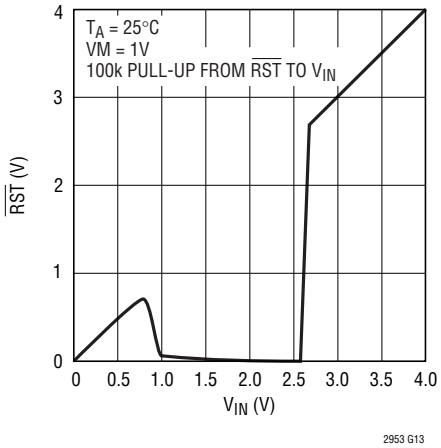
$\overline{EN}$ (LTC2953-2) Voltage vs V_{IN}



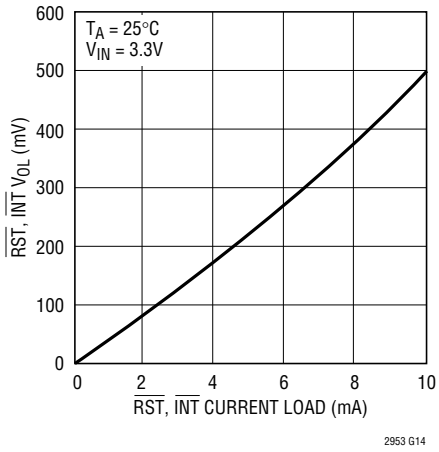
$\overline{PFO}$ Voltage vs V_{IN}



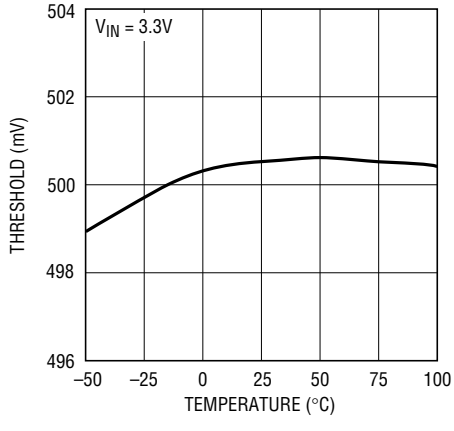
$\overline{RST}$ Voltage vs V_{IN}



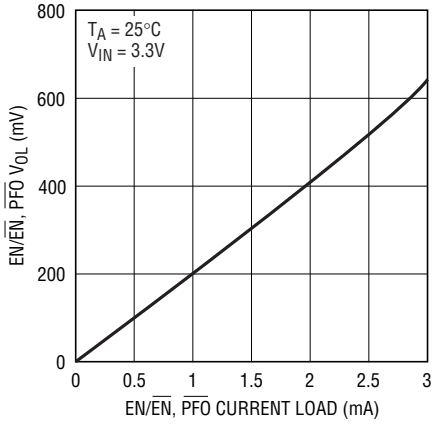
$\overline{RST}$, $\overline{INT}$ V_{OL} vs Current Load



Threshold Voltage (VM, $\overline{PFI}$, UVLO) vs Temperature



EN/$\overline{EN}$, $\overline{PFO}$ V_{OL} vs Current Load



PIN FUNCTIONS

GND (Pin 1): Ground.

VM (Pin 2): Voltage Monitor Input. Input to an accurate comparator with a 0.5V threshold. VM controls the state of the $\overline{RST}$ output pin and is independent of $\overline{PB}$, $\overline{PFI}$ and UVLO status. A voltage below 0.5V on this pin asserts $\overline{RST}$ low. Connect to GND if unused.

$\overline{KILL}$ (Pin 3): $\overline{KILL}$ Input. Forcing $\overline{KILL}$ low releases the enable output. During system turn on, this pin is blanked by a 512ms internal timer ($t_{KILL,\ ON\ BLANK}$) to allow the system to pull $\overline{KILL}$ high. This pin has an accurate 0.6V threshold and can be used as a power kill voltage monitor. Set the pin voltage above its threshold if unused.

PDT (Pin 4): Power Down Time Input. A capacitor to ground determines the additional time (6.4 seconds/µF) that $\overline{PB}$ or UVLO must be held low before releasing the EN/$\overline{EN}$ and $\overline{INT}$ outputs. If this pin is left open, the power down delay time defaults to 64ms.

$\overline{PB}$ (Pin 5): Push Button Input. Connecting $\overline{PB}$ to ground through a momentary switch provides On/Off control via the EN/$\overline{EN}$ and $\overline{INT}$ outputs. An internal 100k pull-up resistor connects to an internal 1.9V bias voltage. The rugged $\overline{PB}$ input withstands ±10kV ESD HBM and can be pulled up to 27V externally without consuming extra current. Voltages below ground will not damage the pin.

V_{IN} (Pin 6): Power Supply Input: 2.7V to 27V.

UVLO (Pin 7): UVLO Comparator Input. When UVLO drops below its falling threshold (0.5V) for more than 32ms, the LTC2953 asserts $\overline{INT}$ low, thereby requesting a system power down. If UVLO remains below its falling threshold (0.5V) for longer than the adjustable power down delay, the enable output is released. Additionally, UVLO provides a $\overline{PB}$ lock out feature that prevents the user from asserting the enable output when UVLO falls below its threshold. Connect to V_{IN} if unused.

$\overline{PFI}$ (Pin 8): Power Fail Comparator Input. Input to an accurate comparator with a 0.5V falling threshold and 4mV of hysteresis. $\overline{PFI}$ controls the state of the $\overline{PFO}$ output pin and is independent of $\overline{PB}$, VM and UVLO status. Connect to GND if unused.

$\overline{PFO}$ (Pin 9): Power Fail Output. This pin is a high voltage open drain pull-down. $\overline{PFO}$ pulls low when $\overline{PFI}$ is below 0.5V. Open circuit when unused.

$\overline{RST}$ (Pin 10): Reset Output. This pin is an open drain pull-down. Pulls low when VM input is below 0.5V and is held low for 200ms after VM input is above 0.5V. Open circuit when unused.

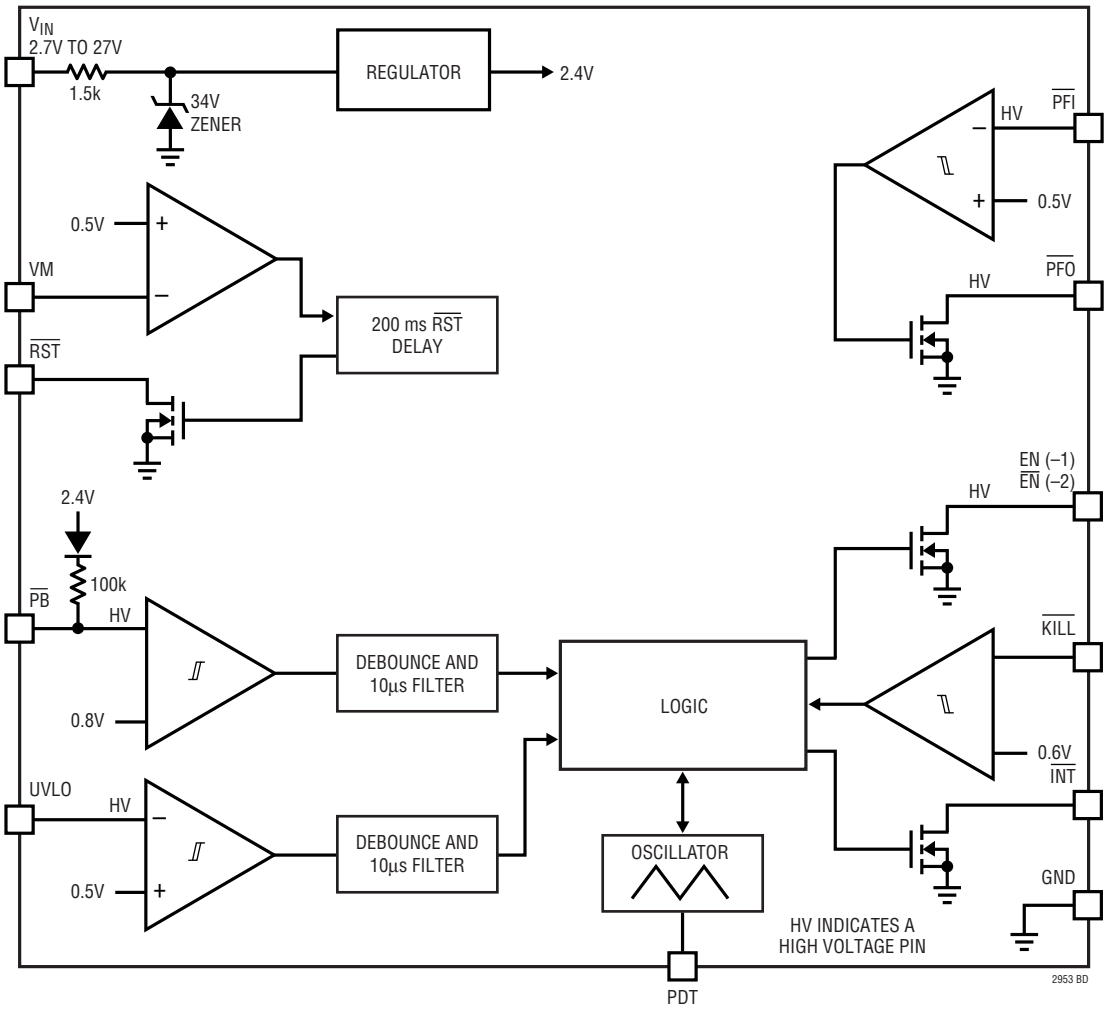
EN (LTC2953-1, Pin 11): Open Drain Enable Output. This output is intended to enable system power. EN is asserted high after a valid $\overline{PB}$ turn on event ($t_{DB,\ ON}$). EN is released low if: a) $\overline{KILL}$ is not driven high (by µP) within 512ms of the initial valid $\overline{PB}$ power turn on event, b) $\overline{KILL}$ is driven low during normal operation, c) $\overline{PB}$ or UVLO is asserted and held low ($t > t_{PD,\ Min} + t_{PDT}$) during normal operation.

$\overline{EN}$ (LTC2953-2, Pin 11): Open Drain Enable Output. This output is intended to enable system power. $\overline{EN}$ is asserted low after a valid $\overline{PB}$ turn on event ($t_{DB,\ ON}$). $\overline{EN}$ is released high if: a) $\overline{KILL}$ is not driven high (by µP) within 512ms of the initial valid $\overline{PB}$ power turn-on event, b) $\overline{KILL}$ is driven low during normal operation, c) $\overline{PB}$ or UVLO is asserted and held low ($t > t_{PD,\ Min} + t_{PDT}$) during normal operation.

$\overline{INT}$ (Pin 12): Open Drain Interrupt Output. After a turn off event is detected ($t_{DB,\ OFF}$) from $\overline{PB}$ or UVLO, the LTC2953 interrupts the system (µP) by asserting $\overline{INT}$ low. The µP would perform power down and housekeeping tasks and then assert the $\overline{KILL}$ pin low, thus releasing the enable output. The $\overline{INT}$ pulse width is a minimum of 32ms and stays low as long as $\overline{PB}$ is asserted. If $\overline{PB}$ is asserted for longer than $t_{PD,\ Min} + t_{PDT}$, however, the $\overline{INT}$ and EN/$\overline{EN}$ outputs are immediately released. Open circuit when unused.

Exposed Pad (Pin 13): Exposed Pad may be left open or connected to ground.

BLOCK DIAGRAM



TIMING DIAGRAMS

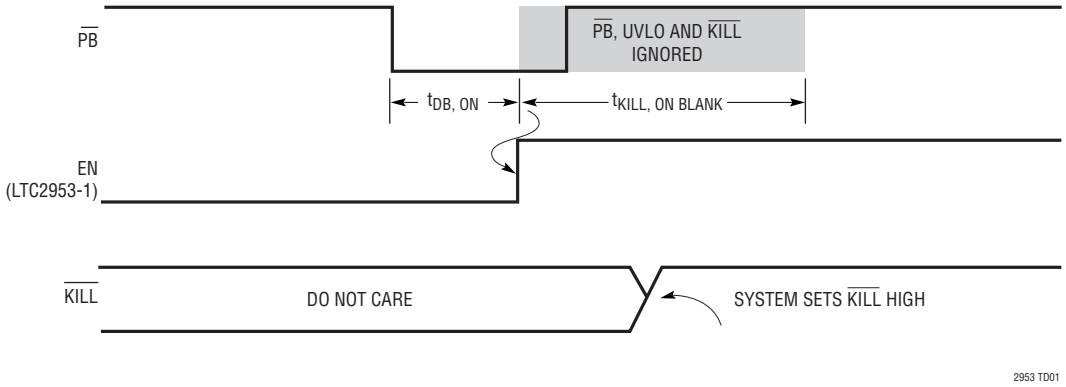


Figure 1. Power On Timing (UVLO > 0.55V)

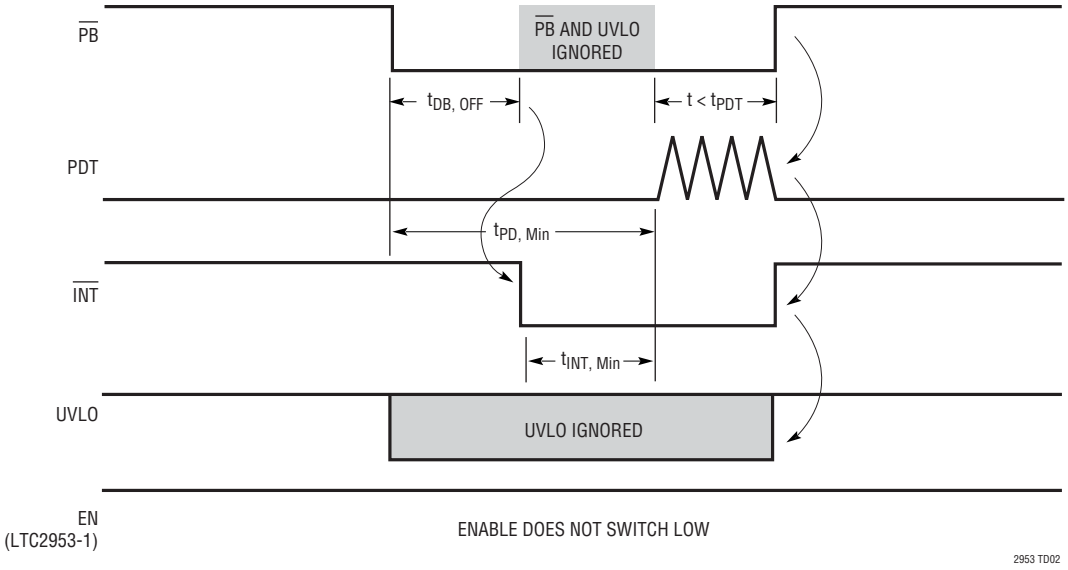


Figure 2. $\overline{PB}$ Interrupt Pulse: $\overline{PB}$ Low for $t_{DB,OFF} < t < (t_{PD,\ Min} + t_{PDT})$ (Enable Remains Active)

TIMING DIAGRAMS

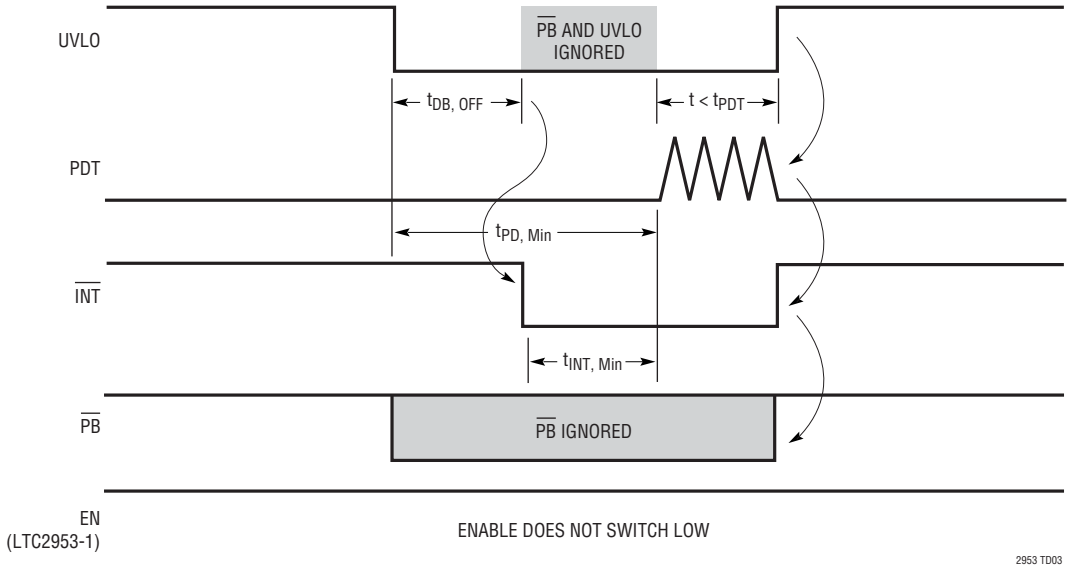


Figure 3. UVLO Interrupt Pulse: UVLO Low for $t_{DB,OFF} < t < (t_{PD, Min} + t_{PDT})$ (Enable Remains Active)

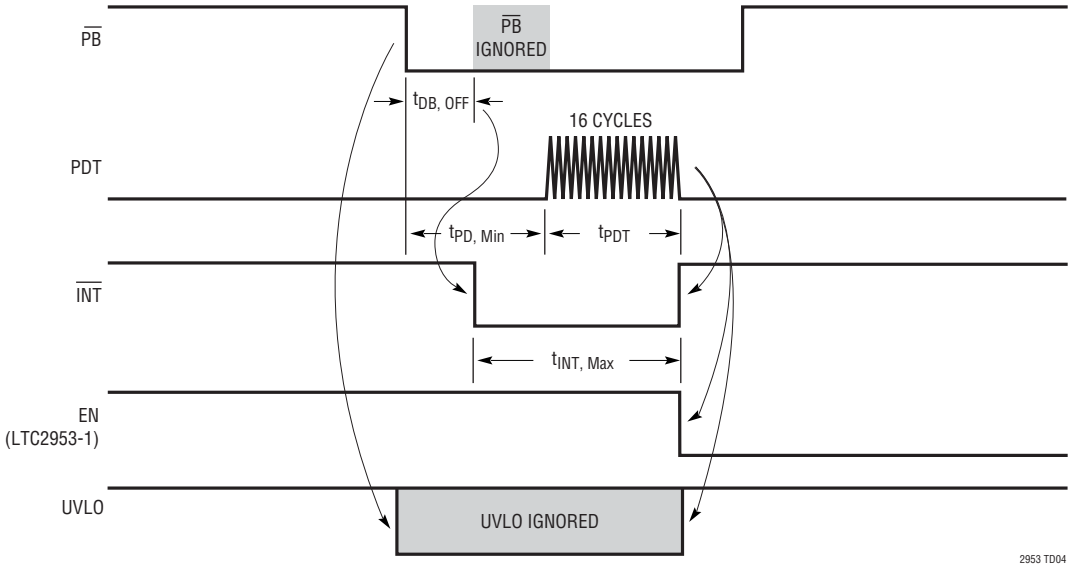


Figure 4. Push Button Power Down Timing: $\overline{PB}$ Pressed and Held Low for $t > (t_{PD, Min} + t_{PDT})$

TIMING DIAGRAMS

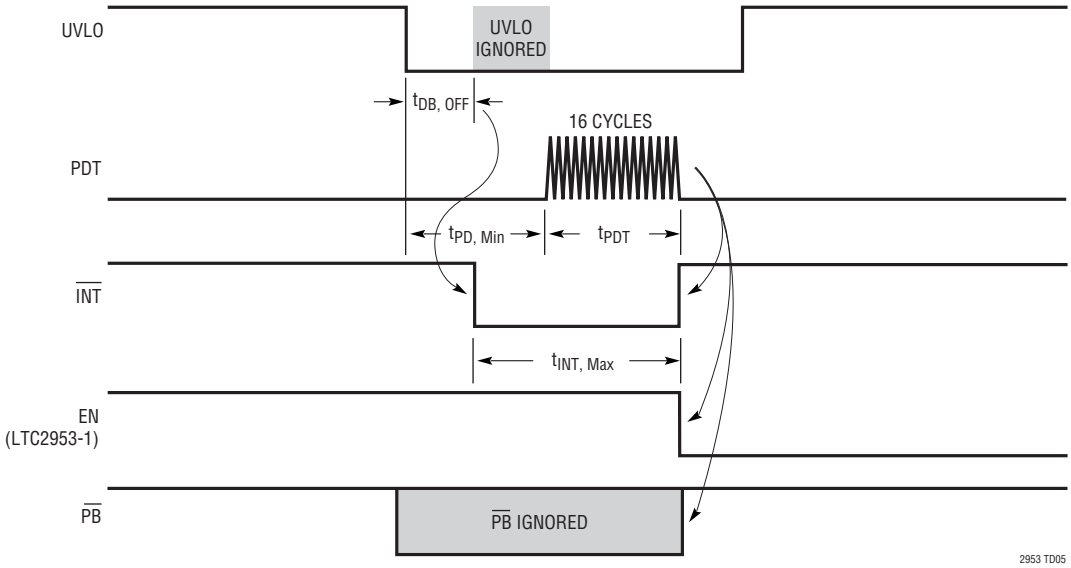


Figure 5. UVLO Power Down Timing: UVLO Low for t > ($t_{PD,\ Min}$ + t_{PDT})

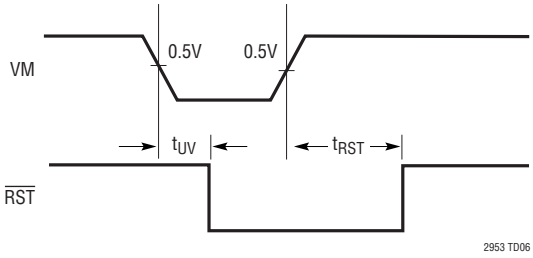


Figure 6. Voltage Monitor Reset Timing

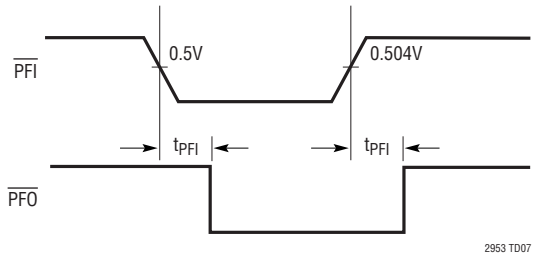


Figure 7. Power Fail Comparator Timing

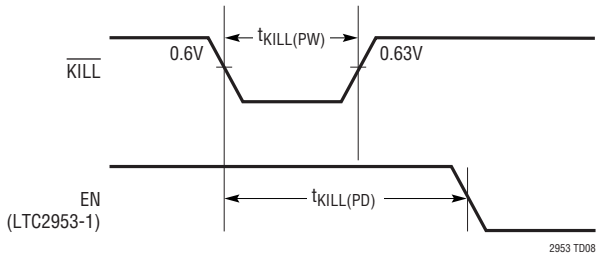


Figure 8. $\overline{KILL}$ Minimum Pulse Width and Propagation Delay

OPERATION

The LTC2953 is a push button On/Off controller with dual function input and output supply monitors. The part contains all the circuitry needed to debounce a push button input and provides a simple µP handshake protocol for reliable toggling of system power. The LTC2953 operates over a wide 2.7V to 27V input voltage range and draws only 14µA of current.

The LTC2953 features dual function supply monitoring: a power fail comparator generates an early warning and an under voltage lock-out comparator initiates a controlled system power down.

Push Button Controller

The push button input controls the enable and interrupt outputs. The enable output toggles system power while the interrupt output provides debounced push button status. The interrupt output can be used in menu driven applications to request a system power down. A power kill input allows a microprocessor or other logic to release the enable output, thus immediately powering down the system.

To assert the enable output (turn on system power), press the push button ($\overline{PB}$) input and hold for at least 32ms. See Figure 1.

Once system power has been enabled, a user can request a system power down by again pressing the push button for at least 32ms and releasing it before the PDT timer counts 16 cycles. The LTC2953 then asserts the interrupt output and the µP subsequently sets the $\overline{KILL}$ input low to turn off system power. Note that the UVLO input can also assert the interrupt output. See Figure 2 and Figure 3 and Dual Function Supply Monitors section.

In the event that the µP does not respond to the interrupt request, the user can force release of the enable output by pressing and holding down the push button (or UVLO) until the PDT timer times out. See Figure 4 and Figure 5.

Dual Function Supply Monitors

An uncommitted power fail comparator provides real time supply threshold information. The power fail input ($\overline{PFI}$) is compared against an accurate internal 0.5V reference and the comparison result is passed directly to the power fail output ($\overline{PFO}$) pin. The operation of the power fail comparator is de-coupled from all other functionality and is always active. See Figure 7.

The under voltage lockout comparator provides the user with another method to initiate a controlled system power down. If the UVLO pin voltage falls below its falling threshold (0.5V) for longer than 32ms, the interrupt output is asserted for a minimum of 32ms. If the UVLO pin voltage remains below its threshold (0.5V) for an additional time given by the PDT external capacitor, then the enable pin is automatically released (thus powering down the system). See Figure 3 and Figure 5.

This comparator also serves as an under voltage lockout. If system power is off (enable released) and UVLO < 0.5V, the UVLO comparator prevents the push button from turning on system power (asserting enable output).

Voltage Supervisor with 200ms µP Reset

The LTC2953 provides a single adjustable supply monitor with a nominal 200ms reset delay. When the VM input voltage drops below 0.5V, the $\overline{RST}$ output is pulled low. $\overline{RST}$ remains low for 200ms after the VM input has risen above 0.5V. The input 0.5V threshold has a guaranteed accuracy of ±1.5% over temperature and process. The operation of the supply monitor is de-coupled from all other functionality and is always active. See Figure 6.

APPLICATIONS INFORMATION

PUSH BUTTON CONTROL

Power On Sequence

To enable system power, the push button input ($\overline{PB}$) must be held low continuously for 32ms ($t_{DB,\ ON}$). Once the enable output (EN/$\overline{EN}$) is asserted, the LTC2953 starts a 512ms internal timer ($t_{KILL,\ ON\ BLANK}$). The $\overline{KILL}$ input must be driven high within this 512ms window. This blanking time represents the maximum time allowed for the system to power up and initialize the circuits driving the $\overline{KILL}$ input. If $\overline{KILL}$ remains low at the end of the blanking period, the enable output is released (see "Aborted Power On Sequence" section). Figure 9 shows a normal power on sequence.

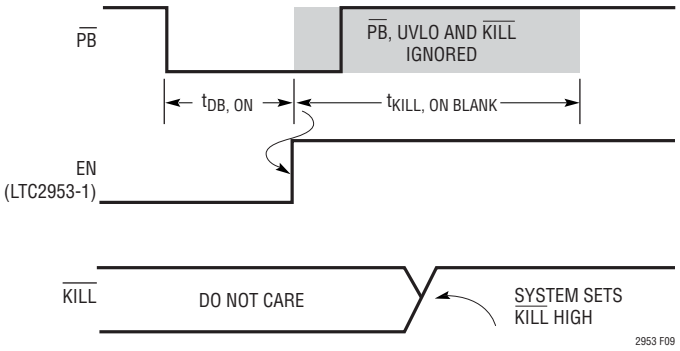


Figure 9. Power On Timing (UVLO > 0.55V)

Note that only the push button input can enable system power. The LTC2953 provides two enable output polarities to allow DC/DC converter control (LTC2953-1) and external power PFET control (LTC2953-2).

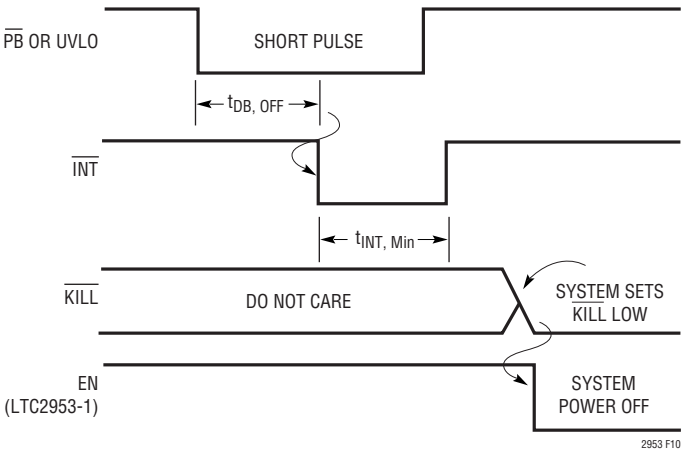


Figure 10. Power Off Interrupt Timing

Short Pulse Interrupt

To interrupt the µP, either $\overline{PB}$ or UVLO must be low for at least 32ms ($t_{DB,\ OFF}$). This signals the µP either that a user has pressed the push button or that the supply is running low. The µP would then perform power down and housekeeping tasks and assert $\overline{KILL}$ low when done. This in turn releases the enable output, thus shutting off system power. See Figure 10.

Note that either $\overline{PB}$ or UVLO can control the power down sequence, but not both at the same time. For example, if both $\overline{PB}$ and UVLO are high and the user presses the push button, $\overline{PB}$ will be active and UVLO will be ignored until $\overline{PB}$ is released or the power down sequence is complete.

Forced Power Off Sequence

The LTC2953 provides a failsafe feature that allows a user to manually force a system power down. For cases when the µP fails to respond to the interrupt signal, the user can force a power down by pressing and holding either the push button or the UVLO inputs low.

The length of time required to release the enable output is given by a fixed internal 64ms delay ($t_{PD,\ Min}$) plus an adjustable power down timer delay (t_{PDT}). The adjustable delay is set by placing an external capacitor on the PDT pin. Use the following equation to calculate the capacitance for the desired extra delay. C_{PDT} is the PDT pin external capacitor:

C_{PDT} = 1.56E-4 [µF/ms] • (t_{PDT} – 1ms)

See Figure 11.

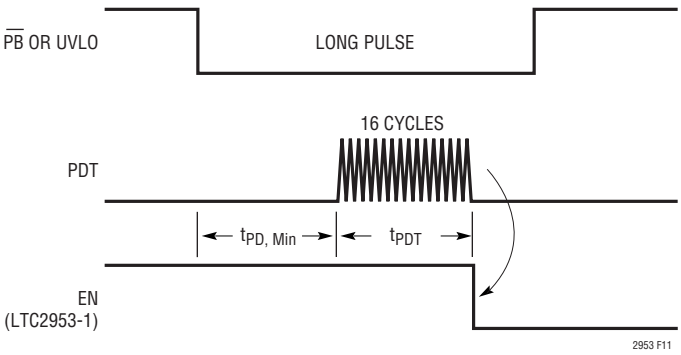


Figure 11. Forced Power Off Timing with Adjustable Delay (See Figure 5 for More Details)

APPLICATIONS INFORMATION

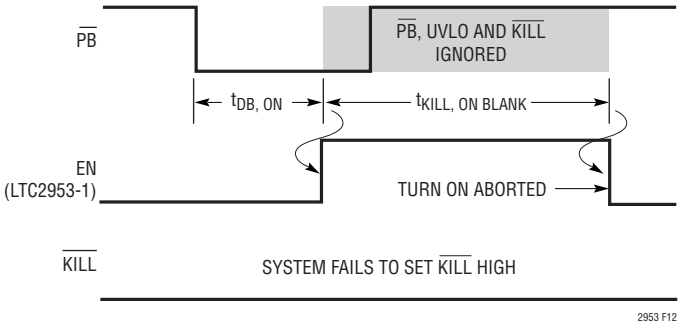


Figure 12. Aborted Power On Sequence, $\overline{KILL}$ Remaining Low Aborts Power On Sequence

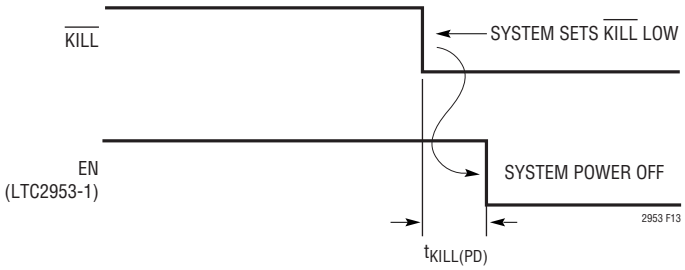


Figure 13. µP Turns Off System Power

Aborted Power On Sequence

The LTC2953 provides an internal 512ms timer to detect when a system fails to power on properly. A power on sequence begins by debouncing the $\overline{PB}$ input. After the enable pin is subsequently asserted, the LTC2953 starts the 512ms blanking timer ($t_{KILL,\ ON\ BLANK}$). If the $\overline{KILL}$ input is not driven high within this 512ms time window, the enable pin is immediately released, thus turning off system power. This failsafe feature prevents a user from turning on the device when the circuits driving the $\overline{KILL}$ input do not respond within 512ms after enable has been asserted. See Figure 12.

µP Turns Off System Power During Normal Operation

Once the system has powered on and is operating normally, the µP can turn off power by asserting the $\overline{KILL}$ input low. See Figure 13.

DUAL FUNCTION BATTERY SUPERVISOR

The LTC2953 provides two comparators for battery monitoring: an uncommitted power fail comparator and a latched low battery comparator with µP interrupt. The application shown in Figure 14 monitors a 2 cell Li-Ion battery stack.

Power Fail Comparator

This comparator provides real time threshold information and can serve as the first warning of a decaying battery or supply. The $\overline{PFO}$ output is driven low when the $\overline{PFI}$ input voltage drops below its falling threshold (0.5V) and is high impedance when $\overline{PFI}$ rises above its rising threshold (0.504V). The low leakage, high voltage $\overline{PFI}$ input (10nA, maximum) allows the use of large valued external resistors, which lowers system current consumption.

UVLO Comparator

The under voltage lockout comparator performs three functions: a) interrupts the µP when a supply glitch drives the UVLO voltage below its falling threshold (0.5V) for longer than 32ms, followed by b) forces system power off when the UVLO voltage falls below its falling threshold (0.5V) for $t_{PD,\ Min} + t_{PDT}$, c) locks out the enable (prevents system power on) output if UVLO voltage is below its falling threshold (0.5V) during system power on. See Figures 15A and 15B.

The low leakage (10nA, maximum), high voltage UVLO input allows the use of large valued external resistors. See Figure 14.

APPLICATIONS INFORMATION

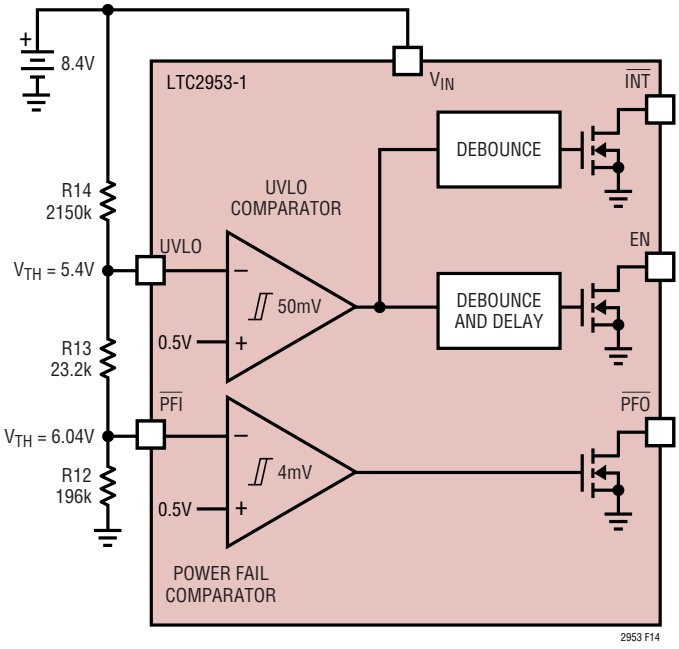


Figure 14. Dual Function Battery Comparators

Which Input Initiated Power Down: $\overline{PB}$ or UVLO?

The circuit in Figure 14 determines whether a power down was initiated by a user pressing the push button or by a battery drooping too low. If both $\overline{INT}$ and $\overline{PFO}$ outputs are low, then a low battery condition initiated a power down.

$\overline{PFI}$ and UVLO Thresholds

The circuit depicted in Figure 14 uses one resistive divider network for both power fail and low battery comparators. The power fail comparator trips at a higher battery voltage than the low battery comparator, thus providing a battery warning before a power down sequence is initiated. Due to the low offset architecture of the comparators, the UVLO and $\overline{PFI}$ thresholds can be set to as close as ±5mV apart. The trip thresholds of the circuit of Figure 14 are 6.04V and 5.40V for the power fail and low battery (UVLO) comparators, respectively.

Push Button Lockout

The LTC2953 provides a push button lock out feature that prevents a user from turning on a system with a dead battery. The push button input is ignored when the UVLO input voltage is less than the falling threshold (0.5V). See Figure 15B.

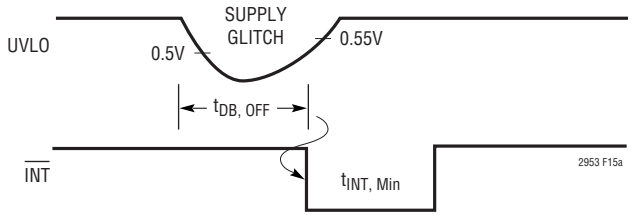


Figure 15A. Supply Glitch Generates µP Interrupt

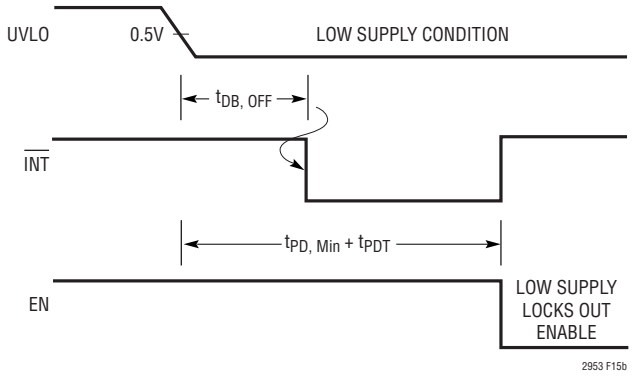


Figure 15B. Low Supply Initiates System Power Down and Locks Out Enable

TYPICAL APPLICATIONS

Push Button Buffer

The circuit of Figure 16 shows the power fail comparator sensing the push button input. The $\overline{PFO}$ output toggles each time the push button crosses 0.5V. This application provides an early warning of push button activity.

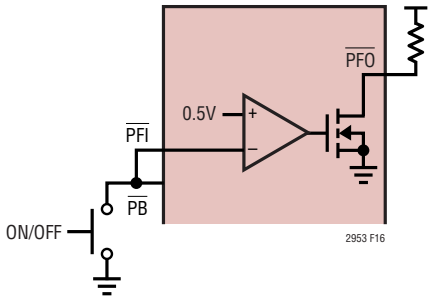


Figure 16. Push Button Buffer

Power Path Switching

The high voltage $\overline{EN}$ output of the LTC2953-2 is designed to switch On/Off an external power PFET. This allows a user to connect/disconnect a power supply (or battery) to its load by toggling the $\overline{PB}$ pin. Figure 17 shows the LTC2953-2 in a 12V wall adapter application.

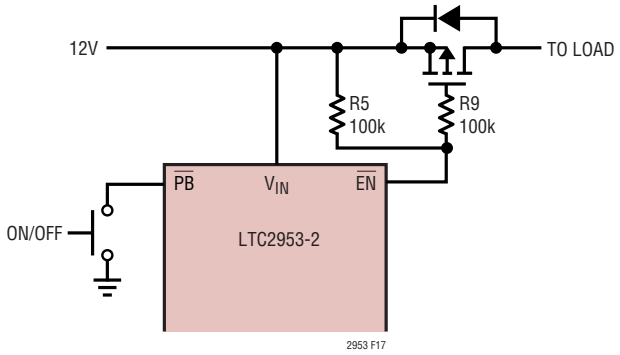


Figure 17. Power Path Switching

Disconnect Input Resistive Divider To Save Power

In order to prolong battery life when system power has been turned off, the LTC2953-2 power fail comparator can be used to disconnect the external battery monitor resistive divider. The circuit in Figure 18 connects $\overline{PFI}$ to $\overline{EN}$ and $\overline{PFO}$ to the bottom end of the resistive divider.

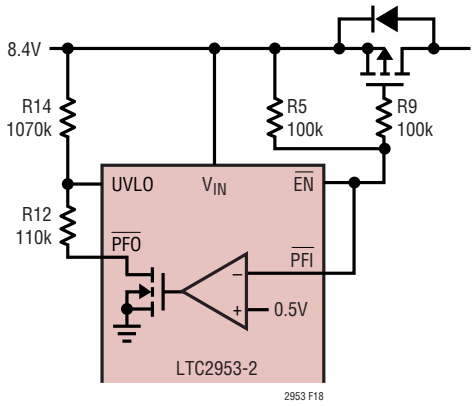


Figure 18. Disconnect Input Resistive Divider to Save Power

When the user presses the push button to turn on system power ($\overline{EN}$ low), the output of the power fail comparator asserts $\overline{PFO}$ low. The low battery external resistive divider is thus enabled to monitor the input supply. If the voltage on the UVLO input falls to less than 0.5V, a system power down sequence is initiated. Note that the IR drop across the internal NFET is typically less than 0.2mV when the UVLO pin voltage is 0.5V.

Once system power has been turned off ($\overline{EN}$ high), the external resistive divider is disconnected and thus consumes zero DC current.

TYPICAL APPLICATIONS

Push Button Controlled µP Reset

The circuit of Figure 19 can be used to keep a µP in reset for 200ms after the push button has enabled system power. After system power has stabilized, the voltage monitor input continues to monitor the supply at the load end.

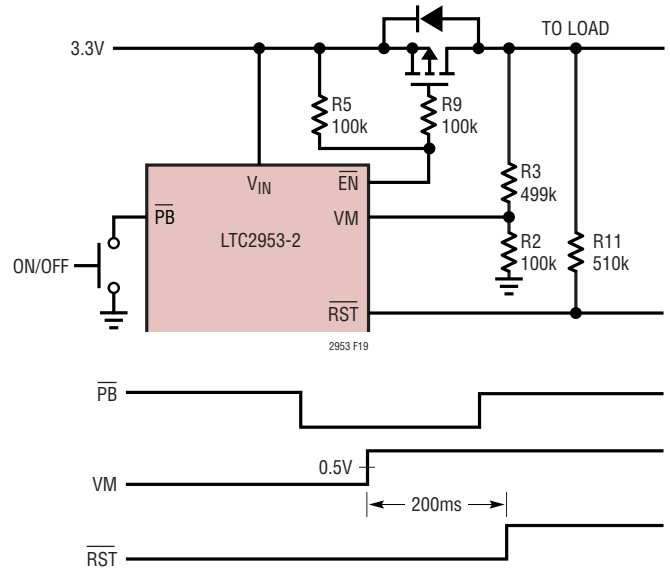


Figure 19. Push Button Controlled µP Reset

Push Button Controlled Supply Sequencing

The circuit in Figure 20 uses the LTC2953-2 to sequence 3 supply rails. Power on sequencing begins by pressing the push button for 32ms. This asserts the $\overline{EN}$ output low, which turns on the V1 supply. 200ms after V1 reaches 80% of its final value (2.66V), the V2 supply is enabled. When the V2 DC voltage reaches 80% of its final value (2V), the V3 supply is enabled. Note that there is no internal delay from the $\overline{PFI}$ input to the $\overline{PFO}$ output and so V3 is enabled at the same time V2 rises above 2V.

A power down supply sequence begins when any of these inputs is asserted: $\overline{PB}$, UVLO or $\overline{KILL}$. When $\overline{EN}$ pulls up to V_{IN}, V1 disconnects first. When V1 decays to 2.66V, V2 is immediately disabled (there is no 200ms delay from VM to $\overline{RST}$ during power down). When V2 decays to 2V, V3 is immediately disabled. See Figure 21 timing diagram.

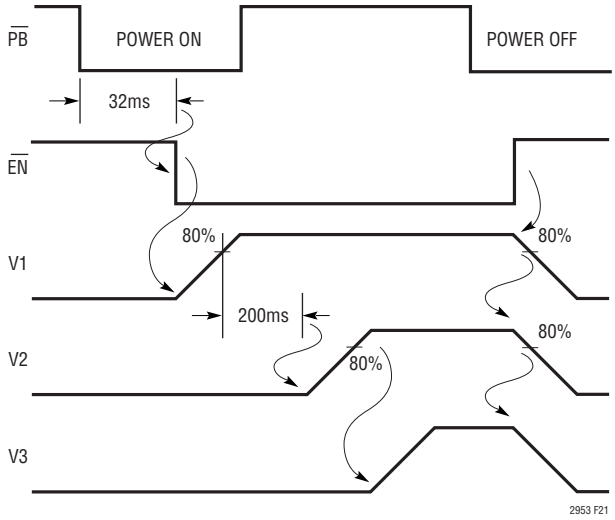


Figure 21. Push Button Controlled Supply Sequence Timing

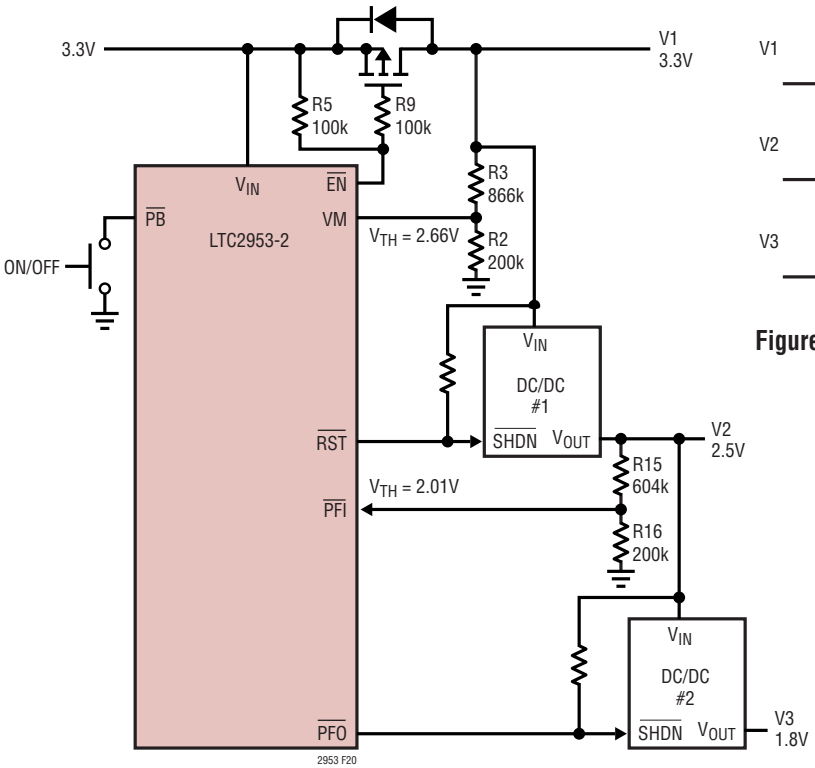


Figure 20. Push Button Controlled Supply Sequencing

TYPICAL APPLICATIONS

Dual Supply Monitor with µP Reset

The circuit of Figure 22 monitors two supplies and provides a µP reset. When either the $\overline{PFI}$ or the VM input voltage falls below its threshold (0.5V), the $\overline{RST}$ output is asserted low. $\overline{RST}$ remains low for 200ms after both inputs rise above 0.5V. The low leakage $\overline{PFO}$ output allows for large valued external resistors.

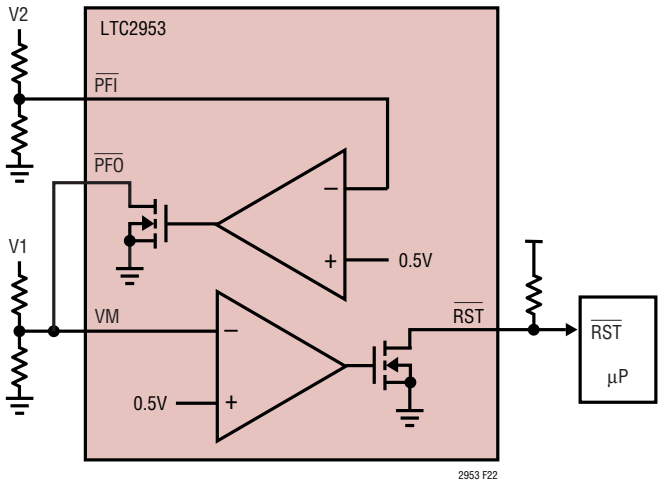


Figure 22. Dual Supply Monitor with µP Reset

Reverse Battery Protection

To protect the LTC2953 from a reverse battery connection, place a 1k resistor (R8) in series with the V_{IN} pin. See Figure 23.

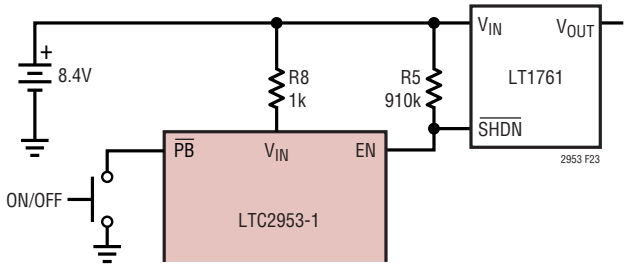


Figure 23. Reverse Battery Protection Using R8

Operation with Supply Transients over 40V

The application circuit of Figure 24 operates from a 24V nominal supply, but can withstand supply transients as high as 40V.

The high voltage $\overline{EN}$ output of the LTC2953-2 has an absolute maximum rating of 50V, which makes it suitable for driving the gate of the external power PFET. The external 30V Zener diode (Z1) and the 10k current limiting resistor (RZ) protect the V_{IN} supply pin of the LTC2953-2. Note that under normal 24V operation, the external Zener diode does not conduct any current. The voltage drop across RZ should be kept below 1V. Z2 should have a breakdown voltage smaller than the PFET's gate-to-source breakdown voltage.

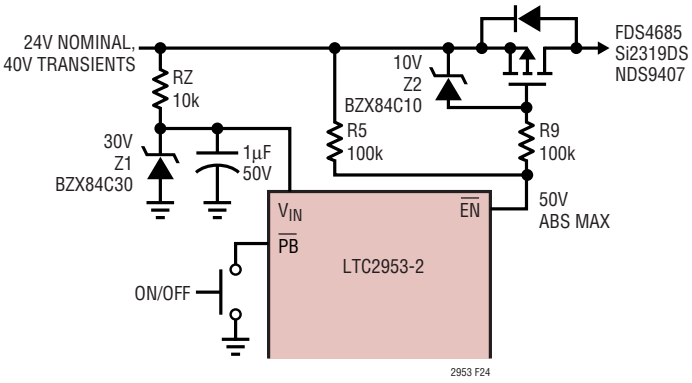


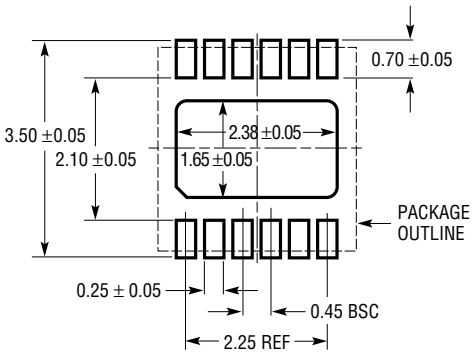
Figure 24. Operation with 40V Supply Transients

Power Path Controller with Low Battery Detect

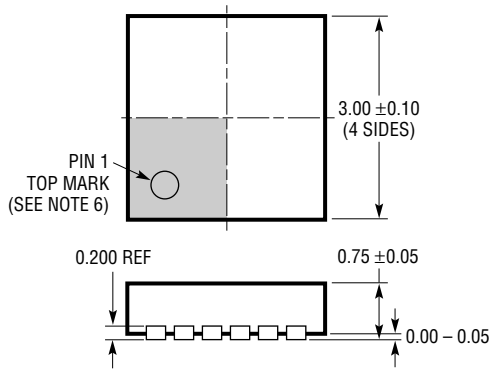
The application in Figure 25 uses the push button to completely disconnect the load from the battery. If the battery voltage falls below the user specified threshold, the push button is prevented from turning on system power (asserting the enable output).

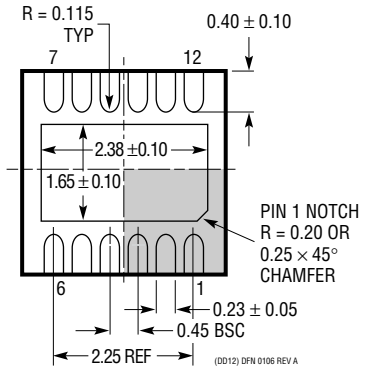
PACKAGE DESCRIPTION

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

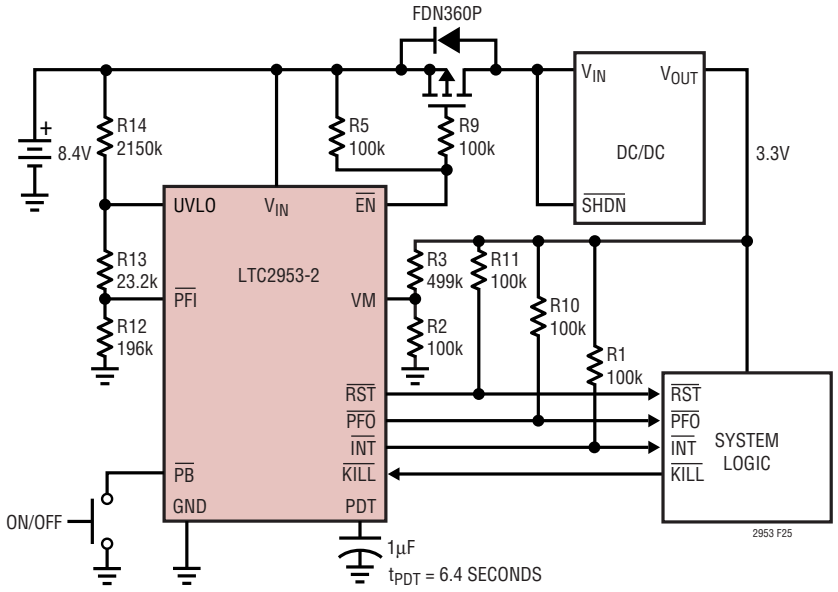


Figure 25. PowerPath Controller with Low Battery Detect

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2900	Programmable Quad Supply Monitor	Adjustable Reset, 10-Lead MSOP and 3mm × 3mm DFN Packages
LTC2904/LTC2905	Pin-Programmable Dual Supply Monitors	Adjustable Reset and Tolerance, 8-Lead SOT-23 and 3mm × 2mm DFN Packages
LTC2909	Precision Tripple/Dual Input UV, OV and Negative Voltage Monitor	6.5V Shunt Regulator for High Voltage Operation
LTC2912	Single UV/OV Monitor	3mm × 2mm DFN, 8-Pin ThinSOT Packages
LTC2950/LTC2951	Push Button On/Off Controllers	High Voltage, Low Power Push Button Controller
LTC2952	Push Button Power Path Controller with Supervisor	Automatic Low Loss Switchover Between DC Sources
LTC2954	Push Button On/Off Controller with µP Interrupt	Allow Controlled Software System Shutdown
LTC4055	USB Power Controller and Li-Ion Charger	Automatic Switchover, Charges 1-Cell Li-Ion Batteries
LTC4411	2.6A Low Loss Ideal Diode in ThinSOT	No External MOSFET, Automatic Switching Between DC Sources
LTC4412HV	PowerPath Controller in ThinSOT	Efficient Diode-ORing, Automatic Switching Between DC Sources, 3V to 36V

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0607 • PRINTED IN USA

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LTC2953IDD-2#TRPBF on WIN SOURCE
- Analog Devices Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management