THE DATASHEET OF

LTM4642EY#PBF

20V_{IN}, Dual 4A or Single 8A DC/DC µModule Regulator

FEATURES

- **Small Form Factor Dual 4A Power Supply**
- **Wide Input Voltage Range: 4.5V to 20V (2.375V Min with CPWR Bias)**
- **Dual 180° Out-of-Phase Outputs with 4A DC**
- **Dual Outputs with 0.6V to 5.5V Range**
- **Output Voltage Tracking**
- **±1.5% Maximum Total DC Output Voltage Error**
- **Up to 95% Maximum Efficiency**
- **Phase-Lockable Fixed Frequency 600kHz to 1.4MHz**
- **Constant On-Time, Valley Current Mode Architecture**
- **Selectable Burst Mode® Operation**
- Output Overvoltage and Overcurrent Protection
- 9mm × 11.25mm × 4.92mm BGA Package

APPLICATIONS

- Telecom and Networking Equipment
- Servers
- FPGA Power

DESCRIPTION

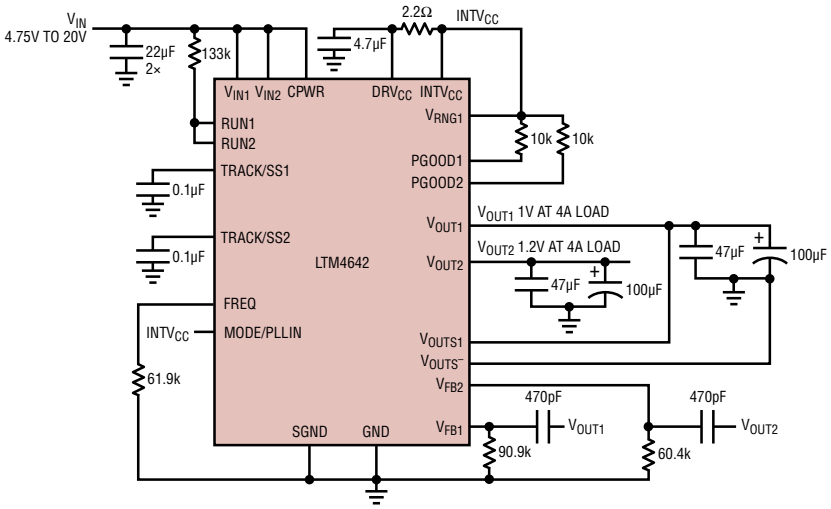
The LTM®4642 is a complete dual 4A or single 8A step-down DC/DC µModule® (micromodule) regulator. Included in the package are the switching controller, power FETs, inductor, and all support components. Operating over input voltage ranges of 4.5V to 20V, (2.375V min with external CPWR bias), the LTM4642 supports two outputs with voltage ranges of 0.6V to 5.5V, set by a single external resistor. Its high efficiency design delivers 4A continuous current (5A peak) for each output.

High switching frequency and a valley current mode architecture enable a very fast transient response to line and load changes without sacrificing stability. The two outputs are interleaved with 180° phase to minimize the ripple noise and reduce the I/O capacitors.

The power module is offered in a 9mm × 11.25mm × 4.92mm BGA package. The LTM4642 is RoHS compliant with Pb-free finish.

TYPICAL APPLICATION

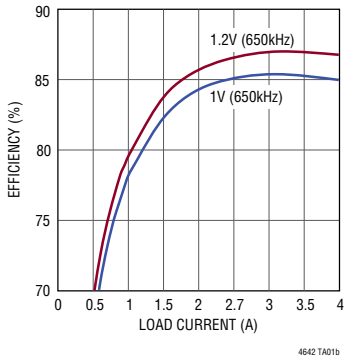
Dual 4A 1V and 1.2V DC/DC µModule Regulator



PINS NOT USED: COMP1, COMP2, PHASEMD, CLKOUT, EXTV_{CC}, SW1, SW2

4642 TA01a

Efficiency vs Load Current at 12V input



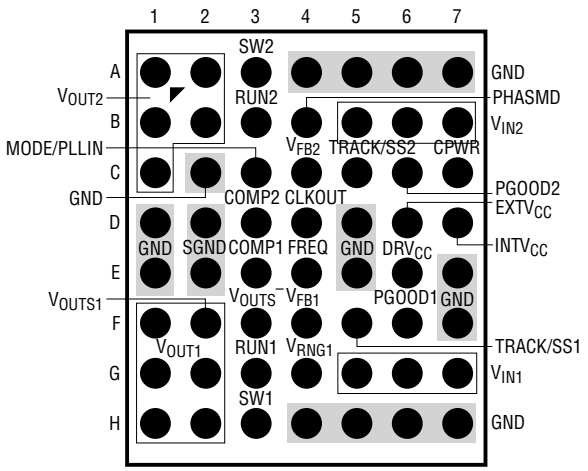
4642 TA01b

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2}, SW1, SW2, CPWR ..... –0.3V to 22V
$INTV_{CC}$, DRV_{CC}, PGOOD1,2, RUN1,2, $EXTV_{CC}$,
V_{FB1}, V_{FB2} (Note 4) .....–0.3V to $INTV_{CC}$ + 0.3V
COMP1, COMP2 (Note 4)..... –0.3V to 2.7V
MODE/PLLIN, FREQ, PHASMD,
V_{RNG1}.....–0.3V to $INTV_{CC}$ + 0.3V
V_{OUT1}, V_{OUT2}, V_{OUTS1}..... –0.3V to 6V
V_{OUTS}^- .....0.3V to 2.75V
TK/SS1, TK/SS2..... 0.3V to 5V
Internal Operating Temperature Range
(Note 2).....–40°C to 125°C
Maximum Reflow Body Temperature..... 245°C
Storage Temperature Range ..... –55°C to 125°C

PIN CONFIGURATION



BGA Package
56-Lead (9mm × 11.25mm × 4.92mm)

T_{JMAX} = 125°C, θ_{JA} = 15°C/W, θ_{JP} = 4°C/W
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS
WEIGHT = 1.2635g

ORDER INFORMATION

http://www.linear.com/product/LTM4642#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4642EY#PBF	SAC305 (RoHS)	LTM4642Y	e1	BGA	3	–40°C to 125°C
LTM4642IY#PBF	SAC305 (RoHS)	LTM4642Y	e1	BGA	3	–40°C to 125°C
LTM4642IY	SnPb (63/37)	LTM4642Y	e0	BGA	3	–40°C to 125°C

- Consult Marketing for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V. Per typical application in Figure 27. Specified as each channel. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage	V_{IN} ≤ 4.5V, Connect CPWR to a Bias > 4.5V	●	2.375		20	V
$V_{OUT1,2(RANGE)}$	Output Voltage Range	V_{IN} = 6V to 20V	●	0.6		5.5	V
$V_{OUT1,2(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF ×2, C_{OUT} = 47µF Ceramic, 100µF POSCAP, R_{SET} = 40.2kΩ V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 4A	●	1.4775	1.5	1.5225	V
Input Specifications							
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 10µF, C_{OUT} = 47µF Ceramic and 100µF POSCAP, V_{OUT} = 1.5V V_{IN} = 12V			0.25		A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V. Per typical application in Figure 27. Specified as each channel. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{CPWR}	CPWR Bias Current	CPWR = 12V, MODE = Continuous				20	mA
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT1} = 1.5V, Switching Continuous V_{IN} = 12V, V_{OUT2} = 1.5V, Switching Continuous V_{IN} = 20V, V_{OUT1} = 1.5V, Switching Continuous V_{IN} = 20V, V_{OUT2} = 1.5V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 12V			25 25 22 22 10		mA mA mA mA µA
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 4A V_{IN} = 20V, V_{OUT} = 1.5V, I_{OUT} = 4A			0.6 0.356		A A
DRV_{CC}	Internal V_{CC} Voltage	6V < V_{IN} < 20V, No Load		5	5.3	5.6	V
$I_{DRVCC(REG)}$	DRV_{CC} Load Regulation	I_{DRVCC} = 0 to 100mA			–1.5	–3	%
$EXTV_{CC(HYS)}$	$EXTV_{CC}$ Switchover Hysteresis				200		mV
$EXTV_{CC}$	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.4	4.6	4.8	V
Output Specifications							
$I_{OUT1,2(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Note 5)		0		4	A
$\frac{\Delta V_{OUT1(LINE)}}{V_{OUT(NOM)}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} from 4.5V to 20V, I_{OUT} = 0A For Each Output	●		0.1	0.2	%
$\frac{\Delta V_{OUT2(LOAD)}}{V_{OUT2(NOM)}}$	Load Regulation Accuracy	For Each Output, V_{OUT} = 1.5V, 0A to 4A (Note 5) V_{IN} = 12V	●		±0.3	±0.5	%
$V_{OUT1,2(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF X5R Ceramic V_{IN} = 12V, V_{OUT} = 1.5V V_{IN} = 20V, V_{OUT} = 1.5V			 15 15		 mV mV
f_S	Output Ripple Voltage Frequency	I_{OUT} = 2A, V_{IN} = 12V, V_{OUT} = 1.5V, FREQ = 49.9k to Ground			800		kHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 100µF and 47µF X5R Ceramic, V_{OUT} = 1.5V, I_{OUT} = 0A V_{IN} = 12V V_{IN} = 20V			 10 10		 mV mV
t_{START}	Turn-On Time	C_{OUT} = 100µF X5R and 47µF Ceramic, V_{OUT} = 1.5V, I_{OUT} = 0A Resistive Load, TRACK/SS = 10nF V_{IN} = 12V			 6		 ms
$\Delta V_{OUT(LS)}$	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load C_{OUT} = 100µF and 47µF X5R Ceramic, V_{OUT} = 1.5V, V_{IN} = 12V			 50		 mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load C_{OUT} = 100µF and 47µF X5R Ceramic, V_{OUT} = 1.5V, V_{IN} = 12V			 15		 µs
$I_{OUT(PK)}$	Output Current Limit	C_{OUT} = 100µF and 47µF X5R Ceramic, V_{IN} = 6V, V_{OUT} = 1.5V V_{IN} = 20V, V_{OUT} = 1.5V			 7 7		 A A
Control Section							
$V_{OUTS1(REG)}$	Regulated Differential Feedback V_{OUTS1}-V_{OUTS}^-	Sensed at Load Point with Resistive Divider	●	0.592	0.6	0.608	V
I_{VOUTS1}	V_{OUTS1} Input Bias Current	(Note 4)			±5	±25	nA
I_{VOUTS}^-	V_{OUTS}^- Input Bias Current	(Note 4)			–25	–50	nA
I_{VFB2}	V_{FB2} Input Bias Current	(Note 4)			–5	±50	nA
V_{FB2}	Voltage at V_{FB2} Pin	I_{OUT} = 0A, V_{OUT} = 2.5V	●	0.592	0.6	0.608	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V. Per typical application in Figure 27. Specified as each channel. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{TRACK/SS1,2}$	Soft-Start Charge Current	0V < TRACK/SS1,2 < 0.6V			1.0		µA
DF_{MAX}	Maximum Duty Factor	In Dropout (Note 4)			97		%
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			30		ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 4)			90		ns
f_{LOW}	Low Frequency	R_{FREQ} = 61.9k		600	650	700	kHz
f_{NOM}	Nominal Frequency	R_{FREQ} = 49.9k		730	800	850	kHz
f_{HIGH}	Highest Frequency	R_{FREQ} = 27.5k		1250	1400	1500	kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				600		kΩ
$V_{PLLIN(HIGH)}$	MODE/PLLIN Clock In High			2			V
$V_{PLLIN(LOW)}$	MODE/PLLIN Clock In Low					0.5	V
$V_{RUN1, 2}$	RUN Pin ON/OFF Threshold	RUN Rising	●	1.1	1.2	1.3	V
$V_{RUN1, 2(HYS)}$	RUN1, 2, Threshold Hysteresis	Delta RUN Rising to RUN Falling			200		mV
$I_{RUN1,2}$	RUN Pin Pull-Up Current When Off	RUN1,2 at SGND			1.2		µA
$I_{RUN1,2(HYS)}$	RUN1,2 Pull-Up Hysteresis	$I_{RUN1,2(HYST)} = I_{RUN1,2(ON)} - I_{RUN1,2(OFF)}$ (Note 4)			5		µA
RUN1,2 Res	RUN1,2 Resistance to Ground				100		kΩ
UVLO	Undervoltage Lockout	$INTV_{CC}$ Falling (Note 4) $INTV_{CC}$ Rising	● ●	3.3	3.7 4.2	 4.5	V V
R_{FB1}, R_{FB2}	Resistor Between V_{OUT} and V_{FB} Pins for Each Channel			60.1	60.4	60.7	kΩ
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±2	µA
ΔV_{PGOOD}	PGOOD Range	V_{FB} Ramping Negative V_{FB} Ramping Positive		–5 5	–7.5 7.5	–10 10	% %
Ch 2 Phase	Channel 2 Phase (Relative to Channel 1)	PHASMD = SGND PHASMD = Floating PHASMD = $INTV_{CC}$			180 180 240		Deg Deg Deg
CLKOUT Phase	CLKOUT Phase (Relative to Channel 1)	PHASMD = SGND PHASMD = Floating PHASMD = $INTV_{CC}$			60 90 120		Deg Deg Deg

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4642E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4642I is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The two outputs are tested separately and the same testing condition is applied to each output.

Note 4: 100% tested at wafer level only.

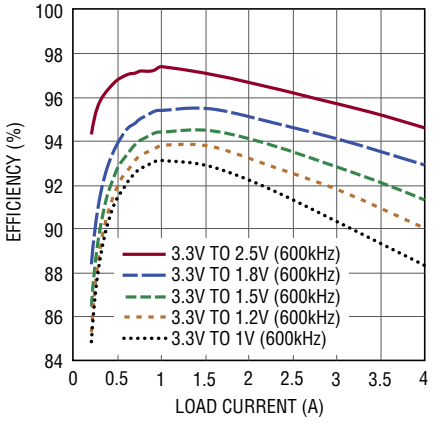
Note 5: See Output Current Derating curves for different V_{IN}, V_{OUT} and T_A.

Note 6: Consult factory for operation down at 2.375V to 2.5V input. Operating frequency nominal will be reduced.

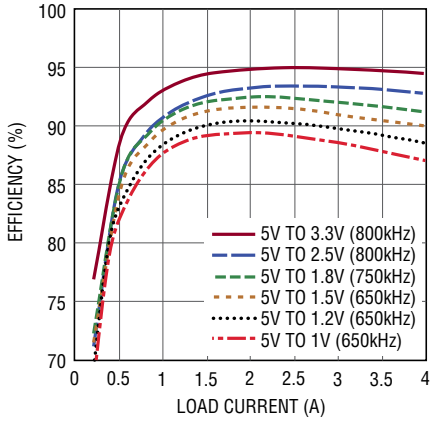
TYPICAL PERFORMANCE CHARACTERISTICS

(Refer to Figures 19 and 20) T_A = 25°C, unless otherwise noted.

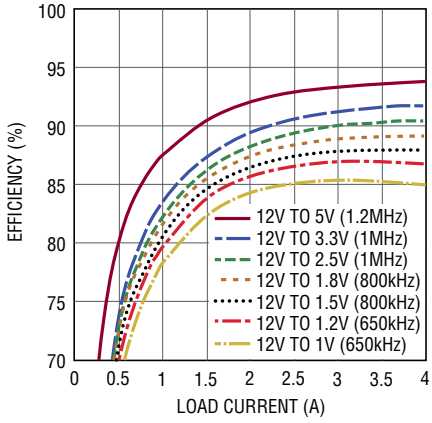
Efficiency vs Load Current at 3.3V_{IN}, CCM Mode, External 5V Bias



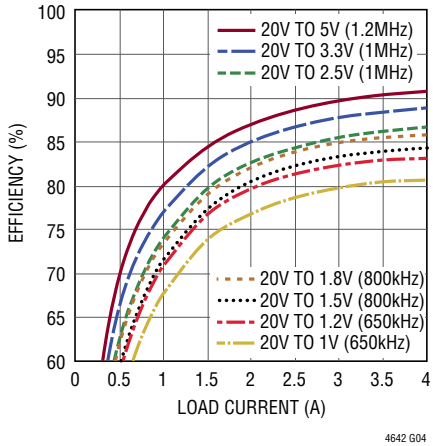
Efficiency vs Load Current at 5V_{IN}, CCM Mode



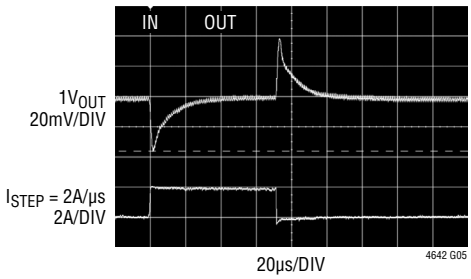
Efficiency vs Load Current at 12V_{IN}, CCM Mode



Efficiency vs Load Current at 20V_{IN}, CCM Mode

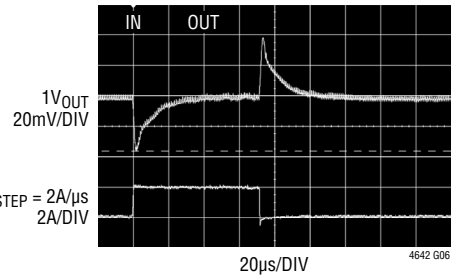


3.3V_{IN} to 1V_{OUT} Transient Response



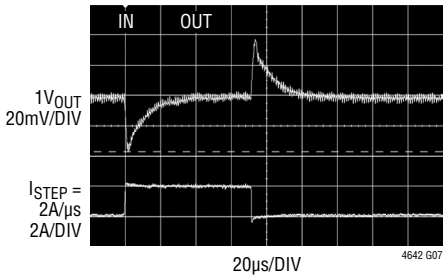
C_{OUT} = 100µF 15mΩ ESR POSCAP,
47µF CERAMIC
C_{FF} = 470pF
f_{SW} = 600kHz

5V_{IN} to 1V_{OUT} Transient Response



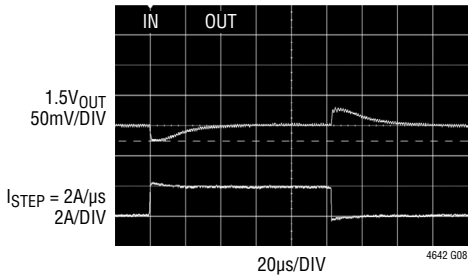
C_{OUT} = 100µF 15mΩ ESR POSCAP,
47µF CERAMIC
C_{FF} = 470pF
f_{SW} = 650kHz

12V_{IN} to 1V_{OUT} Transient Response



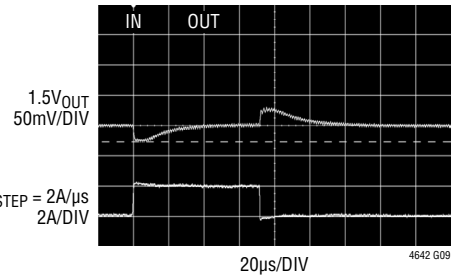
C_{OUT} = 100µF 15mΩ ESR POSCAP,
47µF CERAMIC
C_{FF} = 470pF
f_{SW} = 650kHz

3.3V_{IN} to 1.5V_{OUT} Transient Response



C_{OUT} = 120µF 22mΩ ESR OSCON SVP,
47µF CERAMIC
C_{FF} = 470pF
f_{SW} = 600kHz

5V_{IN} to 1.5V_{OUT} Transient Response

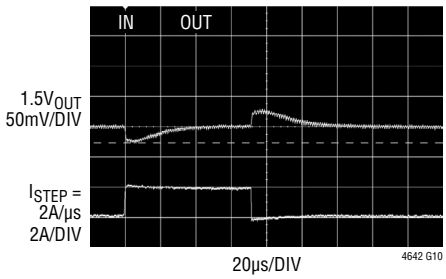


C_{OUT} = 120µF 22mΩ ESR OSCON SVP,
47µF CERAMIC
C_{FF} = 470pF
f_{SW} = 650kHz

TYPICAL PERFORMANCE CHARACTERISTICS

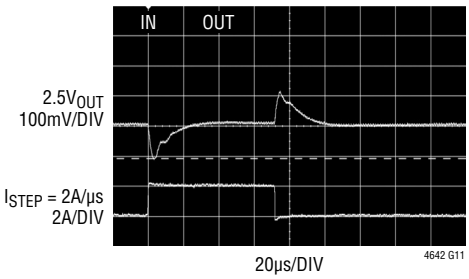
(Refer to Figures 19 and 20) T_A = 25°C, unless otherwise noted.

$12V_{IN}$ to $1.5V_{OUT}$ Transient Response



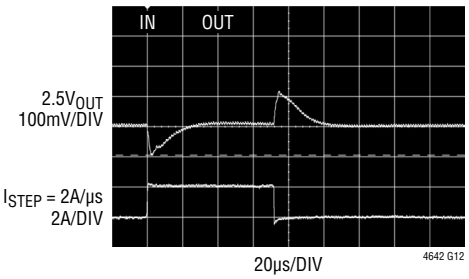
C_{OUT} = 120µF 22mΩ ESR OSCON SVP,
47µF CERAMIC
C_{FF} = 470pF
f_{SW} = 800kHz

$3.3V_{IN}$ to $2.5V_{OUT}$ Transient Response



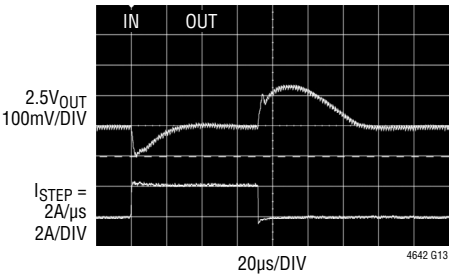
C_{OUT} = 47µF CERAMIC
C_{FF} = 68pF
f_{SW} = 600kHz

$5V_{IN}$ to $2.5V_{OUT}$ Transient Response



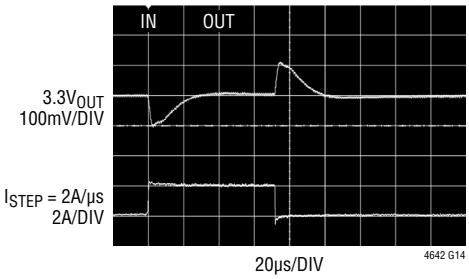
C_{OUT} = 47µF CERAMIC
C_{FF} = 68pF
f_{SW} = 800kHz

$12V_{IN}$ to $2.5V_{OUT}$ Transient Response



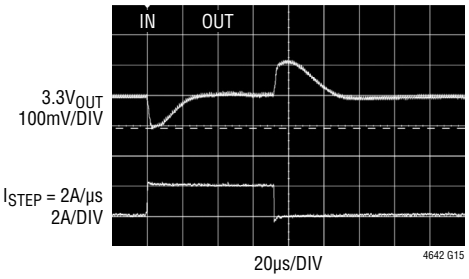
C_{OUT} = 47µF CERAMIC
C_{FF} = 68pF
f_{SW} = 1MHz

$5V_{IN}$ to $3.3V_{OUT}$ Transient Response



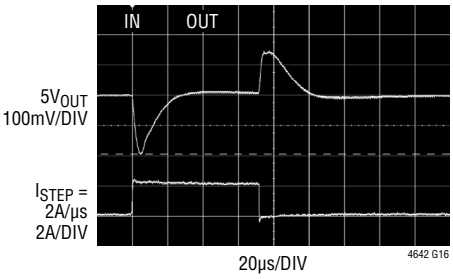
C_{OUT} = 47µF CERAMIC
C_{FF} = 68pF
f_{SW} = 800kHz

$12V_{IN}$ to $3.3V_{OUT}$ Transient Response



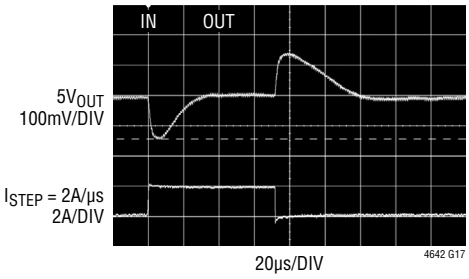
C_{OUT} = 47µF CERAMIC
C_{FF} = 68pF
f_{SW} = 1MHz

$6V_{IN}$ to $5V_{OUT}$ Transient Response



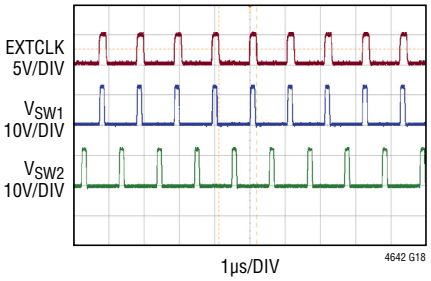
INPUT CAPACITOR 680µF 10V,
LOW IMPEDANCE INPUT CAN USE MUCH LESS
C_{OUT} = 47µF CERAMIC
C_{FF} = 68pF
f_{SW} = 600kHz

$12V_{IN}$ to $5V_{OUT}$ Transient Response



C_{OUT} = 47µF CERAMIC
C_{FF} = 68pF
f_{SW} = 1.2MHz

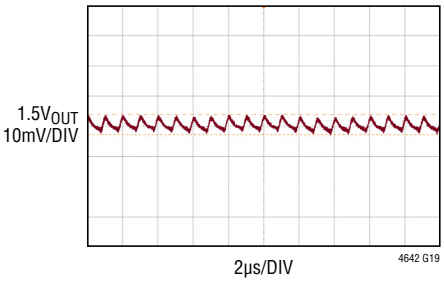
Clock Synchronization



TYPICAL PERFORMANCE CHARACTERISTICS

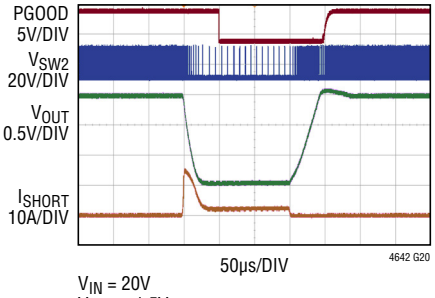
(Refer to Figures 19 and 20) T_A = 25°C, unless otherwise noted.

Output Ripple, 10mV Typical



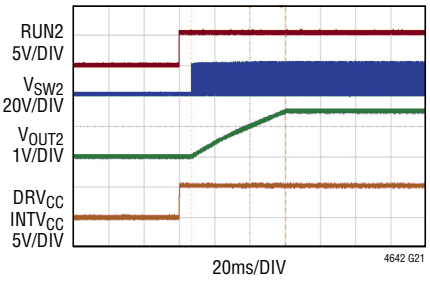
12V TO 1.5V AT 4A
C_{OUT} = 100µF CERAMIC, 47µF CERAMIC
f_{SW} = 800kHz

Shorted Output



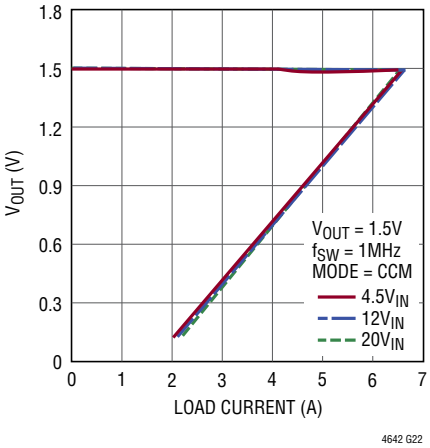
V_{IN} = 20V
V_{OUT} = 1.5V

Start-Up, 20V to 1.5V at 4A



C_{OUT} = 100µF CERAMIC, 47µF CERAMIC
C_{SS} = 0.1µF

Load Regulation and Current Limit (No Airflow)



PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (A4-A7, C2, D1, D5, E1, E5, E7, F7, H4-H7): Power ground pins for both input and output returns.

PHASMD (B4): Phase Mode Selection Pin for Programming Clock Out Phase. See Electrical Characteristics and Applications Information sections.

MODE/PLLIN (C3): Mode Selection or External Synchronization Pin. Tying this pin to SGND enables discontinuous mode. Tying this pin to $INTV_{CC}$ enables forced continuous operation. A clock on the pin will force the controller into the continuous mode of operation and synchronize the internal oscillator. The suitable synchronizable frequency range is 600kHz to 1400kHz subject to inductor ripple current limits described in the FREQ/PLLFLTR pin section. The external clock input high threshold is 2V, while the input low threshold is 0.5V.

CPWR (C7): This pin is the main input power to the control IC. This pin normally connects to the input source directly. This pin can be biased at a voltage greater than 4.5V to allow the V_{IN1} and V_{IN2} to operate down to 2.375V input for applications that operate at 2.5V or 3.3V input. If the bias is less than or equal to 5.3V, connect DRV_{CC} to this pin.

SGND (D2, E2): Signal Ground Pins. Return ground path for all analog and low power circuitry. Tie a single connection to PGND in the application. See the Recommended Layout section.

CLKOUT (D4): Clock Out for Synchronizing Other Regulators to the Common Clock. Used for multiphase applications. See Applications Information section.

$EXTV_{CC}$ (D6): External Power Input to Controller. When $EXTV_{CC}$ is higher than 4.7V, the internal 5.3V regulator is disabled and the external source supplies current to reduce the power dissipation in the module. This will improve the efficiency more at high input voltages.

$INTV_{CC}$ (D7): This pin powers the internal control circuits. Tie this pin to DRV_{CC} with a 2.2Ω resistor. This pin requires a few milliamps.

COMP1, COMP2 (E3, D3): Current Control Threshold and Error Amplifier Compensation Point. The module has been internally compensated for all I/O ranges.

FREQ (E4): Frequency Selection Pin. Tie a resistor from this pin to SGND to set the frequency of operation between 600kHz to 1.4MHz for the specific output voltages. For 3.3V input applications, 650kHz is an optimized frequency. For 5V to 20V input applications, the optimized operating frequency for the output voltage is as follows: 0.8V to 1.2V (650kHz), 1.5V to 1.8V (800kHz), 2.0V to 5V (1.2MHz), 5V from 20V input (1.4MHz). The resistor equation:

$$R_{FREQ}\,(k\Omega) = \frac{41550}{FREQ\,(kHz)} - 2.2$$

DRV_{CC} (E6): This pin is the LDO 5.3V regulator output used to power the internal control circuits and MOSFET drivers. This pin needs a 4.7µF ceramic decoupling capacitor to GND. For input voltages less than or equal to 5.3V, connect this pin directly to the input voltage.

V_{OUTS1} (F2): Output Voltage Sense Point for Channel 1 Remote Sensing. This pin has a 49.9Ω resistor connected to V_{OUT1}. This pin can be connected at the load point for accurate remote sensing.

V_{OUTS}^- (F3): Remote Ground Sense Pin. Connect at remote ground point.

V_{FB1}, V_{FB2} (F4, C4): The negative input of the error amplifier. Internally, this pin is connected to V_{OUT} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and SGND pins. See the Applications Information section for details.

TRACK/SS1, TRACK/SS2 (F5, C5): Output Voltage Tracking and Soft-Start Pins. Internal soft-start currents of 1.0µA charge the soft-start capacitors. See the Applications Information section to use the tracking function.

PGOOD1, PGOOD2 (F6, C6): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point. In single output parallel operation when V_{FB2} is tied to $INTV_{CC}$, the PGOOD2 pin is not to be used.

PIN FUNCTIONS

RUN1, RUN2 (G3, B3): Run Control Pins. A source can be used to enable the RUN pins with an external pull-up resistor. Forcing either of these pins below 1.2V will shut down the corresponding outputs. An additional 5µA pull-up current is added to this pin, once the RUN pin rises above 1.2V. Also, active control or pull-up resistors can be used to enable the RUN pin. The maximum voltage is 6V on these pins. There are 100k resistors on RUN1,2 to ground. It is recommended to use an external pull-up resistor to V_{IN} to enable the RUN pin. See the Applications Information section.

V_{RNG1} (G4): Used at Final Test. Tie to $INTV_{CC}$ in normal operation. This pin can also be used to adjust the current limit of channel 1. An external resistive divider from $INTV_{CC}$ can be used to set the voltage on the V_{RNG} pin between 0.6V to 1V, resulting in a maximum sense voltage between 30mV and 50mV. For applications that require less than 7A of the default peak current limit, the V_{RNG} pin voltage can be scaled down to obtain a desired current limit level.

V_{IN1} (G5, G6, 67), V_{IN2} (B5, B6, B7): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT1} (F1, G1, G2, H1, H2), V_{OUT2} (A1, A2, B1, B2, C1): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing output decoupling capacitance directly between these pins and PGND pins.

SW1, SW2 (H3, A3): Switching Test Pins. These pins are provided externally to check the operation frequency.

SIMPLIFIED BLOCK DIAGRAM

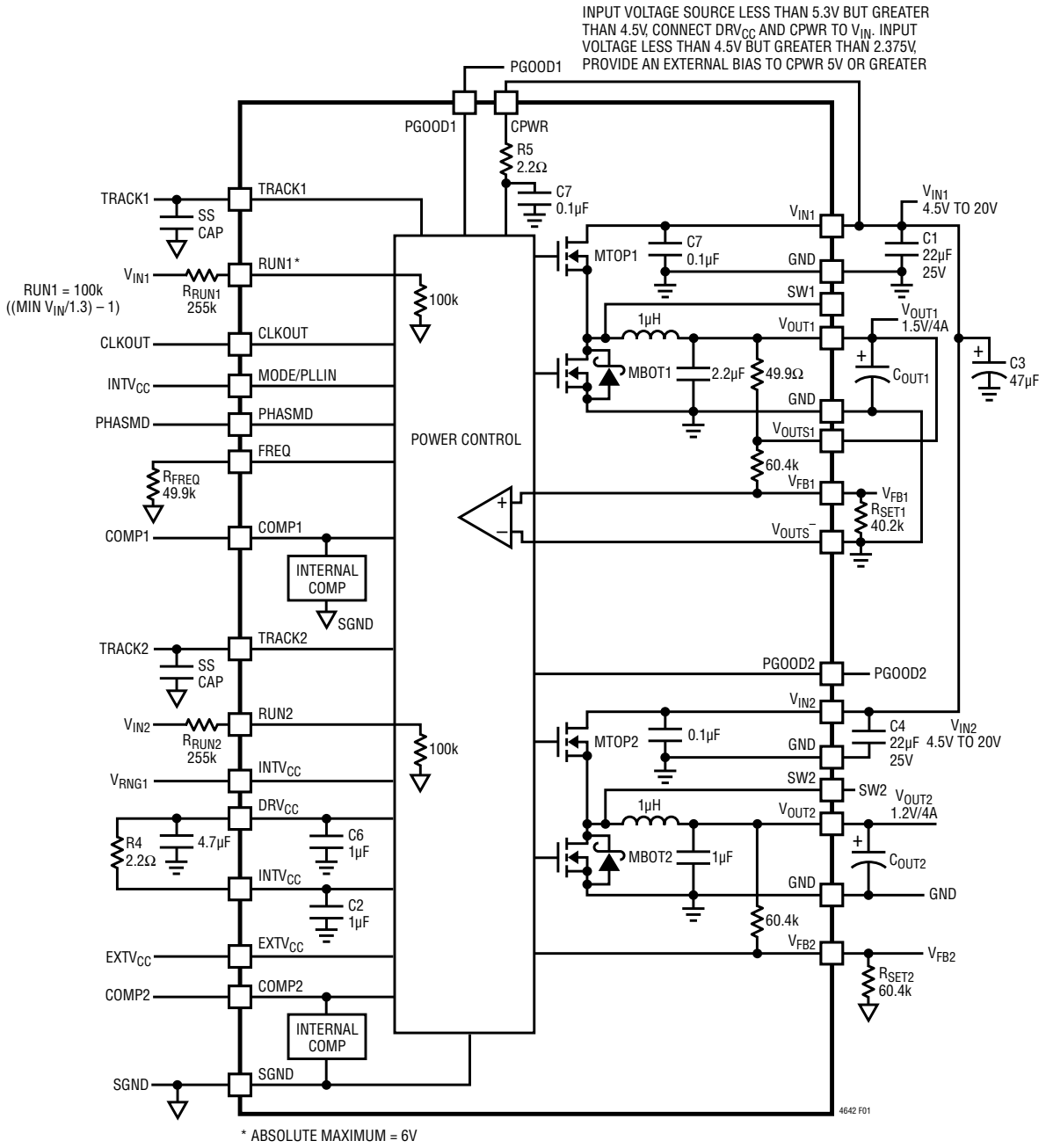


Figure 1. Simplified LTM4642 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement V_{IN} = 4.5V to 20V, V_{OUT1} = 1.5V, V_{OUT2} = 1.5V	I_{OUT1} = 4A, I_{OUT2} = 4A			22		µF
C_{OUT1} C_{OUT2}	External Output Capacitor Requirement V_{IN} = 4.5V to 20V, V_{OUT1} = 1.5V, V_{OUT2} = 1.5V	I_{OUT1} = 4A I_{OUT2} = 4A			150 150		µF µF

OPERATION

The LTM4642 is a dual independent input 4A nonisolated switching mode DC/DC power supply. It can deliver up to 4A (DC current) for each output with few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from 0.6V to 5.5V over a 4.5V to 20V input voltage range. The Typical Application schematic is shown in Figure 27. The input voltage source can operate down to 2.375V with an external bias applied to the CPWR pin. The external bias needs to be 5V or higher. See the Typical Applications schematics for examples.

The LTM4642 has integrated constant on-time valley current mode regulators and built-in power MOSFET devices with fast switching speed. To reduce switching noise, the two outputs are interleaved with 180° phase internally and can be synchronized externally using the MODE/PLLIN pin.

With current mode control and internal feedback loop compensation, the LTM4642 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit and current foldback in a short-circuit condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD pins output low if the output feedback voltage exits a ±7.5% window around the regulation point. The power good pin is disabled during start-up.

Pulling the RUN pins below 1.2V forces the controller into its shutdown state, by turning off both MOSFETs. The TRACK/SS pins are used for programming the output voltage ramp and voltage tracking during start-up. See the Applications Information section.

The LTM4642 is internally compensated to be stable over all operating conditions. LTpowerCAD® is available for transient and stability analysis. The V_{FB} pins are used to program the output voltage with a single external resistor to ground. Multiphase operation can be easily employed with clock synchronization.

High efficiency at light loads can be accomplished with selectable discontinuous mode using the MODE/PLLIN pin. Efficiency graphs are provided for light load operations in the Typical Performance Characteristics section.

APPLICATIONS INFORMATION

The typical LTM4642 application circuit is shown in Figure 27. External component selection is primarily determined by the maximum load current and output voltage.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor R_{FB} connects V_{OUT} to the V_{FB} pin. The output voltage will default to 0.6V with no feedback resistor. Adding a resistor R_{SET} from the V_{FB} pin to SGND programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{60.4k + R_{SET}}{R_{SET}}$$

or equivalently:

$$R_{SET} = \frac{60.4k}{\left(\frac{V_{OUT}}{0.6V} - 1\right)}$$

Table 1. R_{SET} Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5
R_{SET} (kΩ)	Open	90.9	60.4	40.2	30.1	19.1	13.3	8.25

V_{OUT1} supports feedback voltage referred remote sensing, as such the V_{OUTS1} pin can be tied to V_{OUT1} at the load sense point, and V_{OUTS}^- is tied to ground at the load sense point. V_{OUT2} is programmed with a resistor to ground. For a 2-phase single 8A output, the V_{FB2} pin can be connected to $INTV_{CC}$ to disable the channel 2 error amplifier, and internally connect the COMP2 pin to COMP1 pin. The COMP2 pin can be left floating or connected to COMP1 externally. The TRACK/SS2 and PGOOD2 pins are not functional in this mode, thus they can be left floating. See the Typical Applications at the end of the data sheet.

Input Capacitors

The LTM4642 module should be connected to a low AC-impedance DC source. A 47µF to 100µF surface mount aluminum electrolytic capacitor can be used for more input bulk capacitance. This bulk capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated aluminum electrolytic capacitor or a polymer capacitor. One 22µF ceramic input capacitor is typically rated for 2A of RMS ripple current, so the RMS input current at the worst case for each output at 4A maximum current is about 2A. If a low inductance plane is used to power the device, then two 22µF ceramic capacitors are enough for both outputs at 4A load and no external input bulk capacitor is required.

Output Capacitors

The LTM4642 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 47µF to 220µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spikes is required. LTpowerCAD is available for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. LTpowerCAD calculates the output ripple reduction as the number of implemented phases increased by N times. See Table 6 for output capacitor suggestions.

APPLICATIONS INFORMATION

Mode Selections and Phase-Locked Loop

The LTM4642 can be enabled to operate in discontinuous or forced continuous mode. To select the forced continuous operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select discontinuous operation, or tie the MODE/PLLIN pin to ground. This will improve the light load efficiency.

Frequency Selection and External Clock Synchronization

An internal oscillator (clock generator) provides phase interleaved internal clock signals for individual channels to lock on to. The switching frequency and phase of each switching channel is independently controlled by adjusting the top MOSFET turn-on time (on-time) through the one-shot timer. This is achieved by sensing the phase relationship between a top MOSFET turn-on signal and its internal reference clock through a phase detector, and the time interval of the one-shot timer is adjusted on a cycle-by-cycle basis, so that the rising edge of the top MOSFET turn-on is always trying to synchronize to the internal reference clock signal for the respective channel.

The frequency of the internal oscillator can be programmed from 600kHz to 1.4MHz by connecting a resistor, R_{FREQ}, from the FREQ pin to signal ground (SGND). The equation:

$$R_{FREQ}\,(k\Omega) = \frac{41550}{FREQ\,(kHz)} - 2.2$$

For applications with stringent frequency or interference requirements, an external clock source connected to the MODE/PLLIN pin can be used to synchronize the internal clock signals through a clock phase-locked loop (Clock PLL). The LTM4642 operates in forced continuous mode of operation when it is synchronized to the external clock. The external clock frequency has to be within ±30% of the internal oscillator frequency for successful synchronization. The clock input levels should be no less than 2V for “high” and no greater than 0.5V for “low”. The MODE/PLLIN pin has an internal 600k pull-down resistor.

PHASMD Pin Programming

The PHASMD pin determines the relative phases between the internal reference clock signals for the two channels as well as the CLKOUT signal, as shown in Table 2. The phases tabulated are relative to zero degree (0°) being defined as the rising edge of the internal reference clock signal of channel 1. The CLKOUT signal can be used to synchronize additional power regulator modules. The system can be configured for up to 12-phase operation with a multichannel solution. Typical configurations are shown in Table 3 to interleave the phases of the channels. The applications will validate a 6 phase multiple regulator solution with multiple outputs.

Each of the LTM4642 channels can be paralleled up to 8A of output, but cannot be paralleled from one module to the other modules. Twelve phases can be paralleled with no more than two phases per module.

Table 2

PHASMD	SGND	FLOAT	INTVCC
Channel 1	0°	0°	0°
Channel 2	180°	180°	240°
CLKOUT	60°	90°	120°

Table 3

NUMBER OF PHASES	NUMBER OF LTM4642*	PIN CONNECTIONS [PIN NAME (CHIP NUMBER)]
2	1	PHASMD(1) = FLOAT or SGND
3	2 or 1 + ½(LTM4642)	PHASMD(1) = $INTV_{CC}$ MODE/PLLIN(2) = CLKOUT(1)
4	2	PHASMD(1) = FLOAT PHASEMD(2) = FLOAT or SGND MODE/PLLIN(2) = CLKOUT(1)
6	3	PHASMD(1) = SGND PHASMD(2) = SGND MODE/PLLIN(2) = CLKOUT(1) PHASMD(3) = FLOAT or SGND MODE/PLLIN(3) = CLKOUT(2)

*No more than two channels of any one module may be paralleled.

Soft-Start and Tracking

The LTM4642 has the ability to either soft-start by itself with a capacitor or track the output of another channel or external supply. When one particular channel is configured to soft-start by itself, a capacitor should be connected to its TRACK/SS pin. This channel is in the shutdown state if its RUN pin voltage is below 1.2V. Its TRACK/SS pin is actively pulled to ground in this shutdown state.

APPLICATIONS INFORMATION

Once the RUN pin voltage is above 1.2V, the channel powers up. A soft-start current of 1µA then starts to charge its soft-start capacitor. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the TRACK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to 0.6V on the TRACK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFT\text{-}START} = \frac{0.6V \bullet C_{SS}(\mu F)}{1\mu A}$$

Output voltage tracking can be programmed externally using the TRACK/SS pin. The master channel is divided down with an external resistor divider that is the same as the slave channel's feedback divider to implement coincident tracking. The LTM4642 uses an accurate 60.4k resistor internally for the top feedback resistor. Figure 2 shows an example of coincident tracking. Figure 3 shows the output voltages with coincident tracking.

$$V_{SLAVE} = \left(1 + \frac{R1}{R2}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's TRACK/SS2 pin. V_{TRACK} has a control range of 0V to 0.6V. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point.

Ratiometric modes of tracking can be achieved by selecting different divider resistors values to change the output tracking ratio. The master output must be greater than the

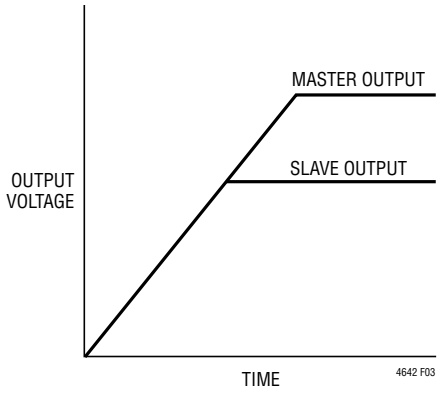
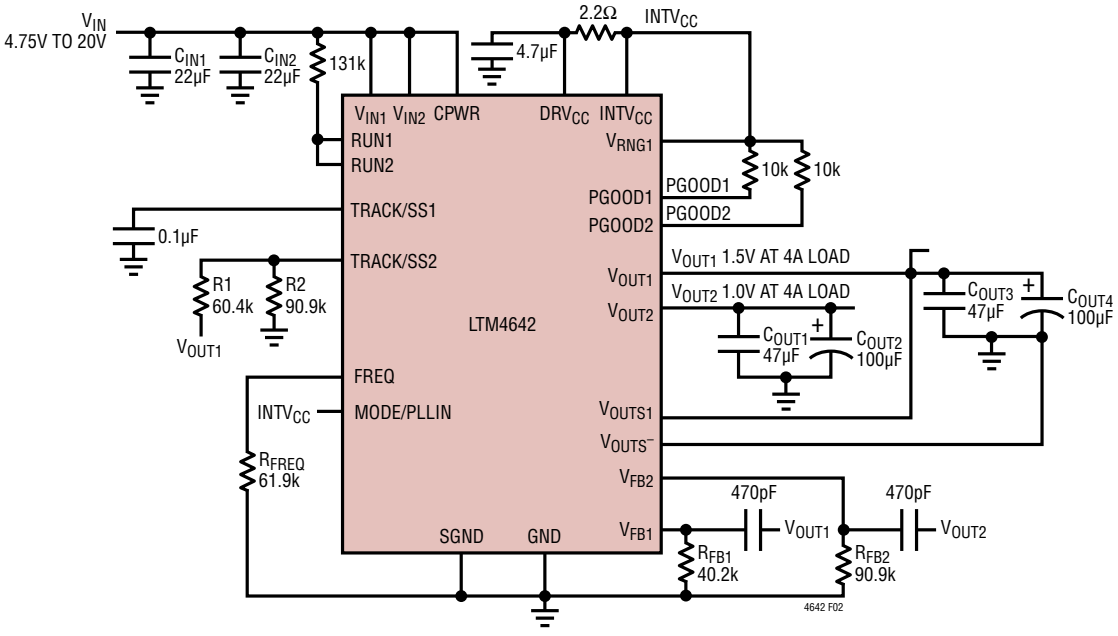


Figure 3. Coincident Tracking



PINS NOT USED: COMP1, COMP2, PHASEMD, CLKOUT, $EXTV_{CC}$, SW1, SW2

Figure 2. Example of Coincident Tracking

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slave output for the tracking to work. Master and slave data inputs can be used to implement the correct resistors values for coincident or ratiometric tracking.

Multiphase Operation

Multiphase operation with the LTM4642 two regulator channels in parallel will lower the effective input RMS ripple current as well as the output ripple current due to the interleaving operation of the regulators. Figure 4 provides a ratio of input RMS ripple current to DC load current as a function of duty cycle and the number of paralleled phases. Choose the corresponding duty cycle and the number of phases to get the correct ripple current value. For example, the 2-phase parallel for one LTM4642 design provides 8A at 2.5V output from a 12V input. The duty cycle is DC = 2.5V/12V = 0.21. The 2-phase curve has a ratio of ~0.25 for a duty cycle of 0.21. This 0.25 ratio of RMS ripple current to a DC load current of 8A equals ~2A of input RMS ripple current for the external input capacitors. No more than two phases of a module may be paralleled.

The effective output ripple current is lowered with multiphase operations as well. Figure 5 provides a ratio of peak-to-peak output ripple current to the normalized output ripple current as a function of duty cycle and the number of paralleled phases. Choose the corresponding duty cycle and the number of phases to get the correct output ripple current ratio value. If a 2-phase operation is chosen at $12V_{IN}$ to $2.5V_{OUT}$ with a duty cycle of 21%, then 0.6 is the ratio of the normalized output ripple current to inductor ripple DIr at the corresponding duty cycle. This leads to ~1.3A of the effective output ripple current ΔI_L if the DIr is at 2.2A. Refer to Application Note 77 for a detailed explanation of the output ripple current reduction as a function of paralleled phases.

The output ripple voltage has two components that are related to the amount of bulk capacitance and effective series resistance (ESR) of the output bulk capacitance. Therefore, the output ripple voltage can be calculated with the known effective output ripple current. The equation:

$$\Delta V_{OUT(P-P)} \approx \Delta I_L/(8 \bullet f \bullet N \bullet C_{OUT}) + ESR \bullet \Delta I_L$$

where f is frequency and N is the number of parallel phases.

RUN Pin

The RUN pins can be used to enable or sequence the particular regulator channel. The RUN pins have their own internal 1.2µA current source to pull up the RUN pins to 1.2V, and the current will increase to 5µA above 1.2V. Board contamination or residue can load down these small pull-up currents, so a 100k resistor is placed from the RUN pins to ground. This 100k resistor can be used with a resistor to V_{IN} to set the turn-on threshold for the RUN pins

The resistor divider needs to be low enough resistance to swamp out the pull-up current sources to prevent unintended activation of the device. The RUN pin has a maximum rated voltage of 6V. See Figure 1 Block Diagram for set turn on equation.

Power Good

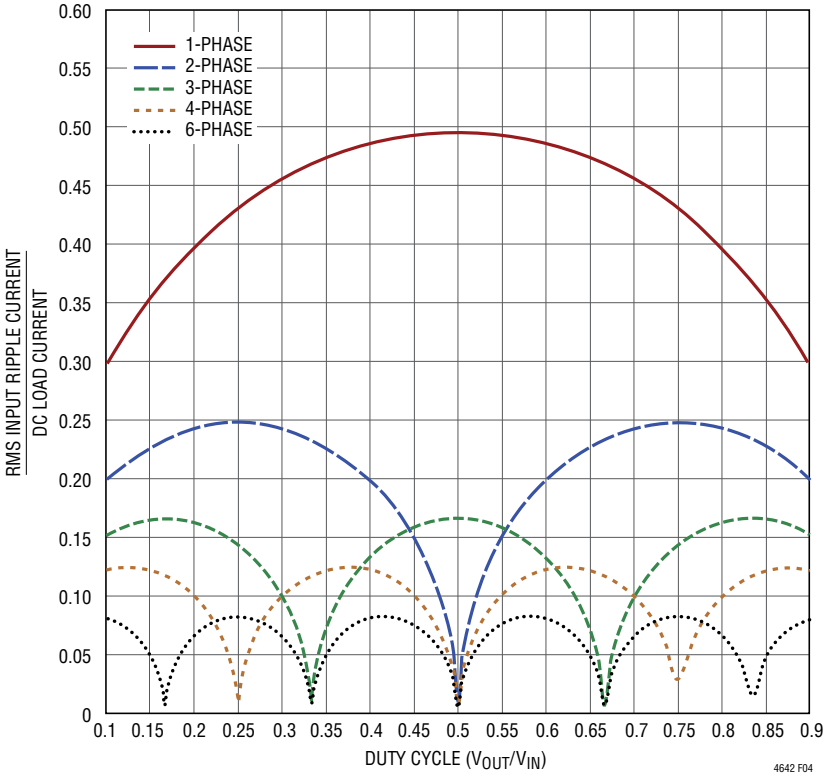
The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when either V_{FB} pin voltage is not within ±7.5% of the 0.6V reference voltage. The PGOOD pin is also pulled low when either RUN pin is below 1.2V or when the LTM4642 is in the soft-start or tracking phase. When the V_{FB} pin voltage is within the ±7.5% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V. The PGOOD pin will flag power good immediately when both V_{FB} pins are within the ±7.5% window. However, there is an internal 17µs power bad mask when either V_{FB} goes out of the ±7.5% window. In parallel single output operation, only use PGOOD1.

CPWR, DRV_{CC}, $INTV_{CC}$ and $EXTV_{CC}$

The CPWR is the main power input to the internal control IC. This pin is normally connected to the input voltage source. This pin can be biased with a 5V supply when operating at input voltages below 4.5V. When $4.5V < V_{IN} < 5.3V$, Then tie CPWR to DRV_{CC}. See the Typical Applications.

The DRV_{CC} is the internal 5.3V regulator that powers the LTM4642 internal MOSFET drivers for the internal power MOSFETs. The DRV_{CC} requires a 4.7µF ceramic capacitor to ground. $INTV_{CC}$ powers the internal controller circuits and is connected to DRV_{CC} through a 2.2Ω resistor. This $INTV_{CC}$ bias is ≤ 20mA.

APPLICATIONS INFORMATION



*THE LTM4642 CAN ONLY HAVE THE TWO CHANNELS PER MODULE PARALLELED

Figure 4. Normalized Input RMS Ripple Current vs Duty Cycle for One to Six Phases*

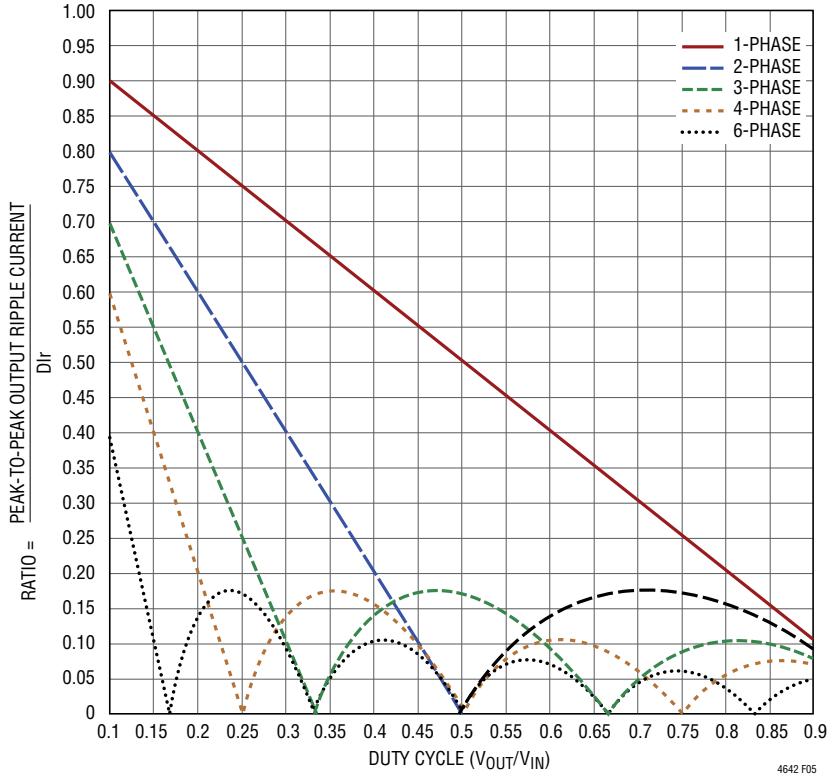


Figure 5. Normalized Output Ripple Current vs Duty Cycle, DIr = V_{OUT} T/L

APPLICATIONS INFORMATION

A 5V output on channel 1 or 2 can be used to power the $EXTV_{CC}$ pin when the input voltage is at the high end of the supply range to reduce power dissipation in the module. For example, the dropout voltage for 20V input would be 20V – 5V = 15V. This 15V headroom then multiplied by the power MOSFET drive current of ~30mA would equal ~0.45W additional power dissipation. So utilizing a 5V output on the $EXTV_{CC}$ would improve design efficiency and reduce device temperature rise. Otherwise try to operate CWPR off of a 5V bias when operating at higher supply voltages. See the Typical Applications section.

Fault Conditions: Current Limit and Overcurrent Foldback

The LTM4642 has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in transient.

To further limit current in the event of an overload condition, the LTM4642 provides foldback current limiting. If the output voltage falls by more than 50%, then the maximum output current is progressively lowered to one-fourth of its full current limit value. Foldback current limiting is disabled during soft-start and tracking up.

SW Pins

The SW pins are generally for testing purposes by monitoring these pins. These pins can also be used to dampen out switch node ringing caused by LC parasitic in the switched current paths. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor. If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$Z_{(L)} = 2\pi fL,$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by: $Z_{(C)} = 1/(2\pi fC)$. These values are a good place to start with. Modification to these components should be made to attenuate the ringing with the least amount of power loss.

Thermal Considerations and Output Current Derating

In different applications, the LTM4642 operates in a variety of thermal environments. The maximum output current is limited by the environmental thermal condition. Sufficient cooling should be provided to ensure reliable operation. When the cooling is limited, proper output current derating is necessary, considering the ambient temperature, airflow, input/output conditions, and the need for increased reliability.

The two outputs of the LTM4642 are paralleled to characterize the output current derating curves. The power loss curves in Figure 8 to Figure 10 can be used in coordination with load current derating curves in Figure 11 to Figure 24 for calculating an approximate θ_{JA} for the module with various cooling methods. Application Note 103 provides detailed explanation of the analysis for the thermal models and the derating curves. Tables 4 and 5 provide a summary of the equivalent θ_{JA} parameters are correlated to the measured values, and are improved with airflow.

The power loss curves are taken at room temperature, and are increased with multiplicative factors according to the ambient temperature. The approximate factors are: 1.35 for 115°C and 1.4 for 120°C. The derating curves are plotted with CH1 and CH2 paralleled output current starting at 8A and the ambient temperature starting at 50°C. The derated output voltages are 1.0V, 2.5V, 3.3V and 5.0V. Tables 4 and 5 specify the approximate θ_{JA} with airflow conditions for 1V and 5V outputs. These two conditions are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance, but any derating curve point along with power loss curve can be used to calculate the θ_{JA}. Thermal models are derived from several temperature measurements in a controlled temperature chamber along

APPLICATIONS INFORMATION

Table 4. 1V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	Θ_{JA} (°C/W)
Figures 11, 13	5, 12	Figures 8, 9	0	none	13
Figures 11, 13	5, 12	Figures 8, 9	200	none	10
Figures 11, 13	5, 12	Figures 8, 9	400	none	9
Figures 12, 14	5, 12	Figures 8, 9	0	BGA Heat Sink	13
Figures 12, 14	5, 12	Figures 8, 9	200	BGA Heat Sink	8
Figures 12, 14	5, 12	Figures 8, 9	400	BGA Heat Sink	7.5

Table 5. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	Θ_{JA} (°C/W)
Figures 21, 23	12, 20	Figures 9, 10	0	none	15
Figures 21, 23	12, 20	Figures 9, 10	200	none	13
Figures 21, 23	12, 20	Figures 9, 10	400	none	12
Figures 22, 24	12, 20	Figures 9, 10	0	BGA Heat Sink	14
Figures 22, 24	12, 20	Figures 9, 10	200	BGA Heat Sink	10
Figures 22, 24	12, 20	Figures 9, 10	400	BGA Heat Sink	10

Table 6. Output Voltage Response vs Component Matrix (Refer to Figure 27) 0A to 2A Load Step Typical Measured Values

CERAMIC CAPACITOR VENDORS	VALUE	PART NUMBER
Murata	C_{OUT}: 47µF 6.3V, X5R	GRM21BR60J476ME15
Murata	C_{OUT}: 47µF 10V, X5R	GRM31CR61A476KE15
Murata	C_{IN}: 22µF, X7R, 16V	GRM32ER71C226KEA8

BULK VENDORS	VALUE	PART NUMBER	ESR
Sanyo OSCON SVPC	C_{OUT}: 120µF 10V	10SVPC120MV	22mΩ
Panasonic SP	C_{OUT}: 100µF 6.3V	EEFCTOJ101R	15mΩ

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)**	C_{OUT1} (CERAMIC)	C_{OUT2} (CER AND BULK)	C_{FF} (pF)	V_{IN} (V)	DROOP (mV)	PEAK TO PEAK	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)	FREQ (kHz)
1	22µF × 2	56µF	47µF	100µF or 120µF	470	3.3, 5, 12	31	62	20	2	90.9	650
1.2	22µF × 2	56µF	47µF	100µF or 120µF	470	3.3, 5, 12	30	63	20	2	60.4	650
1.5	22µF × 2	56µF	47µF	100µF or 120µF	470	3.3, 5, 12	35	70	20	2	40.2	700
1.8	22µF × 2	56µF	47µF	100µF or 120µF	470	3.3, 5, 12	38	80	25	2	30.1	750
2.5	22µF × 2	56µF	47µF		68	3.3, 5, 12	100	200	20	2	19.1	1000
3.3	22µF × 2	56µF	47µF		68	5, 12	120	240	20	2	13.3	1000
5	22µF × 2	56µF	47µF		68		185	390	20	2	8.25	1200

** Bulk capacitance is optional if V_{IN} has very low input impedance.

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Cool Innovations	3-05040	www.coolinnovations.com
Chomerics	T411 Interface	www.chomerics.com

APPLICATIONS INFORMATION

with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 14 the load current is derated to ~7A at ~100°C with no air or heat sink and the power loss for the 12V to 1.0V at 7A output is about 1.2W (power loss at 3.5A load multiplied by 2). The 1.2W loss is multiplied by the 1.4 multiplying factor at 120°C junction to get 1.68W. If the 100°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 20°C divided by 1.68W equals a 12°C/W thermal resistance. Table 4 specifies a 13°C/W value which is very close. Table 4 and Table 5 provide equivalent thermal resistances for 1.0V and 5V outputs with and without airflow and heat sinking. The derived thermal resistances in Tables 4 and 5 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm. The BGA heat sinks are listed below Table 5.

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board defined by JESD51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients is found in JESD51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.

2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don’t generally match the user’s application.

3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don’t generally match the user’s application.

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4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 6; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4642, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4642 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4642 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this

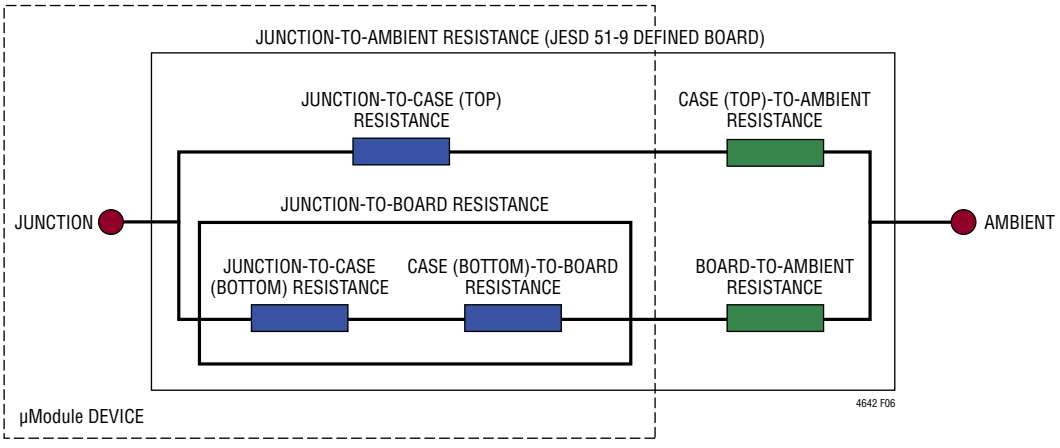

Figure 6. Graphical Representation of JESD51-12 Thermal Coefficients

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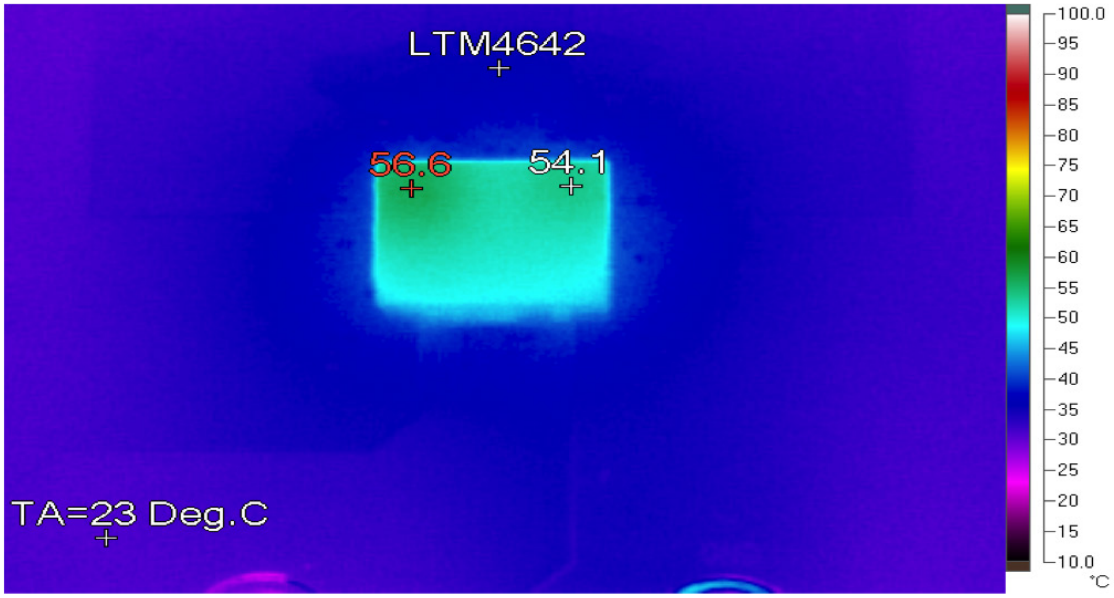
process and due diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory tests have been performed, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the LTM4642 model with no airflow or heat sinking in a properly define chamber. This $\theta_{JB} + \theta_{BA}$ value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink. Each system has its own thermal characteristics, therefore thermal analysis must be performed by the user in a particular system.

The LTM4642 has been designed to effectively remove heat from both the top and bottom of the package. The bottom substrate material has very low thermal resistance to the printed circuit board and the exposed top metal is thermally connected to the power devices and the power inductors. An external heat sink can be applied to the top of the device for excellent heat sinking with airflow. Basically all power dissipating devices are mounted directly to the substrate and the top exposed metal. This provides two low thermal resistance paths to remove heat.

Safety Considerations

The LTM4642 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.



V_{IN} (V)	V_{OUT1} (V)	V_{OUT2} (V)	I_{LOAD} PER PHASE (A)	f_{SW} (kHz)	HOT TEMP PEAK TEMP (°C)
12	2.5	1.5	4	1000	56.6

Figure 7. Thermal Plot for the Specified Operation. The Temperature Rise About 25°C Ambient Is About 30°C Rise

APPLICATIONS INFORMATION

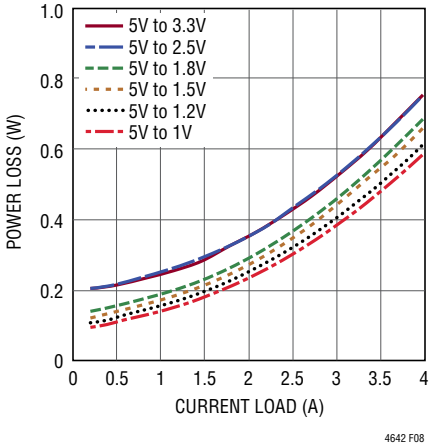


Figure 8. 5V Input Power Loss

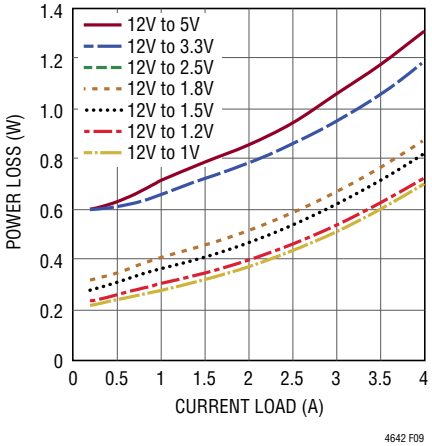


Figure 9. 12V Input Power Loss

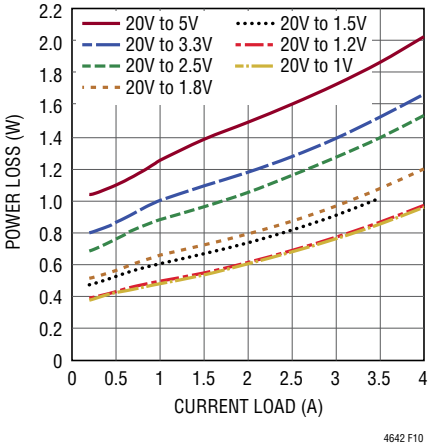


Figure 10. 20V Input Power Loss

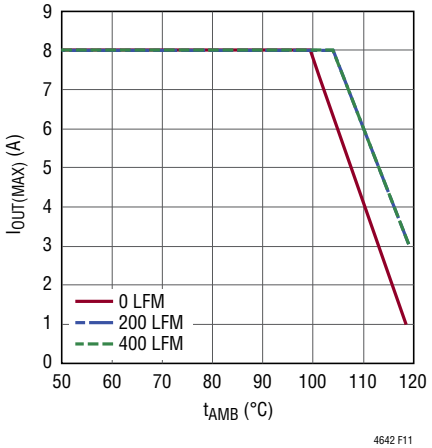


Figure 11. $5V_{IN}$, $1V_{OUT}$ 650kHz, No Heat Sink

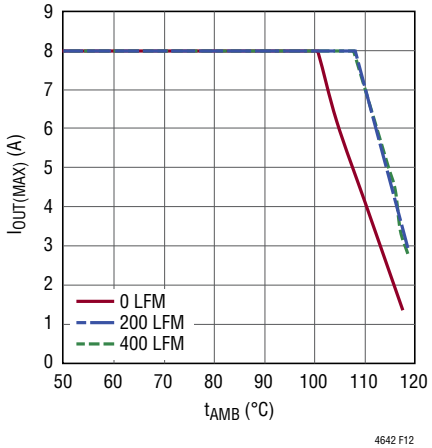


Figure 12. $5V_{IN}$, $1V_{OUT}$ 650kHz, with Heat Sink

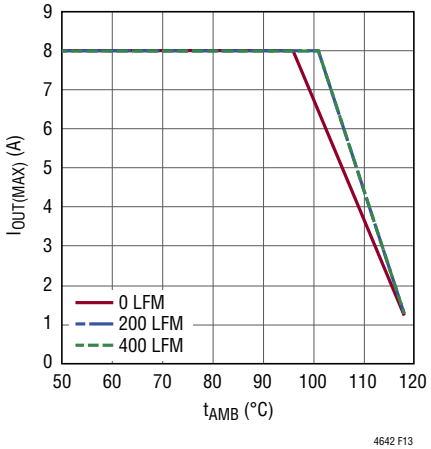


Figure 13. $12V_{IN}$, $1V_{OUT}$ 650kHz, No Heat Sink

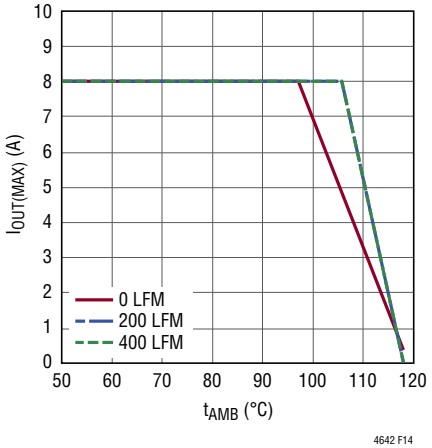


Figure 14. $12V_{IN}$, $1V_{OUT}$ 650kHz, with Heat Sink

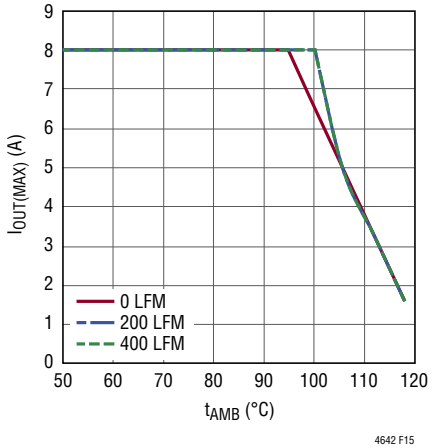


Figure 15. $5V_{IN}$, $3.3V_{OUT}$ 650kHz, No Heat Sink

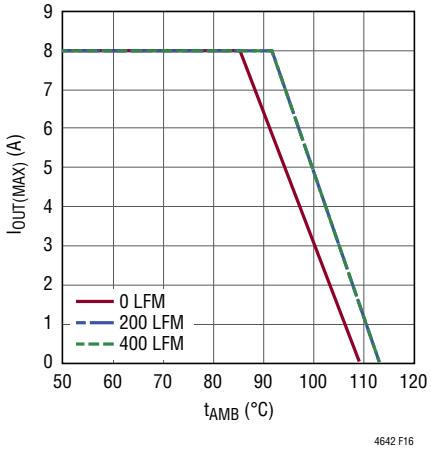


Figure 16. $5V_{IN}$, $3.3V_{OUT}$ 650kHz, with Heat Sink

APPLICATIONS INFORMATION

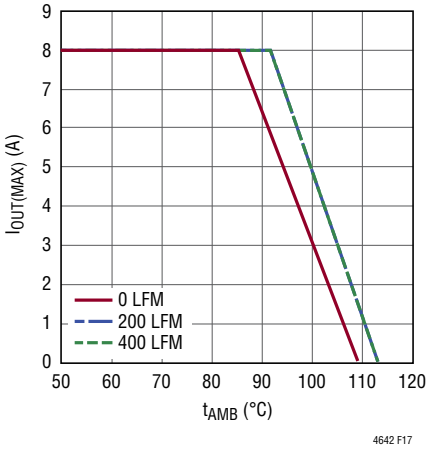


Figure 17. $12V_{IN}$, $2.5V_{OUT}$ 1MHz, No Heat Sink

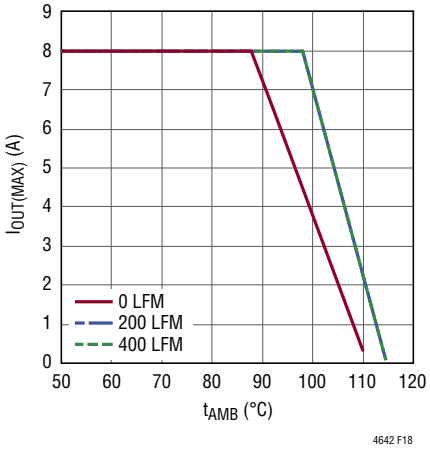


Figure 18. $12V_{IN}$, $2.5V_{OUT}$ 1MHz, with Heat Sink

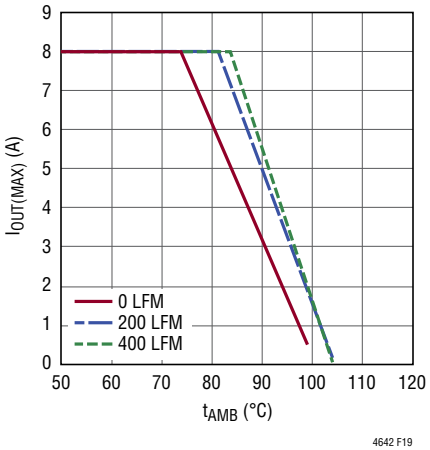


Figure 19. $20V_{IN}$, $2.5V_{OUT}$ 1MHz, No Heat Sink

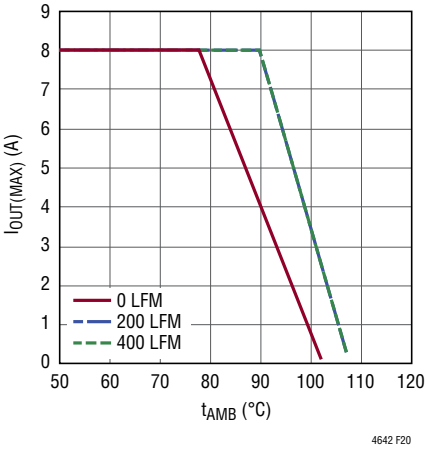


Figure 20. $20V_{IN}$, $2.5V_{OUT}$ 1MHz, with Heat Sink

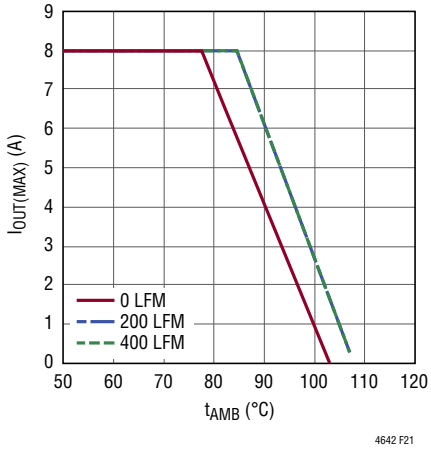


Figure 21. $12V_{IN}$, $5V_{OUT}$ 1.2MHz, No Heat Sink

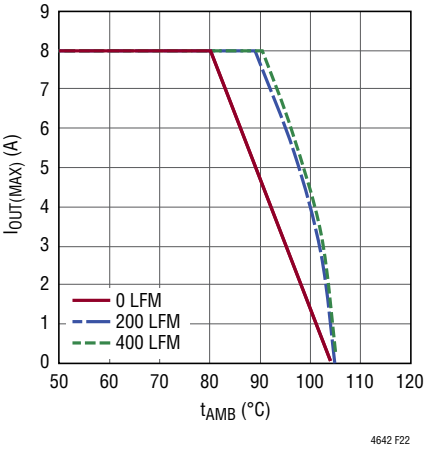


Figure 22. $12V_{IN}$, $5V_{OUT}$ 1.2MHz, with Heat Sink

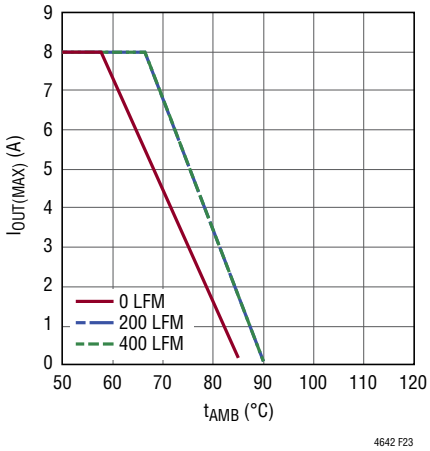


Figure 23. $20V_{IN}$, $5V_{OUT}$ 1.2MHz, No Heat Sink

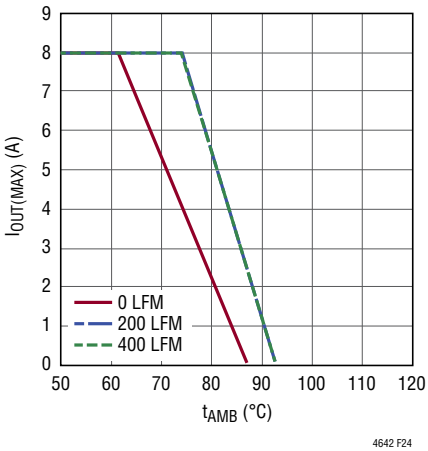


Figure 24. $20V_{IN}$, $5V_{OUT}$ 1.2MHz, with Heat Sink

APPLICATIONS INFORMATION

Layout Checklist/Example

The high integration of LTM4642 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN1}, V_{IN2}, PGND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnections between top layer and other power layers.
- Do not put vias directly on the pads.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.
- Decouple the input and output grounds to lower the output ripple noise.

Figure 25 gives a good example of the recommended layout.

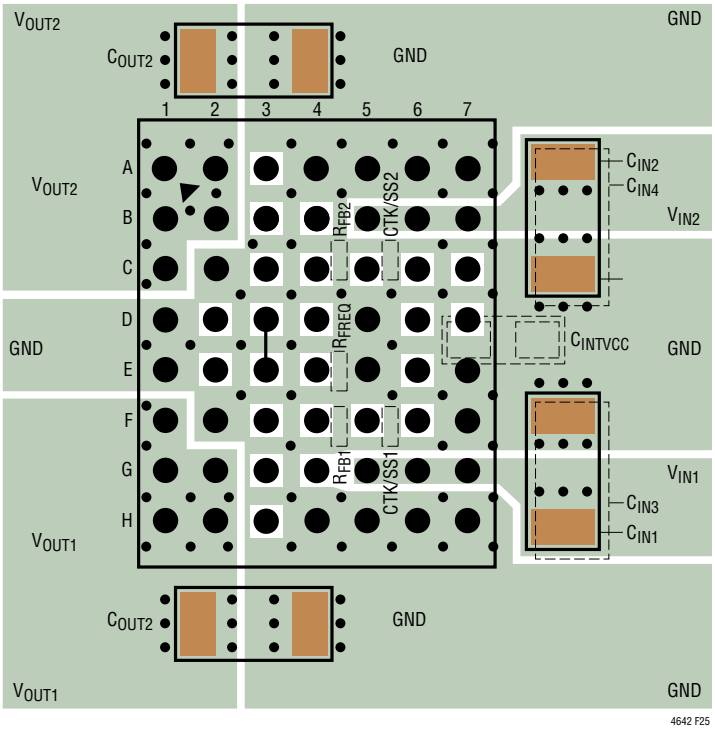
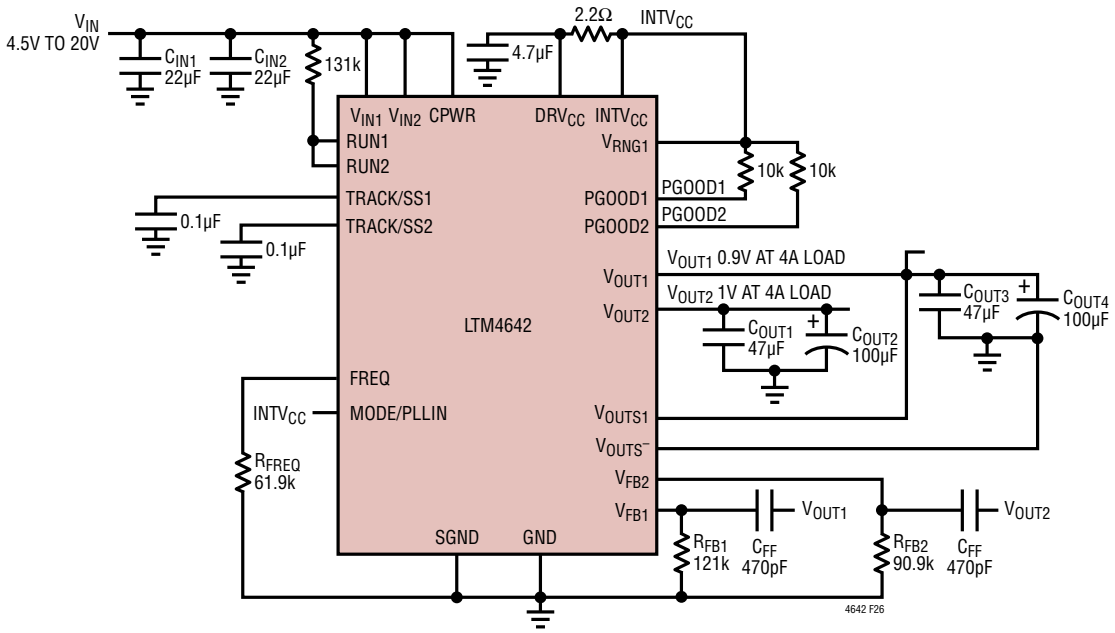


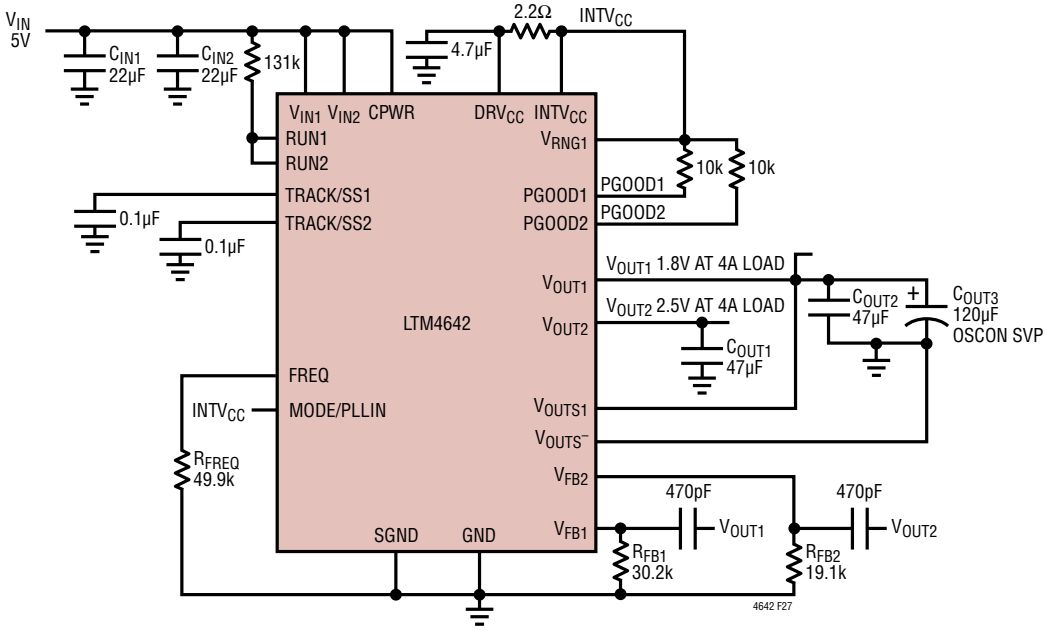
Figure 25. Recommended PCB Layout

TYPICAL APPLICATIONS



PINS NOT USED: COMP1, COMP2, PHASEMD, CLKOUT, $EXTV_{CC}$, SW1, SW2

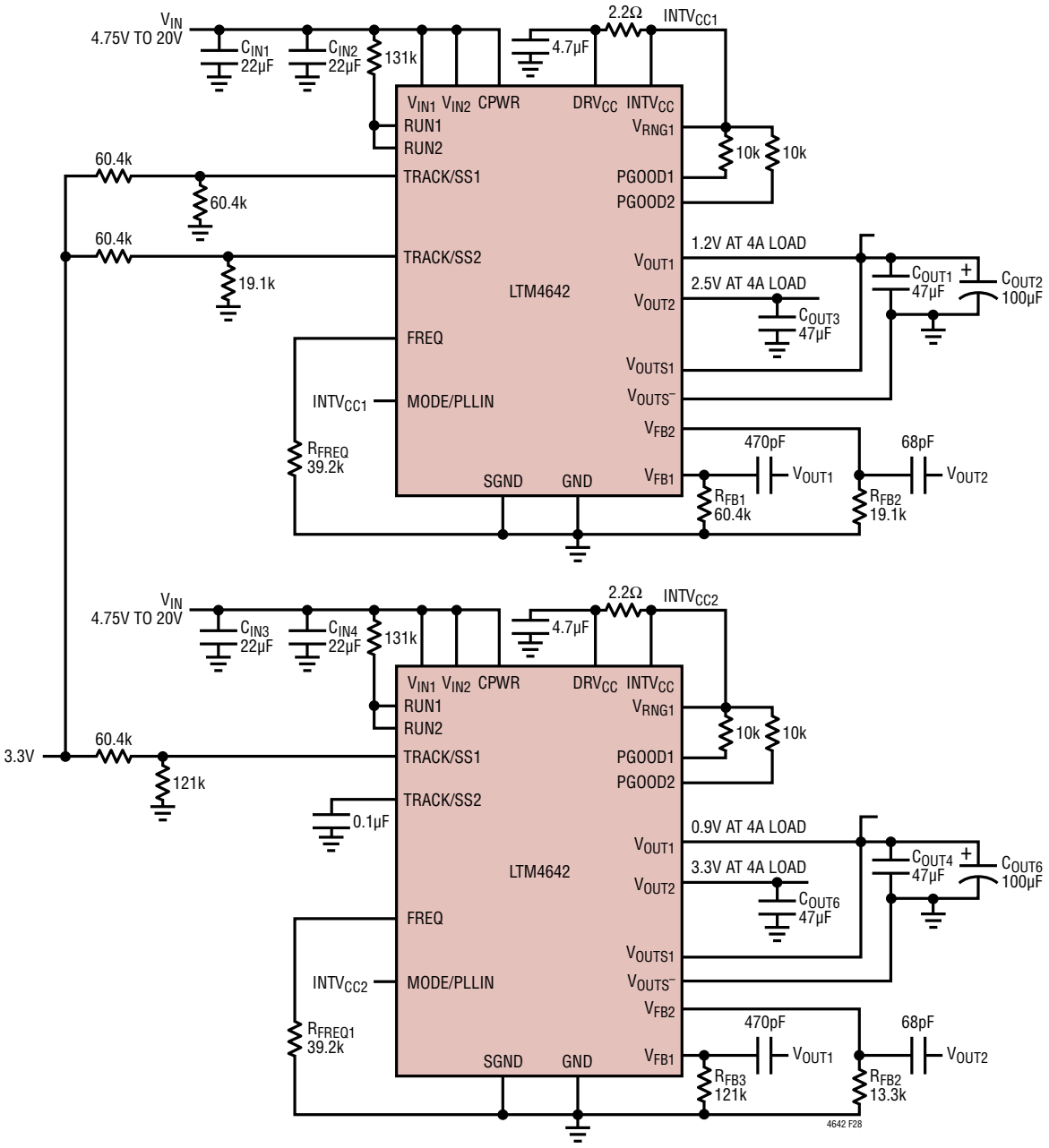
Figure 26. 4.5V to 20V Input, 650kHz, 0.9V and 1.2V Outputs at 4A Each



PINS NOT USED: COMP1, COMP2, PHASEMD, CLKOUT, $EXTV_{CC}$, SW1, SW2

Figure 27. 5V Input, 800kHz, 2.5V and 1.8V Outputs at 4A Each

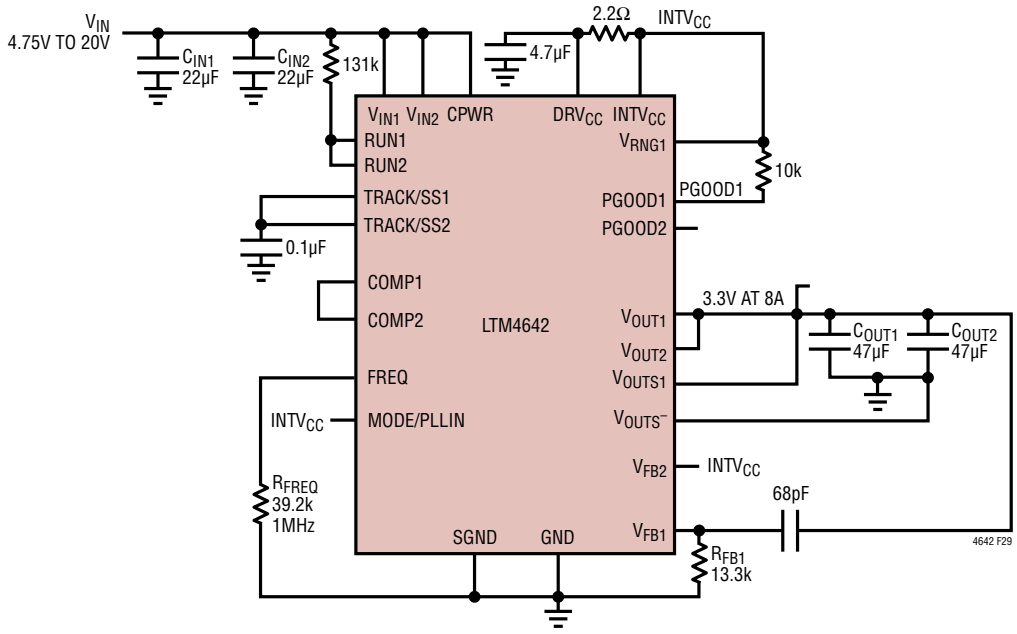
TYPICAL APPLICATIONS



PINS NOT USED: COMP1, COMP2, PHASEMD, CLKOUT, $EXTV_{CC}$, SW1, SW2

Figure 28. 1MHz 4-Phase, Four Outputs (3.3V, 2.5V, 1.2V, 0.9V) with Tracking to the 3.3V Output

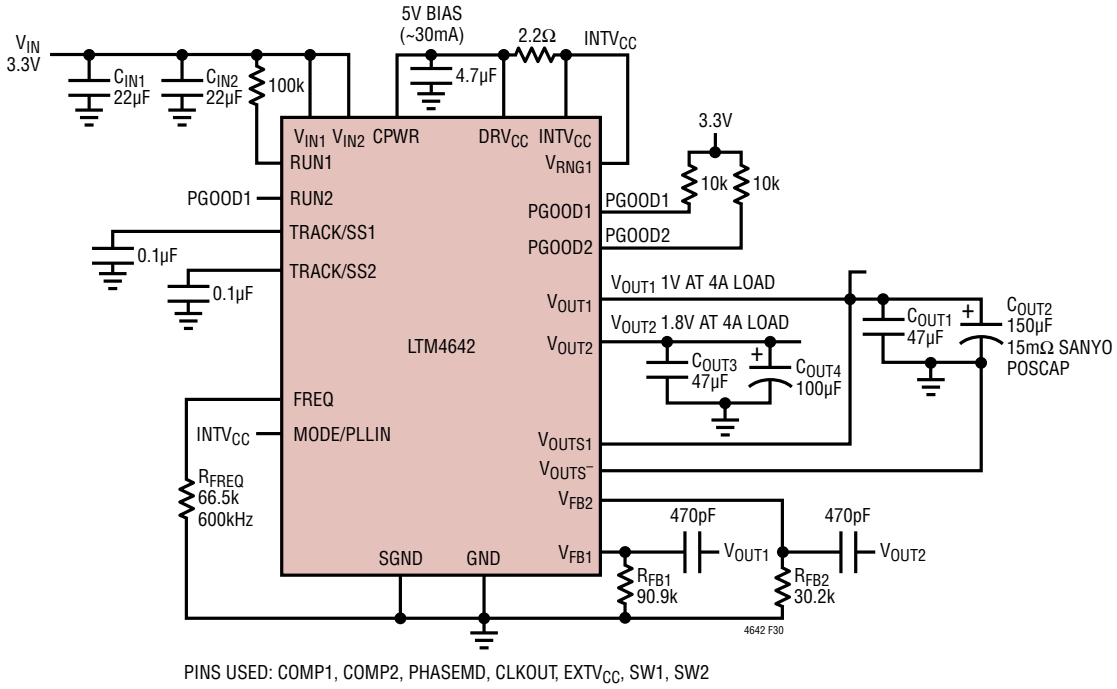
TYPICAL APPLICATIONS



PINS NOT USED: PHASEMD, CLKOUT, $EXTV_{CC}$, SW1, SW2

Figure 29. Output Paralleled LTM4642 Module for 3.3V at 8A Each

TYPICAL APPLICATIONS



PINS USED: COMP1, COMP2, PHASEMD, CLKOUT, $EXTV_{CC}$, SW1, SW2

Figure 30. 3.3V Input to 1V and 1.8V at 4A Each, 1V Sequencing 1.8V Using PGOOD1 to Enable RUN2

PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Table 5. Pin Assignment

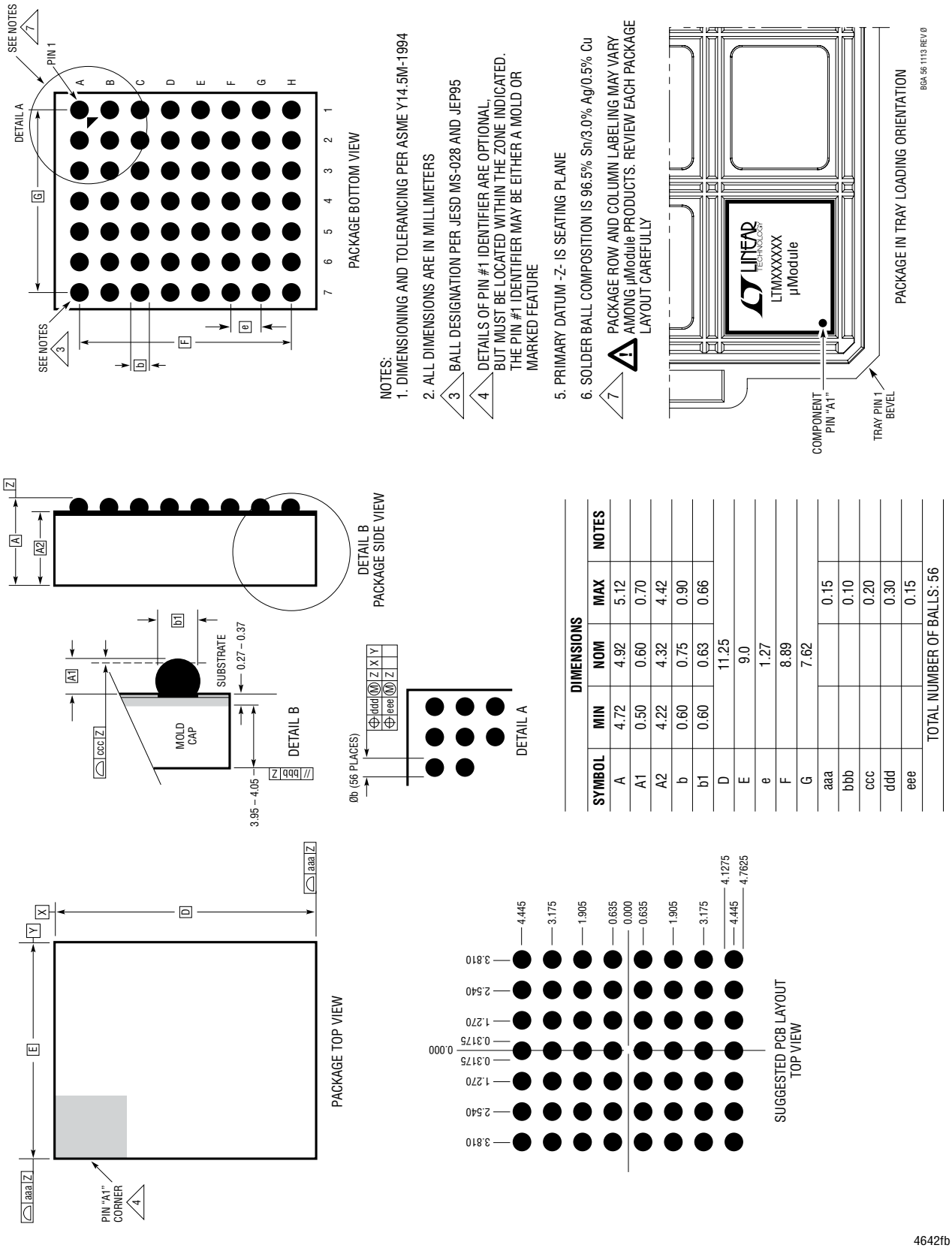
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT2}	B1	V_{OUT2}	C1	V_{OUT2}	D1	GND	E1	GND	F1	V_{OUT1}
A2	V_{OUT2}	B2	V_{OUT2}	C2	GND	D2	SGND	E2	SGND	F2	V_{OUTS1}
A3	SW2	B3	RUN2	C3	MODE/PLLIN	D3	COMP2	E3	COMP1	F3	V_{OUTS}^-
A4	GND	B4	PHASMD	C4	V_{FB2}	D4	CLKOUT	E4	FREQ	F4	V_{FB1}
A5	GND	B5	V_{IN2}	C5	TRACK/SS2	D5	GND	E5	GND	F5	TRACK/SS1
A6	GND	B6	V_{IN2}	C6	PGOOD2	D6	$EXTV_{CC}$	E6	DVR_{CC}	F6	PGOOD1
A7	GND	B7	V_{IN2}	C7	CPWR	D7	$INTV_{CC}$	E7	GND	F7	GND

PIN ID	FUNCTION	PIN ID	FUNCTION
G1	V_{OUT1}	H1	V_{OUT1}
G2	V_{OUT1}	H2	V_{OUT1}
G3	RUN1	H3	SW1
G4	V_{RNG1}	H4	GND
G5	V_{IN1}	H5	GND
G6	V_{IN1}	H6	GND
G7	V_{IN1}	H7	GND

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM4642#packaging for the most recent package drawings.

BGA Package
56-Lead (11.25mm × 9.00mm × 4.92mm)
(Reference LTC DWG# 05-08-1961 Rev Ø)

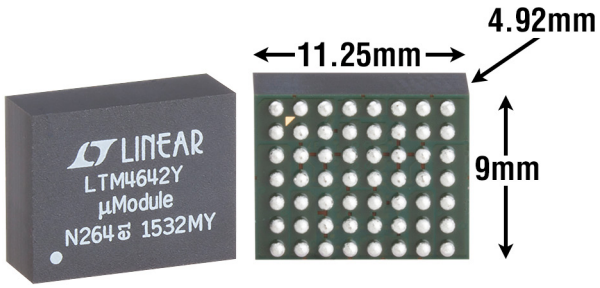


DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		11.25		
E		9.0		
e		1.27		
F		8.89		
G		7.62		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 56				

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/16	Absolute Maximum Rating VFB1, V_{FB2} changed to $INTV_{CC}$ to 0.3V	2
B	6/17	Twelve phases can be paralleled with no more than two phases per regulator output	13

PACKAGE PHOTOGRAPH



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Search	
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of µModule products.	
Digital Power System Management	Linear Technology's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4614	Dual, 4A, Low V_{IN}, DC/DC µModule Regulator	2.375V ≤ V_{IN} ≤ 5.5V, 0.8V ≤ V_{OUT} ≤ 5V, 15mm × 15mm × 2.82mm LGA
LTM4615	Triple, Low V_{IN}, DC/DC µModule Regulator	Two 4A Outputs and One 1.5A, 15mm × 15mm × 2.82mm LGA, 2.375V ≤ V_{IN} ≤ 5.5V
LTM4616	Dual, 8A, Low V_{IN}, DC/DC µModule Regulator	2.7V ≤ V_{IN} ≤ 5.5V, 0.6V ≤ V_{OUT} ≤ 5V, 15mm × 15mm × 2.82mm LGA
LTM4628	Dual, 8A, 26V, DC/DC µModule Regulator	4.5V ≤ V_{IN} ≤ 28.5V, 0.6V ≤ V_{OUT} ≤ 5.5V, Remote Sense Amplifier, Internal Temperature Sensing Diode Output, 15mm × 15mm × 4.32mm LGA
LTM4620A	Dual, 16V, 13A, 26A, Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 5.3V, 15mm × 15mm × 4.41mm LGA

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