Large Current External FET Controller Type Switching Regulators

Step-down,High-efficiency Switching Regulators (Controller type)

BD9040FV,BD9045FV

No.10028EBT03

●Over View

BD9040FV(output type of 1ch) and BD9045FV(output type of 2ch) are switching controllers that can be used within the wide range of the input.Highly effective can be achieved by the synchronous rectification method and it is possible to contribute to the eco-design of all electronic equipment (energy-saving).

●Feature(BD9040FV, BD 9045FV)

1) Wide input voltage range : 4.5V～18V
2) Reference voltage 0.9V±1%
3) The overcurrent of timer latch type, excess voltage, short, and RTO/S protection are built-in
4) The switching frequency is changeable.(200kHz～750kHz)
5) A ceramic capacitor can be used for the output.

●Applications

For thin television, DVD･HDD recorder , STB, amusement and others.

●Absolute maximum rating (Ta=25℃)

Parameter	Symbol	Rating	Unit
Power-supply voltage	Vcc	20	V
EN input voltage	V_{EN}	20	V
SW voltage	V_{SW}	Vcc	V
Voltage between BOOT-SW	V_{BOOT}	6	V
Permissible loss 1	Pd1	0.81** (BD9040FV)	W
Permissible loss 2	Pd2	0.94*** (BD9045FV)	W
Range of operating temperature	Topr	-40～+85	℃
Storage temperature range	Tstg	-55～+150	℃
Junction temperature	Tjmax	150	℃

** Ta=25℃ or more is reduced with 6.5mW/℃.
*** Ta=25℃ or more is reduced with 7.5mW/℃.

●Operation condition (Ta=-40℃～+85℃)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Power supply voltage***	Vcc	4.5	12	18	V
Timing resistance	RT	39	—	130	kΩ
Frequency of oscillator	Fosc	200	—	750	kHz

*** Short EN,EN1,EN2 and VREG5 to VCC when the Vcc is less than 5.5V.
○ The radiation design is not done.

●**Electric characteristics** (Unless otherwise specified Ta=25℃ V_{CC}=12V EN=5V) (BD9040FV)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
VCC Current of bias	ICC	-	3	6	mA	
Standby current	ISTB	-	430	860	μA	V_{EN}=0V
[VREG5]						
Standard voltage output voltage	VREG5	5	5.5	6	V	
Load stability level	VREG5_L	-	20	50	mV	IV_{REG5}=0 to 6mA
[VREG3 part]						
Standard voltage	VREG3	2.85	3.0	3.15	V	
Load stability level	VREG3_L	-	10	20	mV	IV_{REG3}=0 to 1mA
[prevention part for mis-operation of low input]						
VREG5 Threshold voltage	VREG5_UVLO	3.4	3.8	4.2	V	V_{REG5}:Sweep down
VREG3 Threshold voltage	VREG3_UVLO	2.4	2.5	2.6	V	V_{REG3}:Sweep down
[Oscillator]						
Oscillation frequency	FOSC	240	300	360	kHz	RT=91 kΩ
[Error amplifier]						
VO input bias current	Ivo+	-	-	1	μA	
Source current	Isource	-12	-6.5	-2	mA	V_{FB}=1.1V
Sink current	Isink	0.75	1.5	5	mA	V_{FB}=0.7V
Return standard voltage	VOB	0.891	0.900	0.909	V	FB-COMP Short
Output short detection voltage	Vosh	0.37	0.45	0.53	V	V_{FB}:Sweep down
Hysteresis voltage	ΔVosh	22	45	90	mV	V_{FB}:Sweep up
[Soft start part]						
Charge current	ISS	-14	-10	-6	μA	Vss=1V
Discharge current 1	IDIS	0.6	1.7	5	mA	Vss=1V
Discharge current 2	IDIS2	2.35	3.3	4.62		Vss=1V, VEN_SS=0V
Maximum voltage	Vss_MAX	1.75	1.95	2.15	V	
Standby current	Vss_STB	-	-	0.3	V	
[overcurrent protection Division]						
CL inflow current	Iswin	9	10	11	μA	V_{CL}=Vcc-0.2V
[Overvoltage protection Division]						
Detection voltage	Vovp	1.06	1.1	1.14	V	
[Timer latch circuit Division]						
Source current	ITM	-14	-10	-6	μA	V_{TM}=1V
Threshold voltage	Vth_TM	0.9	1	1.1	V	
OFF Sink current	IOFFS	0.6	1.7	5	mA	V_{TM}=0.5V
[Each ch control part]						
EN pull-up resistor	R_{EN}	150	300	450	kΩ	
EN_SS pull-up resistor	R_{EN_SS}	150	300	450	kΩ	

●**Reference data** (Unless otherwise specified Ta=25℃)

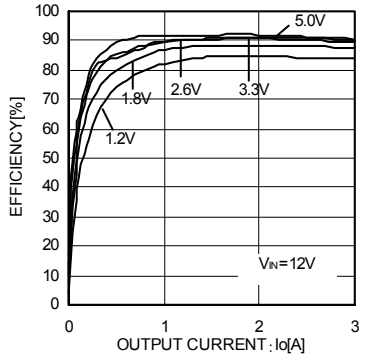


Fig.1 Efficiency 1

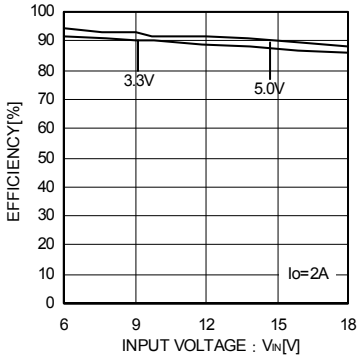


Fig.2 Efficiency 2

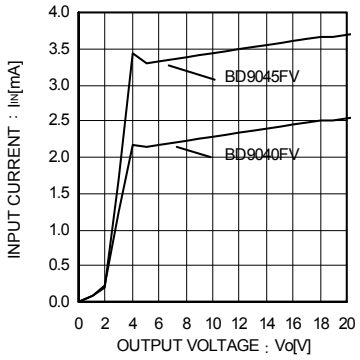


Fig.3 Circuit current

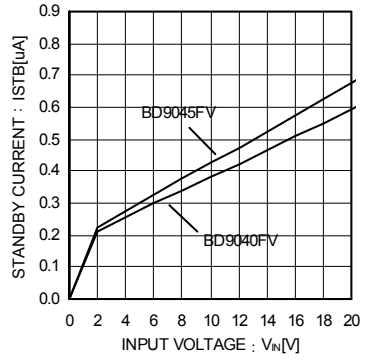


Fig.4 Standby current

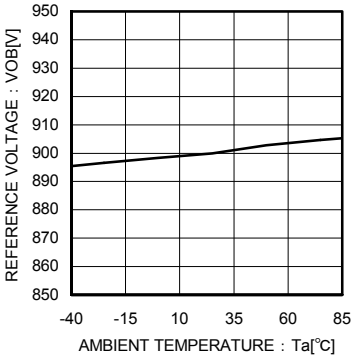


Fig.5 Reference voltage temperature characteristic

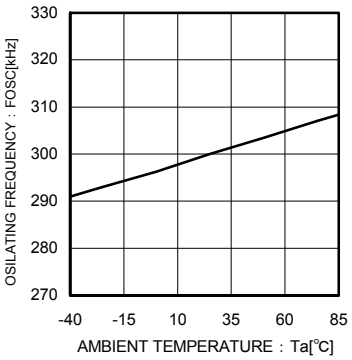


Fig.6 Frequency temperature characteristic

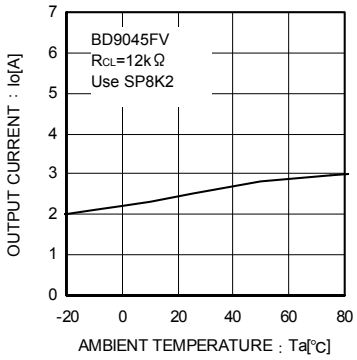


Fig.7 Overcurrent protection temperature characteristic

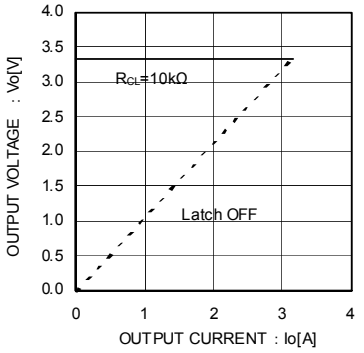


Fig.8 Load regulation

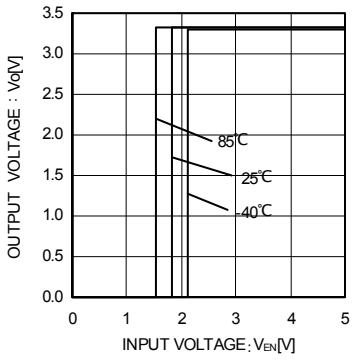


Fig9. EN Threshold voltage

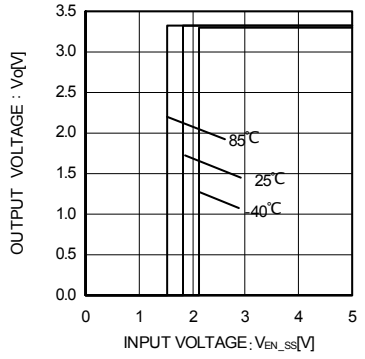


Fig.10 EN_SS Threshold voltage

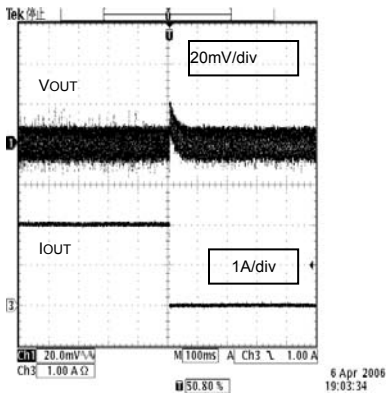


Fig.11 Load response 1

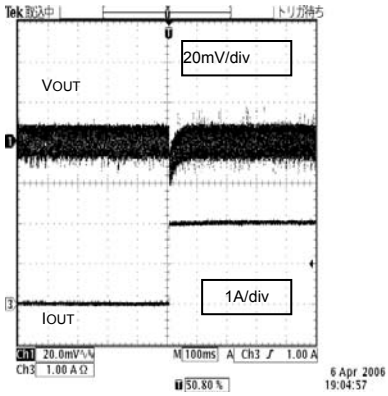
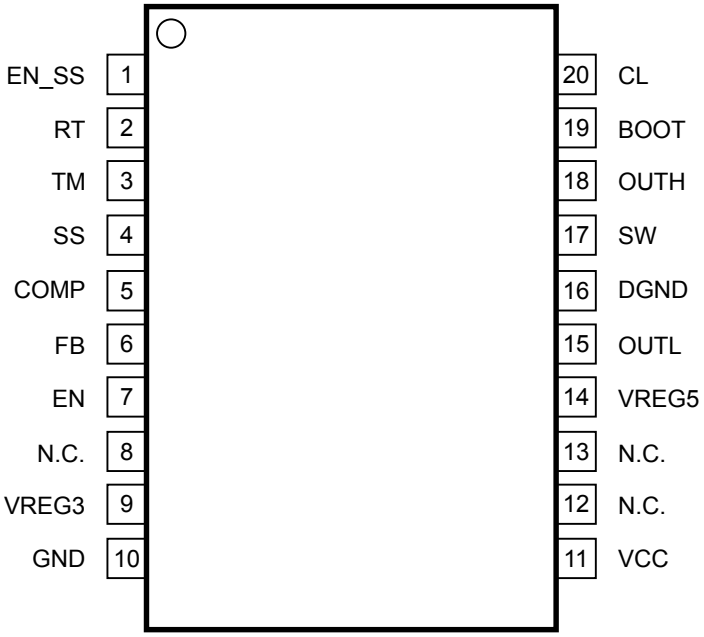


Fig.12 Load response 2

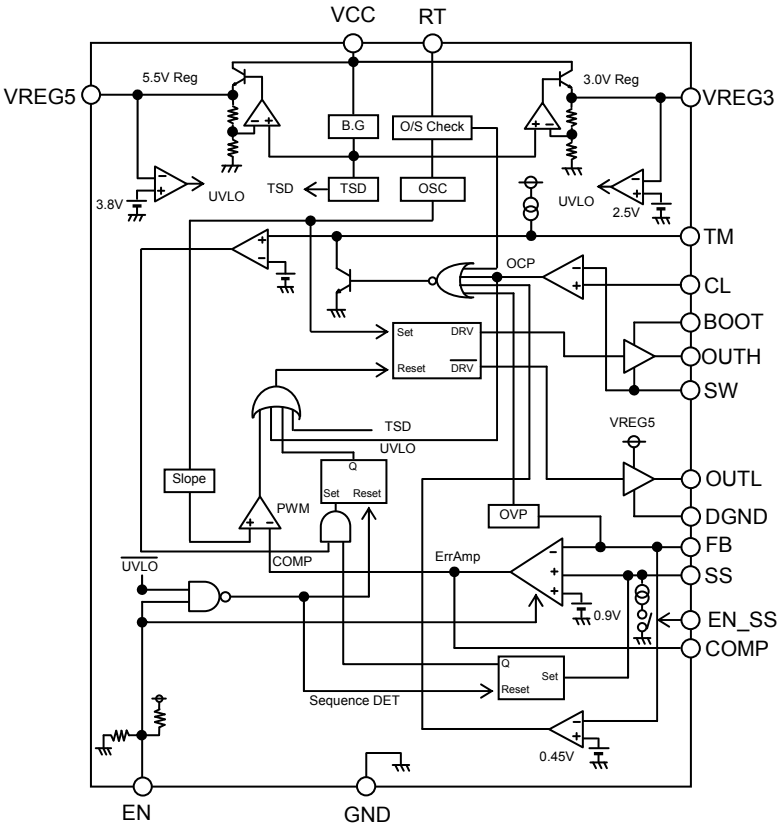
●**Pin configuration** (BD9040FV)



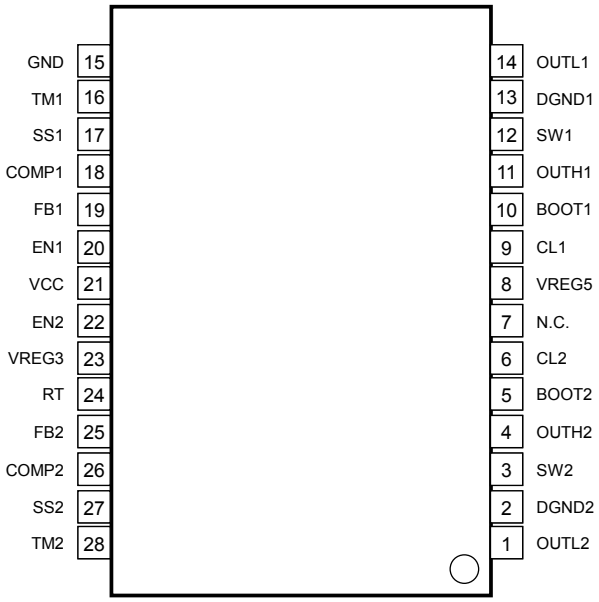
●**Pin function table** (BD9040FV)

Terminal number	terminal name	Function
1	EN_SS	SS discharge Delay ON/OFF terminal
2	RT	Oscillation frequency setting terminal
3	TM	Output OCP and OVP timer latch setting terminal
4	SS	Soft start time setting terminal
5	COMP	Error amplifier output
6	FB	Error amplifier input
7	EN	Output ON/OFF terminal
8	N.C	Unconnected terminal
9	VREG3	REG output for standard power supply
10	GND	GND
11	VCC	Input power supply terminal
12	N.C	Unconnected terminal
13	N.C	Unconnected terminal
14	VREG5	REG output for FET drive
15	OUTL	drive terminal at low side of FET gate
16	DGND	Source terminal at low side of FET
17	SW	High side FET source terminal
18	OUTH	Terminal of drive at high side in FET gate
19	BOOT	OUTH driver power supply terminal
20	CL	Overcurrent detection setting terminal

●**Block diagram** (BD9040FV)



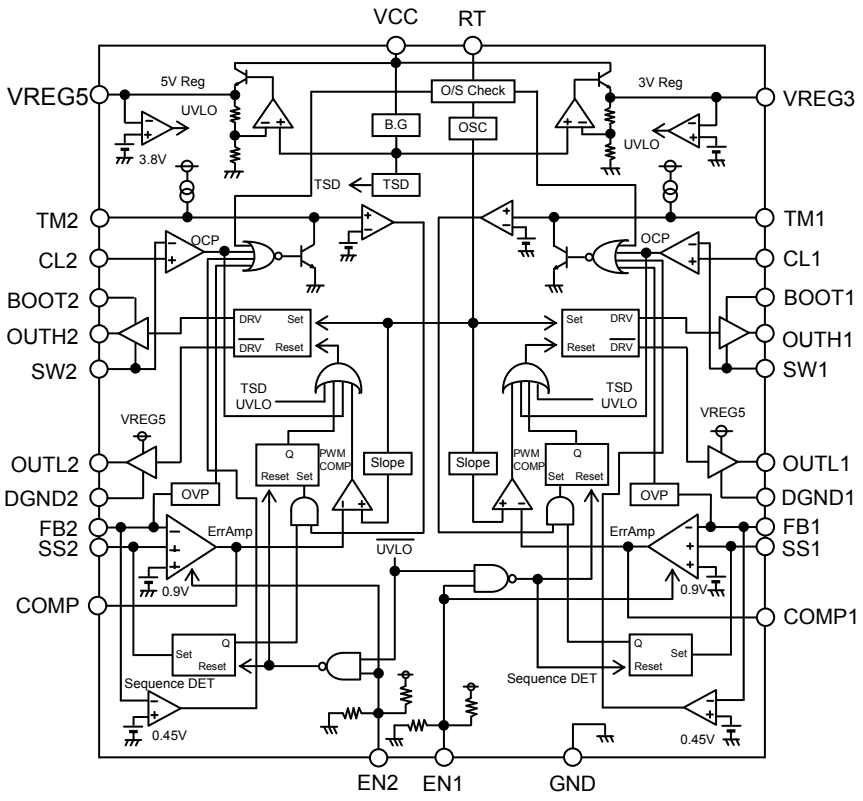
●**Pin configuration** (BD9045FV)



●**Pin function table** (BD9045FV)

Terminal number	terminal name	Functions
1	OUTL2	Terminal 2 of drive at low side FET gate
2	DGND2	Low side FET source terminal2
3	SW2	High side FET source terminal2
4	OUTH2	Terminal 2of drive at high side of FET gate
5	BOOT2	OUTH2 driver power supply terminal
6	CL2	Overcurrent detection setting terminal 2
7	N.C.	Unconnected terminal
8	VREG5	REG output for FET drive
9	CL1	Overcurrent detection setting terminal 1
10	BOOT1	OUTH1 driver power supply terminal
11	OUTH1	Terminal 1of drive at high side of FET gate
12	SW1	High side FET source terminal 1
13	DGND1	Low side FET source terminal 1
14	OUTL1	Terminal 1of drive at low side of FET gate
15	GND	GND terminal
16	TM1	Output 1 OCP and OVP timer latch setting terminal
17	SS1	Soft start time setting terminal 1
18	COMP1	Error amplifier output 1
19	FB1	Error amplifier input1
20	EN1	Outpt1ON/OFF terminal
21	VCC	Input power supply terminal
22	EN2	Output2ON/OFFterminal
23	VREG3	REG output for standard power supply
24	RT	Oscillation frequency setting terminal
25	FB2	Error amplifier input 2
26	COMP2	Error amplifier output 2
27	SS2	Soft start time setting terminal 2
28	TM2	Output 2 OCP and OVP timer latch setting terminal

●**Block diagram** (BD9045FV)

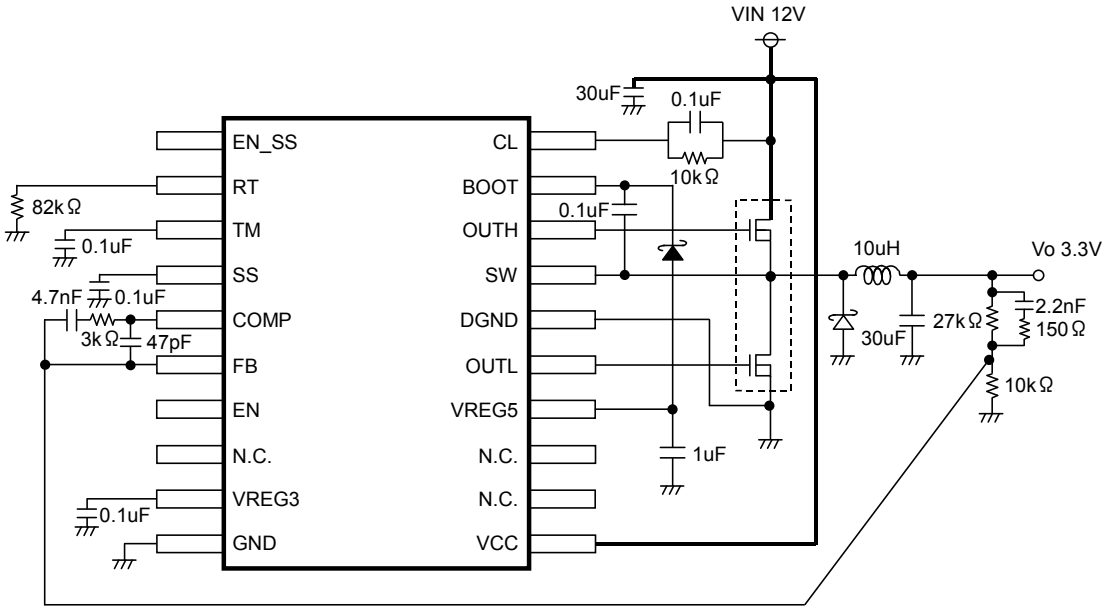


●Block functional descriptions

- Error amplifier(ErrAmp)
  It is a circuit to compare the 0.9V reference voltage and the output voltage's feedback voltage. Switching Duty is determined by the COMP voltage that is the result of the comparison. In addition, due to the SS terminal voltage on start-up, the Soft Start begins operating, and so the COMP voltage is limited by the SS voltage.
- Oscillator(OSC)
  It is a block, the oscillating frequency of which is decided by RT and can be set up to 200kHz～750kHz.
- SLOPE
  It is a block in which triangular wave is created from the clock generated by the OSC. And the generated triangular wave is transmitted to the PWM comparator.
- PWM Comparator(PWM COMP)
  The error amplifier's output COMP voltage and the SLOPE block's triangular wave are compared, and the switching Duty is determined. The switching duty is limited by the maximum Duty ratio internally decided and can not become 100%.
- Reference voltage(5V Reg, 3V Reg)
  It is a block to generate 5.5V and 3V internal reference voltage.
- Overcurrent protection circuit(OCP)
  At the time of OUTH=H, if SW voltage becomes not more than CL voltage, the overcurrent protection circuit operates. When the overcurrent protection operates, the Duty is limited, and so the output voltage is lowered. Moreover, when an overcurrent is detected by the overcurrent protection circuit, the charging of the external capacitor on TM terminal is started. When the voltage on TM terminal exceeds 1V, the output becomes OFF state and then is latched. Once EN is made to be L, the latch is released.
- Overvoltage protection circuit(OVP)
  When FB voltage becomes more than 1.1 V, the overvoltage protection operates. When the overvoltage protection operates, the charging of the external capacitor on TM terminal is started. When the voltage on TM terminal exceeds 1V, the output becomes OFF state and then is latched. Once EN is made to be L, the latch is released.
- Output short circuit protection circuit
  If FB voltage becomes not more than 0.4V, the output short circuit protection circuit operates. When the output short circuit protection operates, the charging of the external capacitor on TM terminal is started. When the voltage on TM terminal exceeds 1V, the output becomes OFF state and then is latched. Once EN is made to be L, the latch is released.
- O/S Check
  When RT terminals become open or short circuit states, RT OPEN and SHORT circuit protections operate respectively.
  When RT terminals' open or short circuit state is detected, the charging of the external capacitor on TM terminal is started. When the voltage on TM terminal exceeds 1V, the output becomes OFF state and then is latched. Once EN is made to be L, the latch is released.
- Under Voltage Lockout (UVLO) / Thermal Shutdown(TSD)
  When VREG5 becomes no more than around 3.8V or VREG3 no more than around 2.5, the output of the under voltage lockout is turned off.
  Then, When VREG5 becomes more than around 4.2V or VREG3 more than around 2.6, the output of the under voltage lockout is reset.
  Moreover, when the temperature of chip becomes more than around 150℃, the output of the thermal shutdown (TSD) is turned off, and when it is returned to a certain temperature, the output is reset.
  When UVLO and TSD operate, the capacitors of TM and SS are discharged.
- Function of EN
  EN is pulled down in regard to GND and pulled up in regard to VCC, and normally EN=H.
  At the time of EN=L, the capacitors of OFF, TM and SS of output are discharged, and become the standby state.
  (As for BD9045, due to EN1 and EN2, the capacitors of OFF, TM and SS of each ch output are discharged. In addition it becomes the standby state when both EN1 and EN2 are made to be L).
- Function of EN_SS(BD9040 alone)
  EN_SS is pulled down in regard to GND and pulled up in regard to VCC, and normally EN_SS=H. At the time of EN_SS=L, the capacitors of OFF, TM and SS of output are discharged.At the time of EN_SS=L, the capacitor of SS is constant-current discharged, so it can be made delayed during output's OFF.

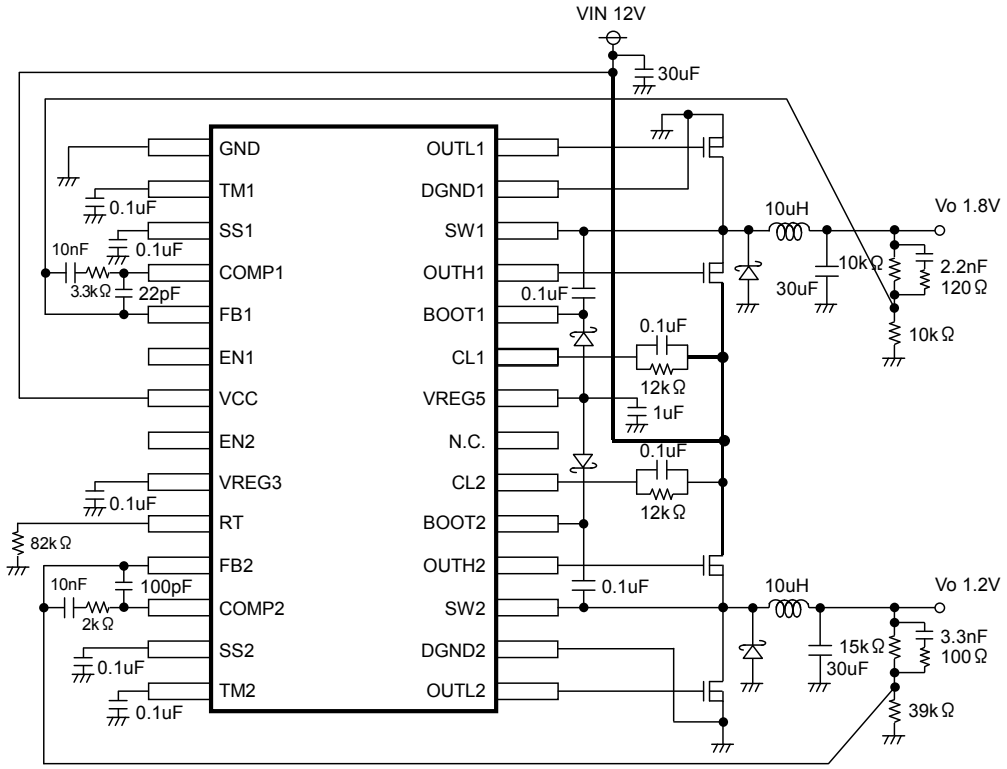
●Application circuit example

BD9040FV



※ There are many factors (The PCB board layout, output current, etc.) that can affect the DCDC characteristics, please Verify and confirm using practical applications.

BD9045FV



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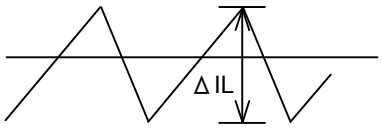
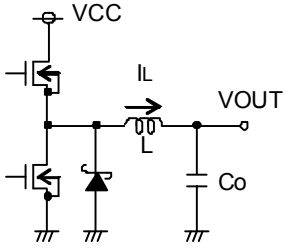
●Application components selection

(1) Setting of output L constant value





Output ripple current

The coil value significantly influences the output ripple current. Thus, as seen in equation (1), the bigger the coil, and the higher the switching frequency, the lower the drop in ripple current.

$$\Delta IL = \frac{(VCC-VOUT)\times VOUT}{L\times VCC\times f} \quad [A]\cdot\cdot\cdot(1)$$

The optimal output ripple current setting is 30% of maximum current.

$$\Delta IL = 0.3\times IOUTmax.[A]\cdot\cdot\cdot(2)$$

$$L = \frac{(VCC-VOUT)\times VOUT}{\Delta IL\times VCC\times f} \quad [H]\cdot\cdot\cdot(3)$$

(ΔIL : output ripple current, f : switching frequency)

※ Outputting a current in excess of the coil current rating will cause magnetic saturation of the coil and decrease efficiency. Please establish sufficient margin to ensure that peak current does not exceed the coil current rating.

※ Use low resistance (DCR, ACR) coils to minimize coil loss and increase efficiency.

(2) Setting of output constant Co

Select the output capacitor with the highest value for ripple voltage (V_{PP}) tolerance and maximum drop voltage (at rapid load change). The following equation is used to determine the output ripple voltage.

Step down $$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{Co} \times \frac{Vo}{Vcc} \times \frac{1}{f} \quad [V]\cdot\cdot(4)$$ provided that f : switching frequency

Be sure to keep the output Co setting within the allowable ripple voltage range.
※Please allow sufficient output voltage margin in establishing the capacitor rating.
Note that low-ESR capacitors enable lower output ripple voltage.

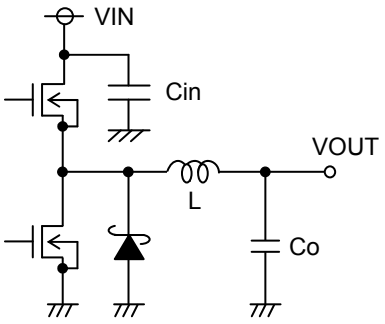
Also, to meet the requirement for setting the output startup time parameter within the soft start time range, please factor in the conditions described in the capacitance equation (5) for output capacitors, below.

$$Co \leqq \frac{Tss \times (ILimit - I_{OUT})}{V_{OUT}} \quad \cdot\cdot\cdot \quad (5)$$

Tss : soft start time
I_{OUT} : load current
V_{OUT} : output voltage
ILimit : over current detection value reference

Note: less than optimal capacitance values may cause problems at startup.

(3) Input capacitor(Cin)selection



Input capacitor

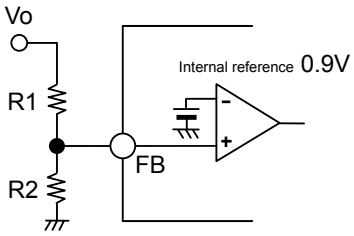
The input capacitor serves to lower the output impedance of the power source connected to the input pin (VCC). Increased power supply output impedance can cause input voltage (VCC) instability, and may negatively impact oscillation and ripple rejection characteristics. Therefore, be certain to establish an input capacitor in close proximity to the VCC and GND pins. Select a low-ESR capacitor with the required ripple current capacity and the capability to withstand temperature changes without wide tolerance fluctuations. The ripple current IRMS is determined using equation (6).

$$IRMS = IOUT \times \frac{\sqrt{VOUT\ (VCC - VOUT)}}{VCC} \quad [A]\cdot\cdot\cdot(6)$$

Also, be certain to ascertain the operating temperature, load range and MOSFET conditions for the application in which the capacitor will be used, since capacitor performance is heavily dependent on the application's input power characteristics, substrate wiring and MOSFET gate drain capacity.

(4) Feedback resistor design

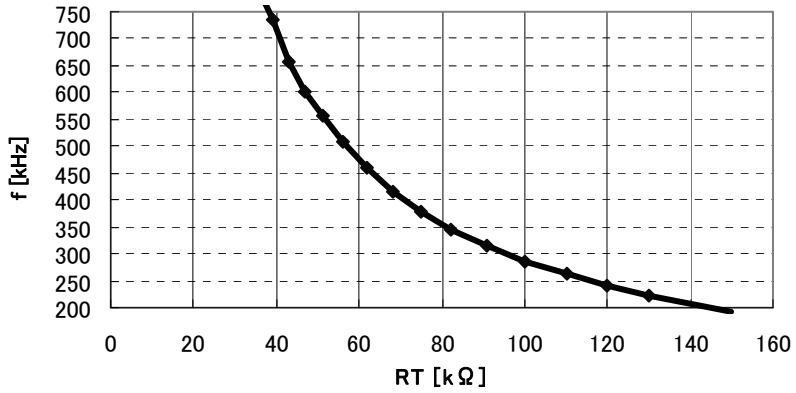
Please refer to the following equation in determining the proper feedback resistance.
The recommended setting is in a range between 1kΩ and 330kΩ. Resistance less than 1kΩ risks decreased power efficiency, while setting the resistance value higher than 330kΩ will result in an internal error amp input bias current of 0.4uA increasing the offset voltage.



$$Vo = \frac{R1 + R2}{R2} \times 0.9\,[V] \quad \cdots (7)$$

(5) Setting switching frequency

The triangular wave switching frequency can be set by connecting a resistor to the RT pin. The RT sets the frequency by adjusting the charge/discharge current in relation to the internal capacitor. Refer to the figure below in determining proper RT resistance. Settings outside this range may render the switching function inoperable, and proper operation of the controller overall cannot be guaranteed when unsupported resistance values are used.



(6) Setting the soft start delay

The soft start function is necessary to prevent an inrush of coil current and output voltage overshoot at startup.
The figure below shows the relation between soft start delay time and capacitance, which can be calculated using equation (8) at right.

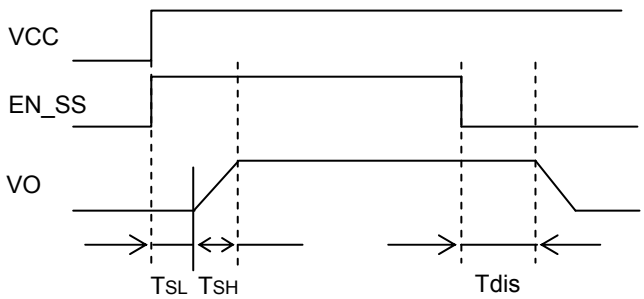
$$T_{SL} = 0.8 \times \frac{Css}{Iss\ (10\mu A\ typ)}\ [sec] \qquad T_{SH} = 0.7 \times \frac{Vo}{Vcc} \times \frac{Css}{Iss\ (10\mu A\ typ)}\ [sec] \quad \cdots (8)$$

If the capacitance value is reduced (to no more than 0.01 uF or so), the overshoot in output may be caused.
Please use high accuracy components (such as X5R) when implementing sequential startups involving other power sources. Be sure to test the actual devices and applications to be used, since the soft start time varies, depending on input voltage, output voltage, load, coil, output capacitance and phase compensation constant etc.

(7) Setting the EN_SS (output delay function)(in the case of BD9040FV)

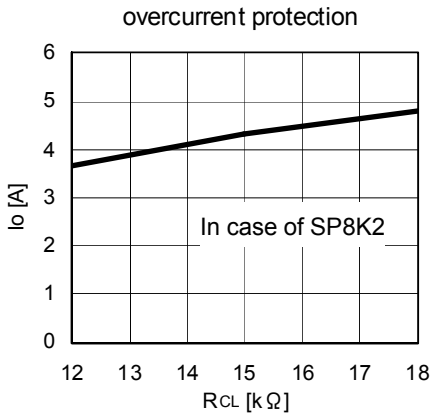
If EN_SS is made to be L, the output voltage's OFF time can be made delayed. The calculating formula for delay time is shown in the following equation.

$$TDIS = \left(Vss\_MAX(1.95VTyp) - \left(0.8 + 0.7 \times \frac{Vo}{Vcc}\right) \right) \times \frac{Css}{Idis(3.3uA,Typ)}\ [sec] \quad \cdots (9)$$

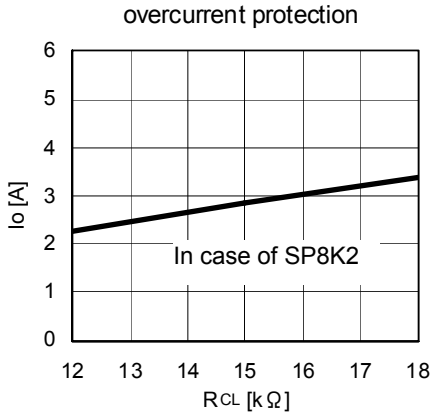


(8) Overcurrent protection

Current limit value (ILimit) is determined by the resistance RCL established between VCC and CL. (refer to the following diagram)The current limit is self-feedback type, when overcurrent is detected, the output Duty is reduced, and the current is limited. When load returns to normal state, the output voltage returns to its former state.



BD9040FV measurement value of our company's substrate



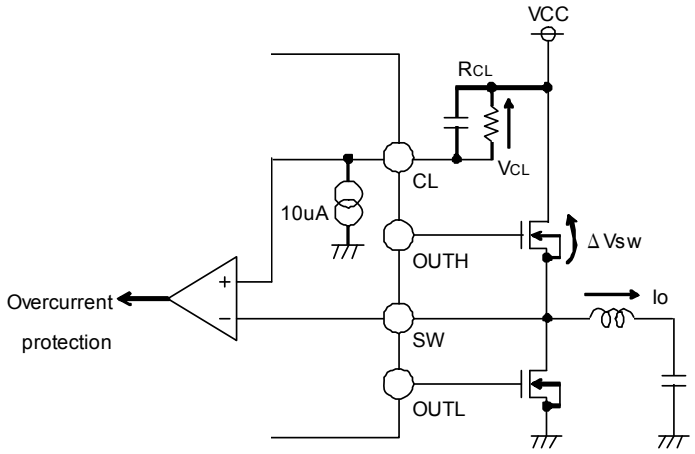
BD9045FV measurement value of our company's substrate

※There are many factors (the layout and service condition) that can affect the characteristics, please verify and confirm using practical applications.Overcurrent protection detection value is dependent on the ON resistance of external FET and so varies with temperature. (Refer to Fig.7 on page 3)

Please determine it in such a way that a good margin is left while setting it. Moreover, in case of different layout of substrate or large gate capacitance of external FET, sufficient voltage between gate and source of external FET can not be provided, the ON resistance becomes high, and so the overcurrent protection value may be greatly changed.

Please use a FET, the gate capacitance of which is no more than1500pF, as external FET. (the recommended: SP8K2, SP8K1)However, There are many factors (the layout and service condition) that can affect the characteristics, please verify and confirm using practical applications.

Compare the VCL that is set by RCL and the ΔVsw that is generated by ON resistance of loxFET.



(9) Setting of OFF latch timer time

・OFF latch timer is charged if one of the following conditions is met.

- ・Current limit is operating.
- ・Overvoltage protection(FB≧1.1V)is operating.
- ・Output short circuit protection(FB≦0.45V)is operating.
- ・Resistor connected on RT terminal becomes open.
- ・RT terminal is shorted with GND.
- ・Resistor connected on CL terminal becomes open.

If the charging is started and continued until the fully-charged, the output is OFF latched. The time from start-up of charging till output OFF is determined by the following formula.

$$T_{TM} = \frac{C_{TM}}{I_{TM}(10uA\,typ)} \quad [sec] \quad \cdot\cdot\cdot (10)$$

This OFF latch is released once EN is made to be「L」or if VCC is once lowered and then rises again.

(10) Method for determining phase compensation

Conditions for application stability

Feedback stability conditions are as follows:

・When gain is 1 (0dB) and phase shift is 150° or less (i.e., phase margin is at least 30°):
a dual-output high-frequency step-down switching regulator is required

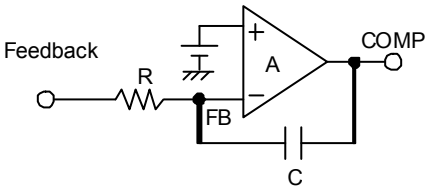
Additionally, in DC/DC applications, sampling is based on the switching frequency; therefore, overall GBW may be set at no more than 1/10 the switching frequency. In summary, target characteristics for application stability are:

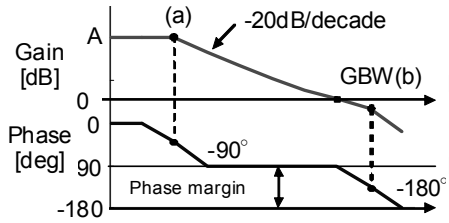
・Phase shift of 150° or less (i.e., phase margin of 30° or more) with gain of 1 (0dB)

・GBW (i.e., gain 0dB frequency) no more than 1/10 the switching frequency.

Stability conditions mandate a relatively higher switching frequency, in order to limit GBW enough to increase response. The key to achieving successful stabilization using phase compensation is to cancel the secondary phase margin/delay (-180°) generated by LC resonance, by employing a dual phase lead. In short, adding two phase leads stabilizes the application.GBW (the frequency at gain 1) is determined by the phase compensation capacitor connected to the error amp. Thus, a larger capacitor will serve to lower GBW if desired.

① General use integrator (low-pass filter) ② Integrator open loop characteristics





Point(a) $fa = \frac{1}{2\pi RCA} 1.25[Hz]$ ・・・(11)

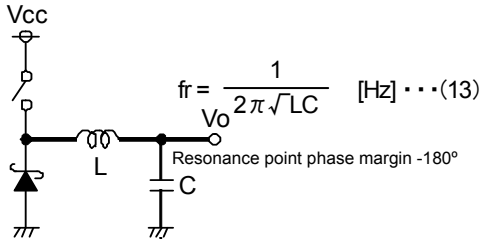
Point(b) $fa = GBW \frac{1}{2\pi RC}$ [Hz] ・・・(12)

The error amp is provided with phase compensation similar to that depicted in figures ① and ② above and thus serves as the system's low-pass filter.In DC/DC converter applications, R is established parallel to the feedback resistance.

When electrolytic or other high-ESR output capacitors are used

Phase compensation is relatively simple for applications employing high-ESR output capacitors (on the order of several Ω). In DC/DC converter applications, where LC resonance circuits are always incorporated, the phase margin at these locations is -180°. However, wherever ESR is present, a 90° phase lead is generated, limiting the net phase margin to -90° in the presence of ESR. Since the desired phase margin is in a range less than 150°, this is a highly advantageous approach in terms of the phase margin. However, it also has the drawback of increasing output voltage ripple components.

③ LC resonance circuit



$fr = \frac{1}{2\pi\sqrt{LC}}$ [Hz] ・・・(13)

④ ESR connected

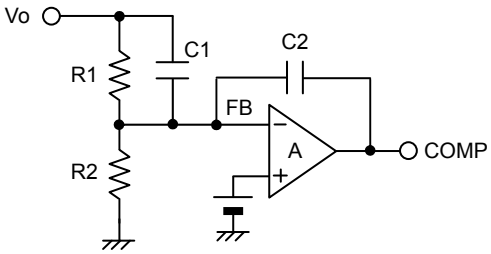
$fr = \frac{1}{2\pi\sqrt{LC}}$ [Hz]: resonance point ・・(14)

$f_{ESR} = \frac{1}{2\pi R_{ESR}C}$ [Hz]: Zero (15)

-90° :Pole

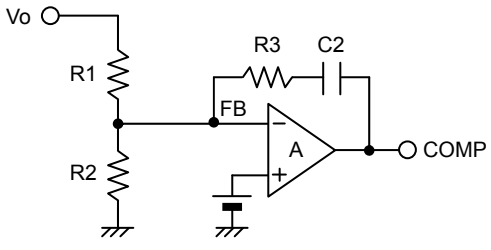
Since ESR changes the phase characteristics, only one phase lead need be provided for high-ESR applications. Please choose one of the following methods to add the phase lead.

⑤ Add C to feedback resistance



Phase lead $fz = \frac{1}{2\pi C1R1}$ [Hz] ・・・(16)

⑥ Add R3 to aggregator

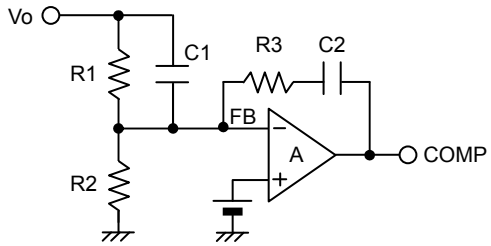


Phase lead $fz = \frac{1}{2\pi C2R3}$ [Hz] ・・・(17)

Set the phase lead frequency close to the LC resonance frequency in order to cancel the LC resonance.

・When using ceramic, OS-CON, or other low-ESR capacitors for the output capacitor:
Where low-ESR (on the order of tens of mΩ) output capacitors are employed, a two phase-lead insertion scheme is required, but this is different from the approach described in figure ③～⑥, since in this case the LC resonance gives rise to a 180° phase margin/delay. Here, a phase compensation method such as that shown in figure ⑦ below can be implemented.

⑦Phase compensation provided by secondary (dual) phase lead



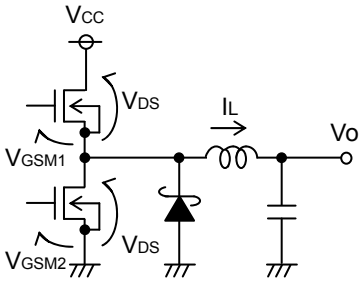
Phase lead $fz1 = \frac{1}{2\pi R1C1}$ [Hz] ・・・(18)

Phase lead $fz2 = \frac{1}{2\pi R3C2}$ [Hz] ・・・(19)

LC resonance frequency $fr = \frac{1}{2\pi\sqrt{LC}}$ [Hz] ・・・(20)

Once the phase-lead frequency is determined, it should be set close to the LC resonance frequency.
This technique simplifies the phase topology of the DCDC Converter. Therefore,it might need a certain amount of trial-and-error process. There are many factors(The PCB board layout, Output Current, etc.)that can affect the DCDC characteristics. Please verify and confirm using practical applications.

(9)MOS FET selection



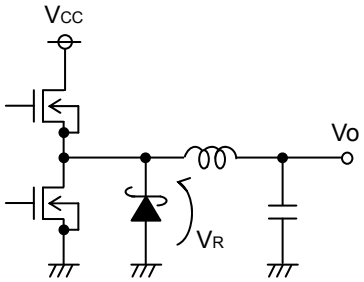
FET uses Nch MOS
- V_{DS}＞Vcc
- V_{GSM1}＞BOOT-SW interval voltage
- V_{GSM2}＞VREG5
- allowable current＞output current + ripple current

※Should be at least the over current protection value

※Select a low ON-resistance MOSFET for highest efficiency

※Attention
If the input capacitance of FET is extremely large or it is used with Duty no more than 10%, it is possible that output FETs on both upper side and under side are simultaneously turned on and so the efficiency deteriorates. The input capacitance of output FET is recommended to be no more than 1000pF. But these characteristics vary with substrates' layouts or varieties of parts etc, so please confirm them thoroughly with actual devices when it is put into mass production.

(10)Schottky barrier diode selection

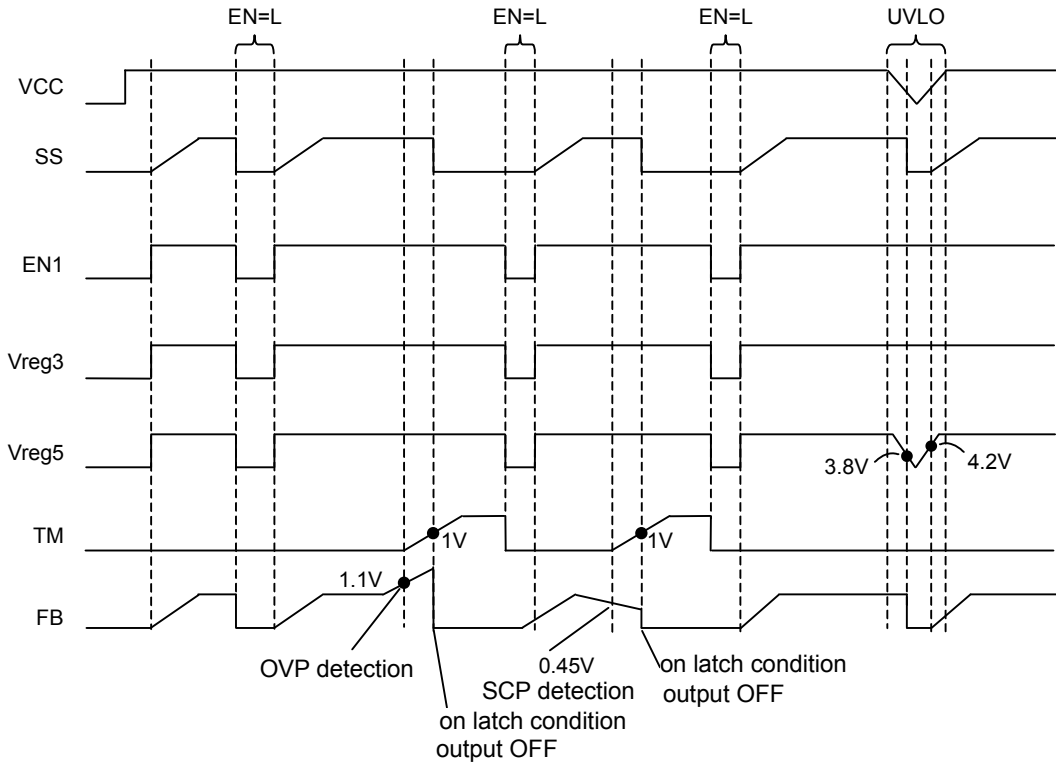


- Reverse voltage V_R＞Vcc
- Allowable current ＞ output current + ripple current

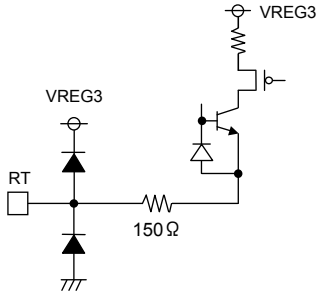
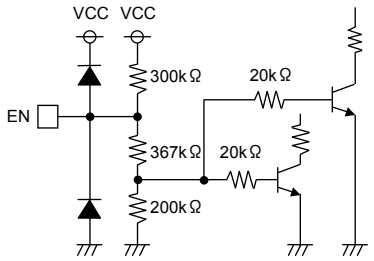
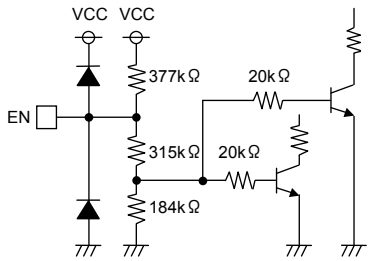
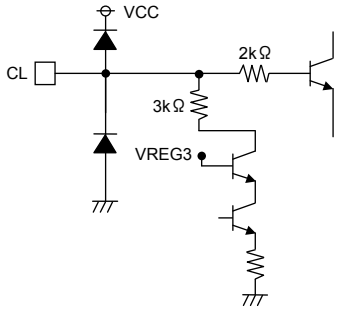
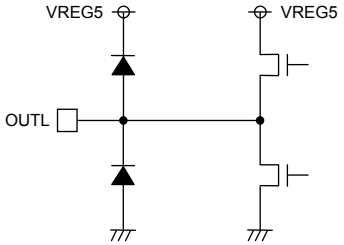
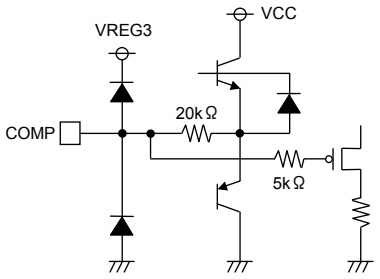
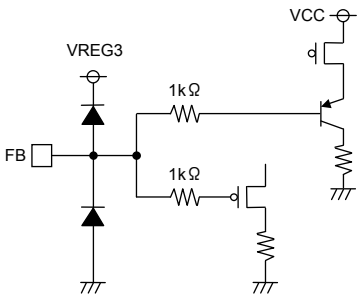
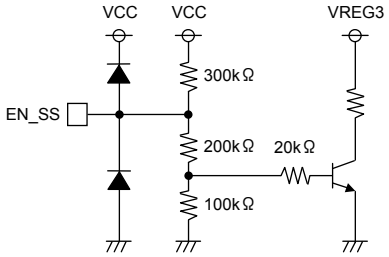
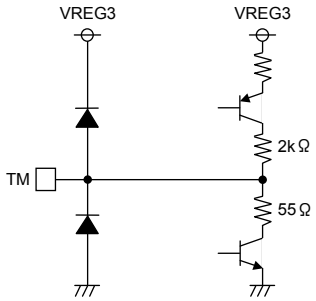
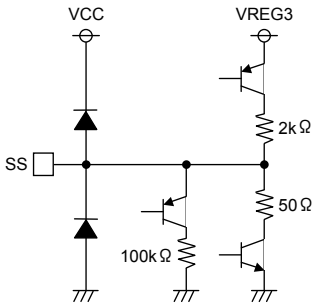
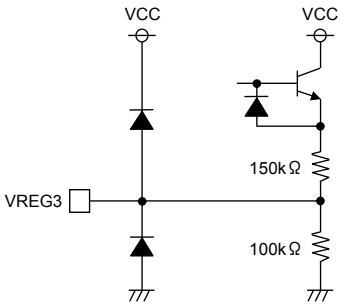
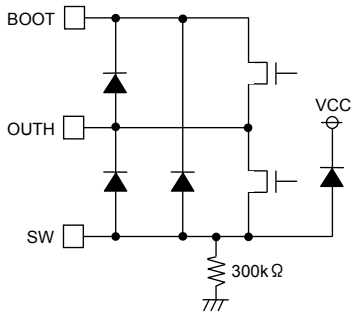
※Should be at least the over current protection value

※Select a low forward voltage, fast recovery diode for highest efficiency

●**Timing chart**



● **Input & output equivalent circuits**

2(24)PIN [RT]	7 PIN [EN]	(20,22)PIN [EN1, EN2]
		
20PIN [CL] (9,6)PIN [CL1, CL2]	15PIN [OUTL] (14, 1)PIN [OUTL1, OUTL2]	5PIN [COMP] (18,26)PIN [COMP1, COMP2]
		
6PIN [FB] (19, 25)IN [FB1, FB2]	1PIN [EN_SS]	3PIN [TM] (6, 28)PIN [TM1, TM2]
		
4PIN [SS] (7, 27)PIN [SS1, SS2]	9PIN [VREG3] (23)PIN [VREG3]	9,17,18PIN [BOOT, SW, OUTH] (10, 5)PIN [BOOT1, BOOT2] (12, 3)PIN [SW1, SW2] (11, 4)PIN [OUTH1, OUTH2]
		

※ The inside of ( ) is of BD9045FV

●Notes for use

1. Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered.
   A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.
2. GND potential
   Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena. if there is a terminal, electric potential of which is lower than that of GND, please take such measures as provide a bypass route etc.
3. Permissible dissipation Pd
   If by any chance you use it in such a way that the permissible dissipation is exceeded, occurs the deterioration of original performances of IC such as reduction of current capacity caused by an increase in temperature of chip, which will lead to a decline in reliability, therefore please use it in such a way that its dissipation is within the permissible one and allows for a sufficient margin.
4. Input power supply
   Please wire and arrange in such a way that, in the wiring pattern and pattern layout, the wiring to the input pin V_{IN} is sufficiently short and furthermore electrical interference is not caused.
   The electrical characteristics included in this specification may vary with such conditions as temperature, power supply voltage and external circuits etc., so please confirm them thoroughly including transient characteristic.
6. Thermal shutdown circuit
   Thermal shutdown circuit is built-in in order to prevent the thermal destruction of IC. Please use it within its permissible dissipation range, but if by any chance the state of exceeding the permissible dissipation continues, the temperature of chip rises, as a result the thermal shutdown circuit operates and so the output is turned off.
   If after that the temperature Tj of chip falls, the circuit resets automatically. Furthermore, the thermal shutdown circuit leads to the state of exceeding the absolute maximum rating, so please absolutely avoid such set design as uses the thermal shutdown circuit.
7. nter-pin shorts and mounting errors
   Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC.
8. Applications with modes that reverse VCC and pin potentials may cause damage to internal IC circuits. For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. Please use 1μF and 0.1μF respectively as the capacitor of VREG5's output terminal and the capacitor of VREG3's output terminal. Moreover, it is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.
9. Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
10. Please insert the protective diode when it is conceivable that the back electromotive force is produced at the time of start-up or output OFF because a load that has a large inductance component is connected on output terminal.
11. Testing on application boards
    When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.
12. GND wiring pattern
    If there are both small-signal GND and large-current GND, then large-current GND pattern and small-signal GND pattern are separated, and in order that the pattern wiring and the voltage change caused by large current do not change the voltage of small-signal GND, it is recommended to carry out the one-point grounding at the reference point of set.
    Please be careful of not changing the GND wiring pattern of external parts.
13. SW terminal
    In case of connecting of application, SW terminal may become a negative electric potential due to the back electromotive force of coil. Please take such measures as provide a bypas route between SW terminal and GND at the time of setting of application.
14. Output
    At the time of EN=L, UVLO, and timer latch, the current flows out from SW terminal. If the service condition is such that the output load becomes no more than 1mA, then please insert a 1kΩ resistor between output and GND.

●Ordering part number

B	D	9	0	4	0	F	V	-	E	2

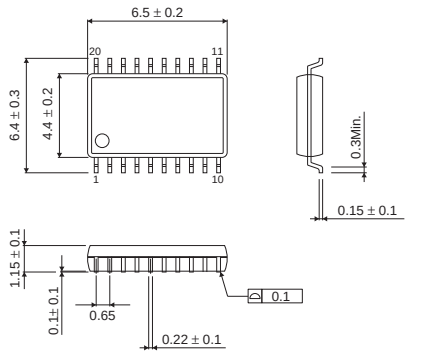
Part No.

Part No.
9040
9045

Package
FV : SSOP-B20
SSOP-B28

Packaging and forming specification
E2: Embossed tape and reel
(SSOP-B20, SSOP-B28)

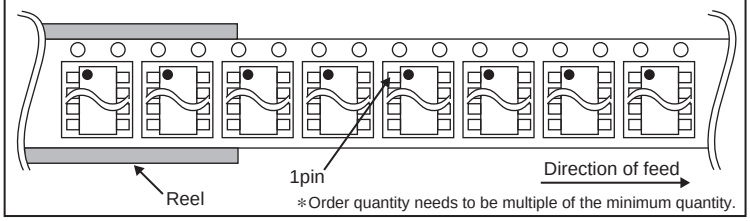
SSOP-B20



(Unit : mm)

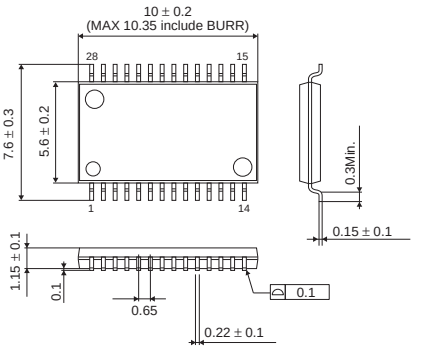
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

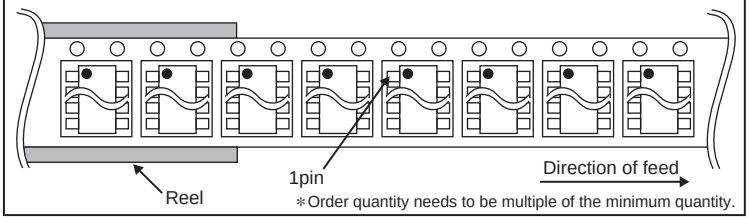
SSOP-B28



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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- Rohm Semiconductor Information

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- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management