THE DATASHEET OF

MAX9240AGTM/V+

MAX9240A

6.25MHz to 100MHz, 25-Bit GMSL Deserializer for Coax or STP Cable with Line Fault Detect

General Description

The MAX9240A compact deserializer is designed to interface with a GMSL serializer over 50Ω coax or 100Ω shielded twisted-pair (STP) cable. The device pairs with the MAX9271 or MAX9273 serializers.

The parallel output is programmable for single or double output. Double output strobes out half of a parallel word on each pixel clock cycle. Double output can be used with GMSL serializers that have the double-input feature.

The device features an embedded control channel that operates at 9.6kbps to 1Mbps. Using the control channel, a microcontroller (µC) can program the serializer/deserializer and peripheral device registers at any time, independent of video timing. Two programmable GPIO ports and a continuously sampled GPI input are available.

For use with longer cables, the device has a programmable equalizer. Programmable spread spectrum is available on the parallel output. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply range is 1.7V to 1.9V and the I/O supply range is 1.7V to 3.6V. The device is available in a 48-pin (7mm x 7mm) TQFN-EP package with 0.5mm lead pitch and operates over the -40°C to +105°C temperature range.

Applications

- Automotive Camera Systems

Ordering Information ***appears at end of data sheet.***

Typical Application Circuit ***appears at end of data sheet.***

Benefits and Features

- Ideal for Camera Applications
  - Works with Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
  - Error Detection/Correction
  - 9.6kbps to 1Mbps Control Channel in I^2C-to-I^2C Mode with Clock Stretch Capability
  - Best-in-Class Supply Current: 90mA (max)
  - Double-Rate Clock for Megapixel Cameras
  - Cable Equalization Allows 15m Cable at Full Speed
  - 48-Pin (7mm x 7mm) TQFN-EP Package with 0.5mm Lead Pitch
- High-Speed Data Deserialization for Megapixel Cameras
  - Up to 1.5Gbps Serial-Bit Rate with Single or Double Output: 6.25MHz to 100MHz Clock
- Multiple Control-Channel Modes for System Flexibility
  - 9.6kbps to 1Mbps Control Channel in UART-to-UART or UART-to-I^2C Modes
- Reduces EMI and Shielding Requirements
  - Programmable Spread Spectrum on the Parallel Output Reduces EMI
  - Tracks Spread Spectrum on Serial Input
- Peripheral Features for Camera Power-Up and Verification
  - Built-In PRBS Checker for BER Testing of the Serial Link
  - Fault Detection of Serial Link Shorted Together, to Ground, to Battery, or Open
  - Two GPIO Ports
  - Dedicated “Up/Down” GPI for Camera Frame Sync Trigger and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
  - -40°C to +105°C Operating Temperature
  - ±10kV Contact and ±15kV Air IEC 61000-4-2 ESD Protection
  - ±10kV Contact and ±30kV Air ISO 10605 ESD Protection

19-7319; Rev 2; 7/21

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Absolute Maximum Ratings*

AVDD to EP.....-0.5V to +1.9V
DVDD to EP.....-0.5V to +1.9V
IOVDD to EP.....-0.5V to +3.9V
IN+, IN- to EP.....-0.5V to +1.9V
LMN_ TO EP (15mA current limit).....-0.5V to +3.9V
All other pins to EP.....-0.5V to (V_{IOVDD} + 0.5V)
IN+, IN- short circuit to ground or supply .....Continuous

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 40mW/°C above +70°C).....3200mW
Junction Temperature.....+150°C
Operating Temperature Range..... -40°C to +105°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

**EP is connected to PCB ground.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....25°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (I2CSEL, LCCEN, GPI, $\overline{PWDN}$, MS/HVEN)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-10		+20	µA
THREE-LEVEL LOGIC INPUTS (CX/TP)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 3)		-10		+10	µA
Input Current	I_{IN}			-150		+150	µA
SINGLE-ENDED OUTPUTS (DOUT_, PCLKOUT)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA	DCS = 0	V_{IOVDD} - 0.3			V
			DCS = 1	V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA	DCS = 0			0.3	V
			DCS = 1			0.2	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Short-Circuit Current	I_{OS}	DOUT_	V_O = 0V, DCS = 0	V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
				V_{IOVDD} = 1.7V to 1.9V	3	7	13	
			V_O = 0V, DCS = 1	V_{IOVDD} = 3.0V to 3.6V	20	35	63	
				V_{IOVDD} = 1.7V to 1.9V	5	10	21	
		PCLKOUT	V_O = 0V, DCS = 0	V_{IOVDD} = 3.0V to 3.6V	15	33	50	
				V_{IOVDD} = 1.7V to 1.9V	5	10	17	
			V_O = 0V, DCS = 1	V_{IOVDD} = 3.0V to 3.6V	30	54	97	
				V_{IOVDD} = 1.7V to 1.9V	9	16	32	
OPEN-DRAIN INPUTS/OUTPUTS (GPIO0/DBL, GPIO1/BWS, RX/SDA/EDC, TX/SCL/ES, $\overline{ERR}$, LOCK, LFLT)								
High-Level Input Voltage	V_{IH2}				0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}						0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 4)		RX/SDA, TX/SCL	-110		+5	µA
				LOCK, $\overline{ERR}$, GPIO_, $\overline{LFLT}$	-80		+5	
				DBL, BWS, EDC, ES	-10		+20	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA		V_{IOVDD} = 1.7V to 1.9V			0.4	V
				V_{IOVDD} = 3.0V to 3.6V			0.3	
OUTPUT FOR REVERSE CONTROL CHANNEL (IN+, IN-)								
Differential High Output Peak Voltage, (V_{IN}+) - (V_{IN}-)	V_{ROH}	No high-speed data transmission (Figure 1)			30		60	mV
Differential Low Output Peak Voltage, (V_{IN}+) - (V_{IN}-)	V_{ROL}	No high-speed data transmission (Figure 1)			-60		-30	mV
DIFFERENTIAL INPUTS (IN+, IN-)								
Differential High Input Threshold (Peak) Voltage, (V_{IN}+) - (V_{IN}-)	$V_{IDH(P)}$	(Figure 2)	Activity detector, medium threshold (0x22 D[6:5] = 01)				60	mV
			Activity detector, low threshold (0x22 D[6:5] = 00)				45	
Differential Low Input Threshold (Peak) Voltage, (V_{IN}+) - (V_{IN}-)	$V_{IDL(P)}$	(Figure 2)	Activity detector, medium threshold (0x22 D[6:5] = 01)		-60			mV
			Activity detector, medium threshold (0x22 D[6:5] = 00)		-45			
Input Common-Mode Voltage ((V_{IN}+) + (V_{IN}-))/2	V_{CMR}				1	1.3	1.6	V
Differential Input Resistance (Internal)	R_I				80	105	130	Ω

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (IN+, IN-)							
Single-Ended High Input Threshold (Peak) Voltage	$V_{ISH(P)}$	Activity detector, medium threshold (0x22 D[6:5] = 01) (Figure 3)				43	mV
		Activity detector, low threshold (0x22 D[6:5] = 00) (Figure 3)				33	
Single-Ended Low Input Threshold (Peak) Voltage	$V_{ISL(P)}$	Activity detector, medium threshold (0x22 D[6:5] = 01) (Figure 3)		-43			mV
		Activity detector, medium threshold (0x22 D[6:5] = 00) (Figure 3)		-33			
Input Resistance (Internal)	R_I			40	52.5	65	Ω
LINE FAULT DETECTION INPUT (LMN0, LMN1)							
Short-to-GND Threshold	V_{TG}	(Figure 4)				0.3	V
Normal Threshold	V_{TN}	(Figure 4)		0.57		1.07	V
Open Threshold	V_{TO}	(Figure 4)		1.45		V_{IO} + 0.06	V
Open Input Voltage	V_{IO}	(Figure 4)		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	(Figure 4)		2.47			V
POWER SUPPLY							
Worst-Case Supply Current (Figure 5)	I_{WCS}	BWS = 0, single output, EQ off	$f_{PCLKOUT}$ = 25MHz		42	65	mA
			$f_{PCLKOUT}$ = 50MHz		61	90	
		BWS = 0, double output, EQ off	$f_{PCLKOUT}$ = 50MHz		42	70	
			$f_{PCLKOUT}$ = 100MHz		62	90	
Sleep Mode Supply Current	I_{CCS}				50	100	µA
Power-Down Current	I_{CCZ}	$\overline{PWDN}$ = EP			15	70	µA
ESD PROTECTION							
IN+, IN- (Note 5)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±8			kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge	±10			
			Air discharge	±15			
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge	±10			
			Air discharge	±30			
All Other Pins (Note 6)	V_{ESD}	Human Body Model, R_D = 1.5kΩ , C_S = 100pF		±4			kV

AC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PARALLEL CLOCK OUTPUT (PCLKOUT)							
Clock Frequency	$f_{PCLKOUT}$	BWS = 0, DRS = 1		8.33		16.66	MHz
		BWS = 0, DRS = 0		16.66		50	
		BWS = 1, DRS = 1		6.25		12.5	
		BWS = 1, DRS = 0		12.5		37.5	
		BWS = 1, DRS = 0, 15-bit double input		25		75	
		BWS = 0, DRS = 0, 11-bit double input		33.33		100	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 6, Note 7)		40	50	60	%
Clock Jitter	t_J	Period jitter, peak to peak, spread off, 1.5Gbps, PRBS pattern, UI = $1/f_{PCLKOUT}$ (Note 7)			0.05		UI
I²C/UART PORT TIMING							
I²C/UART Bit Rate				9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		120	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		120	ns
Input Setup Time	t_{SET}	I²C only (Figure 6, Note 7)		100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 6, Note 7)		0			ns
SWITCHING CHARACTERISTICS							
PCLKOUT Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V (Note 7)	DCS = 1, C_L = 10pF	0.4		2.2	ns
			DCS = 0, C_L = 5pF	0.5		2.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V (Note 7)	DCS = 1, C_L = 10pF	0.25		1.7	
			DCS = 0, C_L = 5pF	0.3		2.0	
Parallel Data Rise-and-Fall Time (Figure 8)	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V (Note 7)	DCS = 1, C_L = 10pF	0.5		3.1	ns
			DCS = 0, C_L = 5pF	0.6		3.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V (Note 7)	DCS = 1, C_L = 10pF	0.3		2.2	
			DCS = 0, C_L = 5pF	0.4		2.4	
Deserializer Delay	t_{SD}	(Figure 9, Notes 7, 8)	Spread spectrum enabled			6960	Bits
			Spread spectrum disabled			2160	
Reverse Control-Channel Output Rise Time	t_R	No forward-channel data transmission (Figure 1, Note 7)		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward-channel data transmission (Figure 1, Note 7)		180		400	ns

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included) (Figure 10)				350	µs
Lock Time	t_{LOCK}	(Figure 11, Note 7)	Spread spectrum enabled			1.5	ms
			Spread spectrum disabled			1	
Power-Up Time	t_{PU}	(Figure 12)				6	ms

Note 2: Limits are 100% production tested at T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 3: To provide a midlevel, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.

Note 4: I_{IN} min due to voltage drop across the internal pullup resistor.

Note 5: Specified pin to ground.

Note 6: Specified pin to all supply/ground.

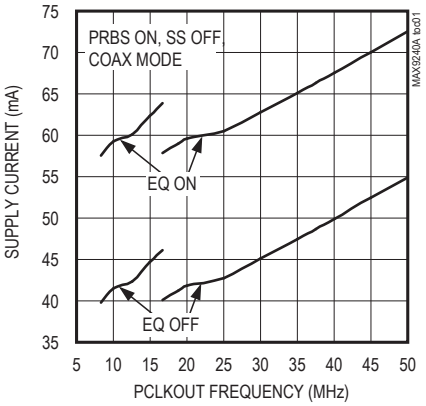
Note 7: Guaranteed by design and not production tested.

Note 8: Measured in serial link bit times. Bit time = 1/(30 x $f_{PCLKOUT}$) for BWS = GND. Bit time = 1/(40 x $f_{PCLKOUT}$) for BWS = 1.

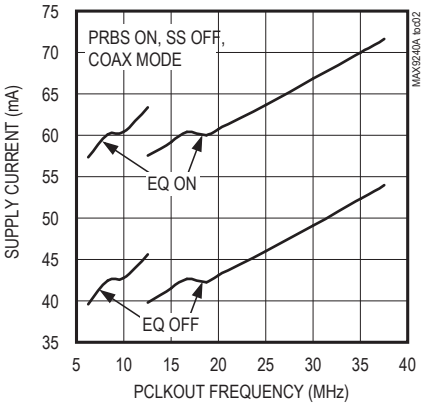
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, DBL = low, T_A = +25°C, unless otherwise noted.)

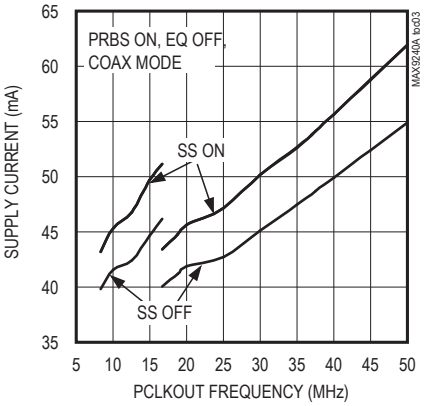
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 0)



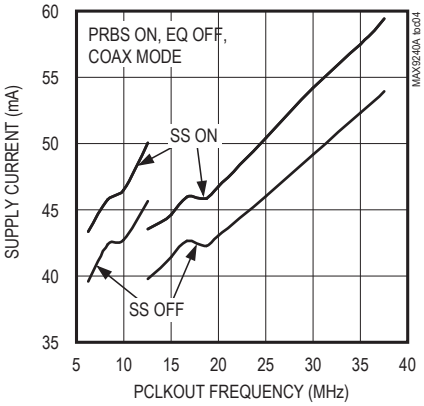
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 1)



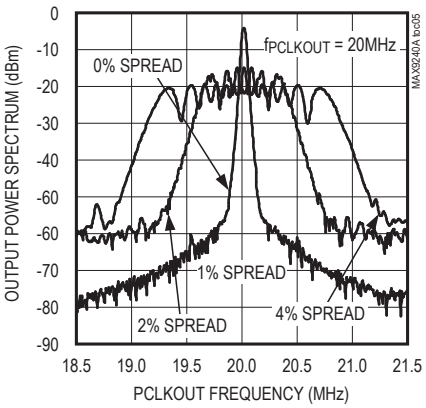
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 0)



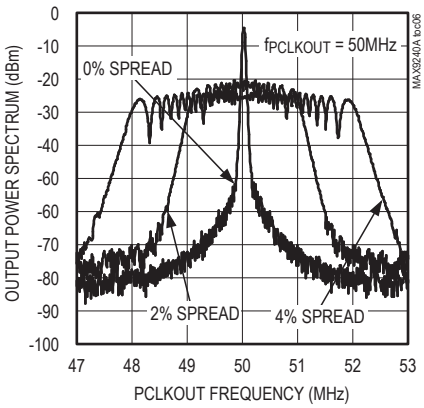
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 1)



OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (VARIOUS SPREAD)



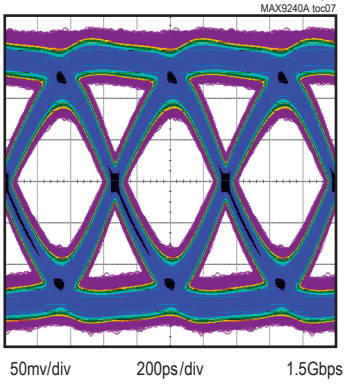
OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (VARIOUS SPREAD)



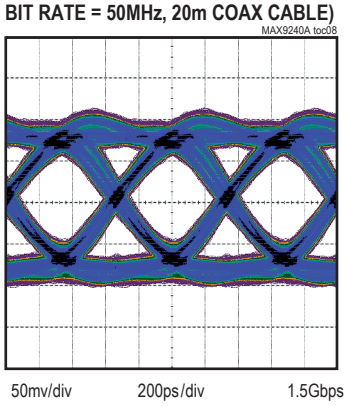
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, DBL = low, T_A = +25°C, unless otherwise noted.)

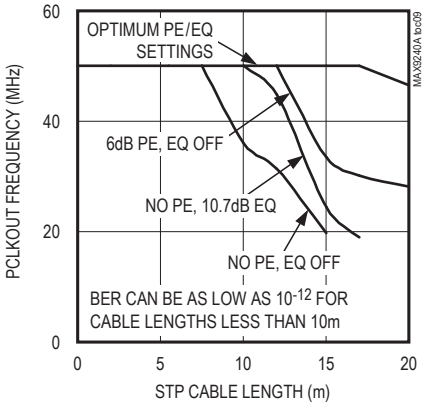
SERIAL LINK SWITCHING PATTERN WITH 6dB PREEMPHASIS (PARALELL BIT RATE = 50MHz, 10m STP CABLE)



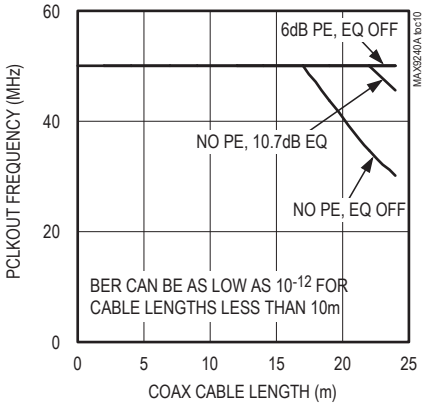
SERIAL LINK SWITCHING PATTERN WITH 6dB PREEMPHASIS (PARALELL BIT RATE = 50MHz, 20m COAX CABLE)



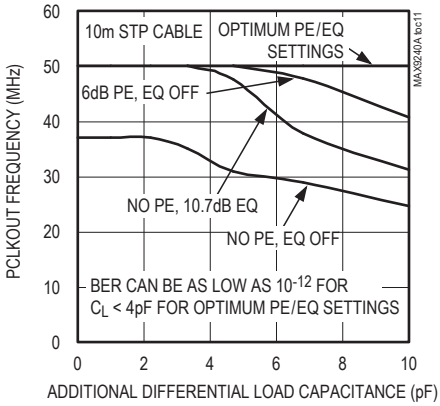
MAXIMUM PCLKOUT FREQUENCY vs. STP CABLE LENGTH (BER ≤ 10^{-10})



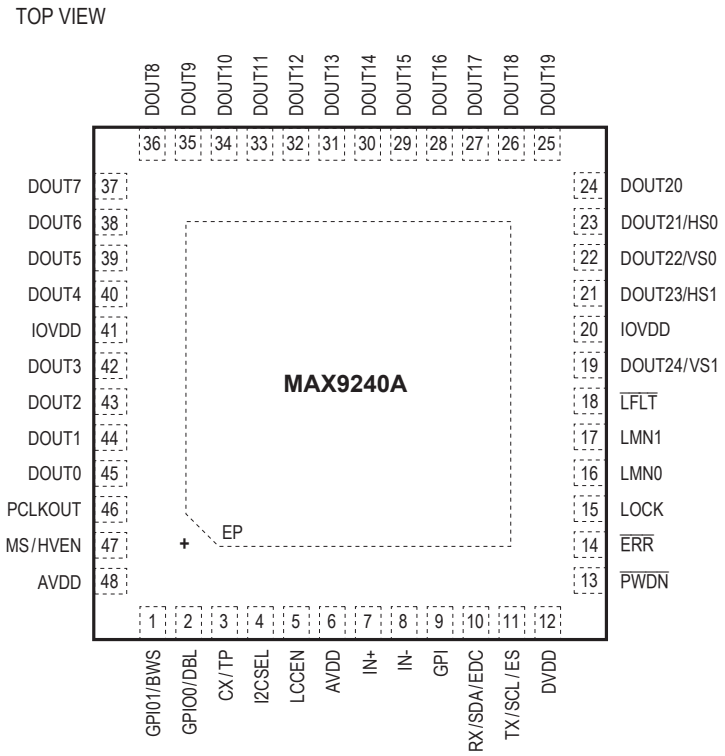
MAXIMUM PCLKOUT FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



MAXIMUM PCLKOUT FREQUENCY vs. ADDITIONAL DIFFERENTIAL C_L (BER ≤ 10^{-10})



Pin Configuration



TQFN
(7mm x 7mm X 0.75mm)
CONNECT EP TO GROUND PLANE

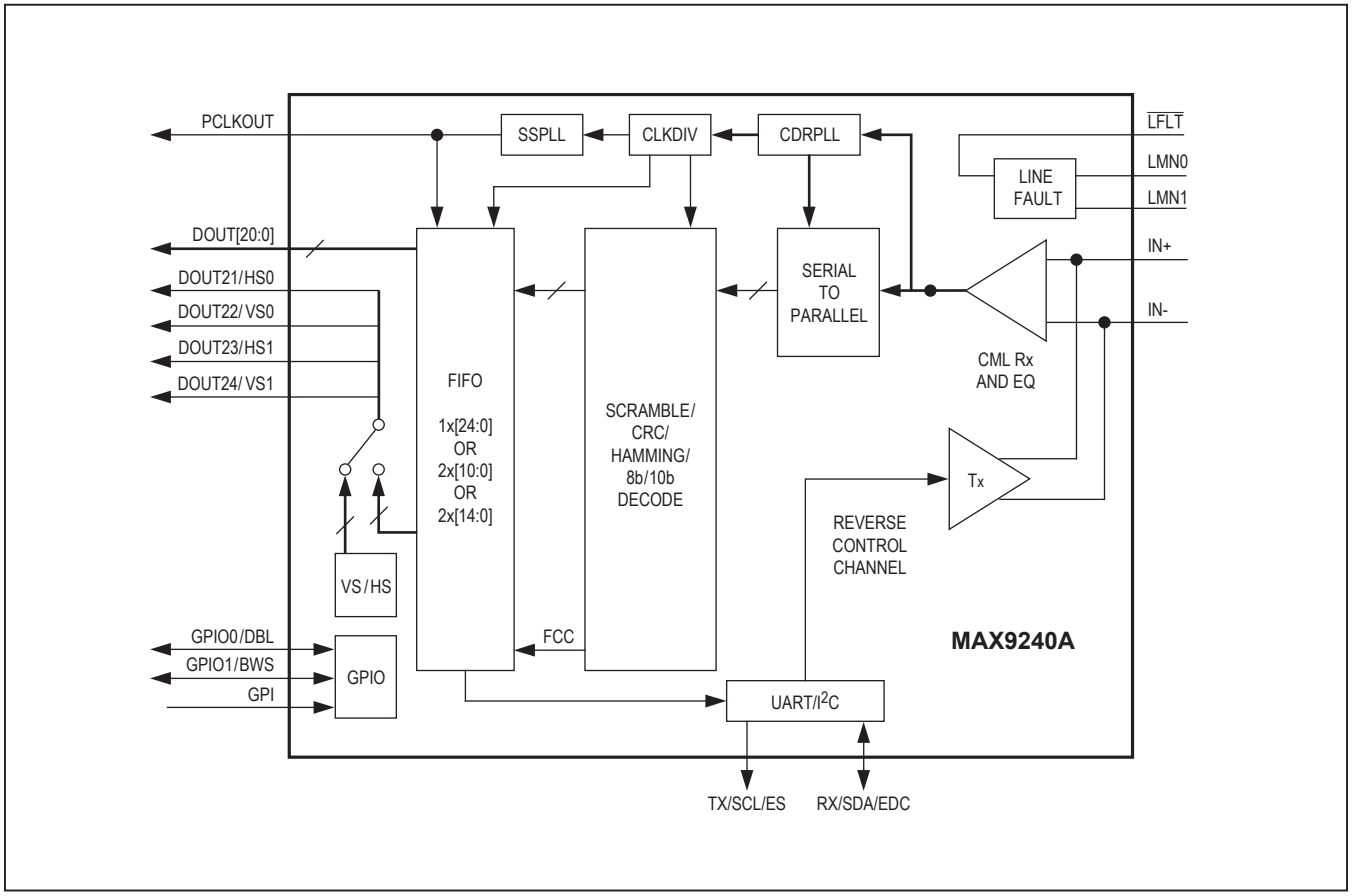
Pin Description

PIN	NAME	FUNCTION
1	GPIO1/BWS	GPIO/Bus Width Select Input. Function is determined by the state of LCCEN (Table 12). GPIO1 (LCCEN = high): Open-drain, general-purpose input/output with internal 60kΩ pullup to IOVDD. BWS (LCCEN = low): Input with internal pulldown to EP. Set BWS = low for 22-bit input latch. Set BWS = high for 30-bit input latch.
2	GPIO0/DBL	GPIO/Double-Mode Input. Function is determined by the state of LCCEN (Table 12). GPIO0 (LCCEN = high): Open-drain, general-purpose input/output with internal 60kΩ pullup to IOVDD. DBL (LCCEN = low): Input with internal pulldown to EP. Set DBL = high to use double-input mode. Set DBL = low to use single-input mode.
3	CX/TP	Coax/Twisted-Pair Three-Level Configuration Input (Table 7)
4	I2CSEL	I^2C Select. Control-channel interface protocol select input with internal pulldown to EP. Set I2CSEL = high to select I^2C slave interface. Set I2CSEL = low to select UART interface.
5	LCCEN	Local Control-Channel Enable Input with Internal Pulldown to EP. LCCEN = high enables the control-channel interface pins. LCCEN = low disables the control-channel interface pins and selects an alternate function on the indicated pins (Table 12).
6, 48	AVDD	1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
7	IN+	Noninverting Coax/Twisted-Pair Serial Input
8	IN-	Inverting Coax/Twisted-Pair Serial Input
9	GPI	General-Purpose Input. The GMSL serializer GPO (or INT) input follows GPI.
10	RX/SDA/EDC	Receive/Serial Data/Error Detection Correction. Function is determined by the state of LCCEN (Table 12). RX/SDA (LCCEN = high): Input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the RX input of the MAX9240A's UART. In the I^2C mode, RX/SDA is the SDA input/output of the MAX9240A's I^2C master/slave. RX/SDA has an open-drain driver and requires a pullup resistor. EDC (LCCEN = low): Input with internal pulldown to EP. Set EDC = high to enable error detection correction. Set EDC = low to disable error detection correction.
11	TX/SCL/ES	Transmit/Serial Clock/Edge Select. Function is determined by the state of LCCEN (Table 12). TX/SCL (LCCEN = high): Input/output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the TX output of the MAX9240A's UART. In the I^2C mode, TX/SCL is the SCL input/output of the MAX9240A's I^2C master/slave. TX/SCL has an open-drain driver and requires a pullup resistor. ES (LCCEN = low): Input with internal pulldown to EP. When ES is high, PCLKOUT indicates valid data on the falling edge of PCLKOUT. When ES is low, PCLKOUT indicates valid data on the rising edge of PCLKOUT. Do not change the ES input while the pixel clock is running.
12	DVDD	1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
13	$\overline{PWDN}$	Active-Low Power-Down Input with Internal Pulldown to EP. Set $\overline{PWDN}$ low to enter power-down mode to reduce power consumption.
14	$\overline{ERR}$	Error Output. Open-drain data error detection and/or correction indication output with internal 60kΩ pullup to IOVDD. $\overline{ERR}$ is output high when $\overline{PWDN}$ = low.

Pin Description (continued)

PIN	NAME	FUNCTION
15	LOCK	Open-Drain Lock Output with Internal 60kΩ Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK remains low when the configuration link is active or during PRBS test. LOCK is output high when $\overline{PWDN}$ = low.
16	LMN0	Line Fault Monitor Input 0 (Figure 4)
17	LMN1	Line Fault Monitor Input 1 (Figure 4)
18	$\overline{LFLT}$	Active-Low Open-Drain Line Fault Output. $\overline{LFLT}$ has a 60kΩ internal pullup to IOVDD. $\overline{LFLT}$ = low indicates a line fault. $\overline{LFLT}$ is output high when $\overline{PWDN}$ = low.
19	DOUT24/VS1	Parallel Data/Vertical Sync 1 Output. Defaults to parallel data output on power-up. Parallel data output when VS/HS encoding is disabled. Decoded vertical sync for upper half of single-output when VS/HS encoding is enabled (Table 1).
20, 41	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
21	DOUT23/HS1	Parallel Data/Horizontal Sync 1 Output. Defaults to parallel data output on power-up. Parallel data output when VS/HS encoding is disabled. Decoded horizontal sync for upper half of single-output when VS/HS encoding is enabled (Table 1).
22	DOUT22/VS0	Parallel Data/Vertical Sync 0 Output. Defaults to parallel data output on power-up. Parallel data output when VS/HS encoding is disabled. Decoded vertical sync for lower half of single-output when VS/HS encoding is enabled (Table 1).
23	DOUT21/HS0	Parallel Data/Horizontal Sync 0 Output. Defaults to parallel data output on power-up. Parallel data output when VS/HS encoding is disabled. Decoded horizontal sync for lower half of single-output when VS/HS encoding is enabled (Table 1).
24–40, 42–45	DOUT20–DOUT0	Parallel Data Outputs
46	PCLKOUT	Parallel Clock Output. Latches parallel data into the input of another device.
47	MS/HVEN	Mode Select/HS and VS Encoding Enable with Internal Pulldown to EP. Function is determined by the state of LCCEN (Table 12). MS (LCCEN = high): Set MS = low to select base mode. Set MS = high to select the bypass mode. HVEN (LCCEN = low): Set HVEN = high to enable HS/VS encoding on DOUT_/HS_ and DOUT_/VS_. Set HVEN = low to use DOUT_/HS_ and DOUT_/VS_ as parallel data outputs.
—	EP	Exposed Pad. EP is internally connected to device ground. **MUST** connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



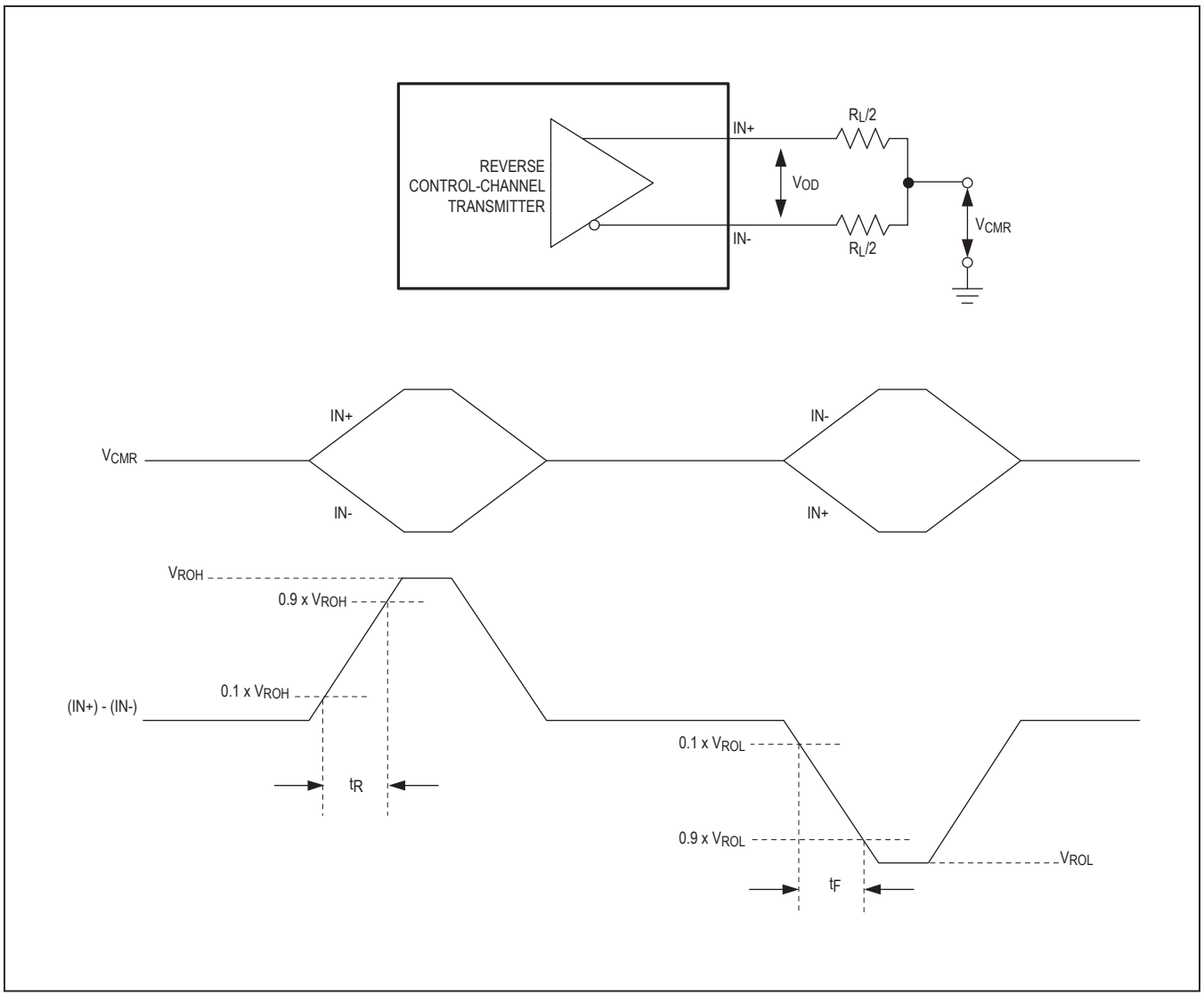


Figure 1. Reverse Control-Channel Output Parameters

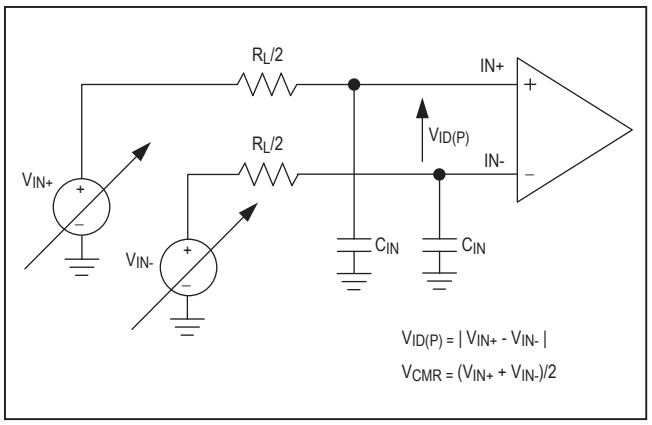


Figure 2. Test Circuit for Differential Input Measurement

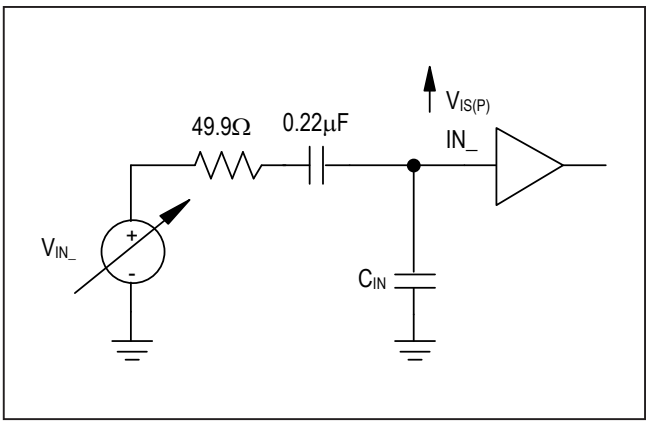


Figure 3. Test Circuit for Single-Ended Input Measurement

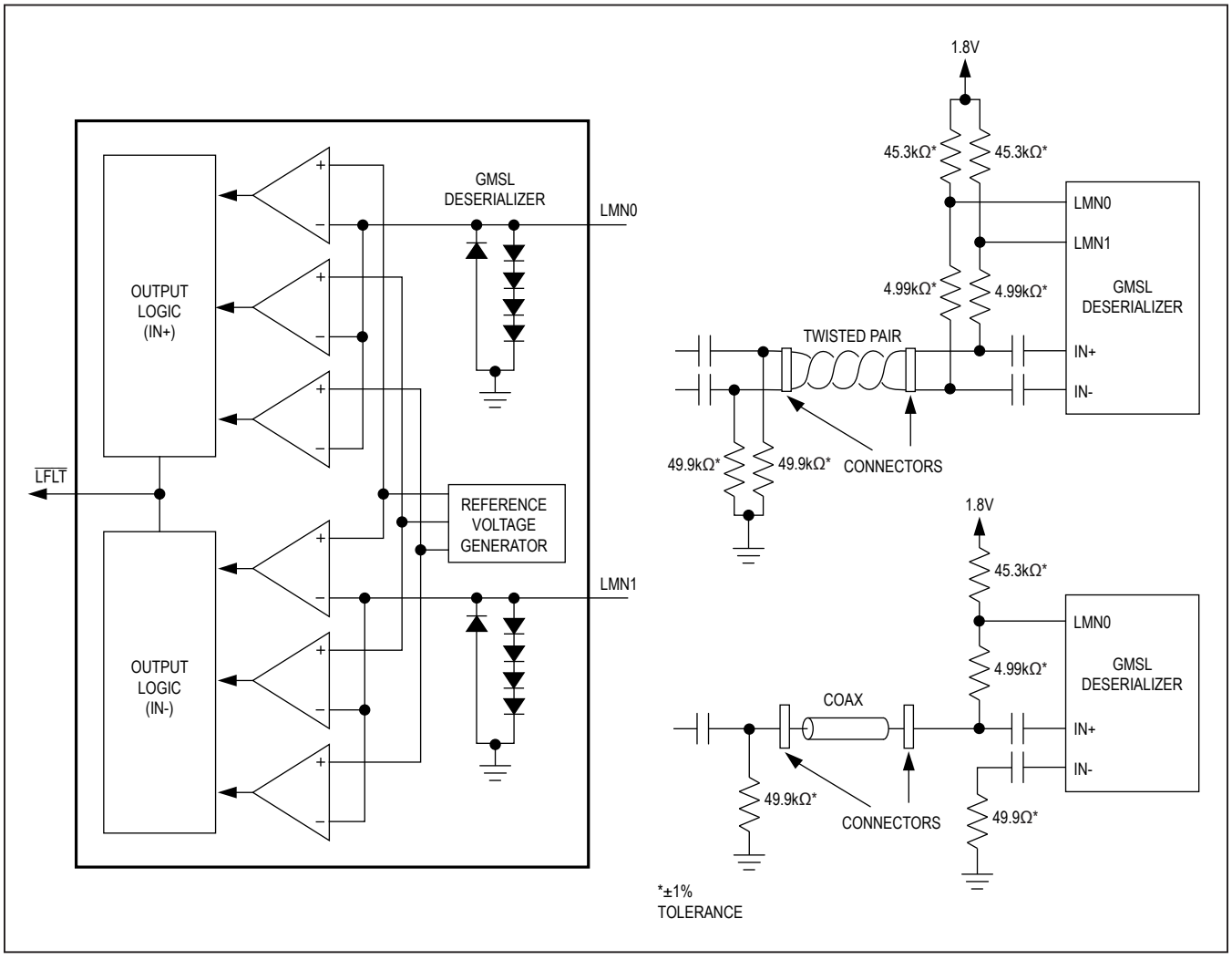


Figure 4. Line Fault

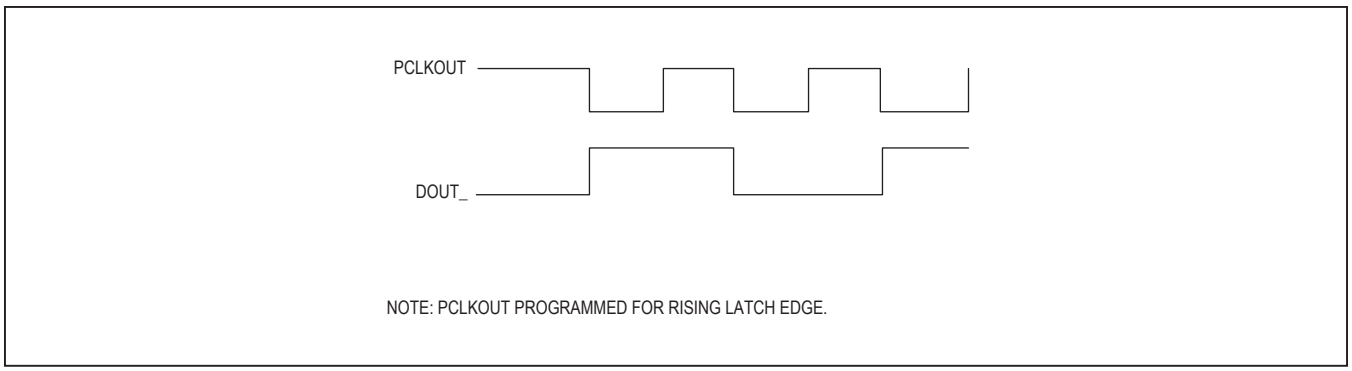


Figure 5. Worst-Case Pattern Output

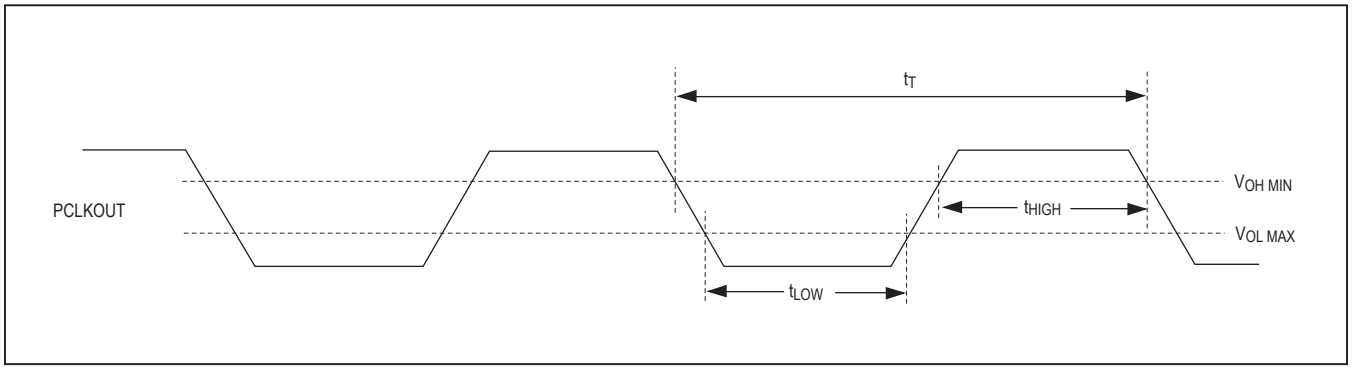


Figure 6. Parallel Clock Output High and Low Times

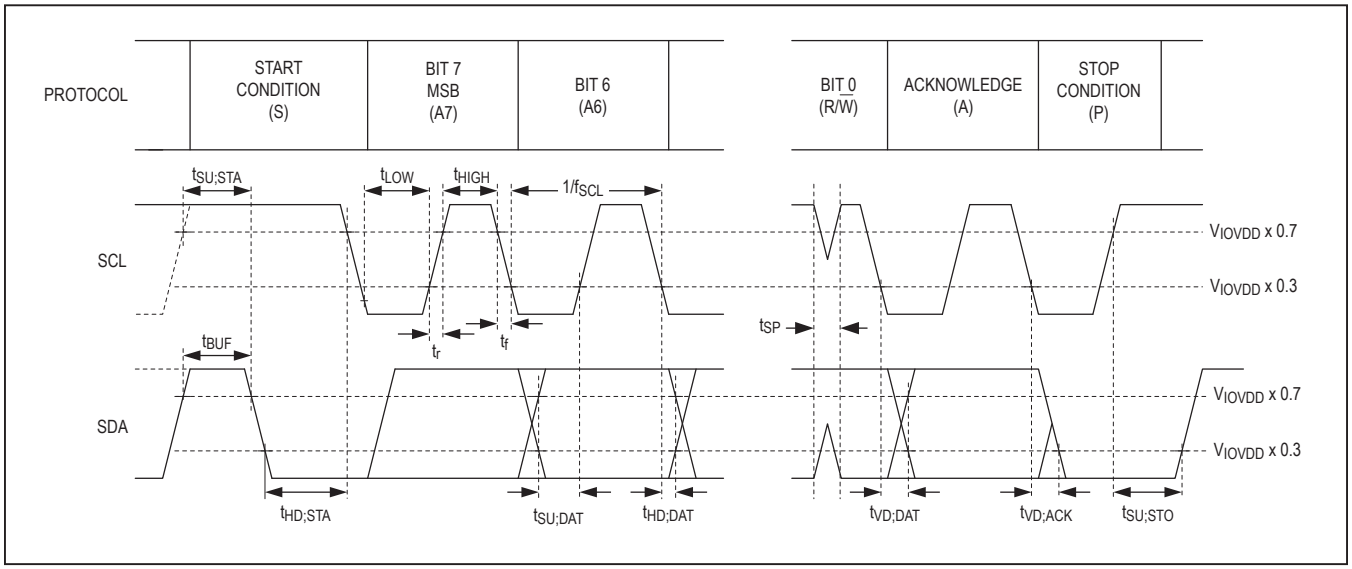


Figure 7. I²C Timing Parameters

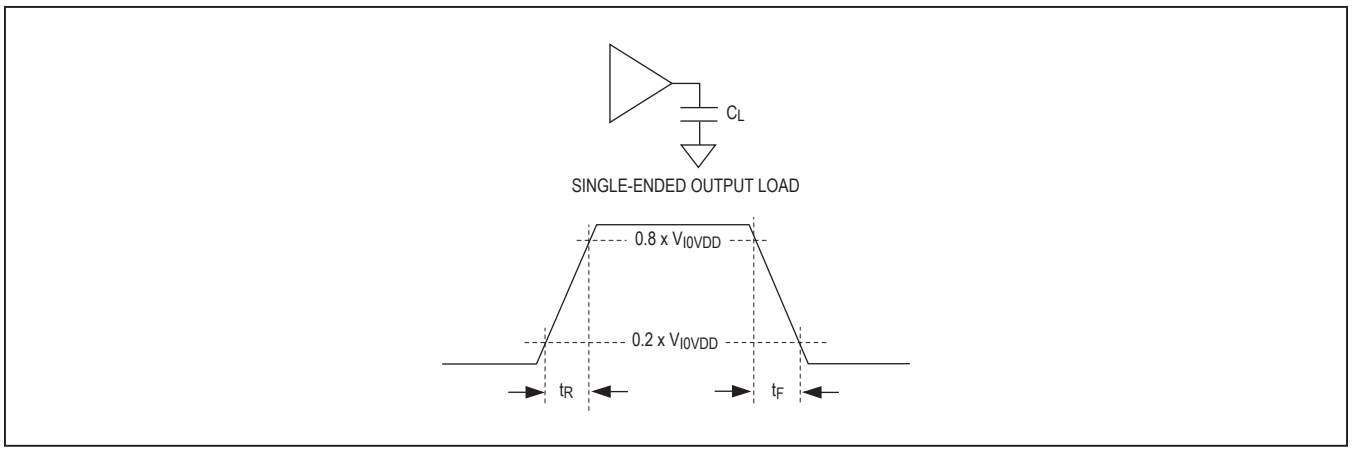


Figure 8. Output Rise-and-Fall Times

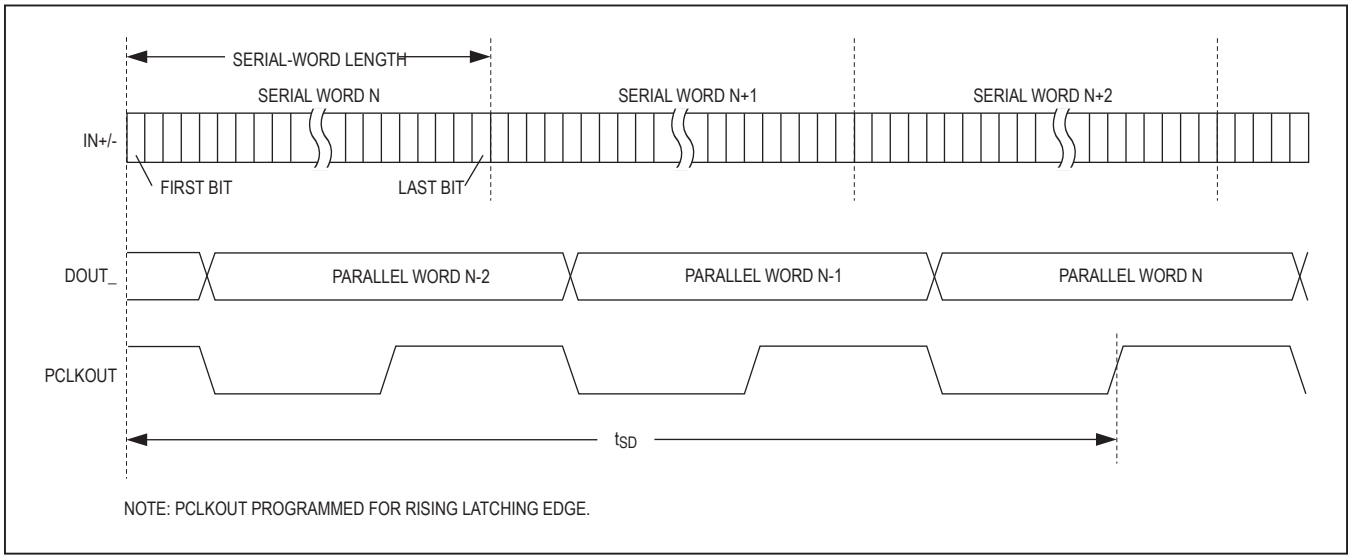


Figure 9. Deserializer Delay

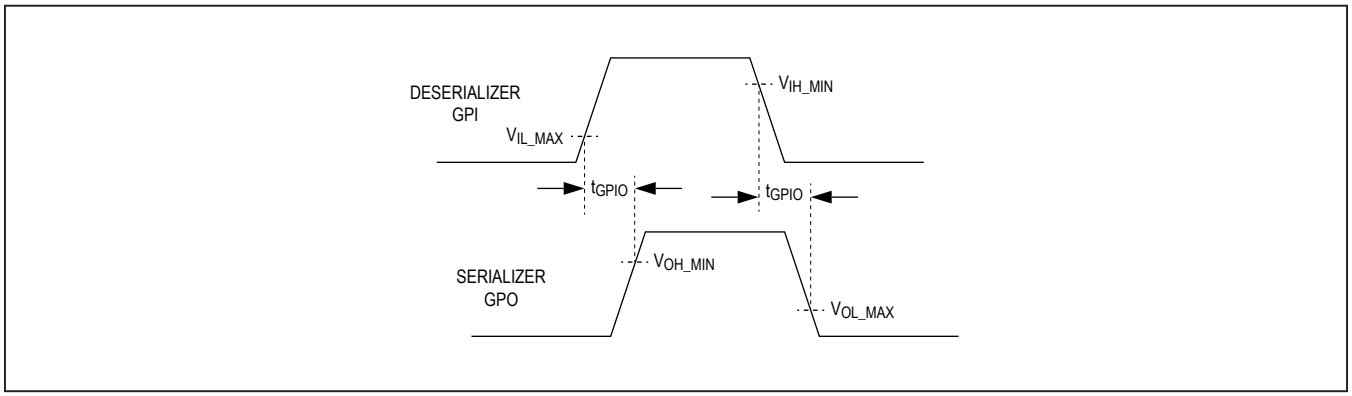


Figure 10. GPI-to-GPO Delay

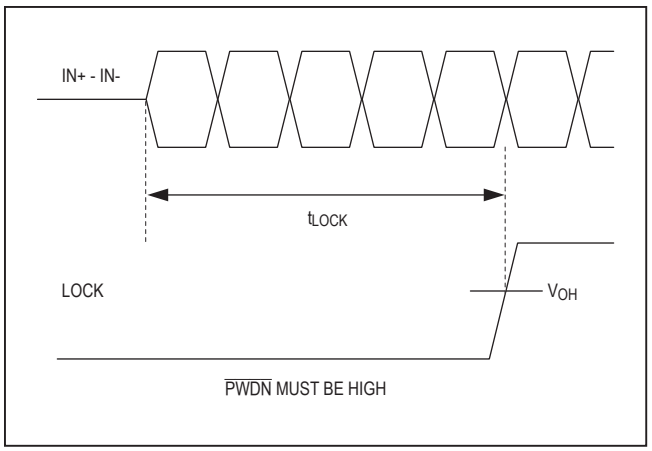


Figure 11. Lock Time

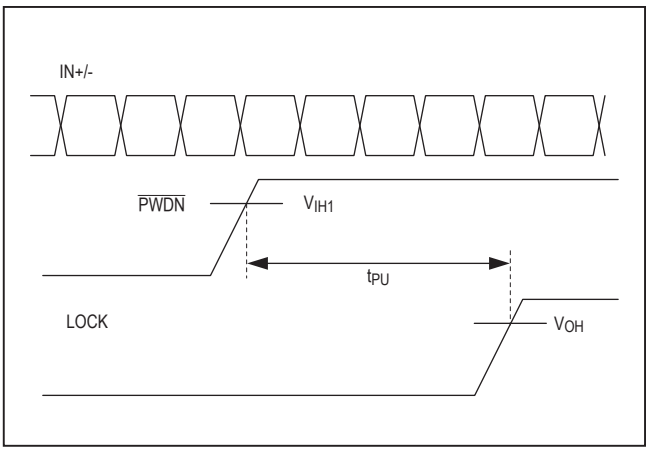


Figure 12. Power-Up Delay

Detailed Description

The MAX9240A deserializer, when paired with the MAX9271 or MAX9273 serializer, provides the full set of operating features, but offers basic functionality when paired with any GMSL serializer.

The deserializer has a maximum serial-bit rate of 1.5Gbps for 15m or more of cable and operates up to a maximum output clock of 50MHz in 25-bit, single-output mode, or 75MHz to 100MHz in 15-bit/11-bit, double-output mode, respectively. This bit rate and output flexibility support a wide range of displays, from QVGA (320 x 240) to WVGA (800 x 480) and higher with 18-bit color, as well as megapixel image sensors. Input equalization, combined with GMSL serializer pre/deemphasis, extends the cable length and enhances link reliability

The control channel enables a µC to program the serializer and deserializer registers and program registers on peripherals. The control channel is also used to configure and access the GPIO. The µC can be located at either end of the link, or when using two µCs, at both ends. Two modes of control-channel operation are available. Base mode uses either I^2C or GMSL UART protocol, while bypass mode uses a user-defined UART protocol. UART protocol allows full-duplex communication, while I^2C allows half-duplex communication.

Spread spectrum is available to reduce EMI on the parallel output. The serial input complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the deserializer and are programmed using the control channel in base mode. The deserializer holds its device address and the device address of the serializer it is paired with. Similarly, the serializer holds its device address and the address of the deserializer. Whenever a device address is changed, the new address should be written to both devices. The default device address of the deserializer is set by the CX/TP input and the default device address of any GMSL serializer is 0x80 (see Table 7). Registers 0x00 and 0x01 in both devices hold the device addresses.

Bit Map

The parallel output functioning and width depend on settings of the double-/single-output mode (DBL), HS/VS encoding (HVEN), error correction used (EDC), and bus width (BWS) pins. Table 1 lists the bit map for the control pin settings. Unused output bits are pulled low.

The parallel output has two output modes: single and double output. In single-output mode, the deserialized parallel data is clocked out every PCLKOUT cycle. The device accepts pixel clocks from 6.25MHz to 50MHz (Figure 13 and Figure 14).

In double-output mode, the device splits deserialized data into two half-sized words that are output at twice the serial-word rate (Figure 15 and Figure 16. The serializer/deserializer use pixel clock rates from 33.3MHz to 100MHz for 11-bit, double-output mode and 25MHz to 75MHz for 15-bit, double-output mode.

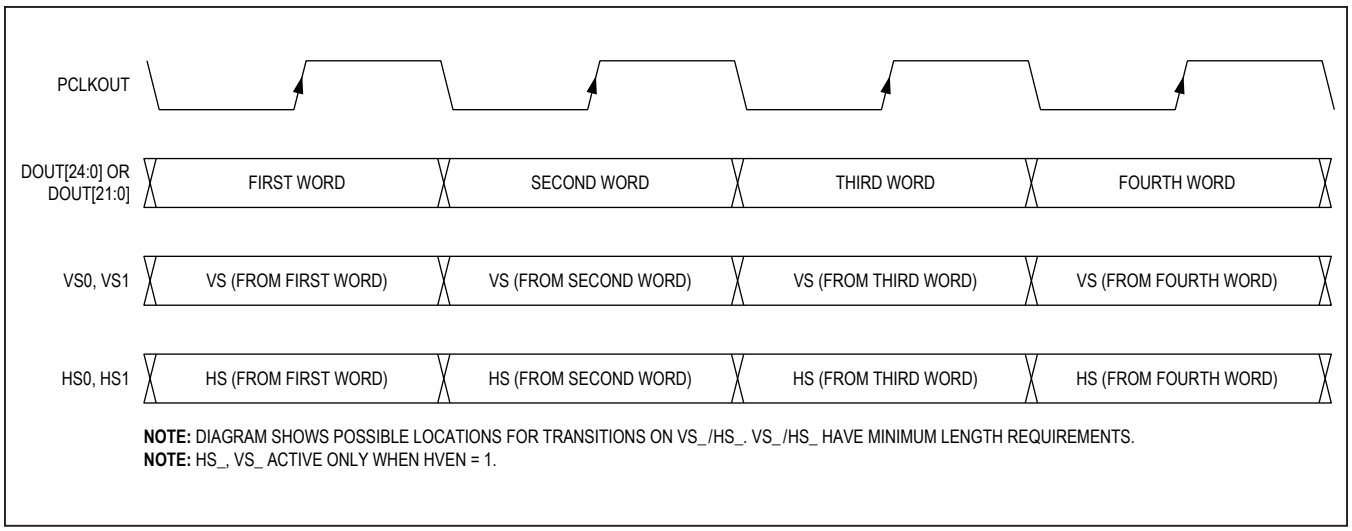


Figure 13. Single-Output Waveform (Serializer Using Single Input)

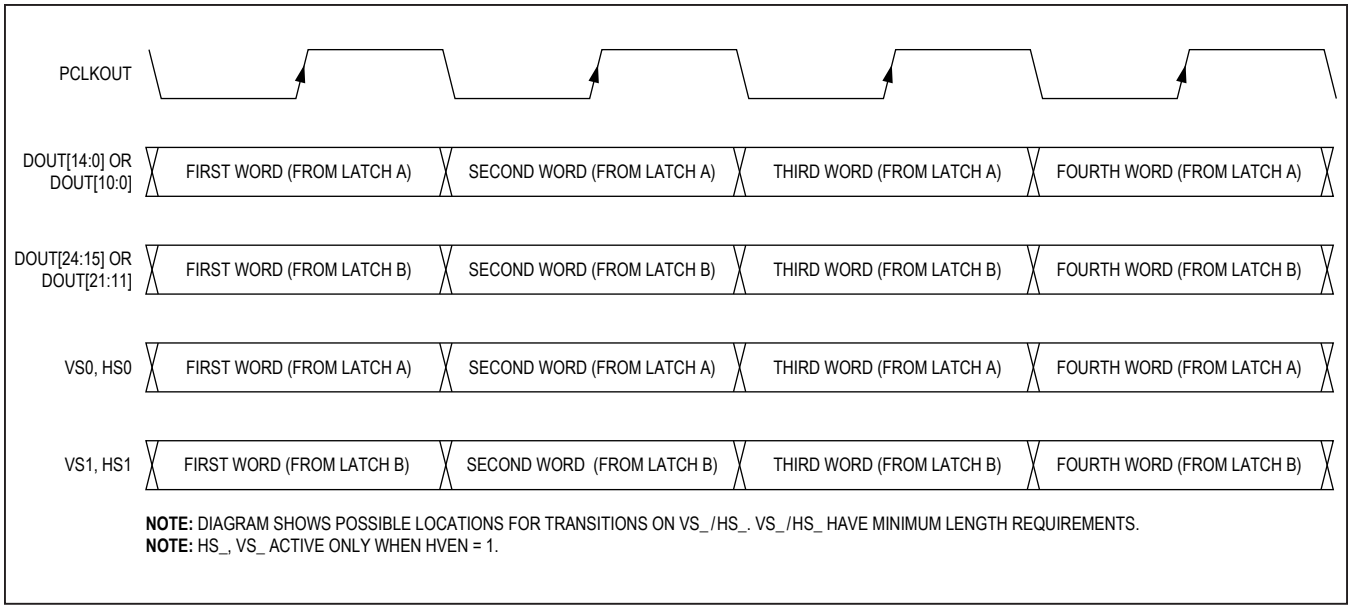


Figure 14. Single-Output Waveform (Serializer Using Double Input)

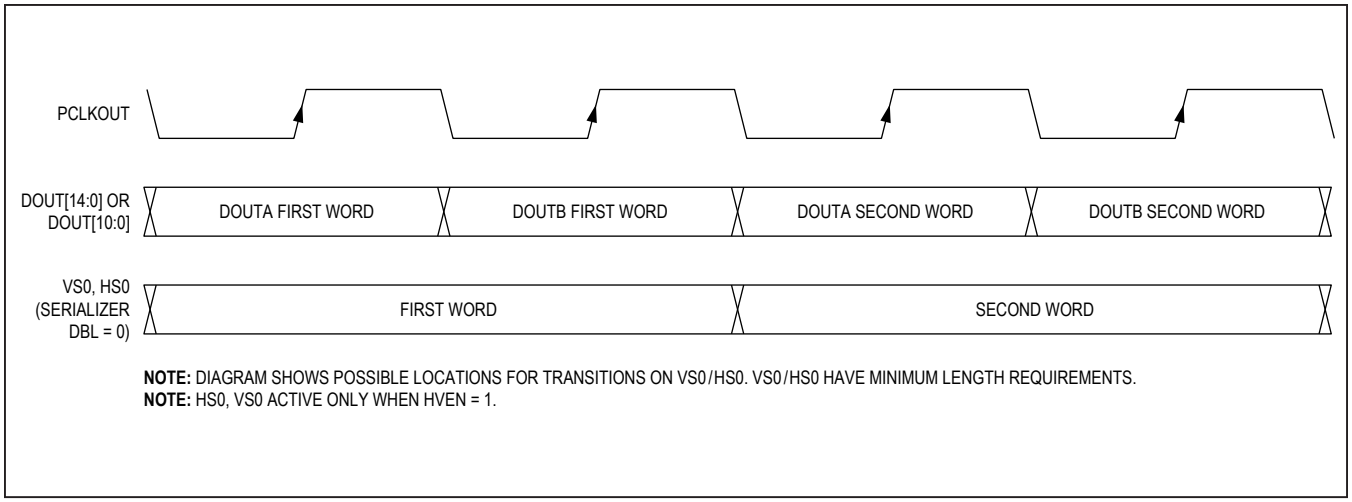


Figure 15. Double-Output Waveform (Serializer Using Single Input)

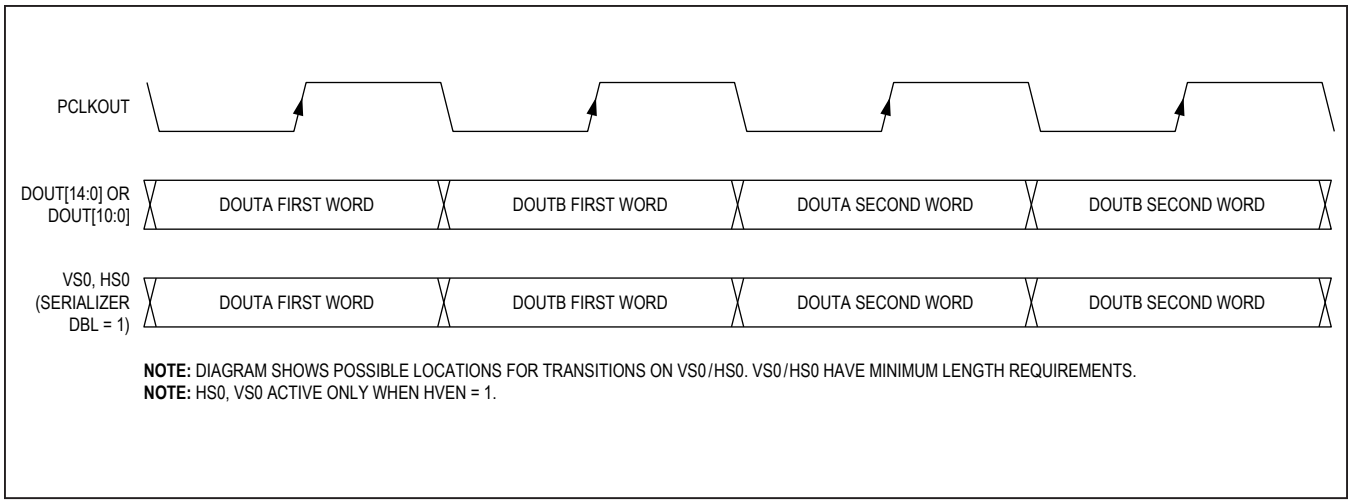


Figure 16. Double-Output Waveform (Serializer Using Double Input)

Table 1. Output Map

EDC	BWS	DBL	HVEN	OUTPUT* (PAIRED WITH MAX9271)	OUTPUT* (PAIRED WITH MAX9273)	PCLK RANGE** (MHz)
00	0	0	0	DOUT0:15	DOUT0:21	16.66 to 50
00	0	0	1	DOUT0:13, HS, VS	DOUT0:20, HS, VS	16.66 to 50
00	0	1	0	DOUT0:10	DOUT0:10	33.33 to 100
00	0	1	1	DOUT0:10, HS, VS	DOUT0:10, HS, VS	33.33 to 100
00	1	0	0	DOUT0:15	DOUT0:21	12.5 to 37.5
00	1	0	1	DOUT0:13, HS, VS	DOUT0:20, HS, VS	12.5 to 37.5
00	1	1	0	DOUT0:14	DOUT0:14	25 to 75
00	1	1	1	DOUT0:13, HS, VS	DOUT0:14, HS, VS	25 to 75
01, 10	0	0	0	DOUT0:15	DOUT0:15	16.66 to 50
01, 10	0	0	1	DOUT0:13, HS, VS	DOUT0:15, HS, VS	16.66 to 50
01, 10	0	1	0	DOUT0:7	DOUT0:7	33.33 to 100
01, 10	0	1	1	DOUT0:7, HS, VS	DOUT0:7, HS, VS	33.33 to 100
01, 10	1	0	0	DOUT0:15	DOUT0:21	12.5 to 37.5
01, 10	1	0	1	DOUT0:13, HS, VS	DOUT0:20, HS, VS	12.5 to 37.5
01, 10	1	1	0	DOUT0:11	DOUT0:11	25 to 75
01, 10	1	1	1	DOUT0:11, HS, VS	DOUT0:11, HS, VS	25 to 75

**The number of available outputs depends on the serializer attached to the MAX9240A.*

***Device is in high-speed mode (DRS = LOW). See Table 2 for PCLK ranges in low-speed mode (DRS = high).*

Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coax cable with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization.

Input data is scrambled and then 8b/10b coded. The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. In 24-bit or 32-bit mode, 22 or 30 bits contain the video data and/or error-correction bits, if used. The 23rd or 31st bit carries the forward control-channel data. The last bit is the parity bit of the previous 23 or 31 bits (Figure 17).

Reverse Control Channel

The serializer uses the reverse control channel to receive I²C/UART and GPO signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same serial cable, forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 2ms after power-up. The serializer temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

Data-Rate Selection

The serializer/deserializer use DRS, DBL, and BWS to set the PCLKOUT frequency range (Table 2). Set DRS = 1 for a PCLKOUT frequency range of 6.25MHz to 12.5MHz (32-bit, single-output mode) or 8.33MHz to 16.66MHz (24-bit, single-output mode). Set DRS = 0 for normal operation. It is not recommended to use double-output mode when DRS = 1.

Table 2. Data-Rate Selection Table

DRS SETTING	DBL SETTING	BWS SETTING	PCLKOUT RANGE (MHz)
0	0 (single input)	0 (24-bit mode)	16.66 to 50
0	0	1 (32-bit mode)	12.5 to 35
0	1 (double input)	0	33.3 to 100
0	1	1	25 to 75
1	0	0	8.33 to 16.66
1	0	1	6.25 to 12.5
1	1	0	Do Not Use
1	1	1	Do Not Use

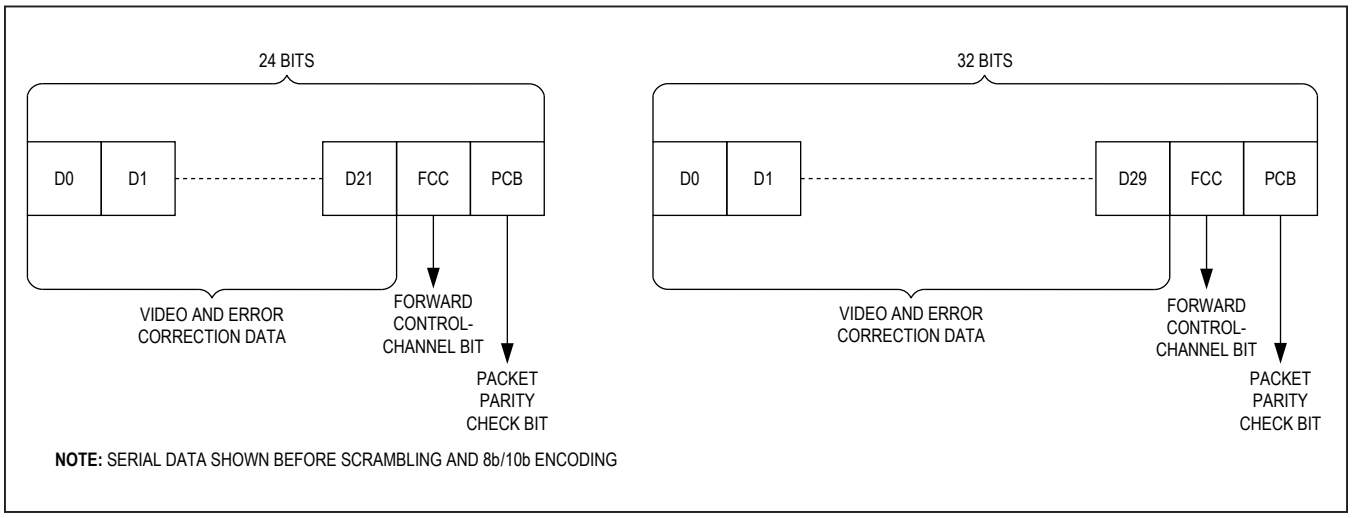


Figure 17. Serial-Data Format

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. The µC controls the link from either the serializer or the deserializer side to support video-display or image-sensing applications. The control channel between the µC and serializer or deserializer runs in base mode or bypass mode, according to the mode selection (MS/HVEN) input of the device connected to the µC. Base mode is a half-duplex control channel and bypass mode is a full-duplex control channel.

UART Interface

In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer, with the UART packets converted to I^2C by the device on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/deserializer. The device addresses of the serializer/deserializer in base mode are programmable. The default value is 0x80 for the serializer and is determined by the CX/TP input for the deserializer (Table 7).

When the peripheral interface is I^2C, the serializer/deserializer convert UART packets to I^2C that have device addresses different from those of the serializer or deserializer. The converted I^2C bit rate is the same as the original UART bit rate.

The deserializer uses differential line coding to send signals over the reverse channel to the serializer. The bit rate of the control channel is 9.6kbps to 1Mbps in both directions. The serializer/deserializer automatically detect the control-channel bit rate in base mode. Packet bit-rate changes can be made in steps of up to 3.5 times higher or lower than the previous bit rate. See the *Changing the Clock Frequency* section for more information.

Figure 18 shows the UART protocol for writing and reading in base mode between the µC and the serializer/deserializer.

Figure 19 shows the UART data format. Even parity is used. Figure 20 and Figure 21 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and GPI generate transitions on the control channel that can be ignored by the µC. Data written to the serializer/deserializer registers do not take effect until after the ACK byte is sent. This allows the µC to verify that write commands are received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART's data rate. If the GPI or MS/HVEN inputs of the deserializer toggle while there is control-channel communication, or if a line fault occurs, the control-channel communication is corrupted. In the event of a missed or delayed acknowledge (~1ms due to control-channel timeout), the µC should assume there was an error in the packet transmission or response. In base mode, the µC must keep the UART Tx/Rx lines high no more than 4 bit times between bytes in a packet. Keep the UART Tx/Rx lines high for at least 16 bit times before starting to send a new packet.

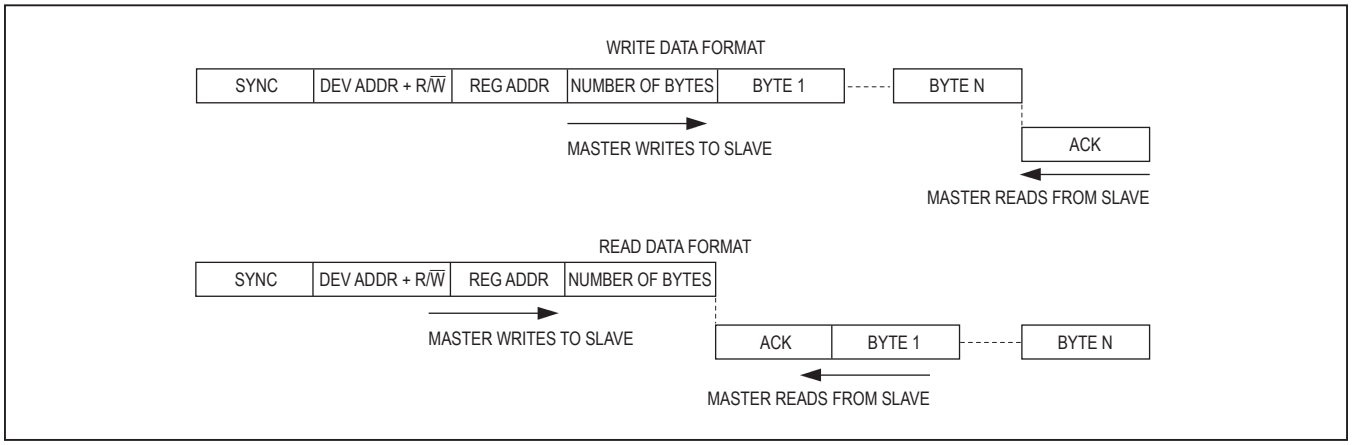


Figure 18. GMSL UART Protocol for Base Mode

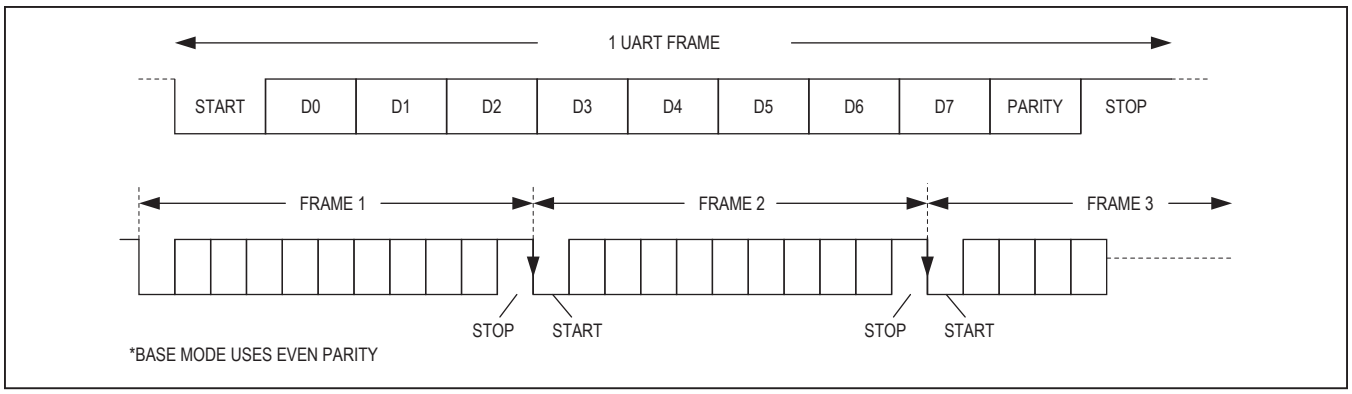


Figure 19. GMSL UART Data Format for Base Mode

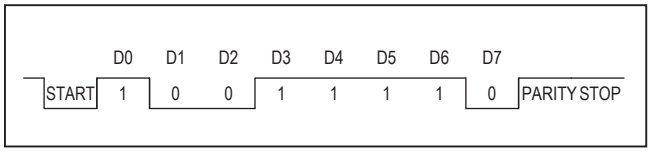


Figure 20. SYNC Byte (0x79)

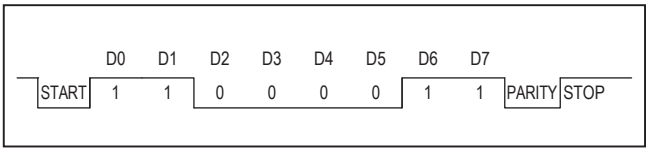


Figure 21. ACK Byte (0xC3)

As shown in Figure 22, the remote-side device converts packets going to or coming from the peripherals from UART format to I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C bit rate is the same as the UART bit rate.

Interfacing Command-Byte-Only I²C Devices with UART

The serializer/deserializer UART-to-I²C conversion can interface with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 23). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

UART Bypass Mode

In bypass mode, the serializer/deserializer ignore UART commands from the µC and the µC communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the serializer/deserializer registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one PCLKOUT period ± 10ns of jitter due to the asynchronous sampling of the UART signal by PCLKOUT. Set MS/HVEN = high to put the control channel into bypass mode. For applications with the µC connected to the deserializer, there is a 1ms wait time between setting MS/HVEN high and the bypass control channel being active. There is no delay time when switching to bypass mode when the µC is connected to the serializer. Do not send a logic-low value longer than 100µs to ensure proper GPO functionality. Bypass mode accepts bit rates down to 10kbps in either direction. See the *GPO/GPI Control* section for GPI functionality limitations. The control-channel data pattern should not be held low longer than 100µs if GPI control is used.

I²C Interface

In I²C-to-I²C mode, the deserializer's control-channel interface sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master and slave(s). A µC master initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer. When an I²C transaction starts on the local-side device's control-channel port, the remote-side device's control-channel port becomes an I²C master that interfaces with remote-side I²C perhipherals. The I²C master must accept clock stretching, which is imposed by the deserializer (holding SCL low). The SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL. Each transmission consists of a START condition (Figure 7) sent by a master, followed by the device's 7-bit slave address plus a R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

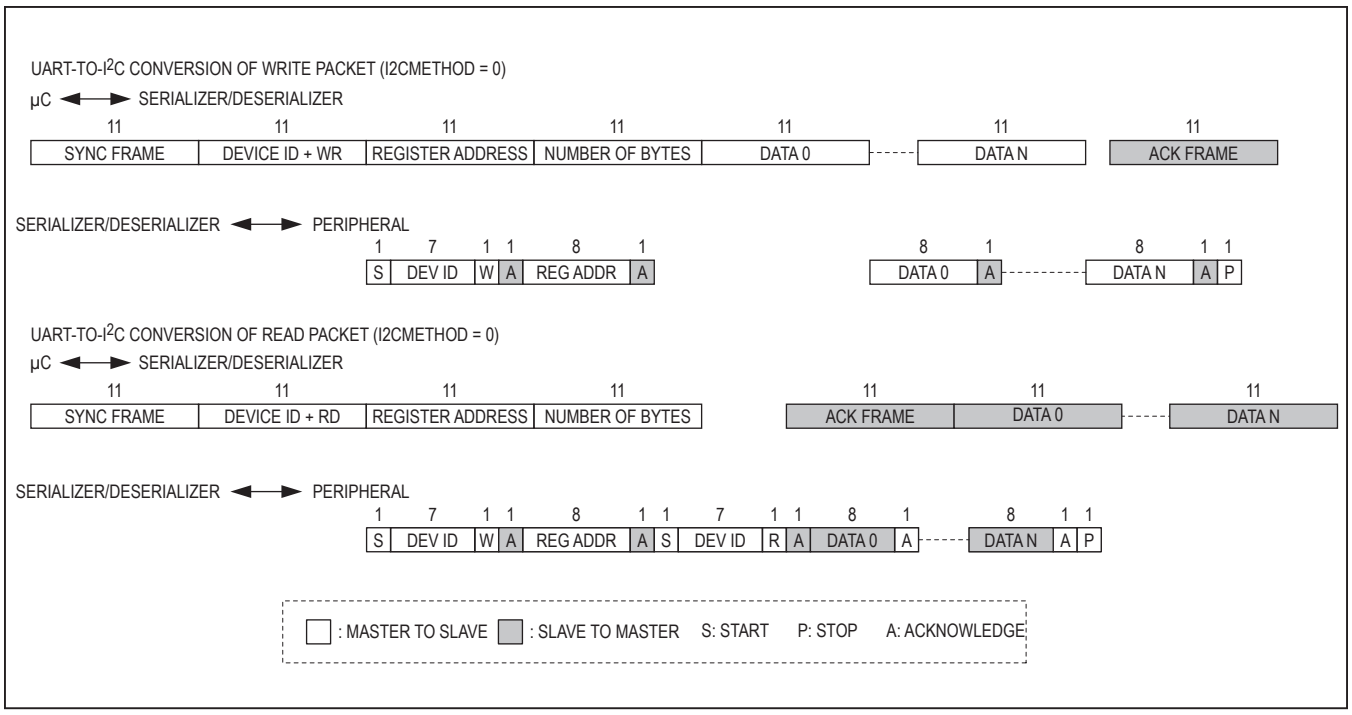


Figure 22. Format Conversion Between GMSL UART and I2C with Register Address (I2CMETHOD = 0)

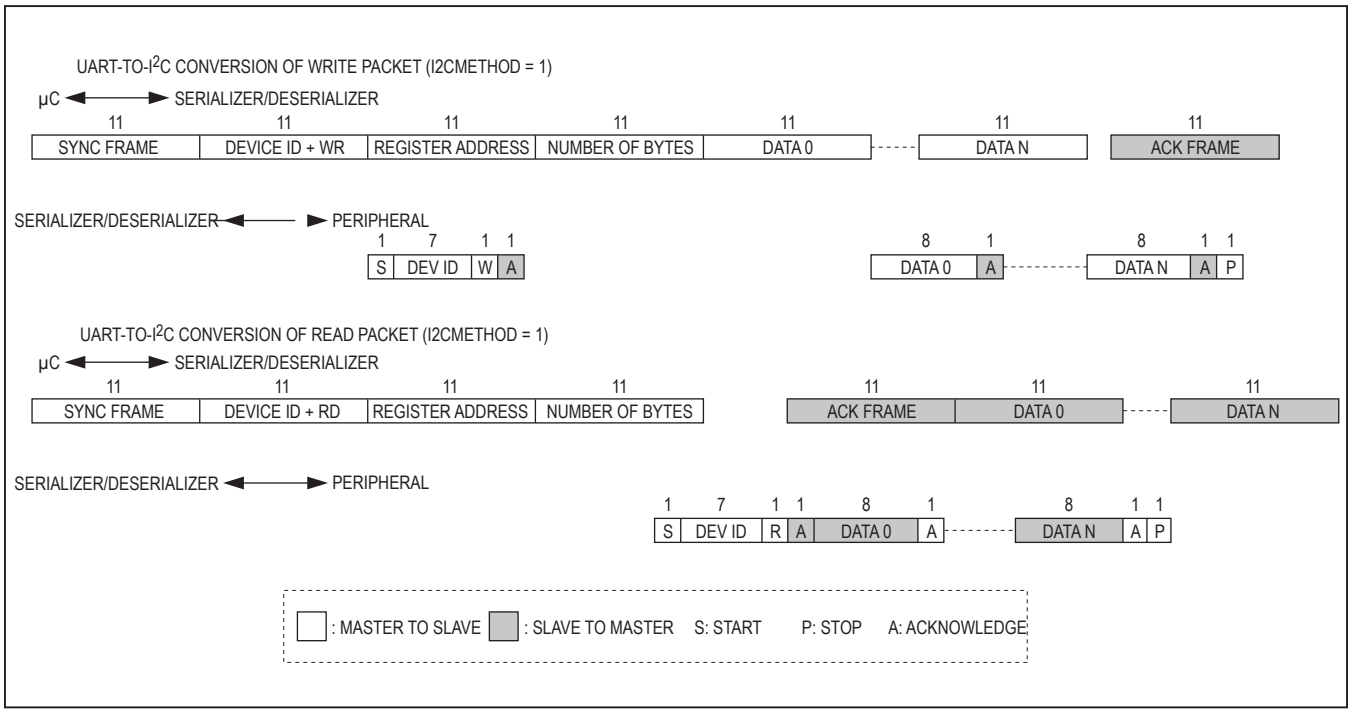


Figure 23. Format Conversion Between GMSL UART and I2C with Register Address (I2CMETHOD = 1)

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 24). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 25). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 26). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the slave device, the slave device generates the acknowledge bit because the slave device is the recipient. When the slave device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. The device generates an acknowledge even when the forward control channel is not active (not locked). To prevent acknowledge generation when the forward control channel is not active, set the I2CLOCACK bit low.

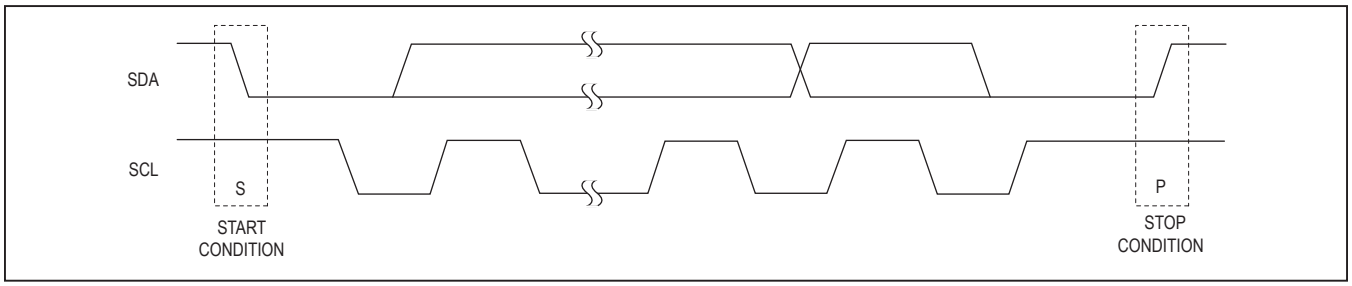


Figure 24. START and STOP Conditions

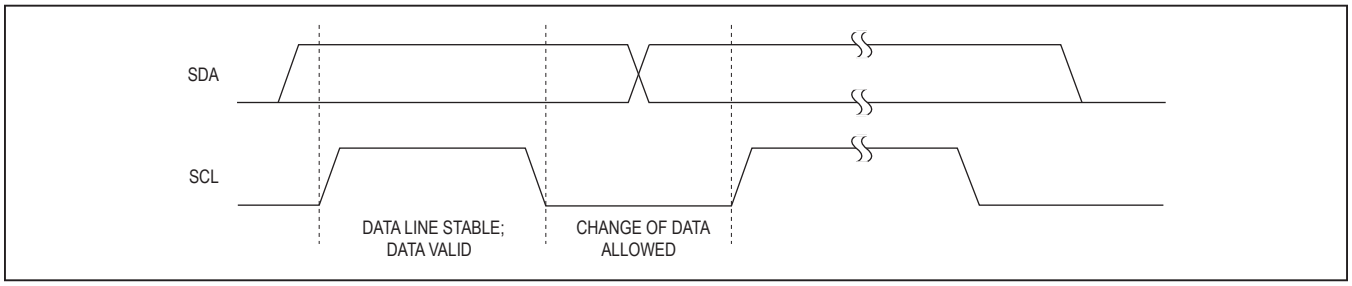


Figure 25. Bit Transfer

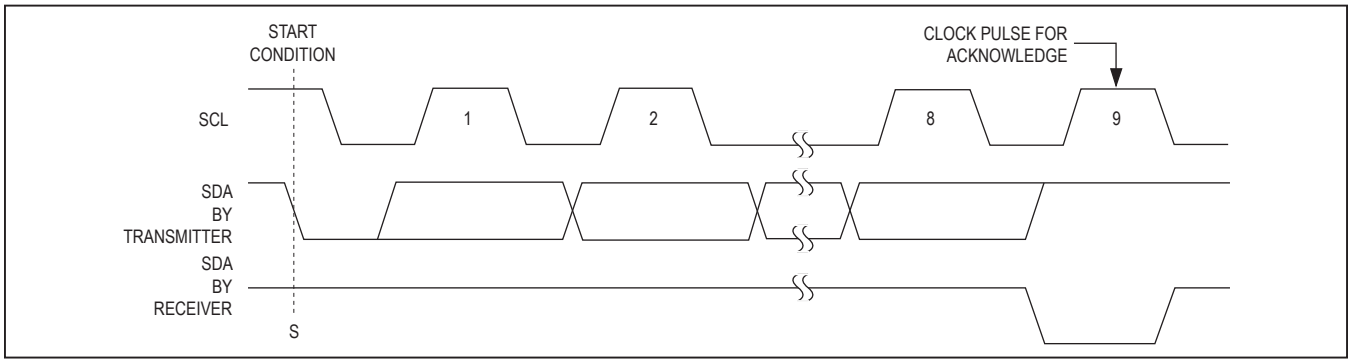


Figure 26. Acknowledge

Slave Address

The serializer/deserializer have a 7-bit-long slave address. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address is 100100X1 for read commands and 100100X0 for write commands. See Figure 27.

Bus Reset

The device resets the bus with the I^2C START condition for reads. When the R/$\overline{W}$ bit is set to 1, the serializer/deserializer transmit data to the master, thus the master is reading from the device.

Format for Writing

A write to the serializer/deserializer comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least one byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, the device takes no further action beyond storing the register address (Figure 28). Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address, and subsequent data bytes go into subsequent registers (Figure 29). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrement.

Format for Reading

The serializer/deserializer are read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 30). The master can now read consecutive bytes from the device, with the first data byte being read from the register address pointed by the previously written register address. Once the master sends a NACK, the device stops sending valid data.

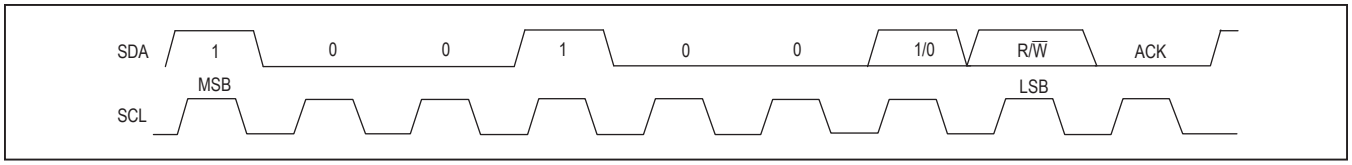


Figure 27. Slave Address

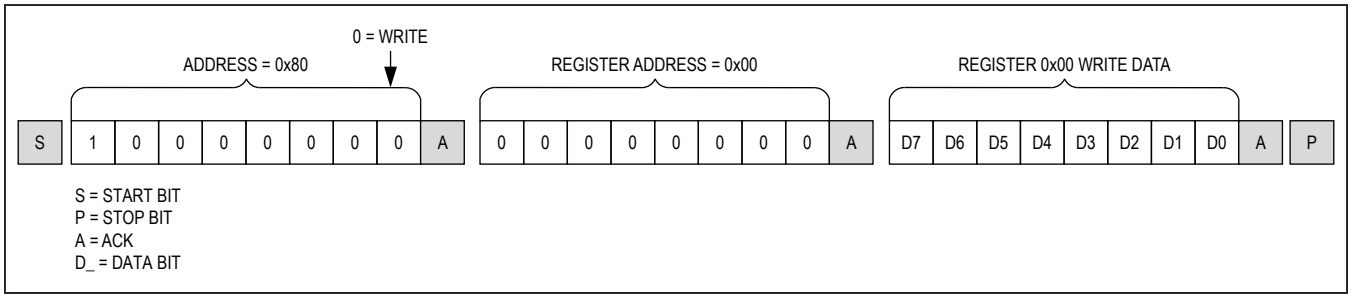


Figure 28. Format for I^2C Write

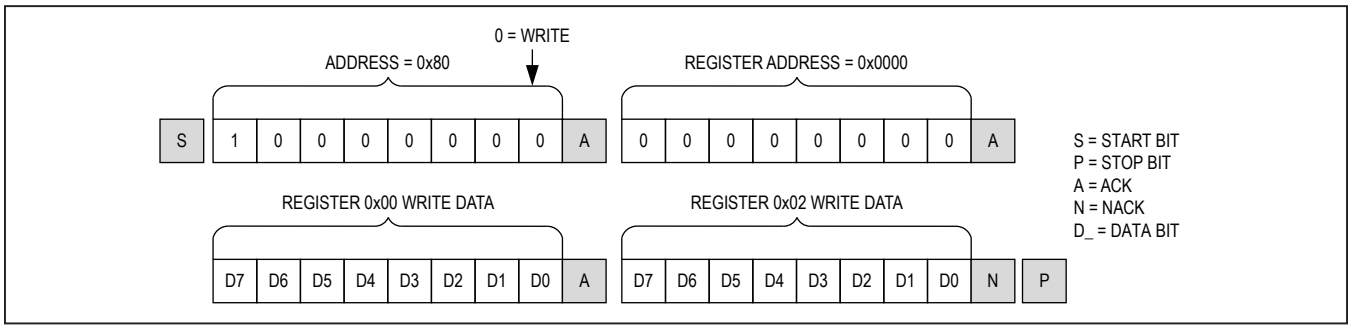


Figure 29. Format for Write to Multiple Registers

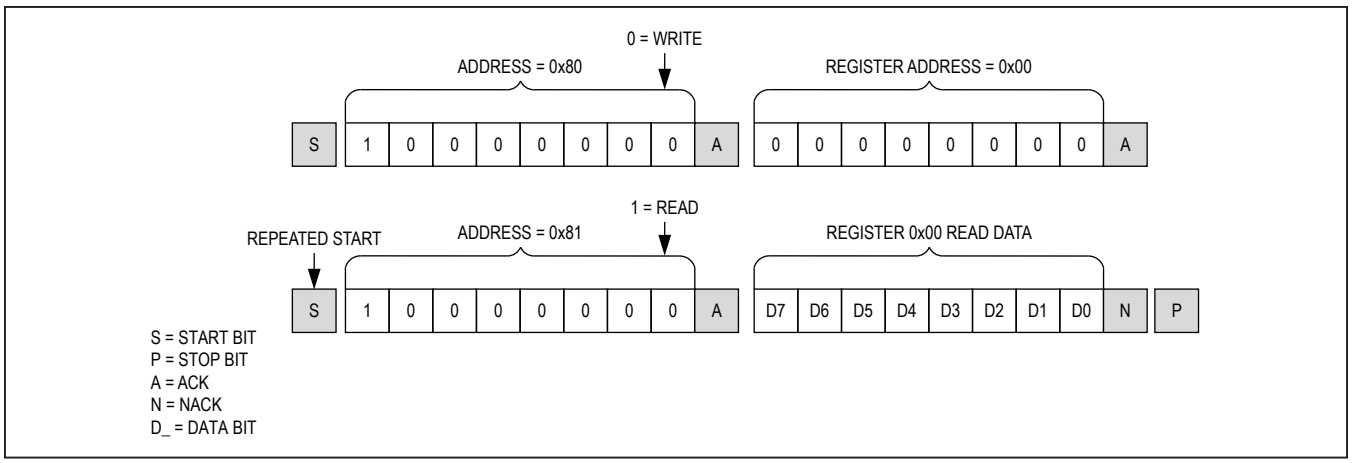


Figure 30. Format for I²C Read

Table 3. I²C Bit-Rate Ranges

LOCAL BIT RATE	REMOTE BIT-RATE RANGE	I2CMSTBT SETTING
f > 50kbps	Up to 1Mbps	Any
20kbps < f < 50kbps	Up to 400kbps	Up to 110
f < 20kbps	Up to 10kbps	000

I²C Communication with Remote-Side Devices

The deserializer supports I²C communication with a peripheral on the remote side of the communication link using SCL clock stretching. While multiple masters can reside on either side of the communication link, arbitration is not provided. The connected masters need to support SCL clock stretching. The remote-side I²C bit-rate range must be set according to the local-side I²C bit rate. Supported remote-side bit rates can be found in Table 3. Set the I2CMSTBT (register 0x0D) to set the remote I²C bit rate. If using a bit rate different than 400kbps, local- and remote-side I²C setup and hold times should be adjusted by setting the SLV_SH register settings on both sides.

I²C Address Translation

The deserializer supports I²C address translation for up to two device addresses. Use address translation to assign unique device addresses to peripherals with limited I²C addresses. Source addresses (address to translate from) are stored in registers 0x09 and 0x0B. Destination addresses (address to translate to) are stored in registers 0x0A and 0x0C.

Control-Channel Broadcast Mode

The deserializer supports broadcast commands to control multiple peripheral devices. Select an unused device address to use as a broadcast device address. Program the remote-side GMSL device to translate the broadcast device address (source address stored in registers 0x09, 0x0B) to the peripheral device address (destination address stored in registers 0x0A, 0x0C). Any commands sent to the broadcast address are sent to all designated peripherals, while commands sent to a peripheral's unique device address are sent to that particular device only.

GPO/GPI Control

GPO on the serializer follows GPI transitions on the deserializer. This GPO/GPI function can be used to transmit signals such as frame sync in a surround-view camera system. The GPI-to-GPO delay is 0.35ms (max). Keep the time between GPI transitions to a minimun 0.35ms. This includes transitions from the other deserializer in coax-splitter mode. Bit D4 of register 0x0E in the deserializer stores the GPI input state. GPO is low after power-up. The µC can set GPO by writing to the serializer SET_GPO register bit. Do not send a logic-low value on the deserializer RX/SDA input (UART mode) longer than 100µs in either base or bypass mode to ensure proper GPO/GPI functionality.

PRBS Test

The serializer includes a PRBS pattern generator that works with bit-error verification in the deserializer. To run the PRBS test, set PRBSEN = 1 (0x04, D5) in the deserializer and then in the serializer. To exit the PRBS test, set PRBSEN = 0 (0x04, D5) in the serializer.

Line Equalizer

The deserializer includes an adjustable line equalizer to further compensate cable attenuation at high frequencies. The cable equalizer has 11 selectable levels of compensation from 2.1dB to 13dB (Table 4). **The device powers up with the equalizer disabled.** To select other equalization levels, set the corresponding register bits in the deserializer (0x05 D[3:0]). Use equalization in the deserializer, together with preemphasis in the serializer, to create the most reliable link for a given cable.

Spread Spectrum

To reduce the EMI generated by transitions, the deserializer output is programmable for spread spectrum. If the serializer driving the deserializer has programmable spread spectrum, do not enable spread for both at the same time or their interaction will cancel benefits. The programmable spread-spectrum amplitudes are ±2% and ±4% (Table 5).

The deserializer includes a sawtooth divider to control the spread-modulation rate. Autodetection of the PCLKOUT operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV: 0x03, D[5:0]) allows the user to set a modulation frequency according to the PCLKOUT frequency. When ranges are manually selected, program the SDIV value for a fixed modulation frequency around 20kHz.

Manual Programming of the Spread-Spectrum Divider

The modulation rate for the deserializer relates to the PCLKOUT frequency as follows:

$$f_M = (1 + DRS)\frac{f_{PCLKOUT}}{MOD \times SDIV}$$

where:

f_M = Modulation frequency

DRS = DRS value (0 or 1)

$f_{PCLKOUT}$ = PCLKOUT frequency

MOD = Modulation coefficient given in Table 6

SDIV = 5-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 6, set SDIV to the maximum value.

Table 4. Cable Equalizer Boost Levels

BOOST SETTING (0x05 D[3:0])	TYPICAL BOOST GAIN (dB)
0000	2.1
0001	2.8
0010	3.4
0011	4.2
0100	5.2
0101	6.2
0110	7
0111	8.2
1000	9.4
1001	**10.7 Default***
1010	11.7
1011	13

Table 5. Parallel Output Spread

SS	SPREAD (%)
00	No spread spectrum. **Power-up default.**
01	±2% spread spectrum.
10	No spread spectrum.
11	±4% spread spectrum.

Table 6. Modulation Coefficients and Maximum SDIV Settings

SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT (dec)	SDIV UPPER LIMIT (dec)
4	208	15
2	208	30

Additional Error Detection and Correction

In default mode (additional error detection and correction disabled), data encoding/decoding is the same as in previous GMSL serializers/deserializers (parity only). At the serializer, the parallel input word is scrambled and a parity bit is added. The scrambled word is divided into 3 or 4 bytes (depending on the BWS setting), 8b/10b encoded, and then transmitted serially. At the deserializer, the same operations are performed in reverse order. The parity bit is used by the deserializer to find the word boundary and for error detection. Errors are counted in an error counter register and an error pin indicates errors.

The deserializer can use one of two additional error-detection/correction methods (selectable by register setting):

1) 6-bit cyclic redundancy check
2) 6-bit hamming code with 16-word interleaving

Cyclic Redundancy Check (CRC)

When CRC is enabled, the serializer adds 6 bits of CRC to the input data. This reduces the available bits in the input data word by 6, compared to the non-CRC case (see Table 1 for details). For example, 16 bits are available for input data instead of 22 bits when BWS = 0, and 24 bits instead of 30 bits when BWS = 1.

The CRC generator polynomial is $x^6 + x + 1$ (as used in the ITU-T G704 telecommunication standard).

The parity bit is still added when CRC is enabled, because it is used for word-boundary detection. When CRC is enabled, each data word is scrambled and then the 6-bit CRC and 1-bit parity are added before the 8b/10b encoding.

At the deserializer, the CRC code is recalculated. If the recalculated CRC code does not match the received CRC code, an error is flagged. This CRC error is reported to the error counter.

Hamming Code

Hamming code is a simple and effective error-correction code to detect and/or correct errors. The MAX9240A deserializer (when used with the MAX9271/MAX9273 GMSL serializers) uses a single-error correction/double-error detection per pixel hamming-code scheme.

The deserializer uses data interleaving for burst error tolerance. Burst errors up to 11 consecutive bits on the serial link are corrected and burst errors up to 31 consecutive bits are detected.

Hamming code adds overhead similar to CRC. See Table 1 for details regarding the available input word size.

HS/VS Encoding and/or Tracking

HS/VS encoding by a GMSL serializer allows horizontal and vertical synchronization signals to be transmitted while conserving pixel data bandwidth. With HS/VS encoding enabled, 10-bit pixel data with a clock up to 100MHz can be transmitted using one video pixel of data per HS/VS transition vs. 8-bit data with a clock up to 100MHz without HS/VS encoding. The deserializer performs HS/VS decoding, tracks the period of the HS/VS signals, and uses voting to filter HS/VS bit errors. When using HS/VS encoding, use a minimum HS/VS low-pulse duration of two PCLKOUT cycles when DBL = 0 on the deserializer. When DBL = 1, use a minimum HS/VS low-pulse duration of five PCLKOUT cycles and a minimum high-pulse duration of two PCLKOUT cycles. When using hamming code with HS/VS encoding, do not send more than two transitions every 16 PCLKOUT cycles.

When the serializer uses double-input mode (DBL = 1), the active duration, plus the blanking duration of HS or VS signals, should be an even number of PCLKOUT cycles. When DBL = 1 in the serializer and DBL = 0 in the deserializer, two pixel clock cycles of HS/VS at the serializer input are output at the HS0/VS0 and HS1/VS1 output of the deserializer in one cycle. The first cycle of HS/VS goes out of HS0/VS0 and the second cycle goes out of HS1/VS1. HS1 and VS1 are not used when HVEN = 0.

If HS/VS tracking is used without HS/VS encoding, use DOUT0 for HSYNC and DOUT1 for VSYNC. In this case, if DBL values on the serializer/deserializer are different, set the UNEQDBL register bit in the deserializer to 1. If the serializer and deserializer have unequal DBL settings and HVEN = 0, then HS/VS inversion should only be used on the side that has DBL = 1. HS/VS encoding sends packets when HSYNC or VSYNC is low; use HS/VS inversion register bits if input HSYNC and VSYNC signals use an active-low convention in order to send data packets during the inactive pixel clock periods.

Serial Input

The device can receive serial data from two kinds of cables: 100Ω twisted pair and 50Ω coax (contact the factory for devices compatible with 75Ω cables).

Coax-Mode Splitter

In coax mode, OUT+ and OUT- of the serializer are active. This enables use as a 1:2 splitter (Figure 31). In coax mode, connect OUT+ to IN+ of the deserializer. Connect OUT- to IN- of the second deserializer. Control-channel data is broadcast from the serializer to both deserializers and their attached peripherals. Assign a unique address

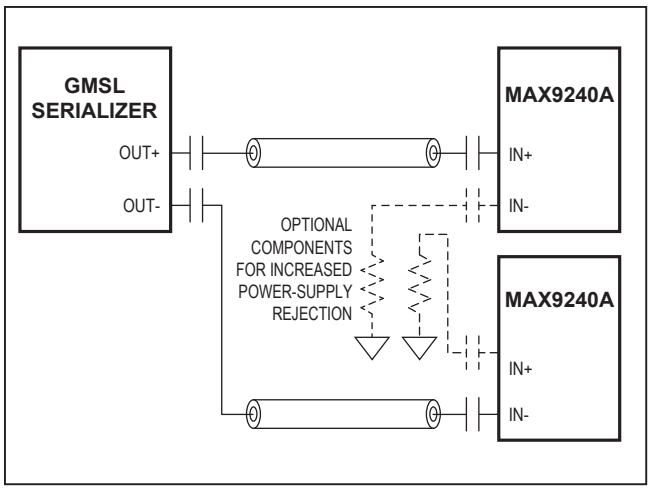


Figure 31. 2:1 Coax-Mode Splitter Connection Diagram

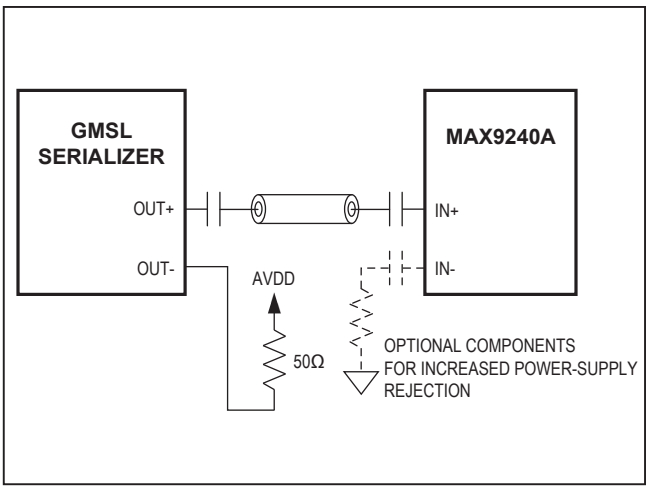


Figure 32. Coax-Mode Connection Diagram

to send control data to one deserializer. Leave all unused IN_ pins unconnected, or connect them to ground through 50Ω and a capacitor for increased power-supply rejection. If OUT- is not used, connect OUT- to AVDD through a 50Ω resistor (Figure 32). When there are µCs at the serializer, and at each deserializer, only one µC can communicate at a time. Disable one splitter control-channel link to prevent contention. Use the DIS_REV_P or DIS_REV_N register bits to disable a control-channel link.

Cable Type Configuration Input (CX/TP)

CX/TP determines the power-up state of the serial input. In coax mode, CX/TP also determines which coax input is active, along with the default device address (Table 7). These functions can be changed after power-up by writing to the appropriate register bits.

Sleep Mode

The deserializer includes a sleep mode to reduce power consumption. The device enters or exits sleep mode by a command from a local µC or a remote µC using the control channel. Set the SLEEP bit to 1 to initiate sleep mode. The serializer sleeps immediately after setting its SLEEP = 1. The deserializer sleeps after serial link inactivity or 8ms (whichever arrives first) after setting its SLEEP = 1. To wake up from the local side, send an arbitrary control-channel command to the deserializer, wait 5ms for the chip to power up, and then write 0 to the SLEEP register bit to make the wake-up permanent. To wake up from the remote side, enable serialization. To deserializer detects the activity on the serial link and then when it locks, it automatically sets its SLEEP register bit to 0.

Table 7. Configuration Input Map

CX/TP	FUNCTION
High	Coax+ input. Device address 0x90.
Mid	Coax- input. Device address 0x92.
Low	Twisted-pair input. Device address 0x90.

Power-Down Mode

The deserializer has a power-down mode that further reduces power consumption compared to sleep mode. Set $\overline{\text{PWDN}}$ low to enter power-down mode. In power-down mode, the outputs of the device remain in high impedance. Entering power-down resets the device's registers. Upon exiting power-down, the state of external pins GPIO1/BWS, GPIO0/DBL, CX/TP, I2CSEL, LCCEN, RX/SDA/EDC, TX/SCL/ES, and MS/HVEN are latched.

Configuration Link

The control channel can operate in a low-speed mode called configuration link in the absence of a clock input. This allows a microprocessor to program configuration registers before starting the video link. An internal oscillator provides the clock for the configuration link. Set CLINKEN = 1 on the serializer to enable the configuration link. The configuration link is active until the video link is enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Link Startup Procedure

Table 8 lists the startup procedure for video-display applications. Table 9 lists the startup procedure for image-sensing applications. The control channel is available after the video link or the configuration link is established. If the deserializer powers up after the serializer, the control channel becomes unavailable until 2ms after power-up.

Table 8. Startup Procedure for Video-Display Applications

NO.	µC	SERIALIZER	DESERIALIZER
—	µC connected to serializer.	Sets all configuration inputs. If any configuration inputs are available on one end of the link but not on the other, always connects that configuration input low.	Sets all configuration inputs. If any configuration inputs are available on one end of the link but not on the other, always connects that configuration input low.
1	Powers up.	Powers up and loads default settings.	Powers up and loads default settings.
2	Enables configuration link by setting CLINKEN = 1 (if not enabled automatically) and gets an acknowledge. Waits for link to be established (~3ms).	Establishes configuration link.	Locks to configuration link signal.
3	Writes one link configuration bit (DRS, BWS, or EDC) in the deserializer and gets an acknowledge.	—	Configuration changed from default settings (loss-of-lock can occur when BWS or EDC changes).
4	Writes corresponding serializer link configuration bit and gets an acknowledge.	Configuration changed from default settings.	Relocks to configuration link signal.
5	Waits for link to be established (~3ms) and then repeats steps 3 and 4 until all serial link bits are configured.	—	—
6	Writes remaining configuration bits in the serializer/deserializer and gets an acknowledge.	Configuration changed from default settings.	Configuration changed from default settings.
7	Enables video link by setting SEREN = 1 and gets an acknowledge. Waits for link to be established (~3ms).	Begins serializing data.	Locks to serial link signal and begins deserializing data.

Table 9. Startup Procedure for Image-Sensing Applications

NO.	µC	SERIALIZER	DESERIALIZER
—	µC connected to deserializer.	Sets all configuration inputs. If any configuration inputs are available on one end of the link but not on the other, always connects that configuration input low.	Sets all configuration inputs. If any configuration inputs are available on one end of the link but not on the other, always connects that configuration input low.
1	Powers up.	Powers up and loads default settings. Establishes serial link.	Powers up and loads default settings. Locks to serial link signal.
3	Writes deserializer configuration bits and gets an acknowledge.	—	Configuration changed from default settings (loss-of-lock can occur).
4	Writes serializer configuration bits. Cannot get an acknowledge (or gets a dummy acknowledge) if loss-of-lock occurred.	Configuration changed from default settings.	Relocks the serial link signal.
5	Enables video link by setting SEREN = 1 (if not enabled automatically). Cannot get an acknowledge (or gets a dummy acknowledge) if loss-of-lock occurred. Waits for link to be established (~3ms).	Begins serializing data.	Locks to serial link signal and begins deserializing data.

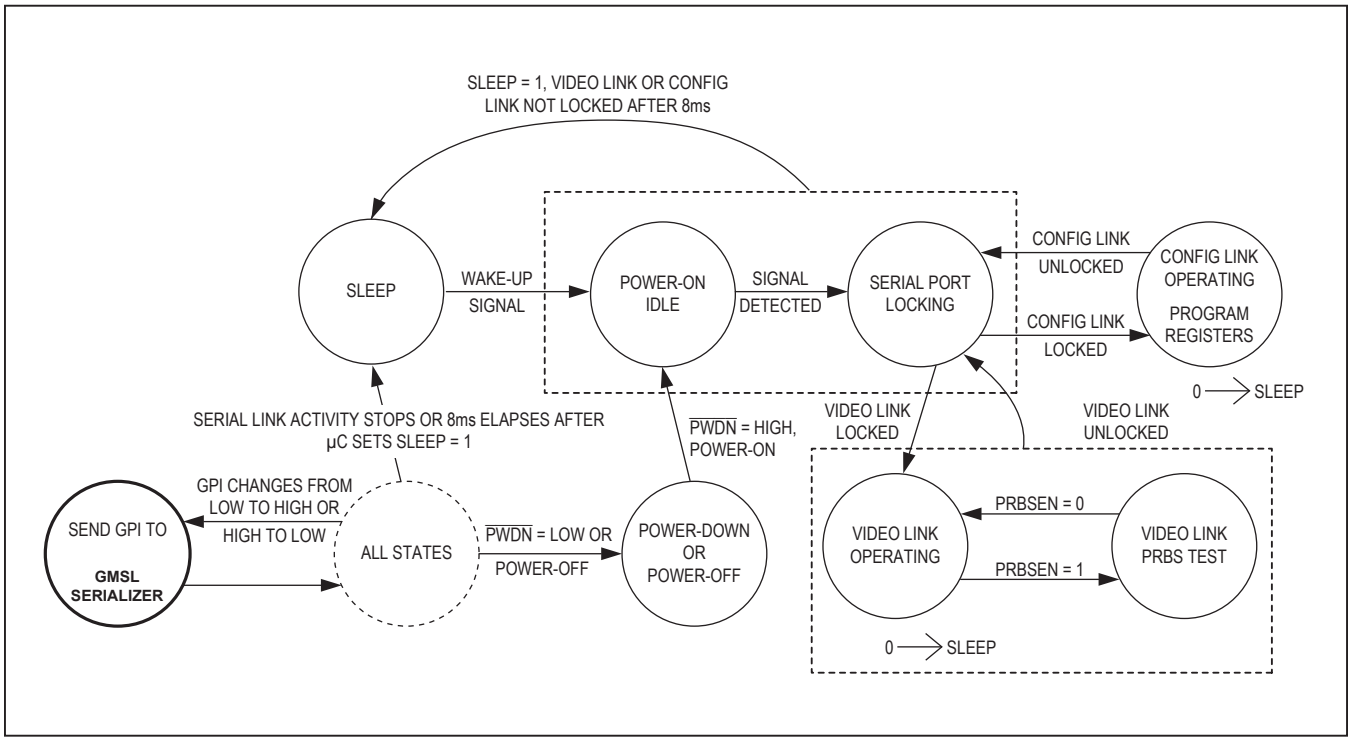


Figure 33. State Diagram, Remote Microcontroller Application

Applications Information

Error Checking

The deserializer checks the serial link for errors and stores the number of detected and corrected errors in the 8-bit registers, DETERR (0x10) and CORRERR (0x12). If a large number of 8b/10b errors are detected within a short duration (error rate > 1/4), the deserializer loses lock and stops the error counter. The deserializer then attempts to relock to the serial data. DETERR and CORRERR reset upon successful video link lock, successful readout of their respective registers (through µC), or whenever autoerror reset is enabled. The deserializer uses a separate PRBS register during the internal PRBS test, and DETERR and CORRERR are reset to 0x00.

$\overline{ERR}$ Output

The deserializer has an open-drain $\overline{ERR}$ output. This output asserts low whenever the number of detected/corrected errors exceeds their respective error thresholds during normal operation, or when at least one PRBS error is detected during PRBS test. $\overline{ERR}$ deasserts high whenever DETERR and CORRERR reset, due to DETERR/CORRERR readout, video link lock, or autoerror reset.

Autoerror Reset

The default method to reset errors is to read the respective error registers in the deserializer (0x10, 0x12, and 0x13). Autoerror reset clears the error counters DETERR/CORRERR and the $\overline{ERR}$ output ~1µs after $\overline{ERR}$ goes low. Autoerror reset is disabled on power-up. Enable autoerror reset through AUTORST (0x08, D2). Autoerror reset does not run when the device is in PRBS test mode.

Dual µC Control

Usually systems have one µC to run the control channel, located on the serializer side for video-display applications or on the deserializer side for image-sensing applications. However, a µC can reside on each side simultaneously and trade off running the control channel. In this case, each µC can communicate with the serializer and deserializer and any peripheral devices.

Contention occurs if both µCs attempt to use the control channel at the same time. It is up to the user to prevent this contention by implementing a higher-level protocol. In addition, the control channel does not provide arbitration between I^2C masters on both sides of the link. An acknowledge frame is not generated when communication fails due to contention. If communication across the serial link is not required, the µCs can disable the forward and reverse control channel using the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the serializer/deserializer. Communication across the serial link is stopped and contention between µCs cannot occur.

As an example of dual µC use in an image-sensing application, the serializer can be in sleep mode and waiting for wake-up by the µC on the deserializer side. After wake-up, the serializer-side µC assumes master control of the serializer's registers.

Changing the Clock Frequency

It is recommended that the serial link be enabled after the video clock ($f_{PCLKOUT}$) and the control-channel clock (f_{UART}/f_{I2C}) are stable. When changing the clock frequency, stop the video clock for 5µs, apply the clock at the new frequency, then restart the serial link or toggle SEREN. On-the-fly changes in clock frequency are possible if the new frequency is immediately stable and without glitches. The reverse control channel remains unavailable for 350µs after serial link start or stop. When using the UART interface, limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps then at 100kbps for reduction ratios of 3 and 3.333, respectively.

Fast Detection of Loss-of-Synchronization

A measure of link quality is the recovery time from loss-of-synchronization. The host can be quickly notified of loss-of-lock by connecting the deserializer's LOCK output to the GPI input. If other sources use the GPI input, such as a touch-screen controller, the µC can implement a routine to distinguish between interrupts from loss-of-sync and normal interrupts. Reverse control-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the GMSL link. LOCK asserts for video link only and not for the configuration link.

Providing a Frame Sync (Camera Applications)

The GPI/GPO provides a simple solution for camera applications that require a frame sync signal from the ECU (e.g., surround-view systems). Connect the ECU frame sync signal to the GPI input, and connect the GPO output to the camera frame sync input. GPI/GPO have a typical delay of 275µs. Skew between multiple GPI/GPO channels is 115µs (max). If a lower skew signal is required, connect the camera's frame sync input to one of the GMSL deserializer's GPIOs and use an I²C broadcast write command to change the GPIO output state. This has a maximum skew of 1.5µs.

Software Programming of the Device Addresses

Both the serializer and the deserializer have programmable device addresses. This allows multiple GMSL devices, along with I²C peripherals, to coexist on the same control channel. The serializer device address is in register 0x00 of each device, while the deserializer device address is in register 0x01 of each device. To change a device address, first write to the device whose address changes (register 0x00 of the serializer for serializer device address change, or register 0x01 of the deserializer for deserializer device address change). Then write the same address into the corresponding register on the other device (register 0x00 of the deserializer for serializer device address change, or register 0x01 of the serializer for deserializer device address change).

Three-Level Configuration Inputs

CX/TP is a three-level input that controls the serial-interface configuration and power-up defaults. Connect CX/TP through a pullup resistor to IOVDD to set a high level, a pulldown resistor to GND to set a low level, or open to set a midlevel. For digital control, use three-state logic to drive the three-level logic input.

Configuration Blocking

The deserializer can block changes to registers. Set CFGBLOCK to make all registers read only. Once set, the registers remain blocked until the supplies are removed or until $\overline{\text{PWDN}}$ is low.

Compatibility with other GMSL Devices

The MAX9240A deserializer is designed to pair with the MAX9271/MAX9273 serializers, but interoperate with any GMSL serializers. See the Table 10 for operating limitations.

GPIOs

The deserializer has two open-drain GPIOs available when not used as configuration inputs. GPIO1OUT and GPIO0OUT (0x0E, D3 and D1) set the output state of the GPIOs. Setting the GPIO output bits to 0 pulls the output low, while setting the bits to 1 leaves the output undriven and pulled high through internal/external pullup resistors. The GPIO input buffers are always enabled. The input states are stored in GPIO1 and GPIO0 (0x0E, D2 and D0). Set GPIO1OUT/GPIO0OUT to 1 when using GPIO1/GPIO0 as an input.

Staggered Parallel Outputs

The deserializer staggers the parallel data outputs to reduce EMI and noise. Staggering outputs also reduces the power-supply transient requirements. By default, the deserializer staggers outputs according to Table 11. Disable output staggering through the DISSTAG bit (0x08, D3).

Table 10. MAX9240A Feature Compatibility

MAX9240A FEATURE	GMSL DESERIALIZER
HSYNC/VSYNC encoding	If feature not supported in the serializer, must be turned off in the deserializer.
Hamming-code error correction	If feature not supported in the serializer, must be turned off in the deserializer.
I²C-to-I²C	If feature not supported in the serializer, must use UART-to-I²C or UART-to-UART.
CRC error detection	If feature not supported in the serializer, must be turned off in the deserializer.
Double output	If feature not supported in the serializer, the data is inputted as a single word at 1/2 the output frequency.
Coax	If feature not supported in the deserializer, must connect unused serial output through 200nF and 50Ω in series to AVDD and set the reverse control-channel amplitude to 100mV.
I²S encoding	If feature is supported in the serializer, must disable I²S in the serializer.

Table 11. Staggered Output Delay

OUTPUT	OUTPUT DELAY RELATIVE TO DOUT0 (ns)	
	DISSTAG = 0	DISSTAG = 1
DOUT0–DOUT5, DOUT21, DOUT22	0	0
DOUT6–DOUT10, DOUT23, DOUT24	0.5	0
DOUT11–DOUT15	1	0
DOUT16–DOUT20	1.5	0
PCLKOUT	0.75	0

Table 12. Double-Function Configuration

LCCEN	GPIO0/DBL FUNCTION	GPIO1/BWS FUNCTION	MS/HVEN FUNCTION	RX/SDA/EDC FUNCTION	TX/SCL/ES FUNCTION
High	Functions as GPIO	Functions as GPIO	MS input (low = base mode, high = bypass mode)	UART/I²C input/output	UART/I²C input/output
Low	DBL input (low = single input, high = double input)	BWS input (low = 24-bit mode, high = 32-bit mode)	HVEN input (low = HS/VS encoding disabled, high = HS/VS encoding enabled)	EDC input (low = error detection/ correction disabled, high = error detection/ correction enabled)	ES input (low = valid DOUT_ on rising edge of PCLKOUT, high = valid DOUT_ on falling edge of PCLKOUT)

Table 13. Line Fault Mapping

REGISTER ADDRESS	BITS	NAME	VALUE	LINE FAULT TYPE
0x14	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage
			01	Negative cable wire shorted to ground
			10	Normal operation
			11	Negative cable wire disconnected
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage
			01	Positive cable wire shorted to ground
			10	Normal operation
			11	Positive cable wire disconnected

Local Control-Channel Enable (LCCEN)

The deserializer provides inputs for limited configuration of the device when a µC is not connected. Connect LCCEN = low upon power-up to disable the local control channel and enable the double-function configuration inputs (Table 12). All input configuration states are latched at power-up.

Line-Fault Detection

The line-fault detector in the deserializer monitors for line failures such as short to ground, short to battery, and open link for system fault diagnosis. Figure 4 shows the required external resistor connections. $\overline{LFLT}$ goes low when a line fault is detected and $\overline{LFLT}$ goes high when the line returns to normal. The line-fault failure type is stored in 0x14 D[3:0] of the deserializer. Filter $\overline{LFLT}$ with the µC to reduce the detector's susceptibility to temporary ground shifts. The fault detector threshold voltages are referenced to the deserializer ground. Additional passive components set the DC level of the cable (Figure 4). If the serializer and GMSL deserializer grounds are different, the link DC voltage during normal operation can vary and cross one of the fault detection thresholds.

For the fault-detection circuit, select the resistor's power rating to handle a short to the battery. In coax mode, leave the unused line-fault inputs unconnected. To detect the short-together case, refer to *Application Note 4709*: MAX9259 GMSL Line-Fault Detection. Table 13 lists the mapping for line-fault types.

Internal Input Pulldowns

The control and configuration inputs, except three-level inputs, include a pulldown resistor to GND. External pulldown resistors are not needed.

Choosing I²C/UART Pullup Resistors

The I²C and UART open-drain lines require a pullup resistor to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise may be required when choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *AC Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time t_R = 0.85 x R_{PULLUP} x C_{BUS} < 300ns. The waveforms are not recognized if the transition time becomes too slow. The deserializer supports I²C/UART rates up to 1Mbps (UART-to-I²C mode) and 400kbps (I²C-to-I²C mode).

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Capacitors at the serializer output and at the deserializer input are needed for proper link operation and to provide protection if either end of the cable is shorted to a battery. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is fixed, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML/coax receiver termination resistor (R_{TR}), the CML/coax driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant, for four equal-value series capacitors, is (C x (R_{TD} + R_{TR}))/4. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω differential and 50Ω single-ended). This leaves the capacitor selection to change the system time constant. Use 0.22µF or larger high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The deserializer uses an AVDD and DVDD of 1.7V to 1.9V. All inputs and outputs, except for the serial input, derive power from an IOVDD of 1.7V to 3.6V that scales with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability. The GPI-to-GPO delay is 0.35ms (max). Keep the time between GPI transmissions to a minimum 0.35ms.

Power-Supply Table

Power-supply currents shown in the *Electrical Characteristics* table are the sum of the currents from AVDD, DVDD, and IOVDD. Typical currents from the individual power supplies are shown in Table 14.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Coax cables typically have a characteristic impedance of 50Ω (contact the factory for 75Ω operation). Table 15 lists the suggested cables and connectors used in the GMSL link.

Table 14. Typical Power-Supply Currents (Using Worst-Case Input Pattern)

PCLK (MHz)	AVDD (mA)	DVDD (mA)	IOVDD (mA)
25	25.1	9.2	10.3
50	33.3	13.7	13.3

Table 15. Suggested Connectors and Cables for GMSL

SUPPLIER	CONNECTOR	CABLE	TYPE
Rosenberger	59S2AX-400A5-Y	RG174	Coax
JAE	MX38-FF	A-BW-Lxxxxx	STP
Nissei	GT11L-2S	F-2WME AWG28	STP
Rosenberger	D4S10A-40ML5-Z	Dacar 538	STP

Board Layout

Separate the LVCMOS logic signals and CML/coax high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/coax, and LVCMOS logic signals. Layout PCB traces close to each other for a 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer. Use a 50Ω trace for the single-ended output when driving coax.

Route the PCB traces for differential CML channel in parallel to maintain the differential characteristic impedance. Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

ESD Protection

ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial link inputs are rated for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 34). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 35). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 36).

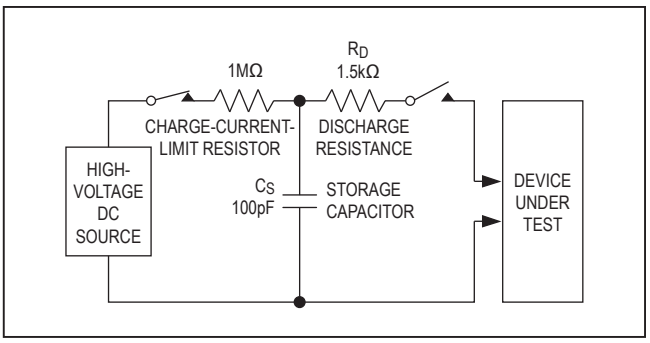


Figure 34. Human Body Model ESD Test Circuit

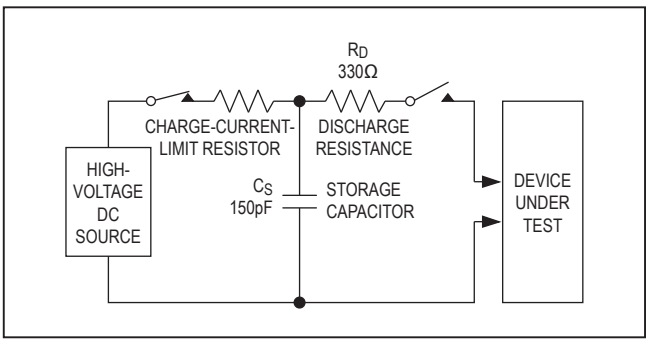


Figure 35 IEC 61000-4-2 Contact Discharge ESD Test Circuit

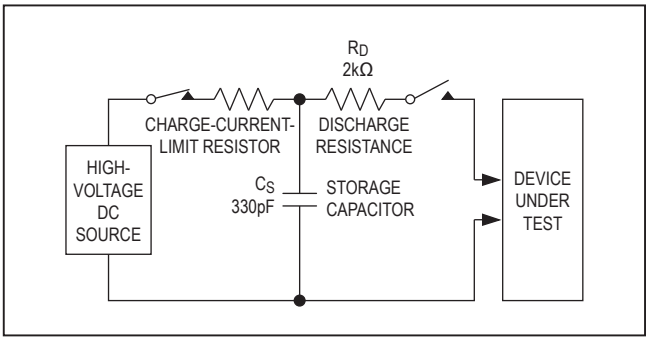


Figure 36. ISO 10605 Contact Discharge ESD Test Circuit

Table 16. Register Table

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address.	1000000
	D0	—	0	Reserved.	0
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address. Default address is determined by the state of the CX/TP input (Table 8).	1001000, 1001001
	D0	CFGBLOCK	0	Normal operation.	0
			1	Registers 0x00 to 0x1F are read only.	
0x02	D[7:6]	SS	00	No spread spectrum.	00
			01	±2% spread spectrum.	
			10	No spread spectrum.	
			11	±4% spread spectrum.	
	D[5:4]	—	01	Reserved.	01
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock.	11
			01	25MHz to 50MHz pixel clock.	
			10	Do not use.	
			11	Automatically detect the pixel clock range.	
	D[1:0]	SRNG	00	0.5Gbps to 1Gbps serial-data rate.	11
			01	1Gbps to 1.5Gbps serial-data rate.	
			10	Automatically detect serial-data rate.	
			11	Automatically detect serial-data rate.	
0x03	D[7:6]	AUTOFM	00	Calibrate spread-modulation rate only once after locking.	00
			01	Calibrate spread-modulation rate every 2ms after locking.	
			10	Calibrate spread-modulation rate every 16ms after locking.	
			11	Calibrate spread-modulation rate every 256ms after locking.	
	D5	—	0	Reserved.	0
	D[4:0]	SDIV	00000	Autocalibrate sawtooth divider.	00000
			XXXXX	Manual SDIV setting. See the *Manual Programming of the Spread-Spectrum Divider* section.	

Table 16. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x04	D7	LOCKED	0	LOCK output is low.	0 (read only)
			1	LOCK output is high.	
	D6	OUTENB	0	Enable PCLKOUT, DOUT_ and I2S outputs.	0
			1	Disable PCLKOUT, DOUT_ and I2S outputs.	
	D5	PRBSEN	0	Disable PRBS test.	0
			1	Enable PRBS test.	
	D4	SLEEP	0	Normal mode.	0
			1	Activate sleep mode.	
	D[3:2]	INTTYPE	00	Local control channel uses I²C when I2CSEL = 0.	01
			01	Local control channel uses UART when I2CSEL = 0.	
			10, 11	Local control channel disabled.	
	D1	REVCCEN	0	Disable reverse control channel to serializer (sending).	1
			1	Enable reverse control channel to serializer (sending).	
	D0	FWDCCEN	0	Disable forward control channel from serializer (receiving).	1
			1	Enable forward control channel from serializer (receiving).	
0x05	D7	I2CMETHOD	0	I²C conversion sends the register address when converting UART to I²C.	0
			1	Disable sending of I²C register address when converting UART to I²C (command-byte-only mode).	
	D6	DCS	0	Normal parallel output driver current.	0
			1	Boosted parallel output driver current.	
	D5	HVTRMODE	0	Partial periodic HS/VS tracking.	1
			1	Full periodic HS/VS tracking.	
	D4	ENEQ	**0**	**Equalizer disabled. Power-up default.**	0
			1	Equalizer enabled.	
	D[3:0]	EQTUNE	0000	2.1dB equalizer-boost gain.	1001
			0001	2.8dB equalizer-boost gain.	
			0010	3.4dB equalizer-boost gain.	
			0011	4.2dB equalizer-boost gain.	
			0100	5.2dB equalizer-boost gain.	
			0101	6.2dB equalizer-boost gain.	
			0110	7dB equalizer-boost gain.	
			0111	8.2dB equalizer-boost gain.	
			1000	9.4dB equalizer-boost gain.	
			1001	10.7dB equalizer-boost gain. **Power-up default.**	
			1010	11.7dB equalizer-boost gain.	
			1011	13dB equalizer-boost gain.	
			11XX	Do not use.	

Table 16. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x06	D[7:0]	—	00000010	Reserved.	00000010
0x07	D7	DBL	0	Single-input mode. **Power-up default when LCCEN = high or GPIO0/DBL = low.**	0, 1
			1	Double-input mode. **Power-up default when LCCEN = low and GPIO0/DBL = high.**	
	D6	DRS	0	High data-rate mode.	0
			1	Low data-rate mode.	
	D5	BWS	0	24-bit mode. **Power-up default when LCCEN = high or GPIO1/BWS = low.**	0, 1
			1	32-bit mode. Power-up default when LCCEN = low and GPIO1/BWS = high.	
	D4	ES	0	Output data valid on rising edge of PCLKOUT. **Power-up default when LCCEN = high or TX/SCL/ES = low.** Do not change this value while the pixel clock is running.	0, 1
			1	Output data valid on falling edge of PCLKOUT. **Power-up default when LCCEN = low and TX/SCL/ES = high.** Do not change this value while the pixel clock is running.	
	D3	HVTRACK	0	HS/VS tracking disabled. **Power-up default when LCCEN = high or MS/HVEN = low.**	0, 1
			1	HS/VS tracking enabled. **Power-up default when LCCEN = low and MS/HVEN = high.**	
	D2	HVEN	0	HS/VS encoding disabled. **Power-up default when LCCEN = high or MS/HVEN = low.**	0, 1
			1	HS/VS encoding enabled. **Power-up default when LCCEN = low and MS/HVEN = high.**	
	D[1:0]	EDC	00	1-bit parity error detection (GMSL compatible). **Power-up default when LCCEN = high or RX/SDA/EDC = low.**	00, 10
			01	6-bit CRC error detection.	
			10	6-bit hamming code (single-bit error correct, double-bit error detect) and 16-word interleaving. **Power-up default when LCCEN = low and RX/SDA/EDC = high.**	
			11	Do not use.	

Table 16. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x08	D7	INVVS	0	No VS or DOUT0 inversion.	0
			1	Invert VS when HVEN = 1. Invert DOUT0 when HVEN = 0. Do not use if DBL = 0 in the deserializer and DBL = 1 in the serializer.	
	D6	INVHS	0	No HS or DOUT1 inversion.	0
			1	Invert HS when HVEN = 1. Invert DOUT1 when HVEN = 0. Do not use if DBL = 0 in the deserializer and DBL = 1 in the serializer.	
	D5	—	0	Reserved.	0
	D4	UNEQDBL	0	Serializer DBL is not the same as deserializer.	0
			1	Serializer DBL same as deserializer (set to 1 only when HVEN = 0 and HVTRACK = 1).	
	D3	DISSTAG	0	Enable staggered outputs.	0
			1	Disable staggered outputs.	
	D2	AUTORST	0	Do not automatically reset error registers and outputs.	0
			1	Automatically reset DETERR and CORRERR registers 1µs after $\overline{ERR}$ asserts.	
	D[1:0]	ERRSEL	00	$\overline{ERR}$ asserts when DETERR is larger than DETTHR.	00
			01	$\overline{ERR}$ asserts when CORRERR is larger than CORRTHR.	
			10, 11	$\overline{ERR}$ asserts when DETERR is larger than DETTHR or CORRERR is larger than CORRTHR.	
0x09	D[7:1]	I2CSRCA	XXXXXXX	I^2C address translator source A.	0000000
	D0	—	0	Reserved.	0
0x0A	D[7:1]	I2CDSTA	XXXXXXX	I^2C address translator destination A.	0000000
	D0	—	0	Reserved.	0
0x0B	D[7:1]	I2CSRCB	XXXXXXX	I^2C address translator source B.	0000000
	D0	—	0	Reserved.	0
0x0C	D[7:1]	I2CDSTB	XXXXXXX	I^2C address translator destination B.	0000000
	D0	—	0	Reserved.	0

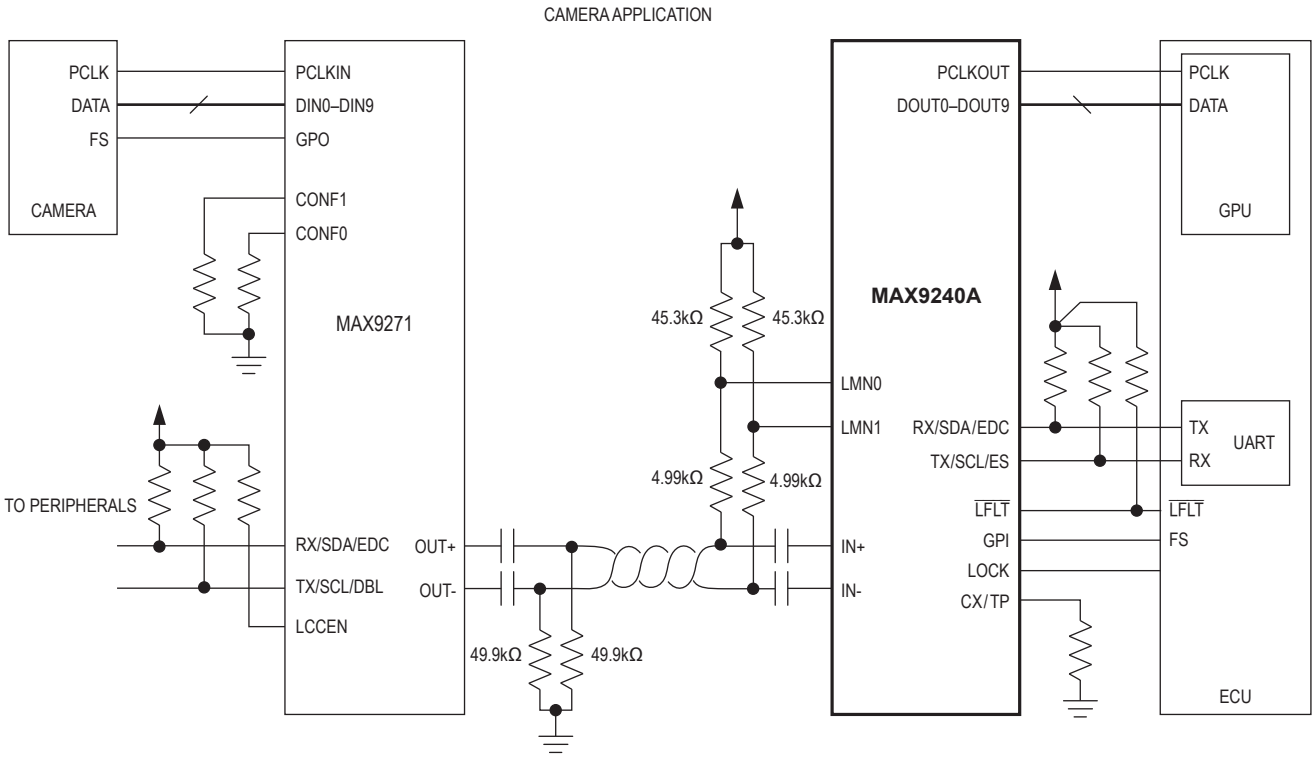
Table 16. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0D	D7	I2CLOCACK	0	Acknowledge not generated when forward channel is not available.	1
			1	I²C-to-I²C slave generates local acknowledge when forward channel is not available.	
	D[6:5]	I2CSLVSH	00	352ns/117ns I²C setup/hold time.	01
			01	469ns/234ns I²C setup/hold time.	
			10	938ns/352ns I²C setup/hold time.	
			11	1046ns/469ns I²C setup/hold time.	
	D[4:2]	I2CMSTBT	000	8.47kbps (typ) I²C-to-I²C master bit-rate setting.	101
			001	28.3kbps (typ) I²C-to-I²C master bit-rate setting.	
			010	84.7kbps (typ) I²C-to-I²C master bit-rate setting.	
			011	105kbps (typ) I²C-to-I²C master bit-rate setting.	
			100	173kbps (typ) I²C-to-I²C master bit-rate setting.	
			101	339kbps (typ) I²C-to-I²C master bit-rate setting.	
			110	533kbps (typ) I²C-to-I²C master bit-rate setting.	
			111	837kbps (typ) I²C-to-I²C master bit-rate setting.	
	D[1:0]	I2CSLVTO	00	64µs (typ) I²C-to-I²C slave remote timeout.	10
			01	256µs (typ) I²C-to-I²C slave remote timeout.	
			10	1024µs (typ) I²C-to-I²C slave remote timeout.	
			11	No I²C-to-I²C slave remote timeout.	
0x0E	D[7:6]	—	01	Reserved.	01
	D5	GPIEN	0	Disable GPI-to-GPO signal transmission to serializer.	1
			1	Enable GPI-to-GPO signal transmission to serializer.	
	D4	GPIIN	0	GPI input is low.	0 (read only)
			1	GPI input is high.	
	D3	GPIO1OUT	0	Set GPIO1 to low.	1
			1	Set GPIO1 to high.	
	D2	GPIO1IN	0	GPIO1 input is low.	0 (read only)
			1	GPIO1 input is high.	
	D1	GPIO0OUT	0	Set GPIO0 to low.	1
			1	Set GPIO0 to high.	
	D0	GPIO0IN	0	GPIO0 input is low.	0 (read only)
			1	GPIO0 input is high.	
0x0F	D[7:0]	DETTHR	XXXXXXXX	Error threshold for detected errors.	00000000
0x10	D[7:0]	DETERR	XXXXXXXX	Detected error counter.	00000000 (read only)
0x11	D[7:0]	CORRTHR	XXXXXXXX	Error threshold for corrected errors.	00000000
0x12	D[7:0]	CORRERR	XXXXXXXX	Corrected error counter.	00000000 (read only)
0x13	D[7:0]	PRBSERR	XXXXXXXX	PRBS error counter.	00000000 (read only)

Table 16. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x14	D7	PRBSOK	0	PRBS test not completed.	0 (read only)
			1	PRBS test completed with success.	
	D[6:4]	—	000	Reserved.	000 (read only)
	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage	10 (read only)
			01	Negative cable wire shorted to ground	
			10	Normal operation	
			11	Negative cable wire disconnected	
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage	10 (read only)
			01	Positive cable wire shorted to ground	
			10	Normal operation	
			11	Positive cable wire disconnected	
0x15	D[7:0]	—	00100XXX	Reserved.	00100XXX
0x16	D[7:0]	—	00110000	Reserved.	00110000
0x17	D[7:0]	—	01010100	Reserved.	01010100
0x18	D[7:0]	—	00110000	Reserved.	00110000
0x19	D[7:0]	—	11001000	Reserved.	11001000
0x1A	D[7:0]	—	XXXXXXXX	Reserved.	00000000 (read only)
0x1B	D[7:0]	—	XXXXXXXX	Reserved.	00000000 (read only)
0x1C	D[7:0]	—	XXXXXXXX	Reserved.	00000000 (read only)
0x1D	D7	CXTP	0	CX/TP input is low.	0 (read only)
			1	CX/TP input is high.	
	D6	CXSEL	0	CXSEL is 0.	0 (read only)
			1	CXSEL is 1.	
	D5	I2CSEL	0	Input is low.	0 (read only)
			1	Input is high.	
	D4	LCCEN	0	Input is low.	0 (read only)
			1	Input is high.	
	D[3:0]	—	XXXX	Reserved.	0000 (read only)
0x1E	D[7:0]	ID	00001100	Device identifier (MAX9240A = 0x0C).	00001100 (read only)
0x1F	D[7:5]	—	000	Reserved.	000 (read only)
	D4	CAPS	0	Not HDCP capable.	0 (read only)
			1	HDCP capable.	
	D[3:0]	REVISION	XXXX	Device revision.	(read only)

Typical Application Circuit



NOTE: NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE PIN DESCRIPTION FOR DETAILS.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9240AGTM+	-40°C to +105°C	48 TQFN-EP*
MAX9240AGTM/V+	-40°C to +105°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+4	21-0144	90-0130

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/14	Initial release	—
1	8/15	Corrected typos and unclear text in data sheet	1–48
2	7/21	Removed future product note and asterisk in *Ordering Information* table.	48

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