Single-chip built-in FET type Switching Regulator Series

Simple Step-down Switching Regulator with Integrated Compensation

BD9322EFJ, BD9323EFJ, BD9324EFJ

●Description

The BD9322EFJ, BD9323EFJ and BD9324EFJ are step-down regulators that integrate a low resistance high side N-channel MOSFET.

It achieves 2A / 3A / 4A continuous output current over a wide input supply range.

Current mode operation provides fast transient response and easy phase compensation.

●Features

1) Wide operating INPUT Range **4.75V～18V**
2) Selectable **2A / 3A / 4A** Output Current
3) Selectable **0.1Ω / 0.15Ω** Internal MOSFET Switch
4) Low ESR Output Ceramic Capacitors are Available
5) Low Stanby Current during Shutdown Mode
6) **380kHz** Operating Frequency
7) Feedback voltage 0.9V **±1.5%** Accuracy
8) Protection circuit: Undervoltage lockout protection circuit
   Thermal shutdown circuit
   Overcurrent protection circuit
9) HTSOP-J8 Package (with Exposed thermal PAD)

●Applications

Distributed Power System

Pre-Regulator for Linear Regulator

●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}	20	V
Switch Voltage	V_{SW}	20	V
Power Dissipation for HTSOP-J8	Pd	3760*	mW
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	150	℃
BST Voltage	V_{BST}	V_{SW}+7	V
All other pins	V_{OTH}	7	V

* Derating in done 30.08 mW/℃ for operating above Ta≧25℃(Mount on 4-layer 70.0mm×70.0mm×1.6mm board)

Apr.2008

● Operation Range(Ta= -40～85℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{IN}	4.75	12	18	V
Output current for BD9322EFJ	I_{SW2}	—	—	2**	A
Output current for BD9323EFJ	I_{SW3}	—	—	3**	A
Output current for BD9324EFJ	I_{SW4}	—	—	4**	A

** Pd, ASO should not be exceeded

● Electrical characteristics (unless otherwise specified VIN=12V Ta=25℃)

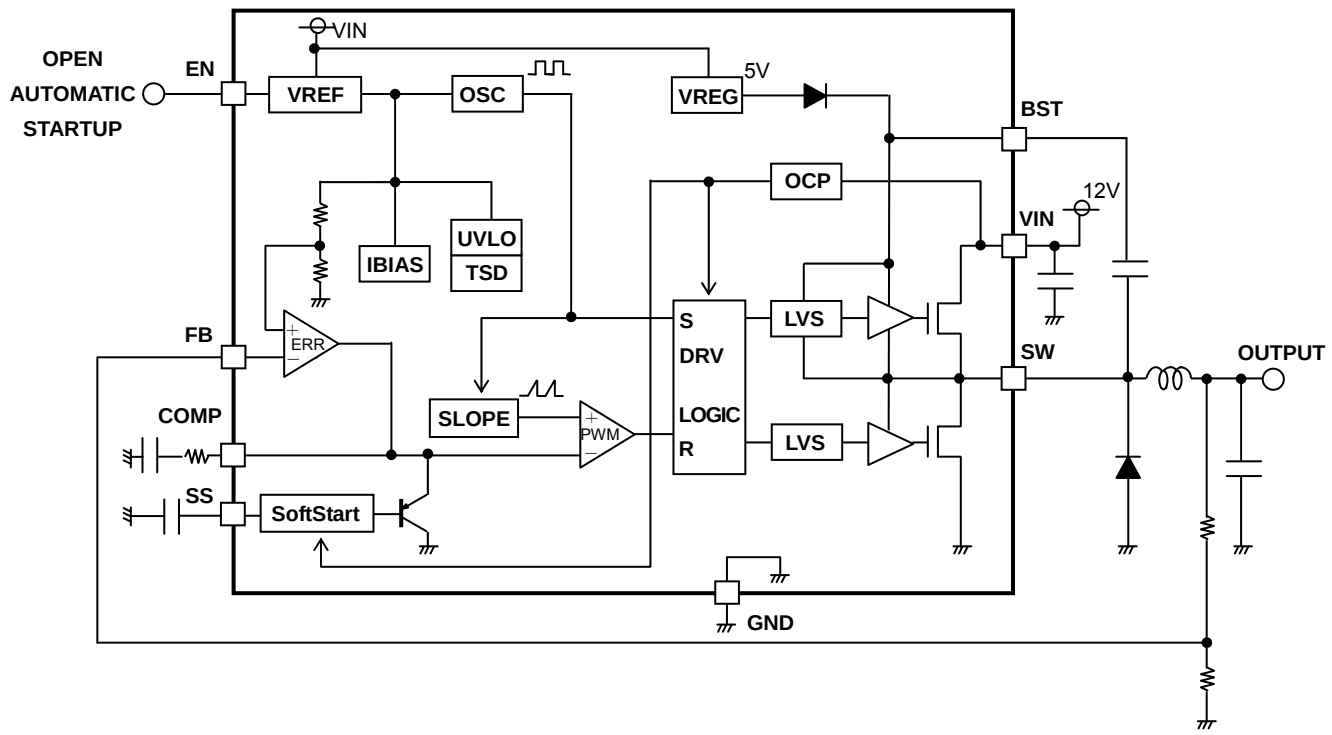
Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Error amplifier block						
FB input bias current	I_{FB}	-	0.1	2	μA	
Feedback voltage	V_{FB}	0.886	0.900	0.914	V	Voltage follower
SW block – SW						
Hi-side FET On-resistance for BD9322EFJ	R_{ON2}	-	0.15	-	Ω	I_{SW}= -0.8A ***
Hi-side FET On-resistance for BD9323EFJ	R_{ON3}	-	0.10	-	Ω	I_{SW}= -0.8A ***
Hi-side FET On-resistance for BD9324EFJ	R_{ON4}	-	0.10	-	Ω	I_{SW}= -0.8A ***
Lo-side FET On-resistance	R_{ONL}	-	10	-	Ω	I_{SW}= 0.1A
Leak current N-channel	I_{LEAKN}	-	0	10	μA	V_{IN}= 18V , V_{SW} = 0V
Switch Current Limit for BD9322EFJ	I_{LIMIT2}	2.5	-	-	A	***
Switch Current Limit for BD9323EFJ	I_{LIMIT3}	3.5	-	-	A	***
Switch Current Limit for BD9324EFJ	I_{LIMIT4}	4.5	-	-	A	***
Maximum duty cycle	M_{DUTY}	-	90	-	%	V_{FB}= 0V
General						
Enable Pull-up current	I_{EN}	12	23	34	μA	V_{EN}= 0V
Enable Threshold voltage	V_{EN}	0.4	0.63	0.9	V	
Under Voltage Lockout threshold	V_{UVLO}	4.05	4.40	4.75	V	V_{IN} rising
Under Voltage Lockout Hysteresis	V_{HYS}	-	0.1	-	V	
Soft Start Current	I_{SS}	23	41	62	uA	V_{SS}= 0.1 V
Soft Start Time	T_{SS}	-	1.6	-	ms	C_{SS}= 0.1 uF
Operating Frequency	F_{OSC}	300	380	460	kHz	
Circuit Current	I_{CC}	-	2.1	4.3	mA	V_{FB}= 1.5V, V_{EN}= OPEN
Quiescent Current	I_{QUI}	-	100	190	μA	V_{EN}= 0V

*** See the series line-up table below.

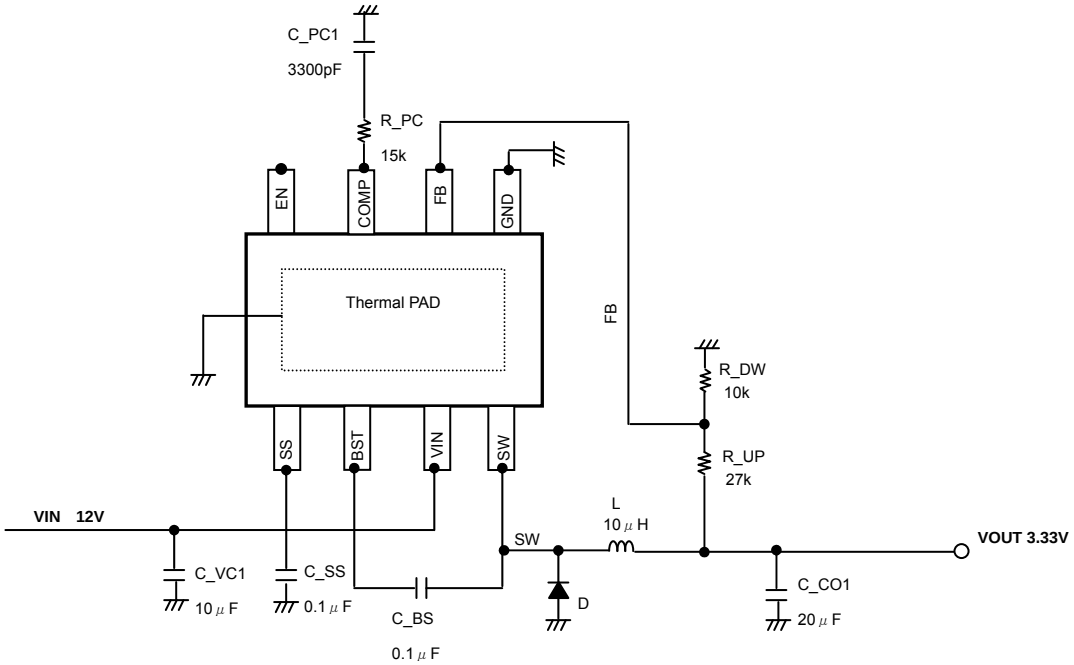
● Series Line-up Table

LINE-UP	BD9322EFJ	BD9323EFJ	BD9324EFJ
FET ON-RESISTANCE	0.15 Ω	0.10 Ω	0.10 Ω
OUTPUT CURRENT	2.0 A	3.0A	4.0 A

● Block Diagram



● Typical Application Circuit



● Block Operation

•VREG

A block to generate constant-voltage for DC/DC boosting.

•VREF

A block that generates internal reference voltage of 2.9 V (Typ.).

•TSD/UVLO

TSD (Thermal shutdown)/UVLO (Under Voltage Lockout) protection block. The TSD circuit shuts down IC at 175℃ (Typ.)
The UVLO circuit shuts down the IC when the Vcc is Low Voltage.

•Error amp block (ERR)

This is the circuit to compare the reference voltage and the feedback voltage of output voltage. The COMP pin voltage resulting from this comparison determines the switching duty. At the time of startup, since the soft start is operated by the SS pin voltage, the COMP pin voltage is limited to the SS pin voltage.

•Oscillator block (OSC)

This block generates the oscillating frequency.

•SLOPE block

This block generates the triangular waveform from the clock created by OSC. Generated triangular waveform is sent to the PWM comparator.

•PWM block

The COMP pin voltage output by the error amp is compared to the SLOPE block's triangular waveform to determine the switching duty. Since the switching duty is limited by the maximum duty ratio which is determined internally, it does not become 100%.

•DRV block

A DC/DC driver block. A signal from the PWM is input to drive the power FETs.

• CURRENT SENSE

Current flowing to the power FET is detected by voltage at the CURRENT SENSE and the overcurrent protection operates at 2.5/3.5/4.5A (min.). When the overcurrent protection operates, switching is turned OFF and the SS pin capacitance is discharged.

• DELAY START

A start delay circuit for positive/negative charge pump and Boost converter.

•Soft start circuit

Since the output voltage rises gradually while restricting the current at the time of startup, it is possible to prevent the output voltage overshoot or the rush current.

● Physical Dimension

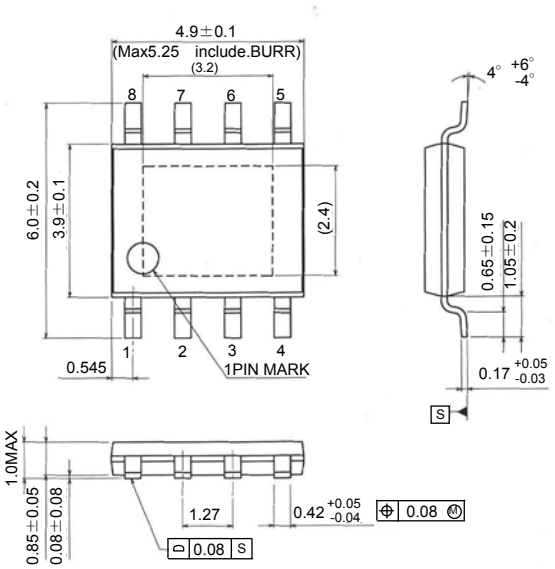


Fig HTSOP-J8 Package
(Unit:mm)

● Pin Assignment and Pin Function

Pin No.	Pin name	Function
1	SS	Soft Start Control Input
2	BST	High-Side Gate Drive Boost Input
3	VIN	Power Input
4	SW	Power Switching Output
5	GND	Ground
6	FB	Feed Back Input
7	COMP	Compensation Node
8	EN	Enable Input

● Typical Performance Characteristics (Unless otherwise specified, VIN= 12V Ta = 25℃)

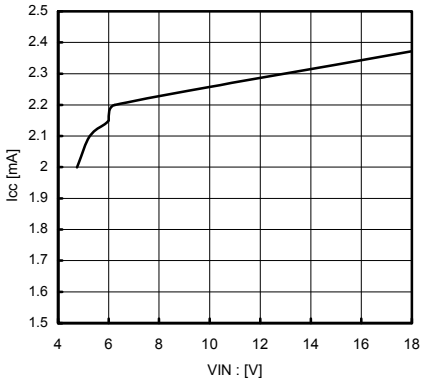


Fig. Circuit Current

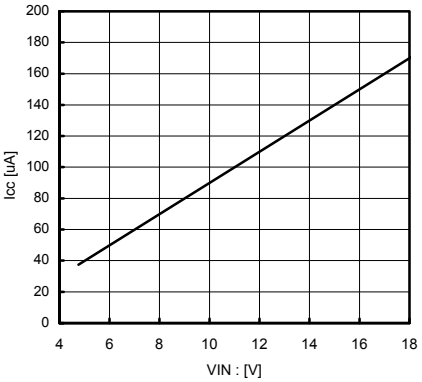


Fig. Quiescent Current

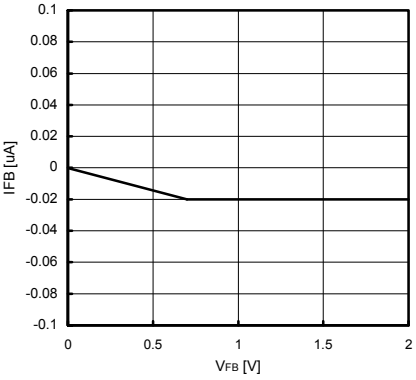


Fig. Input Bias Current

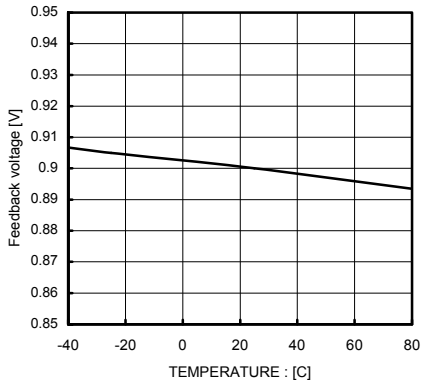


Fig. Feedback voltage

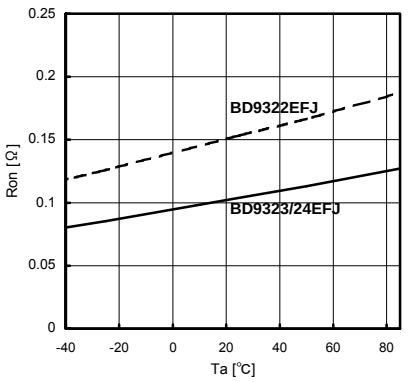


Fig. Hi-Side On-resistance

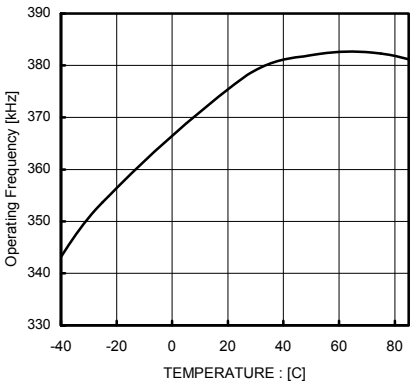


Fig. Operating Frequency

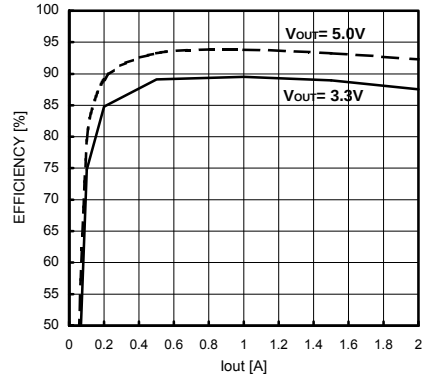


Fig. STEP Down Efficiency
(VIN= 12V VOUT= 3.3V L= 22uH)

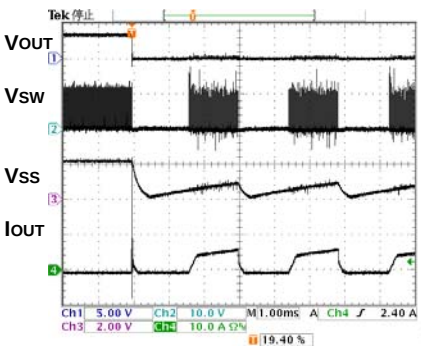


Fig. OverCurrent Protection
(VOUT is shorted to GND)

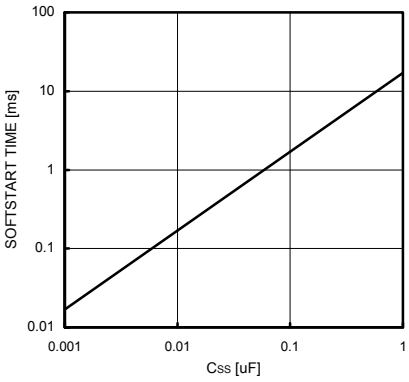


Fig. Soft Start Time

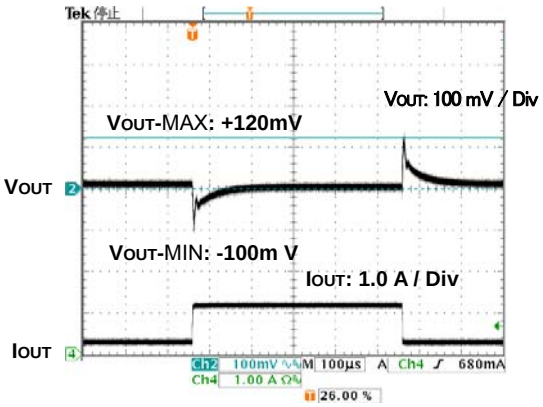


Fig. Transient Response

(VIN= 12V VOUT= 3.3V L= 10uH Cout =22uF Iout= 0.2-1.0A)

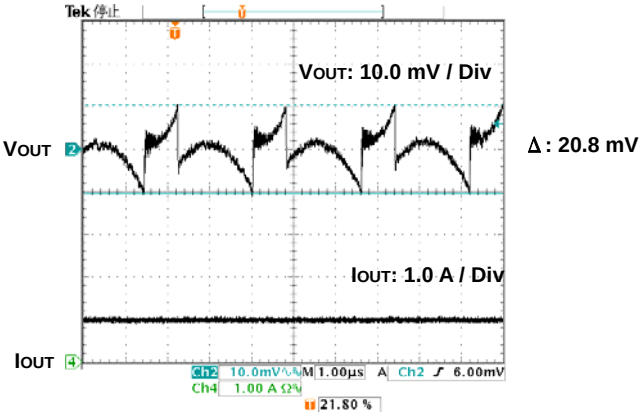


Fig. Output Ripple Voltage

(VIN= 12V VOUT= 3.3V L= 10uH Cout =22uF I out= 1.0A)

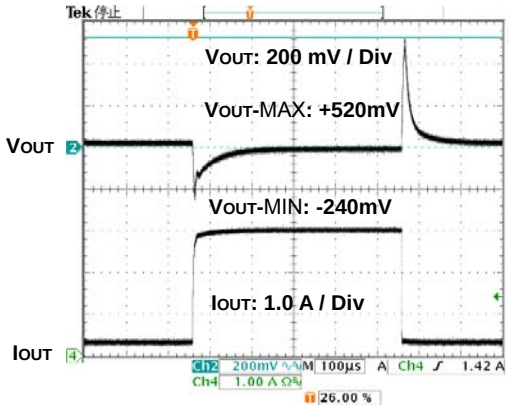


Fig. Transient Response

(VIN= 12V VOUT= 3.3V L= 10uH Cout =22uF Iout= 0.2-3.0A)

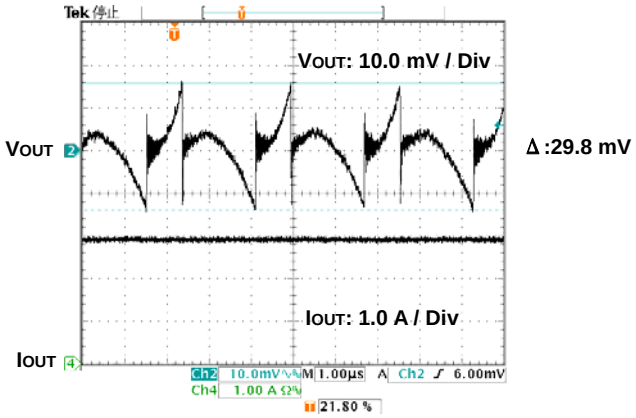


Fig. Output Ripple Voltage

(VIN= 12V VOUT= 3.V L= 10uH Cout =22uF Io=3.0A)

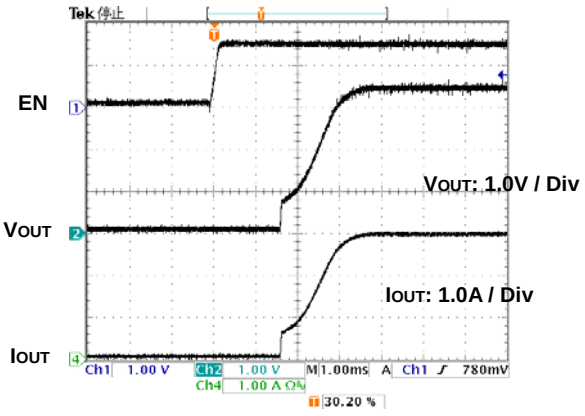


Fig. Start Up waveform

(VIN= 12V VOUT= 3.3V L= 22uH CSS= 0.1uF Iout= 0A)

● Selecting Application Components

(1) Output LC constant (Buck Converter)

The inductance L to use for output is decided by the rated current I_{LR} and input current maximum value I_{OMAX} of the inductance.

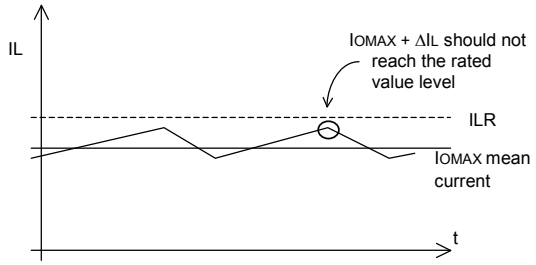


Fig.

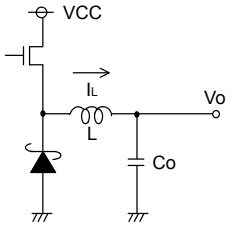


Fig.

Adjust so that $I_{OMAX} + \Delta I_L$ does not reach the rated current value I_{LR}. At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (Vcc - Vo) \times \frac{Vo}{Vcc} \times \frac{1}{f} \quad [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2Co} \times \frac{Vo}{Vcc} \times \frac{1}{f} \quad [V]$$

Perform setting so that the voltage is within the permissible ripple voltage range.
For the drop voltage V_{DR} during sudden load change, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{Co} \times 10\,\mu sec \quad [V]$$

However, 10 μ sec is the rough calculation value of the DC/DC response speed.
Make Co settings so that these two values will be within the limit values.

(2)Loop Compensation

Choosing compensation capacitor C_1 and resistor R_3

The example of DC/DC converter application bode plot is shown below. The compensation resistor R_3 will set the cross over frequency F_C that decides the stability and response speed of DC/DC converter. So compensation resistor R_3 has to be adjusted to adequate value for good stability and response speed.

The cross over frequency F_C can be adjusted by changing the compensation resistor R_3 connected to COMP terminal.
The higher cross over frequency achieves good response speed, but less stability. And the lower cross over frequency shows good stability, but worse response speed.
Usually, the 1/10 of DC/DC converter operating frequency is used for cross over frequency F_C. So please decide the compensation resistor and capacitor using the following formula on setting F_C to 1/10 of operating frequency at first.
After that, please measure and adjust the cross over frequency on your set (on the actual application) to meet the enough response speed and phase-margin.

(i) Choosing phase compensation resistor R_3

Please decide the compensation resistor R_3 on following formula.

Compensation Resistor $R_3 = 5800 \times C_{OUT} \times F_C \times V_{OUT}$ [ohm]

Where
C_{OUT} : Output capacitor connected to DC/DC output
V_{OUT} : Output voltage
F_C : Desired cross over frequency (38kHz)

(ii) Choosing phase compensation capacitor C_1

The stability of DC/DC converter needs to cancel the phase delay that is from output LC filter by inserting the phase advance.
The phase advance can be added by the zero on compensation resistor and capacitor.
The LC resonant frequency F_{LC} and the zero on compensation resistor and capacitor are expressed below.

LC resonant frequency $F_{LC} = \dfrac{1}{2\pi\sqrt{LC_{OUT}}}$ [Hz]

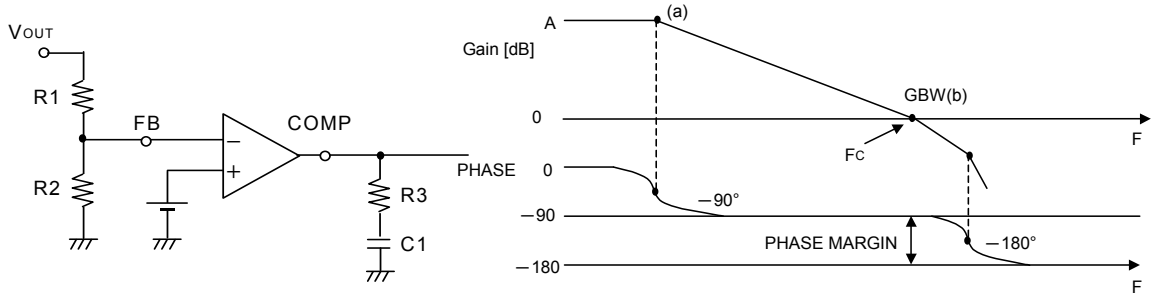
Zero by C_1 and R_3 $F_Z = \dfrac{1}{2\pi C_1 R_3}$ [Hz]

Please choose C1 to make F_Z to 1 / 3 of F_{LC} .

Compensation Capacitor $C_1 = \dfrac{3}{2\pi F_{LC} R_3}$ [F]

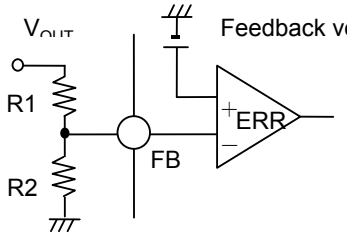
(iii) The condition of the loop compensation stability

The stability of DC/DC converter is important. To secure the operating stability, please check the loop compensation has the enough phase-margin. For the condition of loop compensation stability, the phase-delay must be less than 150 degree where Gain is 0 dB. Namely over 30 degree phase-margin is needed.
Lastly after the calculation above, please measure and adjust the phase-margin to secure over 30 degree.



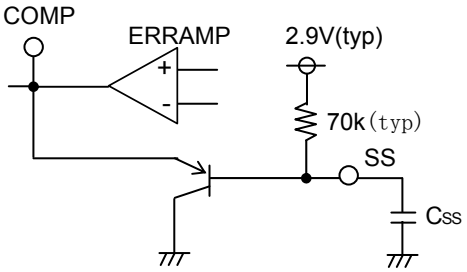
(3) Design of Feedback Resistance constant

Set the feedback resistance as shown below.



$$V_{OUT} = \frac{R1+R2}{R2} \times 0.900 \quad [V]$$

● Soft Start Function



The buck converter has an adjustable SoftStart function to prevent high inrush current during start up.

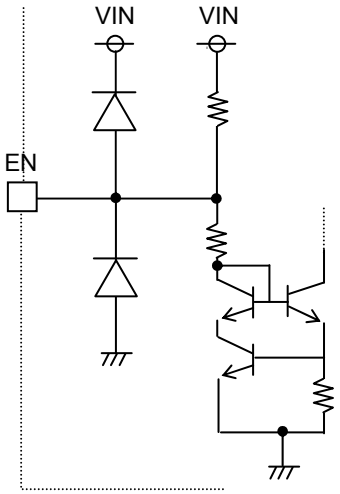
The soft-start time is set by the external capacitor connected to SS pin.

The soft start time is given by;

$$T_{SS} = 16200 \times C_{SS} \quad [s]$$

Please confirm the overshoot of the output voltage and inrush current when deciding the SS capacitor value.

● EN Function



The equivalent internal circuit.

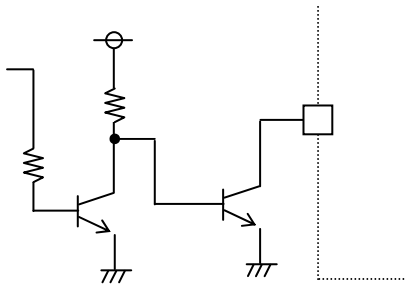
The EN terminal controls IC's shut down.

Leaving EN terminal open, makes IC start up automatically.

To shut down the IC, the external component has to pull the current from EN terminal and make the EN voltage low.

The EN threshold voltage is 0.63V (typ.).

ex)



The example of EN driving circuit.

●Layout Pattern Consideration

Two high pulsing current flowing loops exist in the buck regulator system.

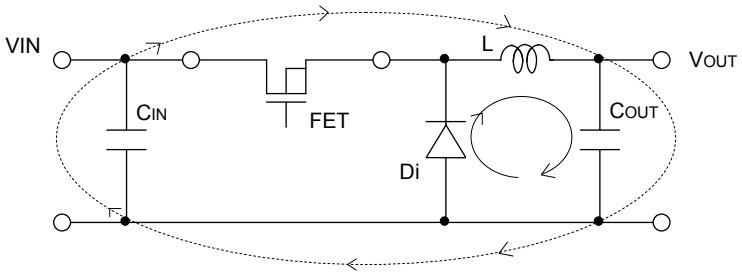
The first loop, when FET is ON, starts from the input capacitors, to the VIN terminal, to the SW terminal, to the inductor, to the output capacitors, and then returns to the input capacitor through GND.

The second loop, when FET is OFF, starts from the shotkey diode, to the inductor, to the output capacitor, and then returns to the shotkey diode through GND.

To reduce the noise and improve the efficiency, please minimize these two loop area.

Especially input capacitor, output capacitor and shotkey diode should be connected to GND plain.

PCB Layout may affect the thermal performance, noise and efficiency greatly. So please take extra care when designing PCB Layout patterns.



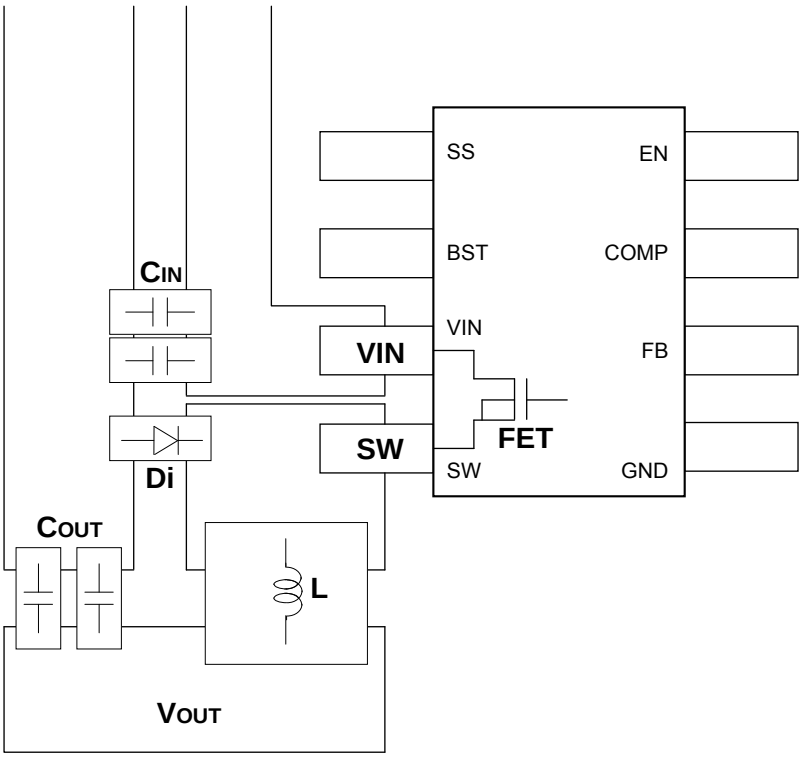
2 Current loop in Buck regulator system

・The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plain as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective.

・The input capacitors should be connected as close as possible to the VIN terminal.

・Keep sensitive signal traces such as trace connected FB and COMP away from SW pin.

・The inductor, the shot key diode and the output capacitors should be placed close to SW pin as much as possible.



The example of PCB layout pattern

● Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when the resistors and transistors are connected to the pins as shown in Fig. , a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

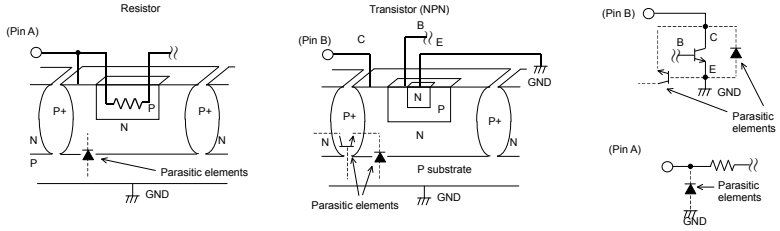


Fig. Example of a Simple Monolithic IC Architecture

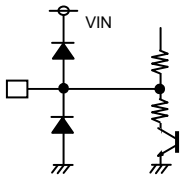
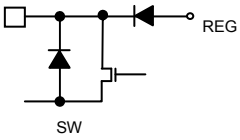
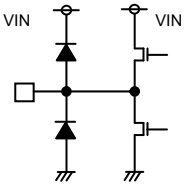
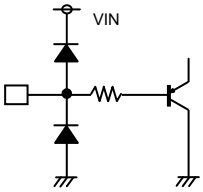
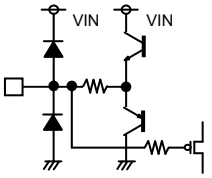
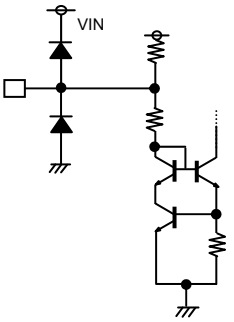
9) Overcurrent protection circuits

An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

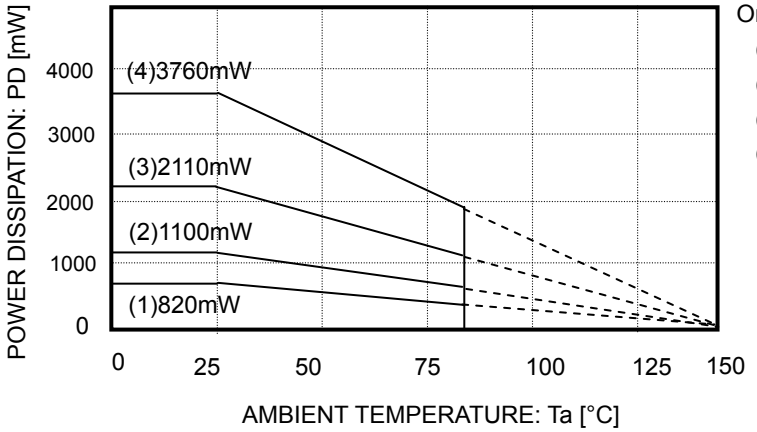
10) Thermal shutdown circuit (TSD)

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

● I/O Equivalent Circuit Diagram Fig.

1.SS	2.BST	4.SW
		
6.FB	**7.COMP**	**8.EN**
		

● Power Dissipation



On 70 × 70 × 1.6 mm glass epoxy PCB

(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)

(2) 2-layer board (Backside copper foil area 15 mm × 15 mm)

(3) 2-layer board (Backside copper foil area 70 mm × 70 mm)

(4) 4-layer board (Backside copper foil area 70 mm × 70 mm)

Notes

- No technical content pages of this document may be reproduced in any form or transmitted by any means without prior permission of ROHM CO.,LTD.
- The contents described herein are subject to change without notice. The specifications for the product described in this document are for reference only. Upon actual use, therefore, please request that specifications to be separately delivered.
- Application circuit diagrams and circuit constants contained herein are shown as examples of standard use and operation. Please pay careful attention to the peripheral conditions when designing circuits and deciding upon circuit constants in the set.
- Any data, including, but not limited to application circuit diagrams information, described herein are intended only as illustrations of such devices and not as the specifications for such devices. ROHM CO.,LTD. disclaims any warranty that any use of such devices shall be free from infringement of any third party's intellectual property rights or other proprietary rights, and further, assumes no liability of whatsoever nature in the event of any such infringement, or arising from or connected with or related to the use of such devices.
- Upon the sale of any such devices, other than for buyer's right to use such devices itself, resell or otherwise dispose of the same, no express or implied right or license to practice or commercially exploit any intellectual property rights or other proprietary rights owned or controlled by
- ROHM CO., LTD. is granted to any such buyer.
- Products listed in this document are no antiradiation design.

The products listed in this document are designed to be used with ordinary electronic equipment or devices (such as audio visual equipment, office-automation equipment, communications devices, electrical appliances and electronic toys).
Should you intend to use these products with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.
It is our top priority to supply products with the utmost quality and reliability. However, there is always a chance of failure due to unexpected factors. Therefore, please take into account the derating characteristics and allow for sufficient safety features, such as extra margin, anti-flammability, and fail-safe measures when designing in order to prevent possible accidents that may result in bodily harm or fire caused by component failure. ROHM cannot be held responsible for any damages arising from the use of the products under conditions out of the range of the specifications or due to non-compliance with the NOTES specified in this catalog.

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact your nearest sales office.

ROHM Customer Support System

THE AMERICAS / EUROPE / ASIA / JAPAN

www.rohm.com

Contact us : webmaster@rohm.co.jp

ROHM CO., LTD. 21 Saiin Mizosaki-cho, Ukyo-ku, Kyoto 615-8585, Japan
TEL : +81-75-311-2121
FAX : +81-75-315-0172

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View BD9322EFJ on WIN SOURCE
- Rohm Semiconductor Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management