System Power Supply LSIs for use in automotive electronics

System Power Supply IC with Connunication Function (Master Type)

BD9400BFP

Pb Free ROHM Electronic Components   RoHS Directive Compliance

●Description

The BD9400BFP can be combined with the BD9401FM/BD9403FV to create application-specific system power supplies.
It can be controlled using an I^2C BUS. The BD9400BFP is a main control chip featuring an I^2C BUS bidirectional communications function, a V_{DD} LDO (for microcontroller use), a V_{DD} reset, and BD9401FM/BD9403FV control circuits. The IC's I^2C BUS communications function allows switching regulator and high-side switch on/off control, as well as switching regulator frequency adjustment, using a maximum of 3 channels. The I^2C BUS read function can be used to send power supply overvoltage and undervoltage detection signals, as well as switching regulator output short detection signals.

●Features

1) The IC can be combined with the BD9401FM/BD9403FV to provide design flexibility.
2) On/off control of up to 6 outputs with I^2C BUS control
3) Broad input voltage range: 7 V to 36 V
4) Built-in LDO regulator for use with microcontrollers
5) LDO regulator: 3.3 V, 250 mA (±2% precision)
6) Built-in regulator voltage detection reset circuit
7) Built-in power supply overvoltage and undervoltage detection circuits
8) Dual reference voltage sources for BD9401FM/BD9403FV (VREF, VREG), and built-in triangular waveform oscillator
9) VREF reference voltage precision: ±1%
10) The triangular waveform oscillator frequency can be changed to ±10% or ±20% using I^2C BUS control.
11) Flag output for undervoltage detection, overvoltage detection, and BD9401FM/BD9403FV short protection detection signals
12) Total system stand-by current of 60 μA (Typ.) when V_{DD}LDO, reset, overvoltage, and undervoltage detection circuits are set.
13) Package: HSOP25

●Applications

Car audio, satellite navigation systems, etc.

Ver.B Oct.2005

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Power supply voltage	Vcc	36*1	V
Applied voltage	SDA, SCL, STBY	7	V
Power dissipation 1	P_{01}	0.85*2	W
Power dissipation 2	P_{02}	1.45*3	W
Operating temperature range	T_{OPR}	-40 to +85	°C
Storage temperature range	T_{STG}	+150	°C
Maximum junction temperature	T_{JMAX}	+150	°C

*1 Not to exceed Pd.

*2 Reduced by 6.8 mW/°C over Ta ≥ 25°C during IC without heat sink operation.

*3 Reduced by 11.6 mW/°C over Ta ≥ 25°C, when mounted on a glass epoxy board (70.0 mm × 70.0 mm × 1.6 mm).

●Recommended operating ranges (Ta = 25°C) (Not to exceed Pd.)

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	Vcc	8	26	V
Oscillating frequency (PWM controller)	fosc	30	500	KHz

●Electrical characteristics (Unless otherwise specified, Ta = 25°C; Va = 13.5 V; STDY = 3.3 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Oscillator block]						
Oscillating frequency	F_{OSC}	162	180	198	KHz	CT = 1000PF, RT = 52 kΩ
Frequency Va fluctuation	I_{ROSC}	—	—	2	%	Vcc = 8 V to 25V
Frequency rate of change 1	ΔF_{OSC1}	—	+10	—	%	Compliant with I^{2}C BUS specifications.
Frequency rate of change 2	ΔF_{OSC2}	—	-10	—	%	Compliant with I^{2}C BUS specifications.
Frequency rate of change 3	ΔF_{OSC3}	—	+20	—	%	Compliant with I^{2}C BUS specifications.
Frequency rate of change 4	ΔF_{OSC4}	—	-20	—	%	Compliant with I^{2}C BUS specifications.
[Reference voltage]						
Output voltage	V_{REF}	2.97	3.00	3.03	V	Io = 1 mA
Line regulation	Δ_{REF1}	—	1	10	mV	Vcc = 8 V to 26 V
Load regulation	Δ_{REF0}	—	5	20	mV	Io = 1 mA
Short current	I_{OVREF}	—	30	—	mA	
[VREG voltage]						
Output voltage	V_{REG}	4.5	5.0	5.5	V	Io = 0 mA
Output current capacity	I_{REG}	10	—	—	mA	
[Standby control]						
On mode voltage	V_{STAH}	2.3	—	3.3	V	
Off mode voltage	V_{STAL}	0	—	1.0	V	
[Overall]						
Total supply current	I_{OC}	—	1.0	2.0	mA	V_{ST} = 3.3 V
Total supply current during standby operation	I_{STBY}	—	60	100	μA	V_{STB} = 0 V

●Electrical characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Output voltage 3.3 V, 250 mA]						
Output voltage	Vo	3.234	3.3	3.366	V	Io = 10 mA
Output peak current	I_{PEAK}	0.25	—	2	A	
Line regulation	ΔV_{OL}	—	10	20	mV	Vcc = 9 V to 26 V, Io = 10 mA
Load regulation	ΔV_{OR}	—	30	60	mV	Io = 10 mA to 200 mA
Ripple rejection	RR	50	60	—	dB	F = 100 Hz, 0.5 V_{P-P}, Io = 10 mA
[RESET]						
Detection voltage	V_{DR}	2.66	2.80	2.94	V	
Hysteresis voltage	Δ_{DR}	—	90	—	mV	
Delay time	T_{DR}	5	10	20	ms	C_{DELAY} = 0.01 uF
[Overvoltage detection]						
Detection voltage	V_{DO}	17.5	18.5	19.5	V	Io = 0 mA
Hysteresis voltage	Δ_{DO}	—	400	—	mV	
[Reduced-voltage detection]						
Detection voltage	V_{DU}	8.0	8.5	9.0	V	
Hysteresis voltage	Δ_{DU}	—	150	—	mV	
[STATUS_FLAG]						
Output current capacity	I_{STF}	1	—	—	mA	$V_{STASTUS\_FLAG}$ = 0.4 V

•I²C BUS specifications

(1) BUS line and I/O timing and electrical characteristics

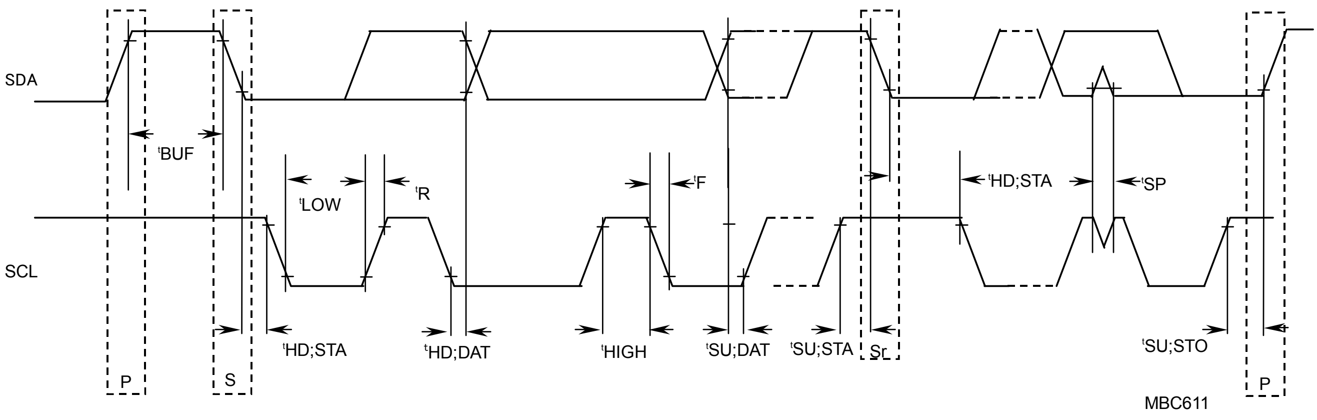


Fig.1 I²C BUS Timing Definitions

Table A: I^{2}C BUS Device SDA, SCL BUS Line Characteristics

Parameter	Symbol	Standard mode I^{2}C BUS		Unit
		Min.	Max.	
SCL frequency	fSCL	0	100	KHz
Stop/start condition open time	tBUF	4.7	—	Ms
Start condition (when repeating) The minimum clock pulse is generated after this period elapses.	tHD;STA	4.0	—	μs
SCL clock low interval	tLOW	4.7	—	μs
SCL clock high interval	tHIGH	4.0	—	μs
Start condition setup time when repeating	tSU;STA	4.7	—	μs
Hold time	tHD;DAT	0*	—	μs
Setup time	tSU;DAT	250	—	NS
SDA and SCL rise time	tR	—	1000	NS
SDA and SCL fall time	tF	—	300	NS
Stop condition setup time	tSU;STO	4.0	—	μs
BUS line allowable capacitance value	Cb	—	400	pF

Note: All values comply with minimum VIH and maximum VLL levels (Table B).

* A minimum hold time of 300 ns must be provided to ensure that the region for which the device's SCL falling edge is not defined is exceeded.

Table B: I^{2}C BUS Device SDA and SCL I/O Stage Characteristics

Parameter	Symbol	Standard mode I^{2}C BUS		Unit
		Min.	Max.	
Low level input voltage				
Fixed input level	VIL	-0.5	0.6	V
(VDD-dependent input level)		(-0.5)	(0.2VDD)	
High level input voltage				
Fixed input level	VIH	3.0	(*1)	V
(VDD-dependent input level)		(0.7 VDD)	(*1)	
Schmitt trigger input				
Fixed input level	Vhys	n/a	n/a	V
(VDD-dependent input level)		(n/a)	(n/a)	
Spike noise width to be rejected by the input filter	tSP	n/a	n/a	ns
Low level output voltage (open drain or open collector)				
(When sinking current is 3 mA.)	VOL1	0	0.4	V
(When sinking current is 6 mA.)	(VOL2)	(n/a)	(n/a)	
VIH min to LIL max fall time when the BUS line capacitance is from 10 pF to 400 pF				
(At VOL1, when the sinking current is 3 mA.)	tOF	—	250*2	ns
(At VOL2, when the sinking current is 6 mA.)		(n/a)	(n/a)	
I/O pin input current when the input voltage is from 0.4 V to 0.9 V	Ii	-10	10	μA
I/O pin capacitance	Ci		10	pF

n/a: Not applicable.

(2) I^2C BUS format (interface protocol)

Write Mode:

MSB		LSB MSB		LSB MSB		LSB	
S	Slave Address	A	Select Address	A	Data	A	P
1 bit	8 bit	1 bit	8 bit	1 bit	8 bit	1 bit	1 bit

S: Start condition (start bit recognition)
Slave Address: Slave address recognition

A: Acknowledge bit (acknowledge recognition)
Slave Address: High-side switch and DC/DC comparator on/off control
DC/DC comparator frequency adjustment

Data: Control and adjustment data
P: Stop condition (stop bit recognition)

Read Mode

MSB		LSB MSB		LSB	
S	Slave Address	A	Data	A	P
1 bit	8 bit	1 bit	8 bit	1 bit	8 bit

S: Start condition (start bit recognition)
Slave Address: Slave address recognition

A: Acknowledge bit (acknowledge recognition)
Slave Address: Short protection detection (SCP)
Overvoltage detection and undervoltage detection

Data: Detection data
P: Stop condition (stop bit recognition)

(3) Slave Address

MSB LSB

	A6	A5	A4	A3	A2	A1	A0	R/W
Write	1	0	0	0	0	0	0	0
Read	1	0	0	0	0	0	0	1

The above slave address is registered to Phillips Electronics.

(4) Select Address

Write mode

Setting	MSB	Select Address						LSB
	A7	A6	A5	A4	A3	A2	A1	A0
Channel on/off control	0	0	0	0	0	0	0	0
DC/DC comparator frequency variation	0	0	0	0	0	0	0	1

Read mode

Setting	MSB	Select Address						LSB
	A7	A6	A5	A4	A3	A2	A1	A0
Reduced voltage, overvoltage, short detection	0	0	0	0	0	0	0	0

(5) Detailed data

Write mode

Setting	Select Address	MSB	Data					LSB
		A7	A6	A5	A4	A3	A2	A1	A0
Channel on/off (1/0) control	00HEX	0	0	CH1 high-side switch	CH1 high-side converter	CH1 high-side switch	CH1 high-side converter	CH1 high-side switch	CH1 high-side converter
DC/DC comparator frequency adjustment	01HEX	0	0	0	0	0	DC/DC comparator frequency adjustment		

DC/DC comparator frequency setting

Frequency	Data (hex)
Initial	00
Initial +10%	01
Initial +20%	02
Initial -20%	03
Initial -10%	04

Read mode

Setting	Select Address	MSB	Data						LSB
		A7	A6	A5	A4	A3	A2	A1	A0
Reduced voltage, overvoltage, short conditions Channel on/off (1/0) condition	00HEX	0	0	0	SCP signal (CH1DC/DC) comparator	SCP signal (CH2DC/DC) comparator	SCP signal (CH3DC/DC) comparator	Overvoltage detection signal	Undervoltage detection signal

●**Reference data** (Unless otherwise specified, Ta = 25°C; Vcc = 13.5 V)

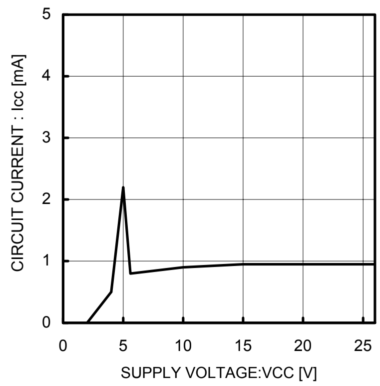


Fig. 2 Total Supply Current (STBY on time)

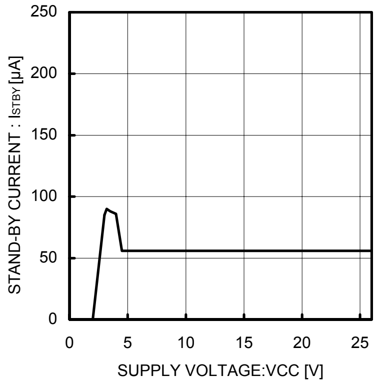


Fig. 3 Total Supply Current (STBY off time)

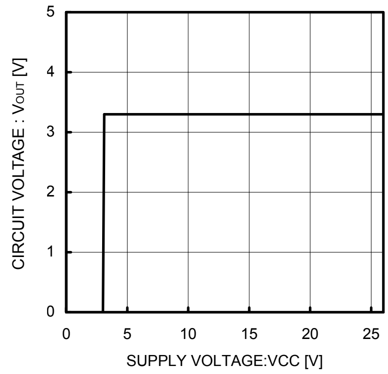


Fig. 4 VOUT Input Stability (Io = 0 mA)

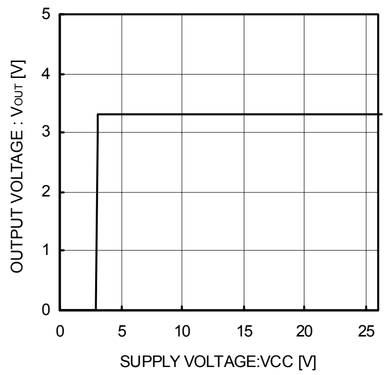


Fig. 5 Input Stability (Io = 200 mA)

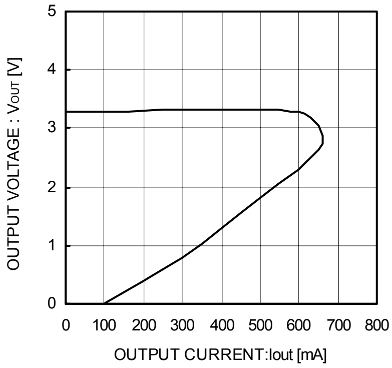


Fig. 6 Load Stability

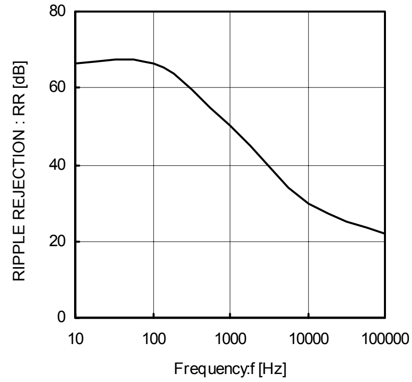


Fig. 7 Ripple Rejection

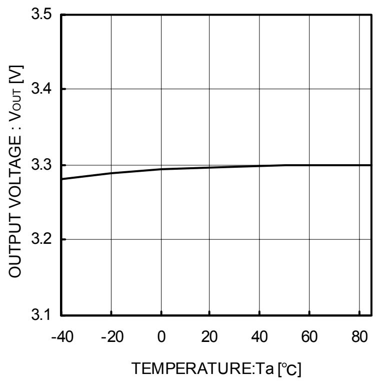


Fig. 8 VOUT Output Voltage vs Temperature

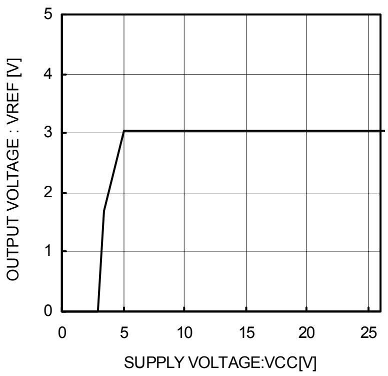


Fig. 9 VREF Input Stability

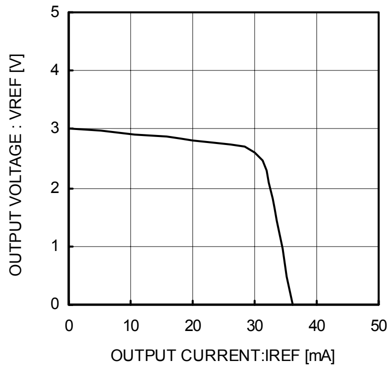


Fig. 10 VREF Load Stability

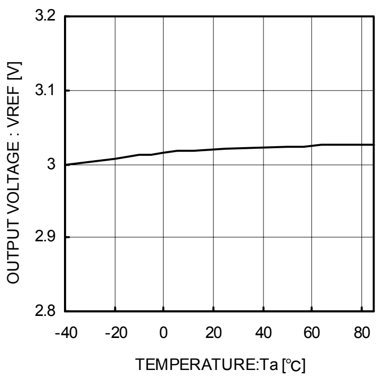


Fig. 11 VREF Output Voltage vs Temperature

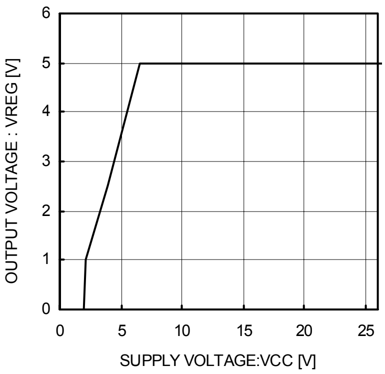


Fig. 12 VREG Input Stability

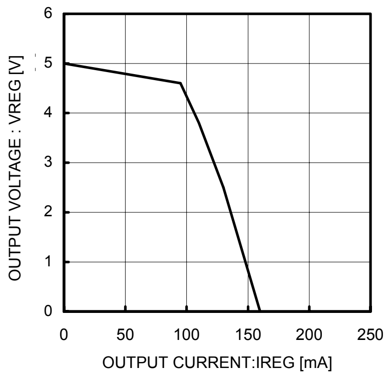


Fig.13 VREG Load Stability

●**Reference data**

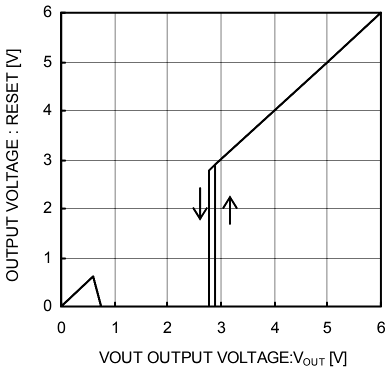


Fig. 14 RESET I/O

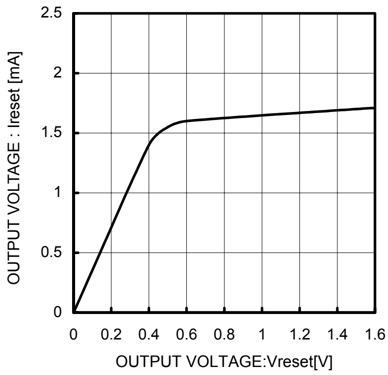


Fig. 15 RESET Output Current Capacity

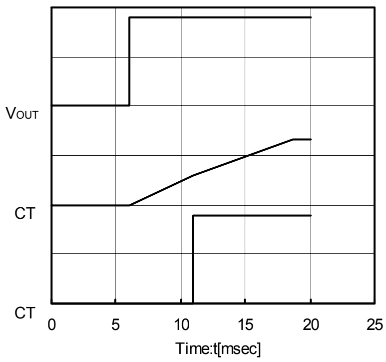


Fig. 16 RESET Delay Time

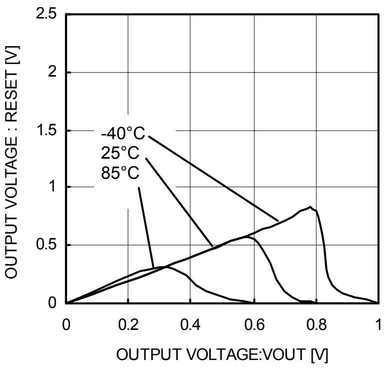


Fig. 17 RESET Minimum Operating Voltage

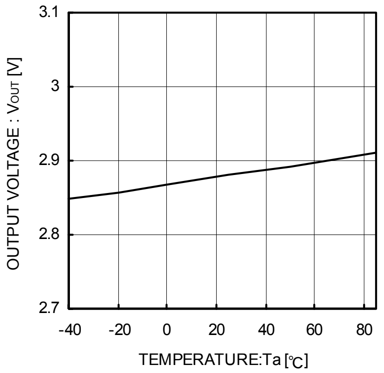


Fig. 18 RESET Detection Voltage vs Temperature

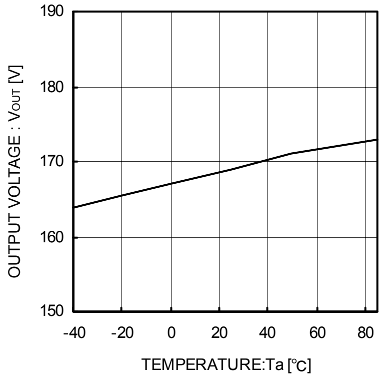


Fig. 19 Triangular Waveform Oscillating Frequency vs Temperature

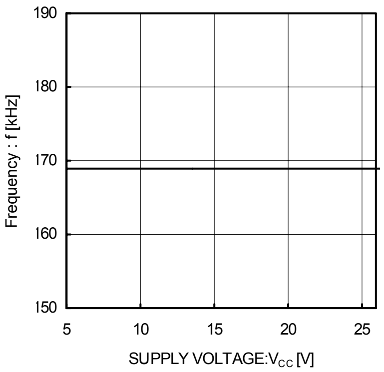


Fig. 20 Triangular Waveform Oscillating Frequency vs Input Stability

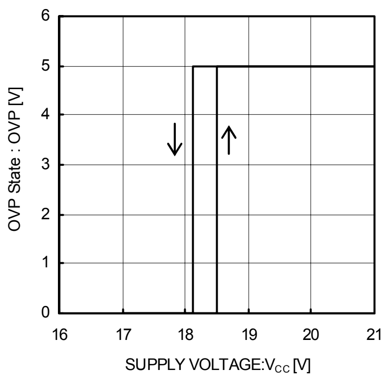


Fig. 21 Overvoltage Detection Threshold

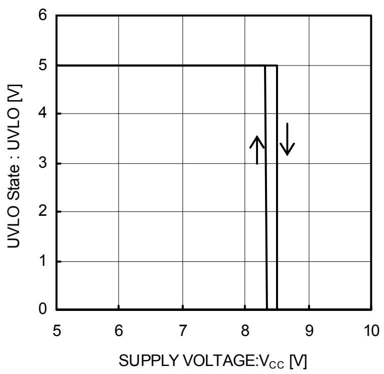


Fig. 22 Undervoltage Detection Threshold

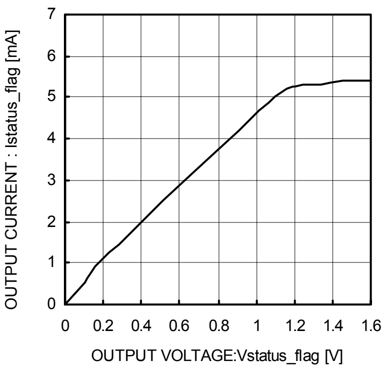


Fig. 23 Status Flag Output Current Capacity

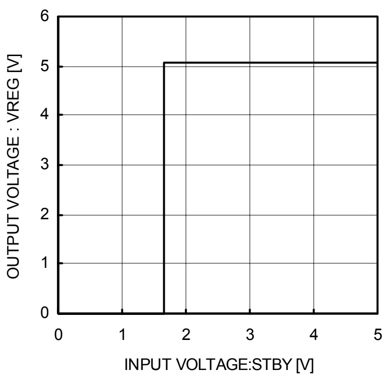


Fig. 24 STBY Voltage vs Output Voltage

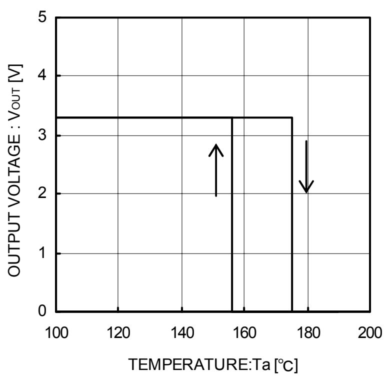


Fig. 25 Thermal Shutdown Circuit

●Block diagram

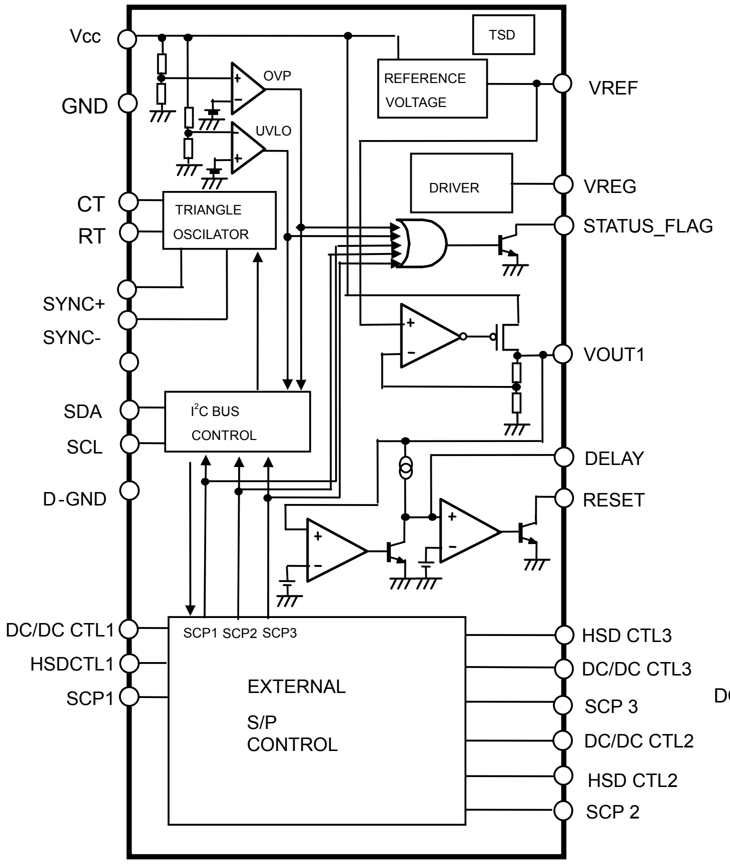


Fig . 26 Block Diagram

●Pin assignment

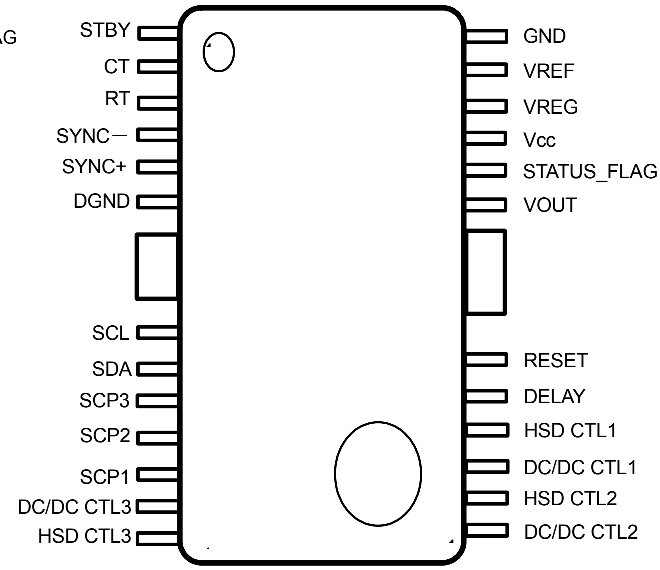


Fig . 27 Pin Assignment Diagram

●Pin function descriptions

PIN No.	PIN name	Function
1	STBY	Standby switch
2	CT	Used for BD9401/03 DC/DC. Triangular waveform frequency setting capacitor connection pin
3	RT	Used for BD9401/03 DC/DC. Triangular waveform frequency setting resistance connection
4	SYNC-	Triangular waveform inverted output pin
5	SYNC+	Triangular waveform non-inverted output pin
6	DGND	Logic ground
7	SCL	I^2C BUS clock input pin
8	SDA	I^2C BUS data input pin
9	SCP3	Short protection detection input from BD9401/03
10	SCP2	Short protection detection input from BD9401/03
11	SCP1	Short protection detection input from BD9401/03
12	DC/DC CTL3	DC/DC control to BD9401/03
13	HSD CTL3	High-side switch control to BD9401/03
14	DC/DC CTL2	DC/DC control to BD9401/03
15	HSD CTL2	High-side switch control to BD9401/03
16	DC/DC CTL1	DC/DC control to BD9401/03
17	HSD CTL1	High-side switch control to BD9401/03
18	DELAY	Reset delay time setting capacitor connection pin
19	RESET	RESET output
20	VOUT	Microcontroller regulator output
21	STATUS_FLAG	OR output for OVP, ULVO, SCP1, SCP2, and SCP3 signals
22	Vcc	Power supply input pin
23	VREG	BD9401FM/BD9403FV reference voltage output pin (5 V)
24	VREF	BD9401FM/BD9403FV reference voltage output pin (3 V)
25	GND	Ground pin
FIN	FIN	Heat dissipation fin; connect to ground.

●**Example application**

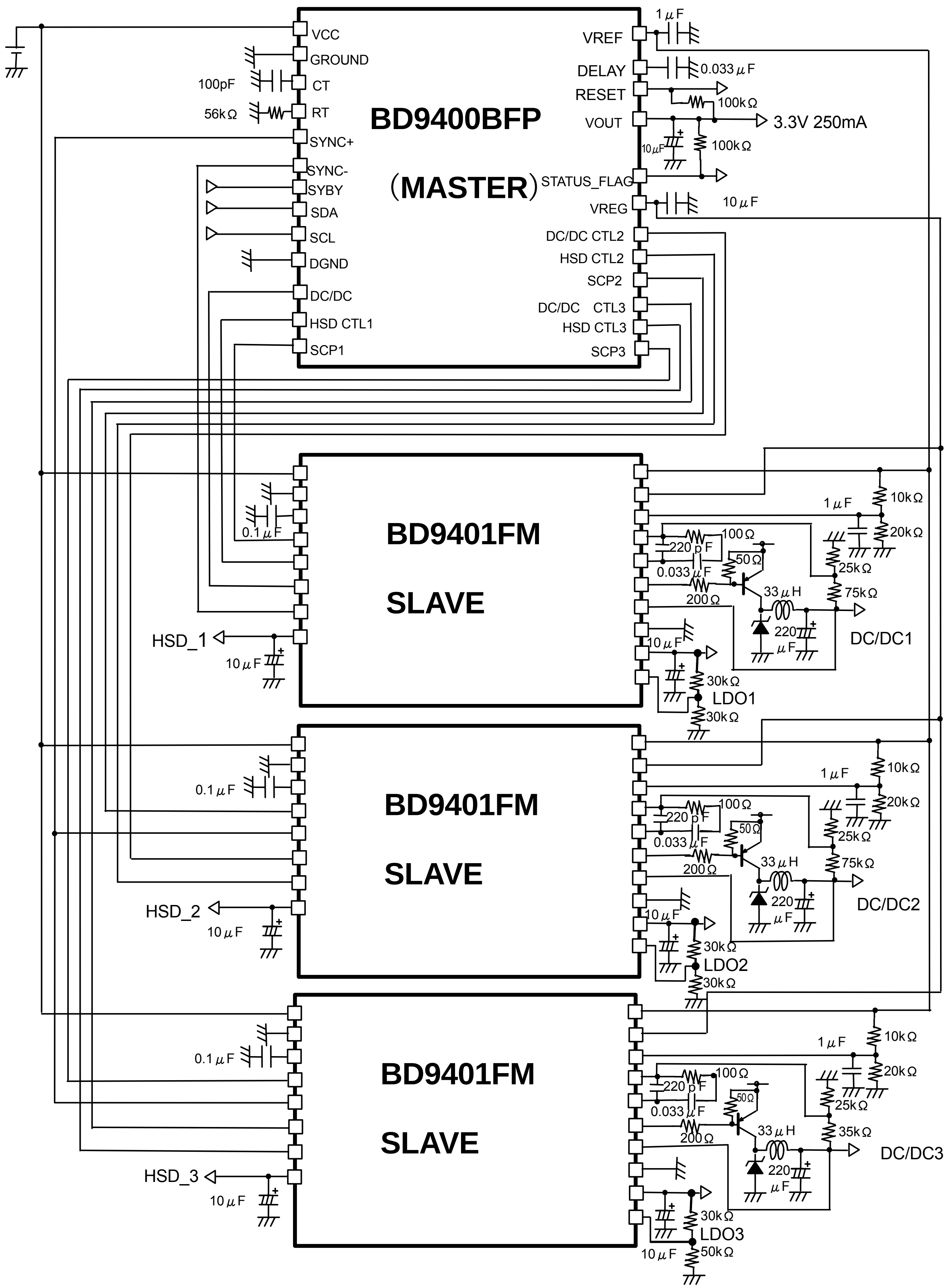


Fig. 28

●Block operation descriptions

- I²C BUS CONTROL/EXTERNAL S/P CONTROL

  I²C BUS control/external S/P control performs BUS communications control, serial/parallel conversion, and parallel/serial conversion. In write mode, outputs BD9401FM/BD9403FV output on/off control and adjusts the triangular waveform oscillator's frequency.

  In read mode, converts switching regulator short protection detection, overvoltage detection, and undervoltage detection information from the BD9401FM/BD9403FV into I²C BUS signals.

- Regulator

  Supports the microcontroller regulator, generating output of 3.3 V at a precision of ±2% and a current capacity of 250 mA. This regulator operates even during standby operation, and low-quiescent current technology delivers a total supply current of 60 μA, including RESET and detectors.

- RESET

  Acts as the VOUT (3.3 V) detection reset circuit. This block's power supply is connected to VOUT, and its operation is linked to VOUT. It uses a detection voltage of 2.80 V (Typ.) and a hysteresis of 90 mV (Typ.). The CT pin capacitor can be used to set the delay time at reset.

- VREF (3.0 V)

  The reference voltage circuit for the BD9400BFP's internal I²C BUS block and triangular waveform oscillator as well as the BD9401FM/BD9403FV.

  It generates output of 3.0 V at a precision of ±1%. Its current capacity is 1 mA.

- VREG (5.0 V)

  The reference voltage circuit for the BD9401FM/BD9403FV. The circuit uses 5.7 V emitter follower output, so the output voltage varies with the output current. Its current capacity is 10 mA.

- OVP/UVLO

  The overvoltage detection/undervoltage detection circuit, with detection voltages of 18.5 V (Typ.) and 8.5 V (Typ.), and hysteresis values of 400 mA (Typ.) and 150 mV (Typ.). The detection signals are output using the I²C BUS read mode.

- OSC

  The BD9401/FM/BD9403FV switching regulator's triangular oscillator. The frequency can be set with the CT pin's capacitor and the RT pin's resistor. SYNC+ and SYNC- outputs are inverted 180°.

- STATUS_FLAG

  This flag is set when either OVP/UVLO detection or BD9401FM/BD9403FV short protection is activated. (Its output changes to low.) Uses open collector output with a current capacity of 1 mA. Signal should be pulled up with a resistor.

●Timing chart

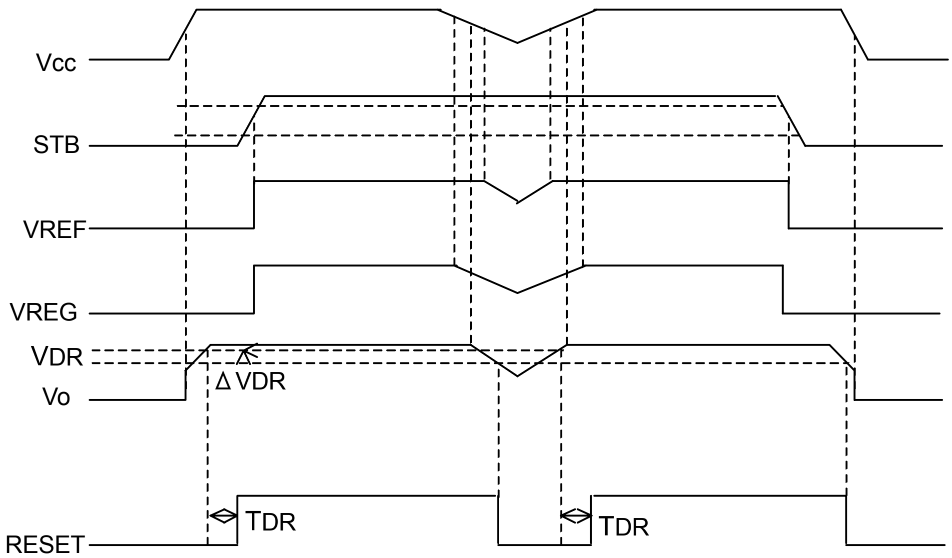


Fig. 29

●Selecting application components

1) 3.3 V regulator

- A capacitor used to eliminate oscillation must be inserted between the VOUT and GND pins. Variations in the capacitance or ESR, due to temperature variations or other factors, may result in oscillation. It is recommended to use a 4.7μF (or higher) ceramic capacitor or an electrolytic capacitor with an ESR of 0.1 Ω to 5 Ω to stop oscillation.

- Protection circuits
  Over current protection circuit
  The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures.

- Back current when Vcc is shorted
  The BD9400BFP does not incorporate a built-in back current protection circuit that operates when Vcc is shorted with the GND pin. To prevent back current, if necessary, a back current prevention diode can be inserted directly into the current flow.

2) RESET
The detection threshold voltage determines the reset triggering point. Regulator output will switch on/off whenever the voltage applied to the input reaches the threshold voltage. A hyst of 50 mV (Typ.) is added to the reset trigger point to eliminate output shudder. The delay time to be implemented when clearing the reset can be set with the CT pin capacitor. An input of 1 V or higher is required for full circuit operation.

3) VREF
Connect a 0.47μF to 10 μF capacitor to VREF pin for noise reduction.

4) VREG
Connect a 0.47μF to 10 μF capacitor to the VREG pin for noise reduction.

5) OSC
The triangular waveform oscillator frequency is determined with the RT pin's resistor and the CT pin's capacitor.
For more information about the RT and CT settings and corresponding frequencies, see Figure 30.
Set the RT resistor from 10 kΩ to 100 kΩ, and the CT pin's capacitor from 33 pF to 2,200 pF.

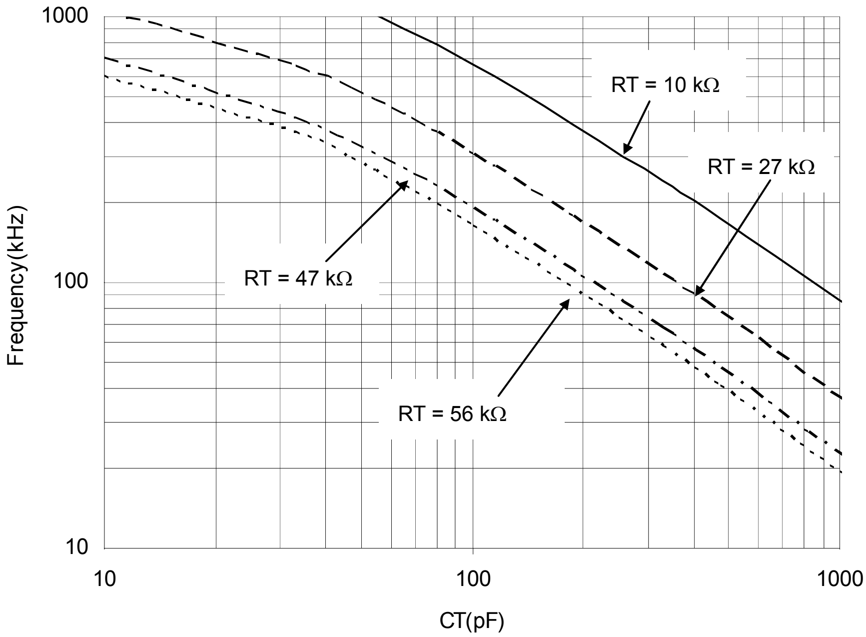


Fig. 30

●I/O Equivalent circuits

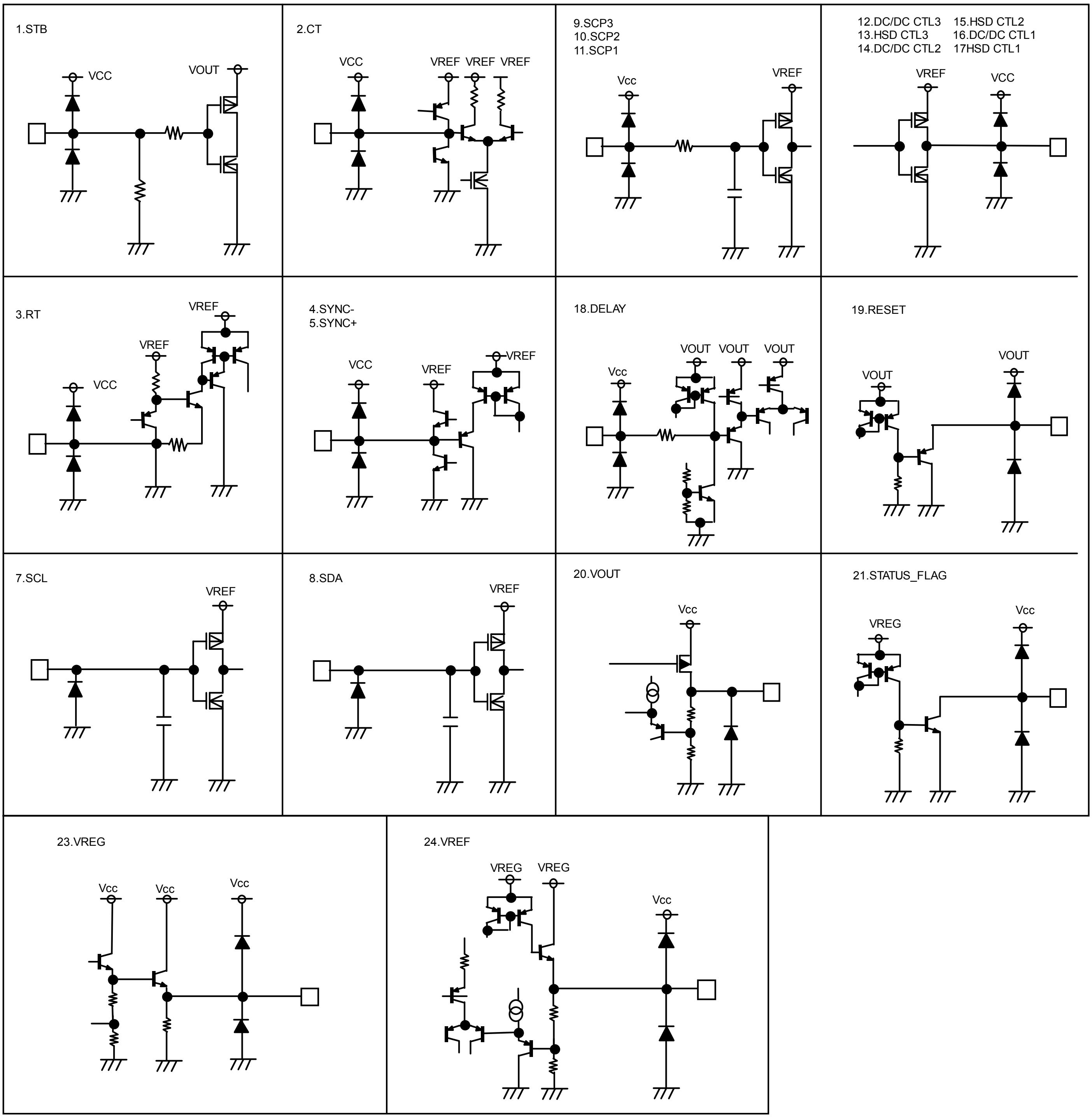


Fig. 31

●**Operation Notes**

1. Absolute maximum ratings

   Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.

2. GND potential

   Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.

3. Thermal design

   Perform thermal design, in which there are adequate margins, by taking into account the permissible dissipation (Pd) in actual states of use.

4. Short circuit between terminals and erroneous mounting

   Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.

5. Operation in strong electromagnetic field

   Using the ICs in a strong electromagnetic field can cause operation malfunction.

6. Testing on application boards

   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

7. Regarding input pin of the IC (Fig. 33)

   This monolithic IC contains P^+ isolation and P substrate layers between adjacent elements to keep them isolated. P–N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

   When GND > Pin A and GND > Pin B, the P–N junction operates as a parasitic diode.

   When Pin B > GND > Pin A, the P–N junction operates as a parasitic transistor.

   Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

8. Ground wiring patterns

   The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

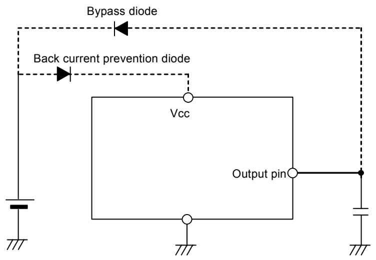
9. Thermal Shutdown Circuit (TSD)

   The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

10. Over current protection circuit

    The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures.

11. When the Vcc pin is opposite in voltage to each pin in the application, the internal circuit or element may be damaged. For example, such damage might occur when Vcc is shorted with the GND pin while an external capacitor is charged.
Use the output pin capacity with a maximum capacitance of 1000 μF. It is recommended to insert a diode in order to prevent back current flow in series with Vcc or bypass diodes between Vcc and each pin.



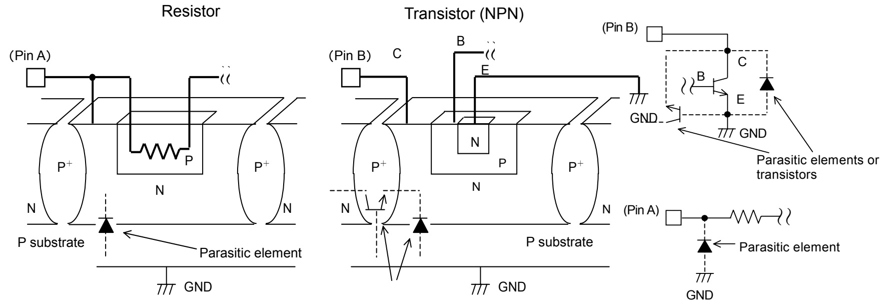
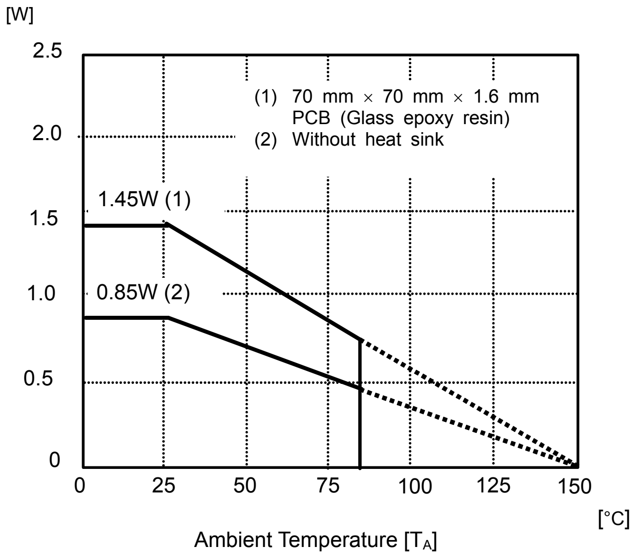


Fig . 32 Bypass diode

Fig. 33 Example of Simple Bipolar IC Architecture

●**Power dissipation reduction**



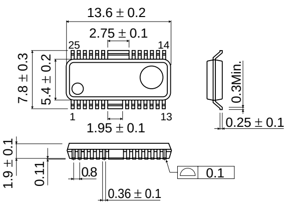
● Selecting a Model Name When Ordering

B	A		9	4	0	0	B		F	P	−	E	2

- ROHM model name: BA
- Model name: 9400B
- Package: FP: HSOP25
- Packaging specifications: E2: Emboss taping

HSOP25

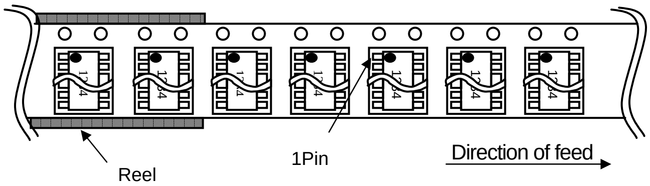
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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