



**THE DATASHEET OF
BD9896FV-E2**



| | |
|-----------------|---|
| STRUCTURE | Silicon Monolithic Integrated Circuit |
| NAME OF PRODUCT | DC-AC Inverter Control IC |
| TYPE | BD9896FV |
| FUNCTION | <ul style="list-style-type: none"> • 2ch control with Push-Pull • Lamp current and voltage sense feed back control • Sequencing easily achieved with Soft Start Control • Circuit protection with Timer Latch • Under Voltage Lock Out • Over Voltage Protection • Mode-selectable the operating or stand-by mode by stand-by pin • BURST mode controlled by PWM and DC input • Output linear Controllable Analog dimming by external DC voltage • Synchronous operating the other several BD9896FV IC' s |

○Absolute Maximum Ratings (Ta = 25°C)

| Parameter | Symbol | Limits | Unit |
|------------------------------|--------|----------|------|
| Supply Voltage | Vcc | 15 | V |
| Operating Temperature Range | Topr | -40~+90 | °C |
| Storage Temperature Range | Tstg | -55~+150 | °C |
| Power Dissipation | Pd | 1062* | mW |
| Maximum Junction Temperature | Tjmax | +150 | °C |

*Pd derated at 8.5mW/°C for temperature above Ta = 25°C (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○Recommended operating condition

| Parameter | Symbol | Limits | Unit |
|------------------------------|------------------|-----------|------|
| Supply voltage | Vcc | 6.0~14.0 | V |
| Output oscillation frequency | f _{out} | 25~90 | kHz |
| BCT oscillation frequency | f _{BCT} | 0.05~1.00 | kHz |

Status of this document

The Japanese version of this document is the official specification.

Please use the translation version of this document as a reference to expedite understanding of the official version.

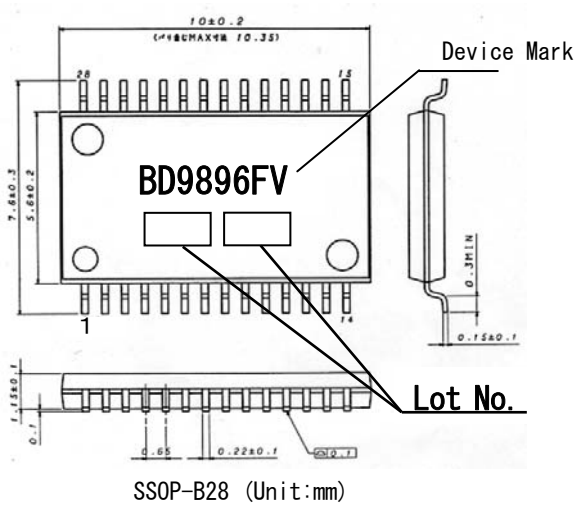
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○Electric Characteristics (Ta=25°C, VCC=7V)

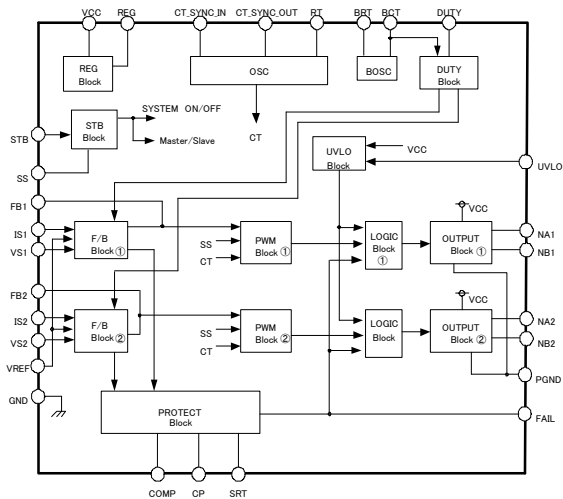
| Parameter | Symbol | Limits | | | Unit | Conditions |
|---------------------------------------|---------------------|----------|---------|----------|------|-------------------------------|
| | | MIN. | TYP. | MAX. | | |
| ((WHOLE DEVICE)) | | | | | | |
| Operating current | Icc1 | — | — | 17.0 | mA | CT_SYNC_IN=Low |
| Stand-by current | Icc2 | — | — | 10 | μA | CT_SYNC_IN=OPEN |
| ((OVER VOLTAGE DETECT)) | | | | | | |
| FB over voltage detect voltage | Vovf | 2.20 | 2.40 | 2.60 | V | |
| ((STAND BY CONTROL)) | | | | | | |
| Stand-by voltage L | VstL | -0.3 | — | 0.8 | V | |
| Input voltage range of Slave setting | Vsth1 | 1.8 | — | 2.25 | V | |
| Input voltage range of Master setting | Vsth2 | 2.55 | — | VCC | V | |
| ((TIMER LATCH)) | | | | | | |
| Timer Latch voltage | Vcp | 1.9 | 2.0 | 2.1 | V | |
| Timer Latch current | Icp | 0.5 | 1.0 | 1.5 | μA | |
| ((BURST MODE)) | | | | | | |
| BOSC Max voltage | VburH | 1.94 | 2.0 | 2.06 | V | fBCT=0.3kHz |
| BOSC Min Voltage | VburL | 0.4 | 0.5 | 0.6 | V | fBCT=0.3kHz |
| BOSC constant current | IBCT | 1.35/BRT | 1.5/BRT | 1.65/BRT | A | |
| BOSC frequency | fBCT | 292.5 | 300 | 307.5 | Hz | BRT=36kΩ BCT=0.048μF |
| ((OSC BLOCK)) | | | | | | |
| MAX DUTY | MAXDUTY | 44 | 46.5 | 49 | % | fout=60kHz |
| Soft start current | Iss | 1.0 | 2.0 | 3.0 | μA | |
| IS COMP detect Voltage | Visc | 0.45 | 0.50 | 0.55 | V | |
| SS COMP detect voltage | Vssc | 2.0 | 2.2 | 2.4 | V | |
| SRT ON resistance | RSRT | — | 200 | 400 | Ω | |
| ((UVLO BLOCK)) | | | | | | |
| Detect voltage (VCC_UVLO) | Vcc_vuvlo | 5.100 | 5.300 | 5.500 | V | |
| Hysteresis width (VCC_UVLO) | ΔVcc_vuvlo | 0.150 | 0.200 | 0.250 | V | |
| Operating voltage (UVLO) | Vuvlo | 2.260 | 2.340 | 2.420 | V | |
| Hysteresis width (UVLO) | ΔVuvlo | 0.075 | 0.100 | 0.125 | V | |
| ((REG BLOCK)) | | | | | | |
| REG output voltage | VREG | 3.038 | 3.100 | 3.162 | V | |
| REG source current | IREG | 5.0 | — | — | mA | |
| ((FEED BACK BLOCK)) | | | | | | |
| IS threshold voltage ① | Vis① | 1.225 | 1.250 | 1.275 | V | VREF pin:OPEN, REG is shorted |
| IS threshold voltage ② | Vis② | — | VREFIN | VIS① | V | VREF pin is supplied |
| VS threshold voltage | Vvs | 1.220 | 1.250 | 1.280 | V | |
| IS source current 1 | Iis1 | — | — | 1.5 | μA | DUTY=2.2V |
| IS source current 2 | Iis2 | 13.0 | 20.0 | 27.0 | μA | DUTY=0V, IS=0.5V |
| VS source current | Ivs | — | — | 1.0 | μA | |
| VREF input voltage range | VREF IN | 0.6 | — | 1.6 | V | Over 1.25V is not effective |
| ((OUTPUT BLOCK)) | | | | | | |
| NB c h output voltage H | VoutNBH | VCC-0.3 | VCC-0.1 | — | V | |
| NA c h output voltage H | VoutNAH | VCC-0.3 | VCC-0.1 | — | V | |
| NB c h output voltage L | VoutNBL | — | 0.1 | 0.3 | V | |
| NA c h output voltage L | VoutNAL | — | 0.1 | 0.3 | V | |
| NB c h output sink resistance | RsinkNB | — | 5 | 10 | Ω | I _{sink} = 10mA |
| NB c h output source resistance | RsourceNB | — | 8 | 16 | Ω | I _{source} = 10mA |
| NA c h output sink resistance | RsinkNA | — | 5 | 10 | Ω | I _{sink} = 10mA |
| NA c h output source resistance | RsourceNA | — | 8 | 16 | Ω | I _{source} = 10mA |
| Drive output frequency | fout | 57.9 | 60.0 | 62.1 | KHz | RT=15.94kΩ |
| ((COMP BLOCK)) | | | | | | |
| Overr voltage detect | VCOMP | 2.4 | 2.5 | 2.6 | V | |
| Hysteresis width (COMP) | ΔVCOMP | 0.040 | 0.060 | 0.080 | V | |
| ((PROTECT CLOCK)) | | | | | | |
| FAIL-pin On resistor value | R_FAIL | — | 200 | 400 | Ω | |
| ((SYNCRO BLOCK)) | | | | | | |
| CT_SYNC_IN_High input Voltage Range | VCT_SYNC_IN_H | 2.0 | — | VCC+0.8 | V | |
| CT_SYNC_IN_Low input Voltage Range | VCT_SYNC_IN_L | -0.3 | — | 1.5 | V | |
| CT_SYNC_IN Pull-up resistor | RCT_SYNC_IN_pull_up | 500 | — | — | kΩ | |
| CT_SYNC_IN Self-oscillation voltage | VCT_SYNC_IN | VCC*0.9 | — | VCC | V | |
| CT_SYNC_OUT sink resistor value | RCT_SYNC_OUT_sink | — | 150 | 300 | Ω | |
| CT_SYNC_OUT source resistor value | RCT_SYNC_OUT_source | — | 370 | 740 | Ω | |
| CT_SYNC_OUT_High output Voltage Range | VCT_SYNC_OUT_H | 2.8 | 3.1 | 3.4 | V | |
| CT_SYNC_OUT_Low output Voltage Range | VCT_SYNC_OUT_L | — | — | 0.5 | V | |
| SRT SYNC Exchange detect Voltage | Vsrvc | 0.5 | 0.8 | 1.1 | V | |

(This product is not designed for normal operation with in a radio active environment.)

○Package Dimensions



○Block Diagram



○Pin Description

| 端子番号 | 端子名 | 機能 |
|------|-------------|--|
| 1 | NA1 | FET driver for 1ch |
| 2 | NB1 | FET driver for 1ch |
| 3 | CP | External capacitor from CP to GND for Timer Latch |
| 4 | REG | Internal regulator output |
| 5 | FAIL | Protect clock output |
| 6 | VREF | Reference voltage |
| 7 | CT_SYNC_OUT | Output pin of CT synchronous signal |
| 8 | CT_SYNC_IN | Input pin of CT synchronous signal |
| 9 | RT | External resistor from SRT to RT for adjusting the triangle oscillator |
| 10 | SRT | External resistor from SRT to RT for adjusting the triangle oscillator |
| 11 | GND | GROUND |
| 12 | BCT | External capacitor from BCT to GND for adjusting the BURST triangle oscillator |
| 13 | BRT | External resistor from BRT to GND for adjusting the BURST triangle oscillator |
| 14 | DUTY | Control PWM mode and BURST mode |
| 15 | STB | Stand-by switch, Master/Slave selection |
| 16 | VS2 | Error amplifier input④ |
| 17 | IS2 | Error amplifier input③ |
| 18 | FB2 | Error amplifier output② |
| 19 | VS1 | Error amplifier input② |
| 20 | IS1 | Error amplifier input① |
| 21 | FB1 | Error amplifier output① |
| 22 | SS | External capacitor from SS to GND for Soft Start Control |
| 23 | COMP | Over voltage detector |
| 24 | VCC | Supply voltage input |
| 25 | UVLO | External Under Voltage Lock OUT |
| 26 | NB2 | FET driver for 2ch |
| 27 | NA2 | FET driver for 2ch |
| 28 | PGND | Ground for FET drivers |

○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and the IC. Use adequate margins for steady state and transient characteristics.
2. Recommended Operating Range
The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however, the variation will be small.
3. Mounting Failures
Mounting failures, such as misdirection or miscounts, may harm the device.
4. Electromagnetic Fields
A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within $\pm 0.3V$ compared with the PGND pin
6. BD9896FV has the short circuit protection with Thermal Shut Down System. When STB or Vcc pin re-supplied, They enables to cancel the latch. If It rise the temperature of the chip more than 170°C(TYP), It make the external FET OFF
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
10. By STB voltage, BD9896FV is changed to 3 states. Therefore, do not input STB pin voltage between one state and the other state (0.8~1.8, 2.25~2.55).

11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
12. This IC is a monolithic IC which (as shown is Fig-1)has P⁺ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,

○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)

○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND(P substrate)voltage to an input pin.

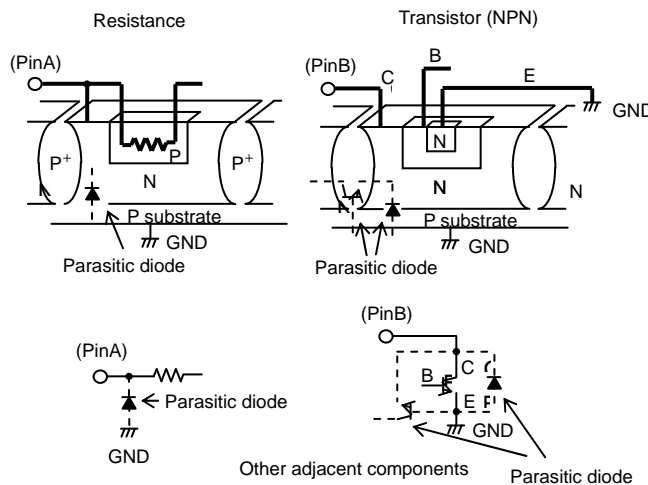


Fig-1 Simplified structure of a Bipolar IC

Notes

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