THE DATASHEET OF

MP2454GQ-Z

MP2454

36V, 0.6A
Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2454 is a frequency-programmable (350kHz to 2.3MHz), step-down switching regulator with an integrated internal high-side, high-voltage power MOSFET. It outputs efficiently up to 0.6A and has current-mode control for fast loop response.

The wide 3.3V to 36V input range accommodates a variety of step-down applications in automotive-input environments. A 3.5μA shutdown mode quiescent current allows for use in battery-powered applications. Also, the device has a high duty cycle and low drop-out mode for automotive cold-crank conditions.

The MP2454 achieves high-power conversion efficiency over a wide load range by scaling down the switching frequency at light-load conditions to reduce both switching and gate driving losses.

Frequency foldback prevents inductor current runaway during start-up and short circuit. Thermal shutdown provides reliable, fault-tolerant operation. An open-drain power good (PG) signal indicates when the output is within its nominal voltage.

The MP2454 is available in MSOP-10 EP and QFN-10 (3mm x 3mm) packages.

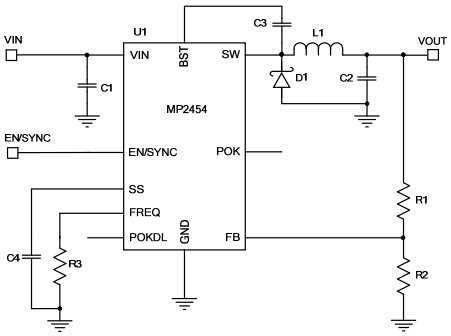
FEATURES

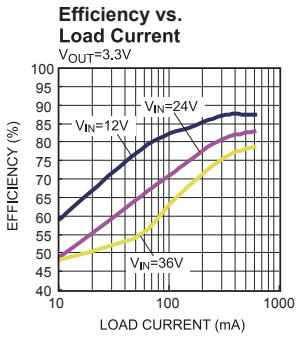
- 60μA Operating Quiescent Current
- Wide 3.3V to 36V Operating Input Range
- 200mΩ Internal Power MOSFET
- Up to 2.3MHz Programmable Switching Frequency
- Stable with Ceramic Output Capacitors
- Internal Compensation
- External Soft Start
- > 90% Efficiency
- Low Dropout Operation for Cold Crank
- 3.5μA Low Shutdown Supply Current
- Synchronization to External Clock
- Power Good Output
- Programmable Power Good Delay Time
- MSOP-10 EP and QFN-10 (3mm x 3mm) Packages

APPLICATIONS

- High-Voltage Power Conversion
- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2454GH	MSOP-10 EP	*See Below*
MP2454GQ	QFN-10 (3mm x 3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP2454GH–Z)

TOP MARKING (MP2454GH)

YWLLL
M2454

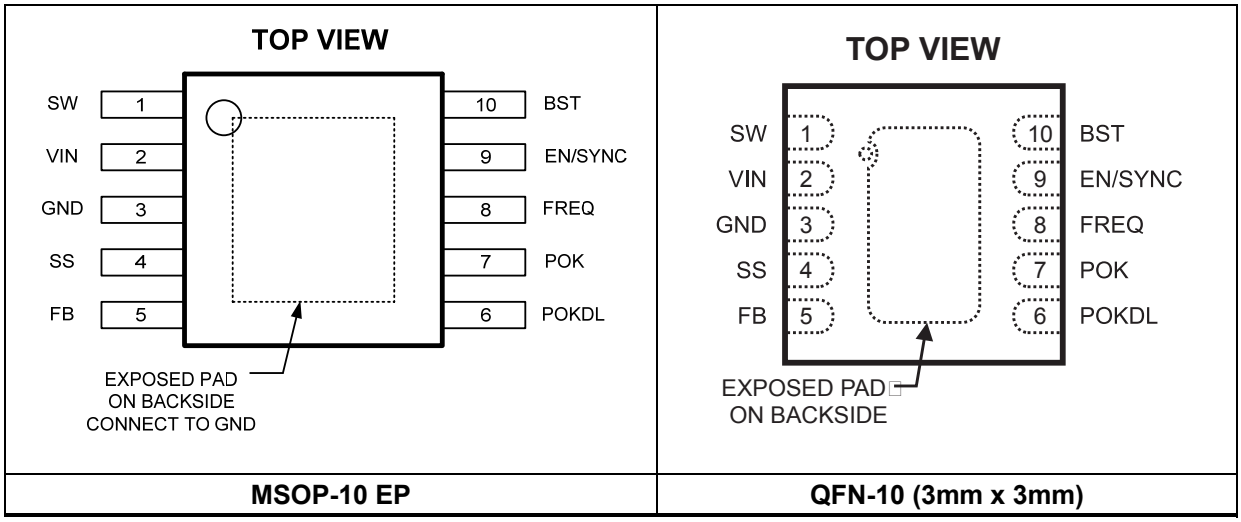
Y: Year code
W: Week code
LLL: Lot number
M: Product code of MP2454GH
2454: Four digits of the part number

TOP MARKING (MP2454GQ)

AEFY
LLL

AEF: Product code of MP2454GQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



MSOP-10 EP	QFN-10 (3mm x 3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to 40V
Switch voltage (V_{SW}) .....–0.3V to $V_{IN\ (MAX)}$+0.3V
BST to SW .....-0.3 to 6.0V
All other pins .....-0.3V to 5.0V
EN sink current 150µA
Continuous power dissipation .... (T_A = +25°C) (2)
MSOP-10 EP 2.27W
QFN-10 (3mm x 3mm)..... 2.50W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to 150°C

Recommended Operating Conditions

Supply voltage (V_{IN}) .....3.3V to 36V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
MSOP-10 EP	55	12...	°C/W
QFN-10 (3mm x 3mm).....	50	12...	°C/W

NOTES:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A). The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\ \theta_{JA}$. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_A= +25°C, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
Feedback voltage	V_{IN} = 3.3V to 36V	0.784	0.8	0.816	V
Switch on resistance	V_{BST} - V_{SW} = 5V		200	350	mΩ
Switch leakage	V_{EN} = 0V, V_{SW} = 0V		0.1	1	μA
Current limit	Duty Cycle = 30%	1	1.8	2.7	A
VIN UVLO rising threshold		2.6	2.9	3.2	V
VIN UVLO falling threshold		2.35	2.65	2.95	V
VIN UVLO hysteresis			0.25		V
Soft-start current	V_{SS} = 1.2V	0.9	1.8	2.7	μA
Oscillator frequency	R_{FREQ} = 130kΩ	300	400	500	kHz
	R_{FREQ} = 49.9kΩ	800	1000	1200	kHz
	R_{FREQ} = 17.4kΩ	1840	2300	2760	kHz
Sync. frequency range		350		2300	kHz
Minimum switch-on time(4)			60		ns
Shutdown supply current	V_{EN} = 0V		3.5	10	μA
Quiescent supply current	No load, V_{FB} = 0.83V, V_{BST} - V_{SW} = 5.5V		60	85	μA
EN input logic-low voltage				1	V
EN input logic-high voltage		1.8			V
POK threshold	FB in respect to the nominal value, V_{OUT} rising		90		%
	FB in respect to the nominal value, V_{OUT} falling		107		%
POK hysteresis	FB in respect to the nominal value		4.5		%
POK output voltage low	I_{SINK} = 5mA			0.4	V
POK delay current source		0.9	1.8	2.7	μA
Thermal shutdown(4)			170		°C
Thermal shutdown hysteresis(4)			25		°C

NOTE:

4) Derived from bench characterization. Not tested in production.

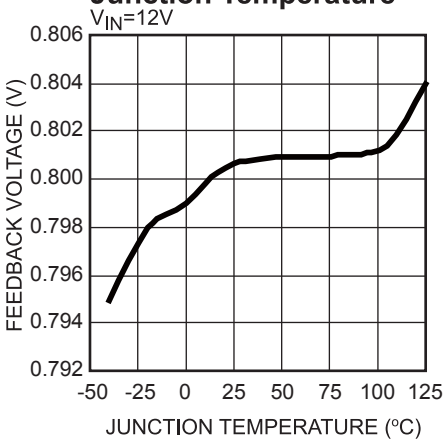
PIN FUNCTIONS

Pin #	Name	Description
1	SW	**Switch node.** The output from the high-side switch. SW requires a low V_F Schottky diode to ground (close to SW) to reduce switching spikes.
2	VIN	**Input supply**. VIN provides power to all the internal control circuitry (both the BST regulators and the high-side switch). VIN requires a decoupling capacitor to ground (close to VIN) to minimize the switching spikes.
3	GND	**Ground.** Place the output capacitor as close to GND as possible to shorten the high-current switching paths.
4	SS	**Soft start.** Place a capacitor from SS to SGND to set the soft-start period. The MP2454 sources 1.8μA from SS to the soft-start capacitor at start-up. As the SS voltage rises, the feedback threshold voltage increases to limit the inrush current during start-up.
5	FB	**Feedback.** Connect FB to the tap of the external resistor divider. The feedback threshold voltage is 0.8V.
6	POKDL	**POK signal delay.** Connect a capacitor from POKDL to GND to program the POK signal delay time.
7	POK	**Open-drain power good output.** POK goes high when V_O is within the ±10% window of the nominal voltage. POK is pulled down during shutdown.
8	FREQ	**Switching frequency program.** Connect a resistor from FREQ to ground to set the switching frequency.
9	EN/SYNC	**Enable and SYNC input.** Pull EN/SYNC below the specified threshold to shut the chip down. Pull EN/SYNC above the specified threshold to enable the chip. Floating EN/SYNC shuts the chip down. Apply a clock signal (350kHz to 2.3MHz) to synchronize the internal oscillator frequency to the external clock.
10	BST	**Bootstrap**. The positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between BST and SW.
	Exposed Pad	Connect the exposed pad to the GND plane to optimize thermal performance.

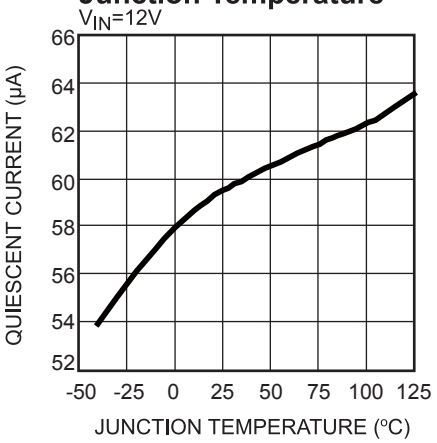
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, C_{OUT} = 2 x 10µF, f_S = 1MHz, T_A = +25°C, unless otherwise noted.

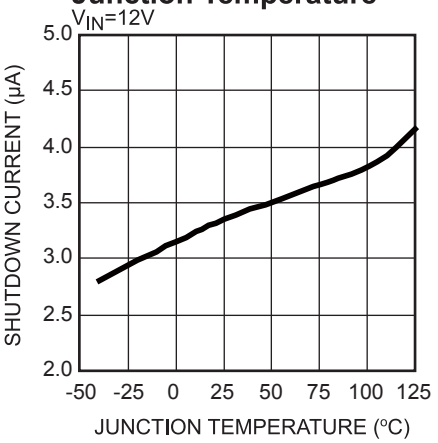
Feedback Voltage vs. Junction Temperature



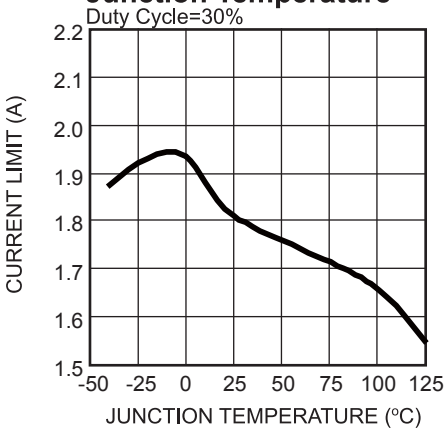
Quiescent Current vs. Junction Temperature



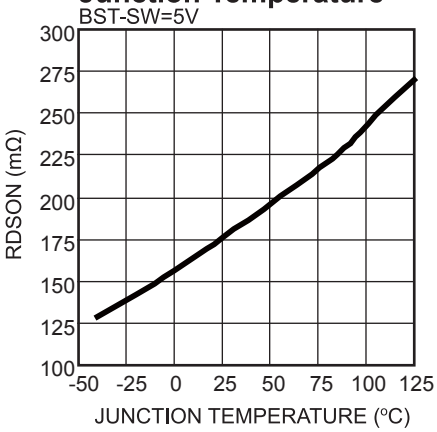
Shutdown Current vs. Junction Temperature



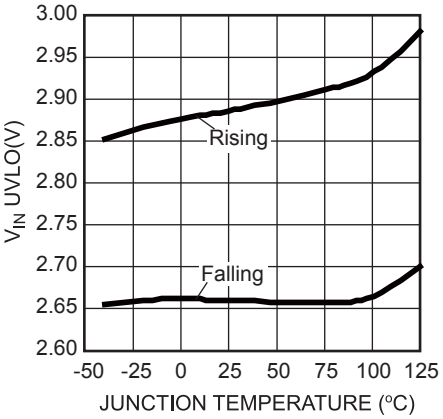
Current Limit vs. Junction Temperature



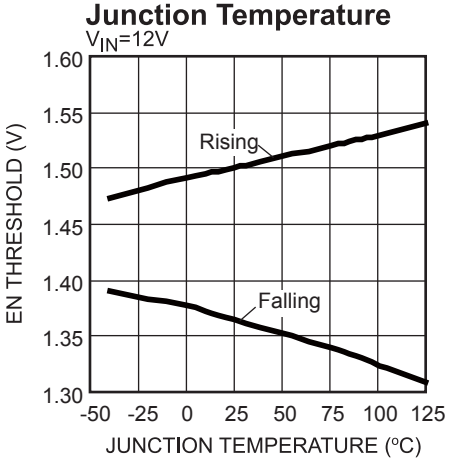
Switch-On Resistance vs. Junction Temperature



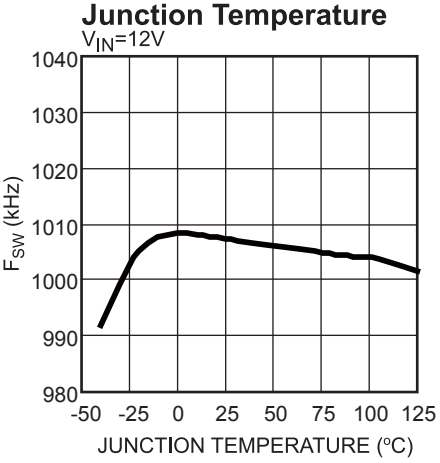
V_{IN} UVLO vs. Junction Temperature



EN Threshold vs. Junction Temperature



F_{SW} vs. Junction Temperature

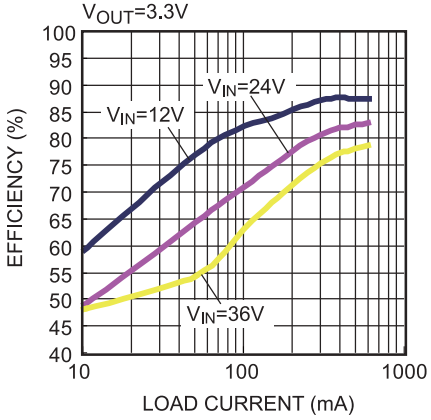


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, C_{OUT} = 2 x 10µF, f_S = 1MHz, T_A = +25°C, unless otherwise noted.

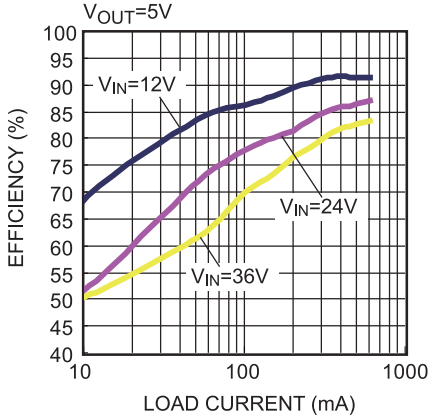
Efficiency vs. Load Current

V_{OUT}=3.3V

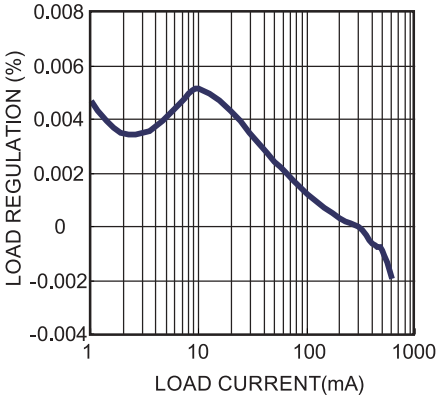


Efficiency vs. Load Current

V_{OUT}=5V

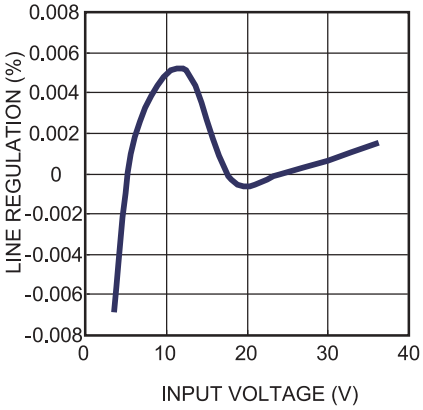


Load Regulation

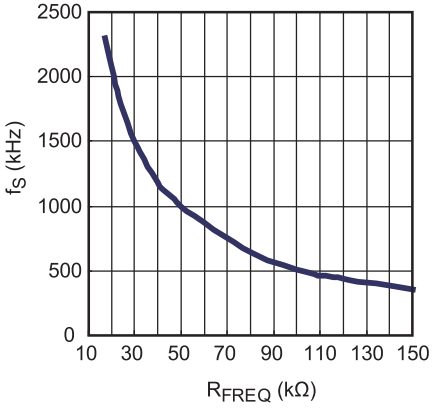


Line Regulation

I_{OUT}=0.3A



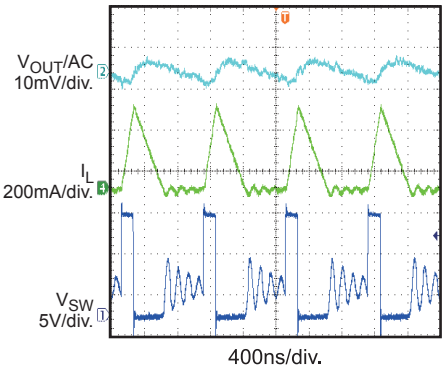
f_S vs. R_{FREQ}



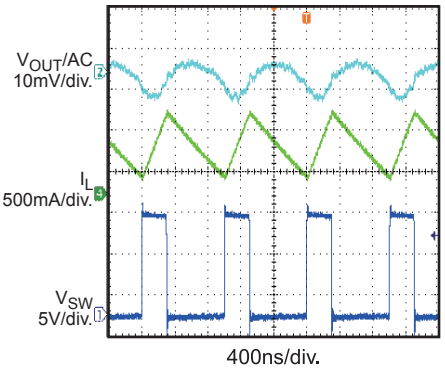
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, C_{OUT} = 2 x 10µF, f_S = 1MHz, T_A = +25°C, unless otherwise noted.

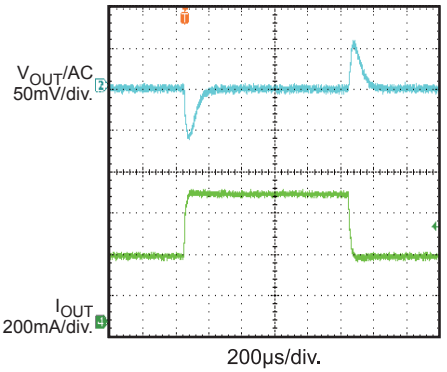
Steady State
I_{OUT}=0.1A



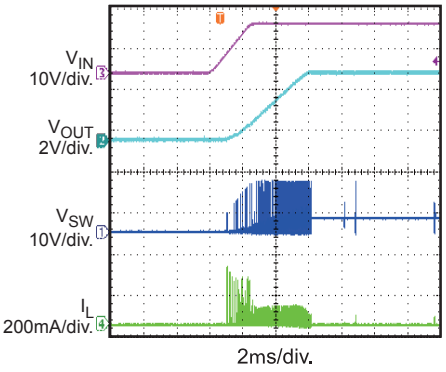
Steady State
I_{OUT}=0.6A



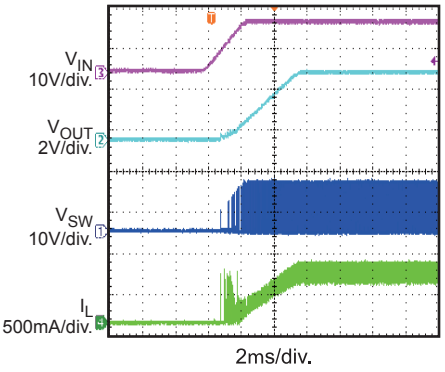
Load Transient
I_{OUT} = 0.3A-0.6A, 1.6A/µs



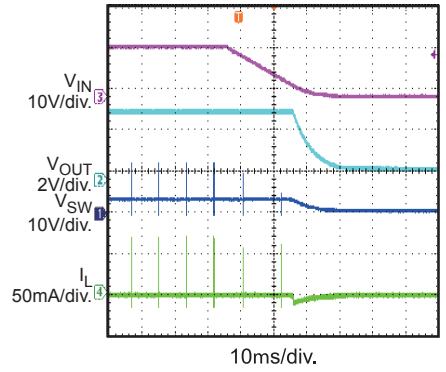
Start-Up through V_{IN}
I_{OUT} = 0A



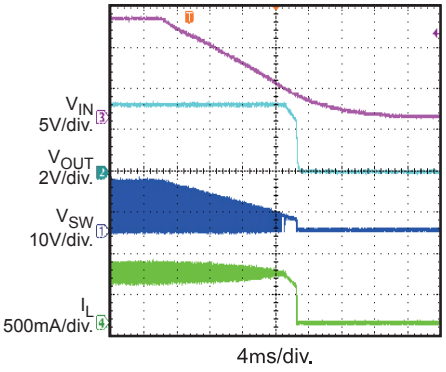
Start-Up through V_{IN}
I_{OUT} = 0.6A



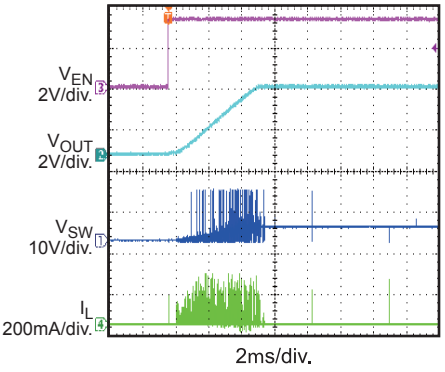
Shutdown through V_{IN}
I_{OUT} = 0A



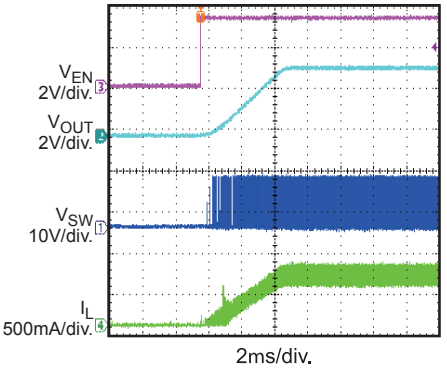
Shutdown through V_{IN}
I_{OUT} = 0.6A



Start-Up through EN
I_{OUT} = 0A



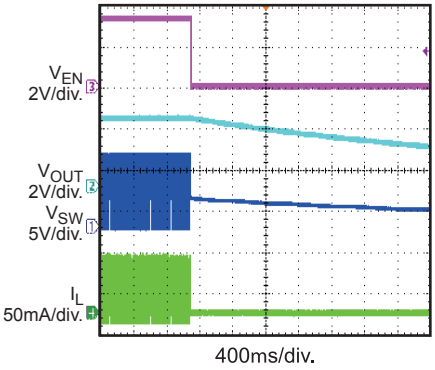
Start-Up through EN
I_{OUT} = 0.6A



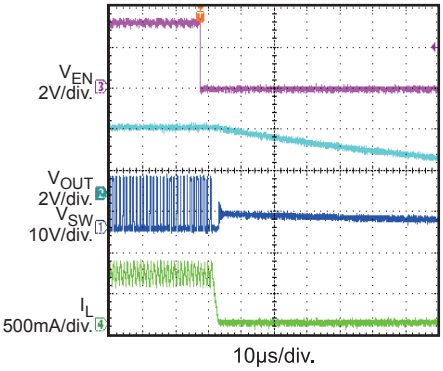
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, C_{OUT} = 2 x 10µF, f_S = 1MHz, T_A = +25°C, unless otherwise noted.

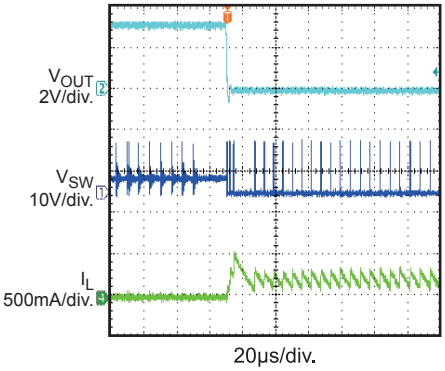
Shutdown through EN
I_{OUT}=0A



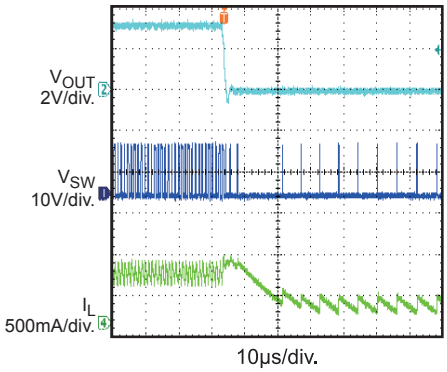
Shutdown through EN
I_{OUT}=0.6A



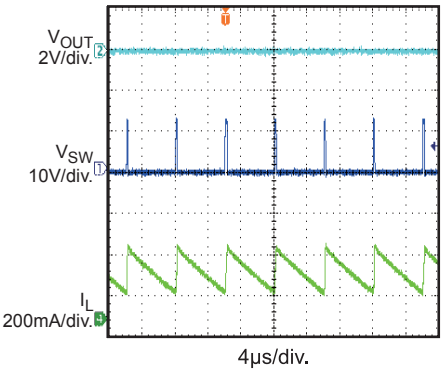
SCP Entry
I_{OUT}=0A to Short Circuit



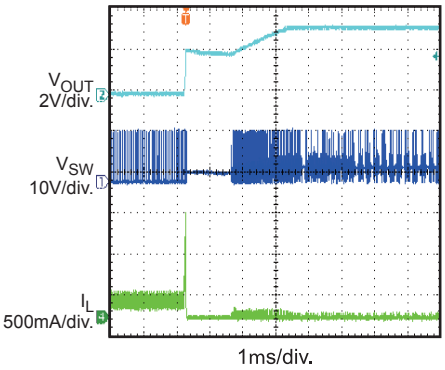
SCP Entry
I_{OUT}=0.6A to Short Circuit



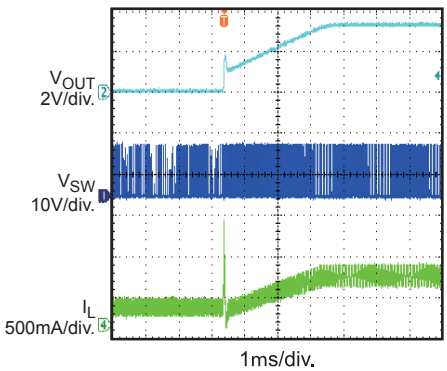
SCP Steady State



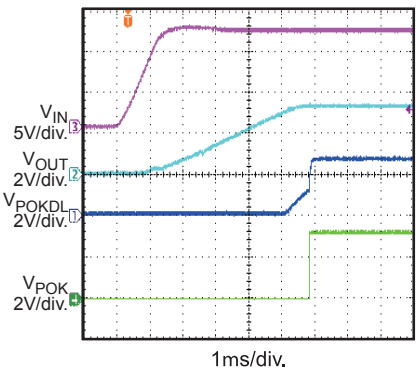
SCP Recovery
Short Circuit to I_{OUT}=0A



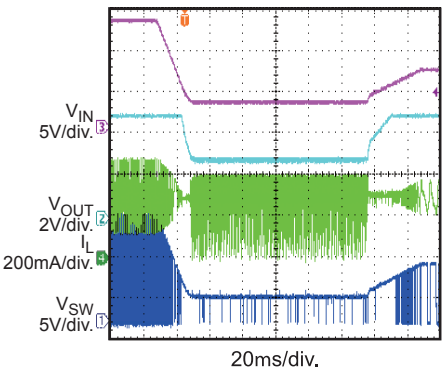
SCP Recovery
Short Circuit to I_{OUT}=0.6A



POK through Power On



Cold-Crank
V_{OUT} = 5V, I_{OUT} = 0.3A



FUNCTIONAL BLOCK DIAGRAM

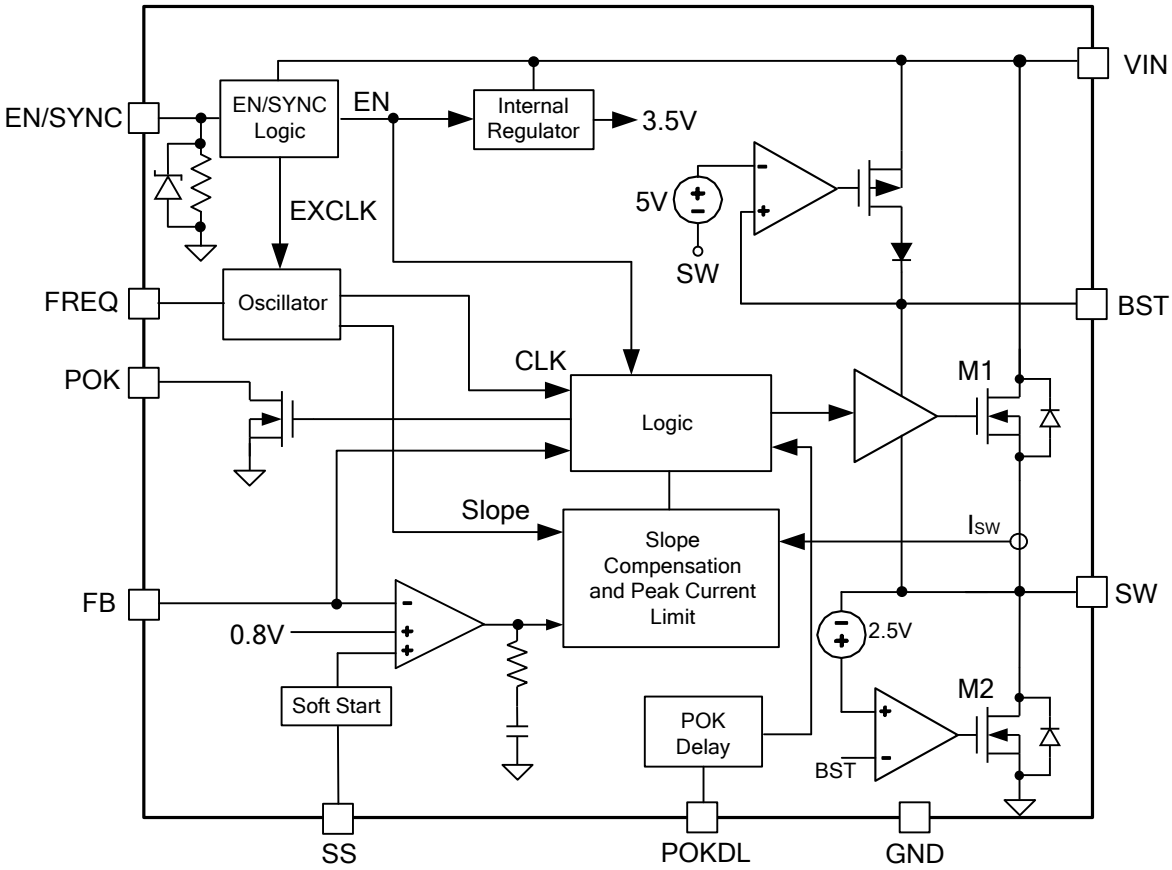


Figure 1: MP2454 Block Diagram

OPERATION

The MP2454 is a non-synchronous, step-down, switching regulator with an internal high-side, high-voltage power MOSFET. It provides an internally compensated, highly-efficient output of 0.6A with current-mode control.

It features a wide input voltage range, a switching frequency programmable up to 2.3MHz, an external soft start, and a precise current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

PWM Control

At moderate to high output currents, the MP2454 operates in a fixed frequency, peak-current-control mode to regulate the output voltage. Once the internal clock initiates a PWM cycle, the power MOSFET turns on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off for at least 100ns before the next cycle starts. If the current in the power MOSFET does not reach the COMP set current value (within one PWM cycle), the power MOSFET remains on, skipping a turn-off period.

Pulse-Skipping Mode

In light-load conditions, the MP2454 enters pulse-skipping mode to improve light-load efficiency. Pulse skipping occurs when the internal COMP voltage falls below the internal sleep threshold, which generates a pause command to block the turn-on clock pulse that controls the power MOSFET. The power MOSFET therefore does not turn on, subsequently reducing gate drive and switching losses. This pause command puts the chip largely into sleep mode, which consumes very low quiescent current and further improves the light-load efficiency.

When the COMP voltage exceeds the sleep threshold, the pause signal resets, so the chip enters normal PWM operation. Every time the pause signal goes from low to high, a signal turns on the power MOSFET.

Error Amplifier (EA)

The error amplifier circuit is composed of an internal op amp with an RC feedback network connected between its output node (internal COMP node) and GND. When the FB voltage (V_{FB}) is less than its internal reference voltage (V_{REF}), the op amp drives the COMP output higher, increasing the switch peak current output and hence increases the energy delivered to the output. Conversely, when V_{FB} rises above V_{REF}, the output energy drops.

When connecting to FB, connect FB to the tap of a resistor divider between V_O and GND.

Internal Regulator

The 3.5V internal regulator powers most of the internal circuitry. This regulator takes the V_{IN} input and operates in the full VIN range. When V_{IN} exceeds 3.5V, the output of the regulator is in full regulation; conversely, when V_{IN} is lower than 3.5V, the output degrades.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. A dedicated internal bootstrap regulator charges and regulates the bootstrap capacitor to about 5V. When the voltage between the BST and SW nodes falls below the regulation voltage, a PMOS pass transistor connected from VIN to BST turns on. The charging current path is from VIN to BST and then to SW. The external circuit must provide enough voltage headroom to facilitate charging.

As long as V_{IN} is sufficiently higher than SW, the bootstrap capacitor will charge. When the power MOSFET is on, V_{IN} is about equal to SW and prevents the bootstrap capacitor from charging.

When the external free-wheeling diode is on, the difference between V_{IN} to SW is at its largest, making this period the best time to charge. When there is no current in the inductor, SW equals V_O, so the difference between V_{IN} and V_O charges the bootstrap capacitor.

At higher duty cycles, the time period available for bootstrap charging is smaller, so the bootstrap capacitor may not fully charge. In case the external circuit does not have sufficient voltage and time to charge the bootstrap

capacitor, add external circuitry to ensure that the bootstrap voltage is in the normal operation region.

Low Dropout Operation (LDO)

The MP2454 is designed to operate at a 100% duty cycle as long as the voltage difference across BST to SW is greater than 2.5V; this improves dropout. When the voltage from BST to SW drops below 2.5V, an under-voltage lockout (UVLO) circuit turns off the high-side MOSFET (HS-FET), and an internal low-current switch pulls the SW node low to refresh the charge on the BST capacitor. After the BST capacitor voltage is re-charged, the HS-FET turns on again to regulate the output. Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor, thus increasing the effective duty cycle of the switching regulator. The low-dropout operation makes the MP2454 suitable for the automotive cold crank.

The voltage drop across the power MOSFET, the inductor resistance, the low-side diode, and the printed circuit board resistance influence heavily the effective duty cycle during regulator dropout.

Enable Control and Frequency Synchronization

EN/SYNC is a digital control pin that turns the regulator on and off. When EN is pulled below 1V for longer than 2μs, the chip enters the lowest shutdown current mode. Forcing EN/SYNC above 1.8V for longer than 200ns turns on the device. Internally, a 1.2MΩ resistor is connected from EN to GND. So when left floating, the device pulls EN down to GND, and the chip is disabled.

A Zener diode is connected from EN to GND internally. The typical clamping voltage of the Zener diode is 7.5V, so VIN can be connected to EN through a high value resistor if the system does not have another logic input acting as an enable signal. The resistor needs to be designed to limit the EN sink current to less than 150μA.

An external clock with a frequency range of 350kHz to 2.3MHz can be used to synchronize the device through EN/SYNC. The internal clock's rising edge is synchronized to the external clock's rising edge.

If a clock on period exceeds 4μs or an off period exceeds 2μs, the device interprets the signal as an enable input and disables synchronization.

Frequency Programmable

An external resistor (R_{FREQ}) from FREQ to GND sets the MP2454's oscillating frequency. For additional details on the relationship between R_{FREQ} and f_S, refer to the "Application Information" section.

The oscillating frequency is related to the FB voltage. When the FB voltage decreases, the oscillating frequency decreases accordingly and becomes one fifth of the nominal value (when FB is 0). This frequency foldback scheme prevents inductor current runaway during start-up or an output short circuit.

Under-Voltage Lockout (UVLO)

VIN UVLO protects the chip from operating at an insufficient supply voltage. The UVLO rising threshold is 2.9V while its falling threshold is 2.65V.

Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the soft-start period begins, an internal current source charges the external soft-start capacitor. When the SS voltage falls below the internal reference (REF), the SS overrides REF as the error amplifier reference. When SS exceeds REF, REF acts as the reference.
The SS time is calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

Where I_{SS} is the soft-start current, and V_{REF} is the 0.8V reference voltage. It can be used for tracking and sequencing.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from thermal runaway. When the die temperature exceeds the upper threshold (170°C), the entire

chip shuts down. When the temperature falls below the lower threshold (145°C), the chip is enabled again.

Current Comparator and Current Limit

A current sense MOSFET senses accurately the power MOSFET current. The sensed current goes to the high-speed current comparator for current-mode control. When the power MOSFET turns on, the comparator is blanked first (until the end of the turn-on transition) to reduce noise. Then, the comparator compares the power-switch current against the reference current set by the COMP voltage. When the power-switch current exceeds the reference current, the comparator outputs low to turn off the power MOSFET.

The maximum current of the internal power MOSFET is limited internally cycle-by-cycle. The current limit is related to the FB voltage and deceases as Vo decreases, which prevents inductor current runaway during start-up or an output short circuit.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and stable currents, and then the internal regulator is enabled. The regulator provides a stable supply for the rest of the circuit. After this occurs, the soft-start block starts working and output ramps up slowly.

Three events shut down the chip: V_{EN} low, V_{IN} low, and thermal shutdown. During shutdown, the signaling path is blocked initially to avoid triggering any faults. Then the COMP voltage and the internal supply rail are pulled down.

Power Good Output

The MP2454 includes an open-drain power good output that indicates whether the regulator's output is within ±10% of its nominal value. When the output voltage falls outside this range, the POK output is pulled to ground. It should be connected to a voltage source of no more than 5V through a resistor (e.g. 100kΩ). There is a 20μs de-glitch time when POK asserts high (if POKDL is left floating). The de-glitch time can be programmed by adding a capacitor on POKDL. To select a capacitor for POKDL, use Equation (2):

$$C_{DL}(nF) = \frac{t_{POKDL}(ms) \times I_{POKDL}(\mu A)}{V_{th\_POKDL}(V)} \quad (2)$$

Where I_{POKDL} is the POKD source current, and V_{th_POKDL} is 1.2V.

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APPLICATION INFORMATION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB. The voltage divider divides the output voltage down to the feedback voltage by the ratio from Equation (3):

$$V_{FB}=V_{OUT}\times\frac{R2}{R1+R2} \quad (3)$$

The output voltage is calculated by Equation (4):

$$V_{OUT}=V_{FB}\times\frac{R1+R2}{R2} \quad (4)$$

Choose R2 around 100kΩ, then R1 can be calculated by Equation (5):

$$R1=R2\times(\frac{V_{OUT}}{V_{FB}}-1) \quad (5)$$

For example, for a 3.3V output voltage, choose R2 as 95.3kΩ, then R1 is 300kΩ.

Setting the Switching Frequency

The switching frequency (f_S) is set using a resistor (R_{FREQ}) between FREQ and GND. Table 1 shows the recommended R_{FREQ} values for a typical f_S.

Table 1: f_S vs. R_{FREQ}

R_{FREQ} (kΩ)	f_S (kHz)
150	350
105	500
49.9	1000
30	1500
21	2000
17.4	2300

For detailed R_{FREQ} values for various f_s values, refer to the f_S vs. R_{FREQ} curve in the “Typical Performance Characteristics” section.

For high f_S applications (especially when V_{IN} is high and V_{OUT} is low), avoid kicking the minimum switch-on time. Once the minimum switch-on time is kicked, pulse skipping occurs, resulting in a large output ripple. The typical minimum switch-on time is 60ns. For V_{OUT} = 3.3V, the recommended operating input is 24V (or lower) at a 2MHz f_S and 20V (or lower) at a 2.3MHz f_S.

Output Rectifier Diode

An inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current, which results in lower output ripple voltage. However, the larger value inductor will be larger physically, have a higher series resistance, and/or lower saturation current.

A good rule for determining the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated using Equation (6):

$$L1=\frac{V_{OUT}}{f_s\times\Delta I_L}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage; f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current is calculated using Equation (7):

$$I_{LP}=I_{LOAD}+\frac{V_{OUT}}{2\times f_S\times L1}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Where I_{LOAD} is the load current.

Output Rectifier Diode

The output rectifier diode supplies the current to the inductor when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky diode.

Choose a diode with a maximum reverse voltage rating greater than the maximum input voltage, and a current rating that is greater than the maximum load current.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore, a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for best performance. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors will suffice.

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current. The input capacitor (C_{IN}) can be electrolytic, tantalum, or ceramic.

When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (i.e. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure they have enough capacitance to provide sufficient charge in order to prevent an excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Output Capacitor

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_{OUT}}\right) \quad (9)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

External Bootstrap Diode

An external bootstrap diode is recommended to reduce the quiescent current at no load and light load and enhance efficiency, especially for a high duty cycle (>65%) or high switching frequency applications (e.g. >2MHz).

At no load or light load, the part enters sleep mode, and the internal BST regulator turns off to save power. This makes the BST capacitor voltage drop easily to its UVLO and the internal low-side switch turn on frequently to refresh the BST capacitor. The high frequency switching brings in a relative high quiescent current. Adding an external BST diode reduces greatly the BST refresh frequency, thus producing a lower quiescent current.

A power supply between 3V and 5V can be used to power the external bootstrap diode. V_{OUT} is a good choice for this power supply (see Figure 2).

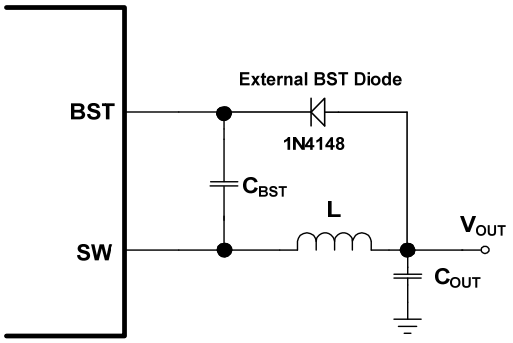
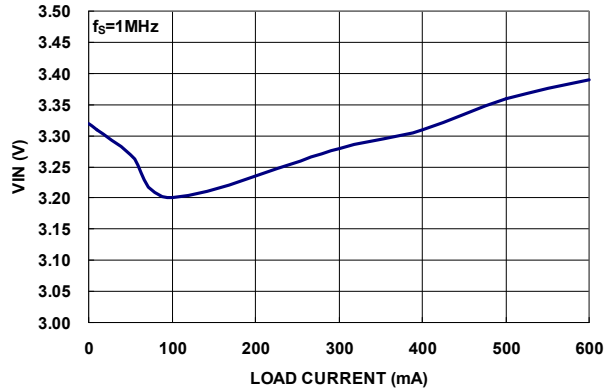


Figure 2: External Bootstrap Diode

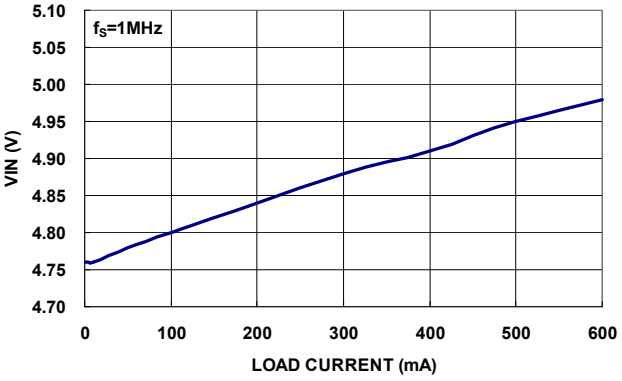
The bootstrap diode can be low cost (i.e., a IN4148 or a BAT54).

Minimum Input Voltage

The low dropout and active BST refresh operations allow the MP2454 to start up and regulate the output at a very low input voltage. Figure 3 shows the minimum input voltage necessary to regulate the output voltage within 5% of the nominal value (at different loads). Note that the minimum input voltage curve is the same when VIN ramps up or down.



(a) V_{OUT}=3.3V



(b) V_{OUT}=5V

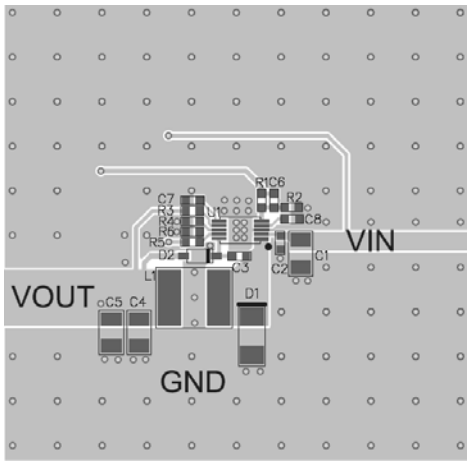
Figure 3 : Minimum Input Voltage vs. Load Current

PCB Layout Guidelines

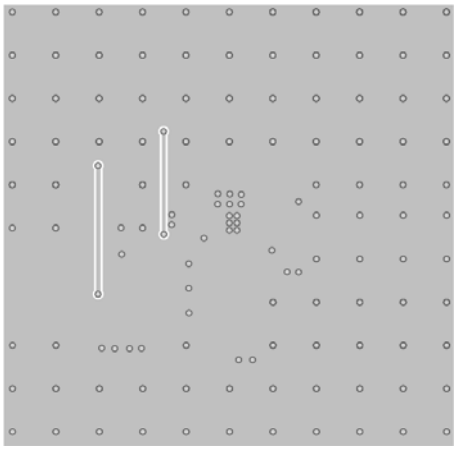
Efficient PCB layout is critical for stable operation. For best results, refer to Figure 4 and follow the guidelines below:

1) Keep the path of the switching current short and minimize the loop area formed by the input capacitor, high-side MOSFET, and Schottky diode.
2) Place the input capacitor as close to VIN as possible.
3) Keep the connection from the power ground→Schottky diode→SW as short and wide as possible.
4) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the chip as possible.
5) Route SW away from sensitive analog areas such as FB.
6) Connect IN, SW, the exposed pad, and especially GND to large copper areas to cool the chip for improved thermal performance and long-term reliability.

Below is the recommended PCB layout for the MSOP10 package. The recommended layout for the QFN10 package is similar.



Top Layer



Bottom Layer

Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

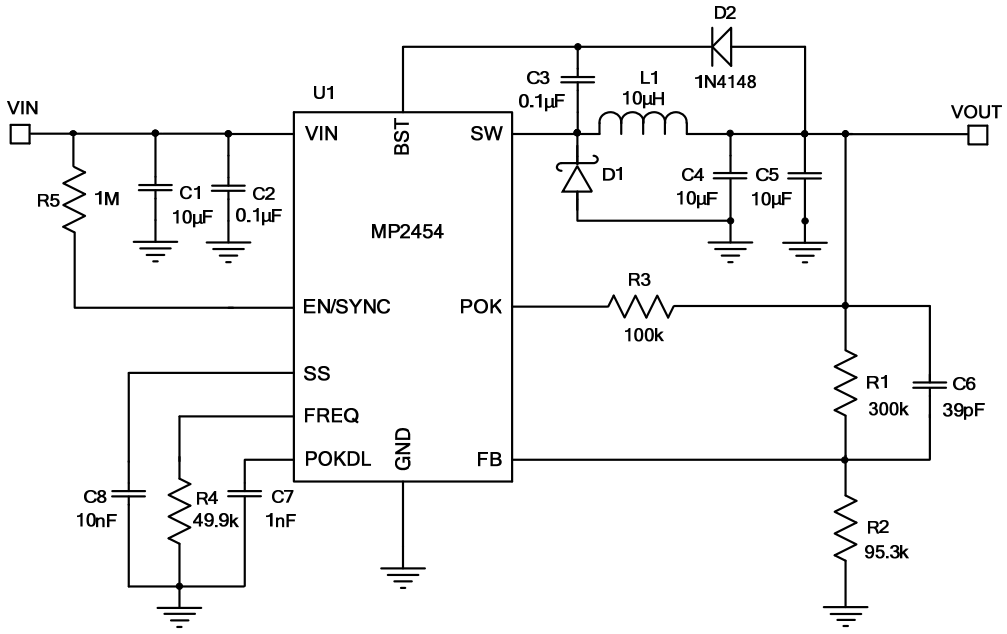
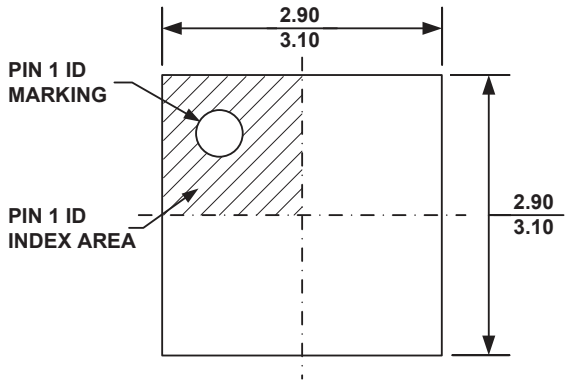


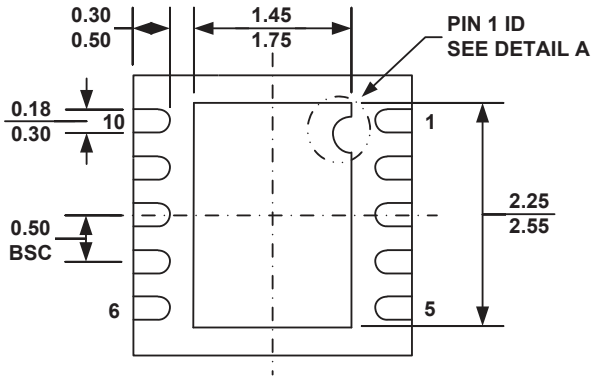
Figure 5: 3.3V Output Typical Application Circuit

PACKAGE INFORMATION

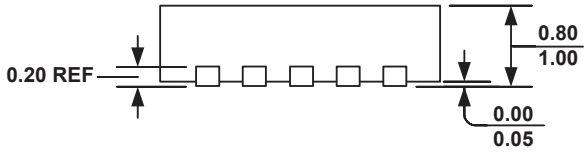
QFN-10 (3mm x 3mm)



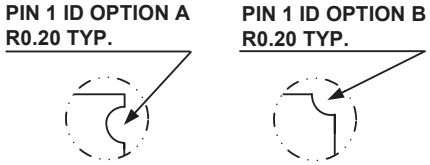
TOP VIEW



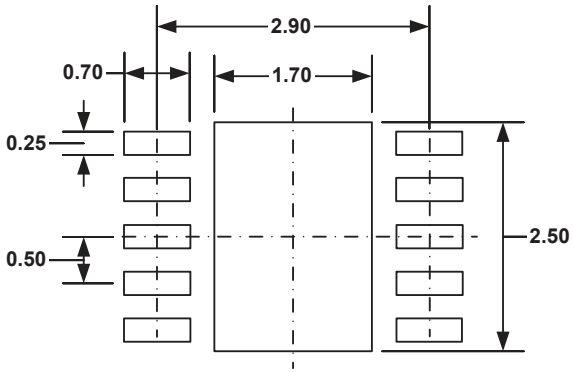
BOTTOM VIEW



SIDE VIEW



DETAIL A



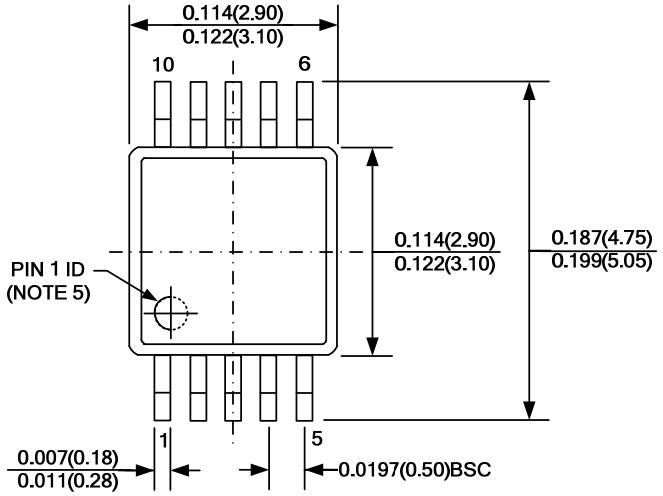
RECOMMENDED LAND PATTERN

NOTE:

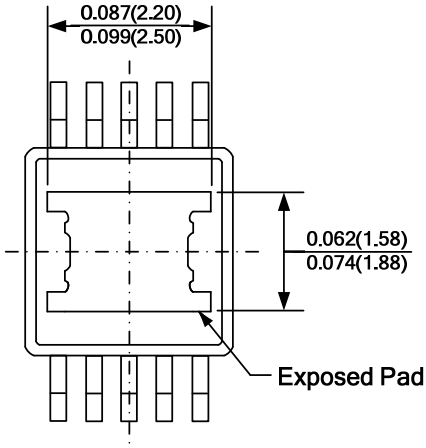
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

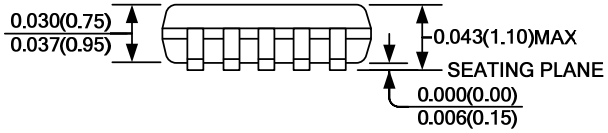
MSOP-10 EP



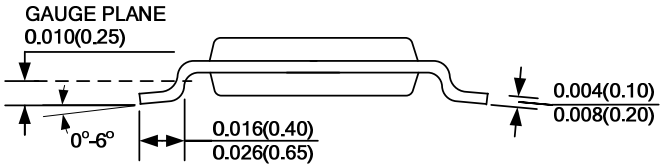
TOP VIEW



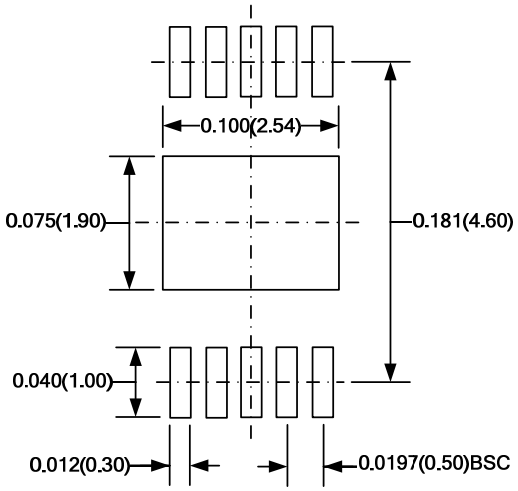
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION BA-T.
7) DRAWING IS NOT TO SCALE.

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