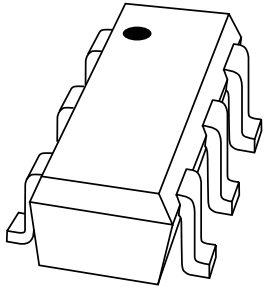


DATA SHEET



BF1203 Dual N-channel dual gate MOS-FET

Product specification
Supersedes data of 2000 Dec 04

2001 Apr 25



Dual N-channel dual gate MOS-FET

BF1203

FEATURES

- Two low noise gain controlled amplifiers in a single package
- Superior cross-modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio.

APPLICATIONS

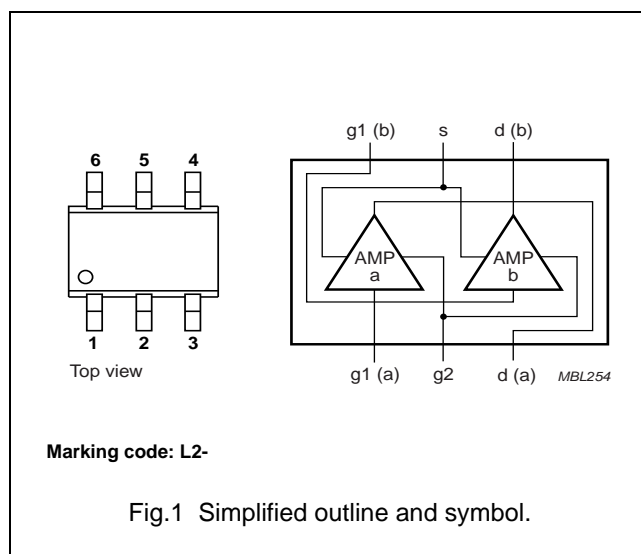
- Gain controlled low noise amplifiers for VHF and UHF applications with 3 to 9 V supply voltage, such as digital and analog television tuners and professional communications equipment.

DESCRIPTION

The BF1203 is a combination of two different dual gate MOS-FET amplifiers with shared source and gate 2 leads. The source and substrate are interconnected. Internal bias circuits enable DC stabilization and a very good cross-modulation performance during AGC. Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor is encapsulated in a SOT363 micro-miniature plastic package.

PINNING - SOT363

PIN	DESCRIPTION
1	gate 1 (a)
2	gate 2
3	drain (a)
4	drain (b)
5	source
6	gate 1 (b)



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per MOS-FET unless otherwise specified						
V_{DS}	drain-source voltage		–	–	10	V
I_D	drain current (DC)		–	–	30	mA
$ y_{fs} $	forward transfer admittance	amp. a: $I_D = 15$ mA	23	28	35	mS
		amp. b: $I_D = 12$ mA	25	30	40	mS
C_{ig1-s}	input capacitance at gate 1	amp. a: $I_D = 15$ mA; $f = 1$ MHz	–	2.6	3.1	pF
		amp. b: $I_D = 12$ mA; $f = 1$ MHz	–	1.7	2.2	pF
C_{rss}	reverse transfer capacitance	$f = 1$ MHz	–	15	–	fF
NF	noise figure	amp. a: $f = 400$ MHz; $I_D = 15$ mA	–	1	1.8	dB
		amp. b: $f = 800$ MHz; $I_D = 12$ mA	–	1.1	1.8	dB
X_{mod}	cross-modulation	amp. a: input level for $k = 1\%$ at 40 dB AGC	105	–	–	dB μ V
		amp. b: input level for $k = 1\%$ at 40 dB AGC	100	105	–	dB μ V

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

Dual N-channel dual gate MOS-FET

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

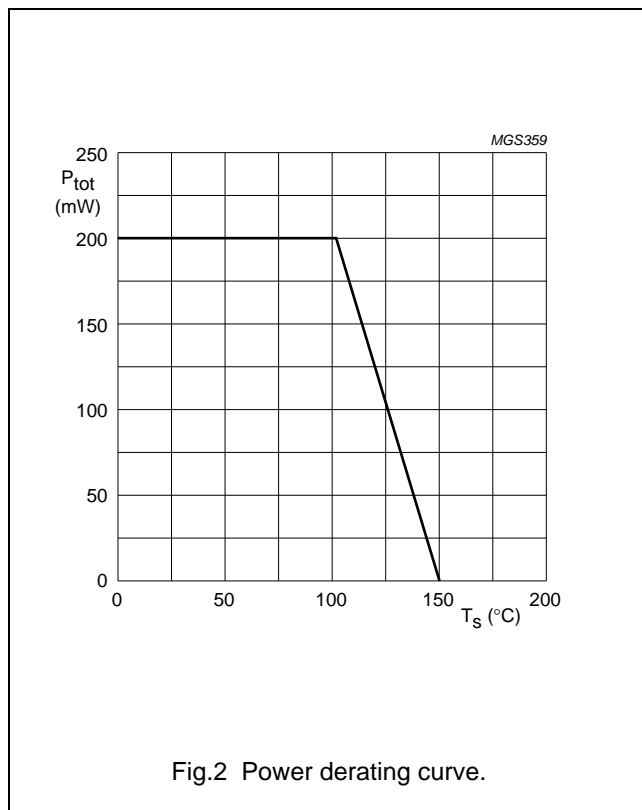
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per MOS-FET unless otherwise specified					
V _{DS}	drain-source voltage		–	10	V
I _D	drain current (DC)		–	30	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation	T _s ≤ 102 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	150	°C

Note

1. T_s is the temperature at the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-s}	thermal resistance from junction to soldering point	240	K/W



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STATIC CHARACTERISTICS $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per MOS-FET unless otherwise specified					
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\text{ }\mu\text{A}$	10	–	V
$V_{(BR)G1-SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0$; $I_{G1-S} = 10\text{ mA}$	6	10	V
$V_{(BR)G2-SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0$; $I_{G2-S} = 10\text{ mA}$	6	10	V
$V_{(F)S-G1}$	forward source-gate voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate-source threshold voltage	$V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate-source threshold voltage	$V_{DS} = 5\text{ V}$; $V_{G1-S} = 4\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	amp. a: $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_G = 62\text{ k}\Omega$; note 1	11	19	mA
		amp. b: $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_G = 120\text{ k}\Omega$; note 1	8	16	mA
I_{G1-S}	gate cut-off current	$V_{G1-S} = 5\text{ V}$; $V_{G2-S} = V_{DS} = 0$	–	50	nA
I_{G2-S}	gate cut-off current	$V_{G2-S} = 5\text{ V}$; $V_{G1-S} = V_{DS} = 0$	–	20	nA

Note

- R_{G1} connects gate 1 to $V_{GG} = 5\text{ V}$.

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DYNAMIC CHARACTERISTICS AMPLIFIER aCommon source; $T_{amb} = 25\text{ °C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 15\text{ mA}$; unless otherwise specified.

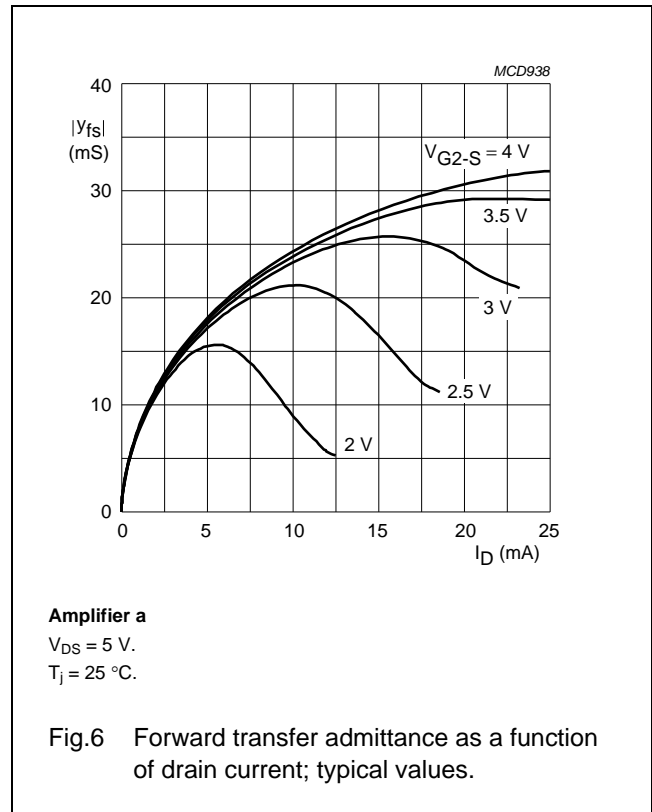
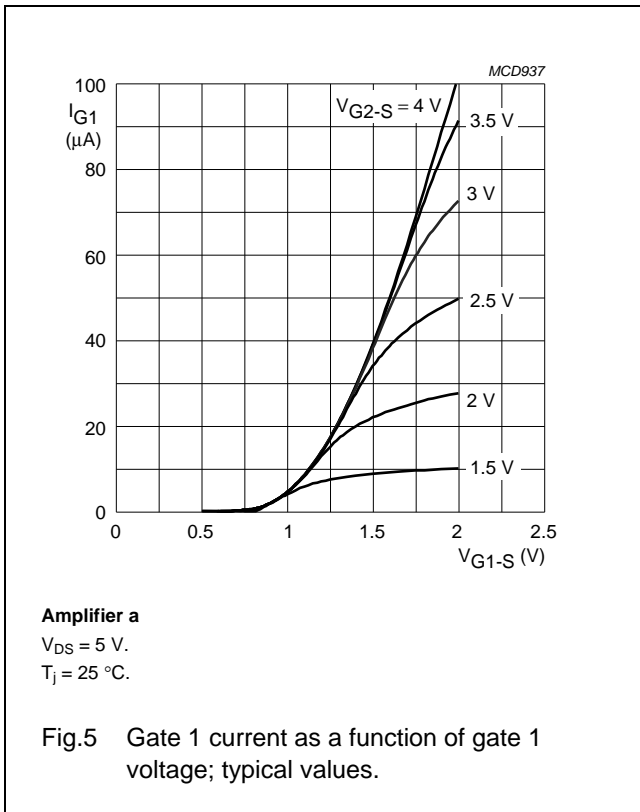
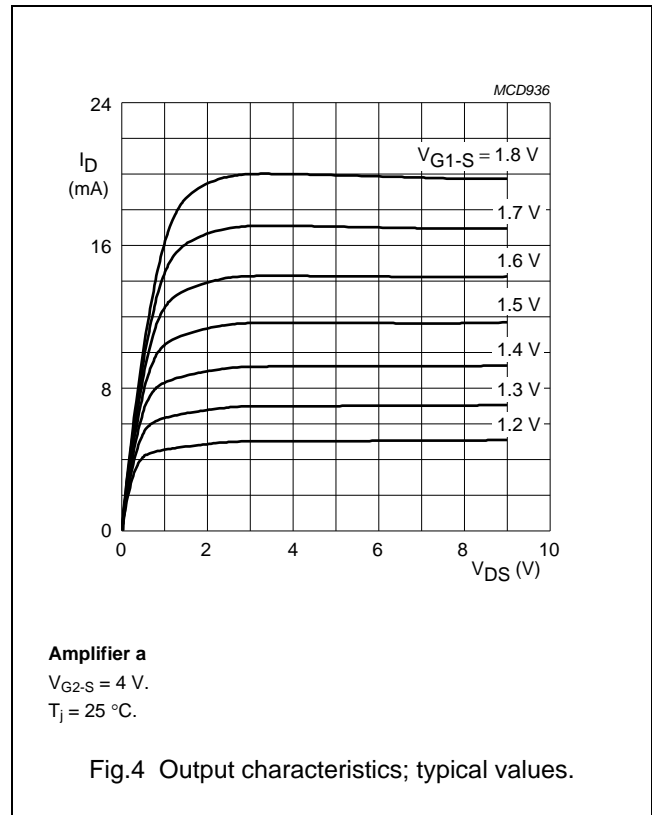
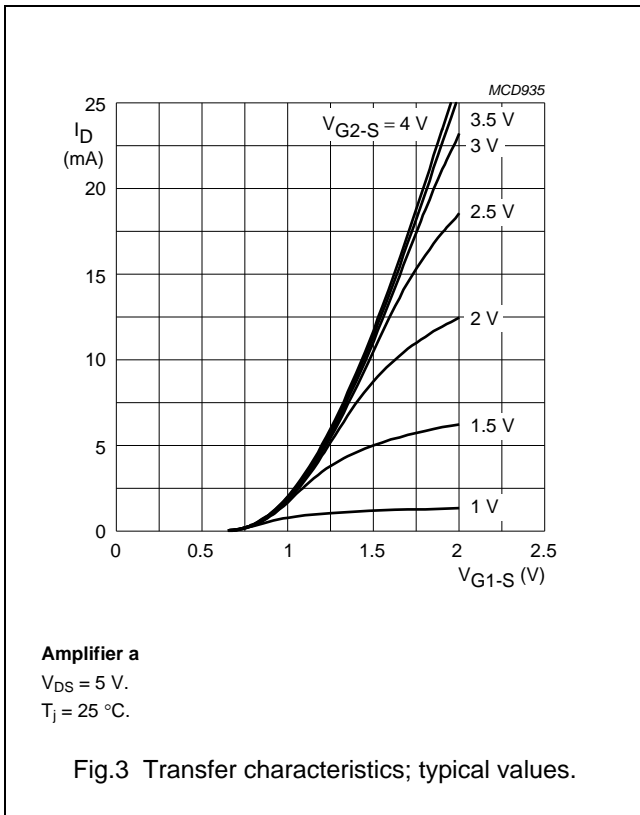
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ °C}$	23	28	35	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	2.6	3.1	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	3	–	pF
C_{oss}	output capacitance	$f = 1\text{ MHz}$	–	0.9	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	15	30	fF
F	noise figure	$f = 10.7\text{ MHz}$; $G_S = 20\text{ mS}$; $B_S = 0$	–	5	7	dB
		$f = 400\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	1	1.8	dB
		$f = 800\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	1.9	2.5	dB
G_{tr}	power gain	$f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 0.5\text{ mS}$; $B_L = B_{L\text{ opt}}$; note 1	–	32.5	–	dB
		$f = 400\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$; note 1	–	27	–	dB
		$f = 800\text{ MHz}$; $G_S = 3.3\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$; note 1	–	21	–	dB
X_{mod}	cross-modulation	input level for $k = 1\%$; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 2				
		at 0 dB AGC	90	–	–	dB μ V
		at 10 dB AGC	–	95	–	dB μ V
	at 40 dB AGC	105	–	–	dB μ V	

Notes

1. Calculated from measured s-parameters.
2. Measured in Fig.35 test circuit.

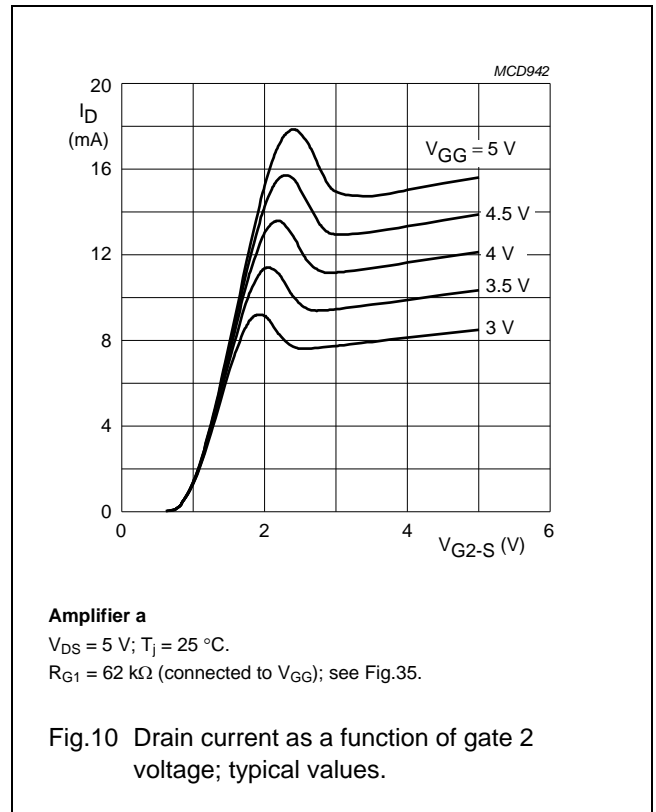
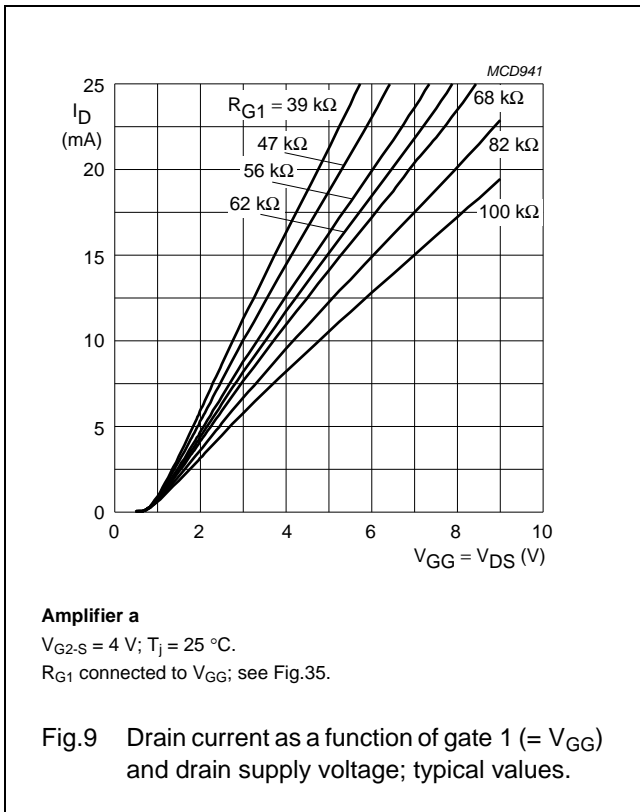
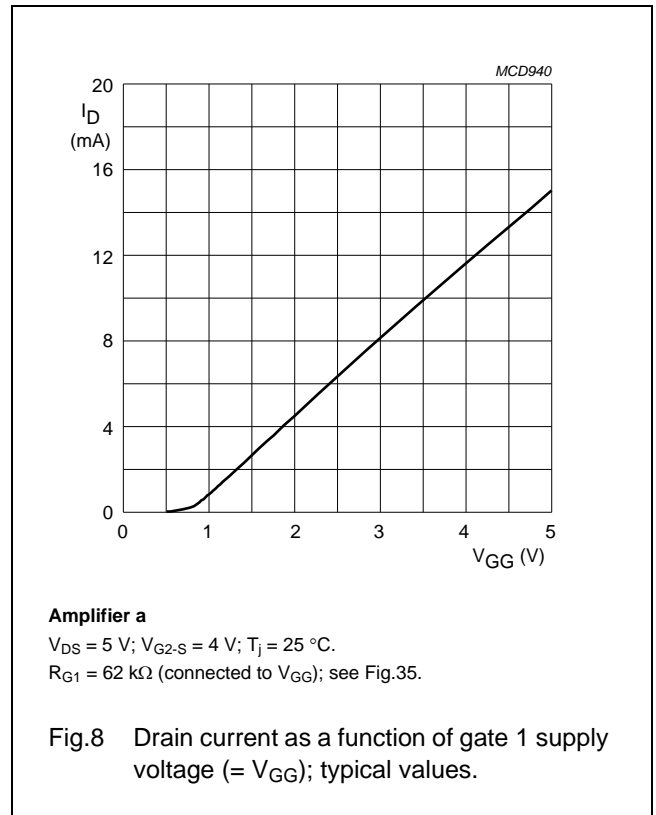
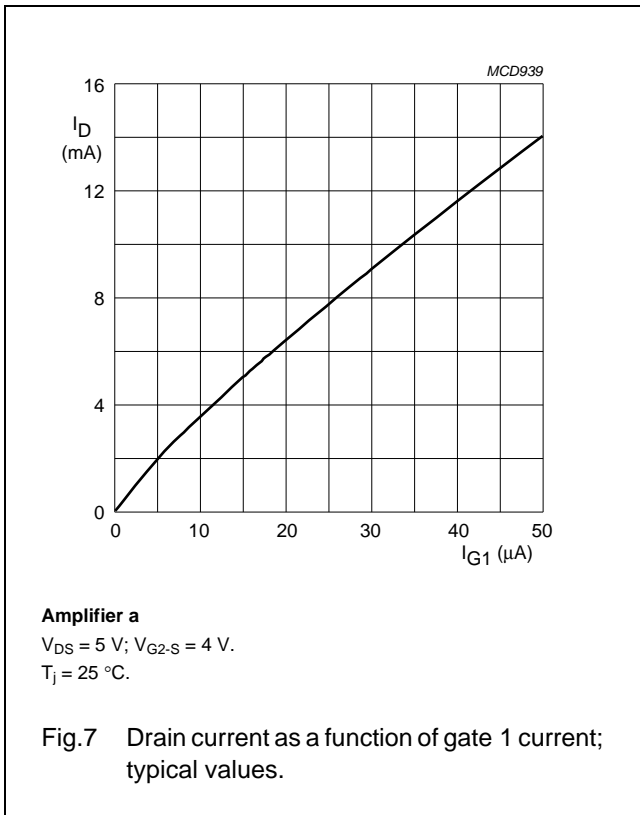
Dual N-channel dual gate MOS-FET

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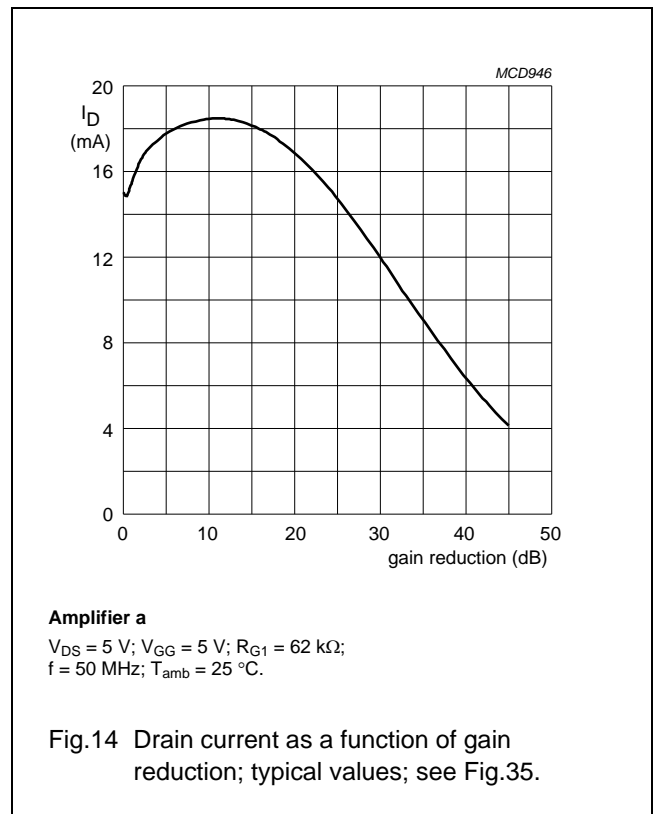
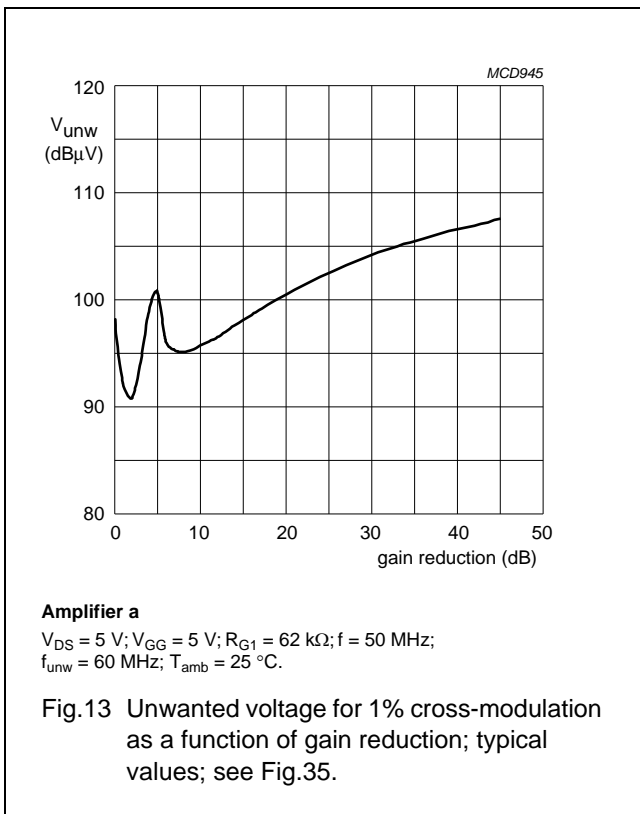
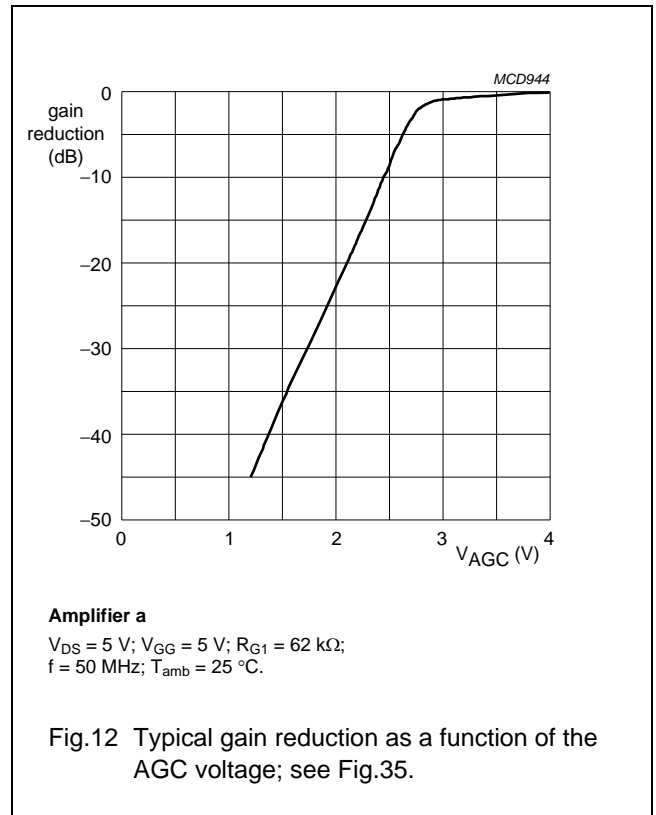
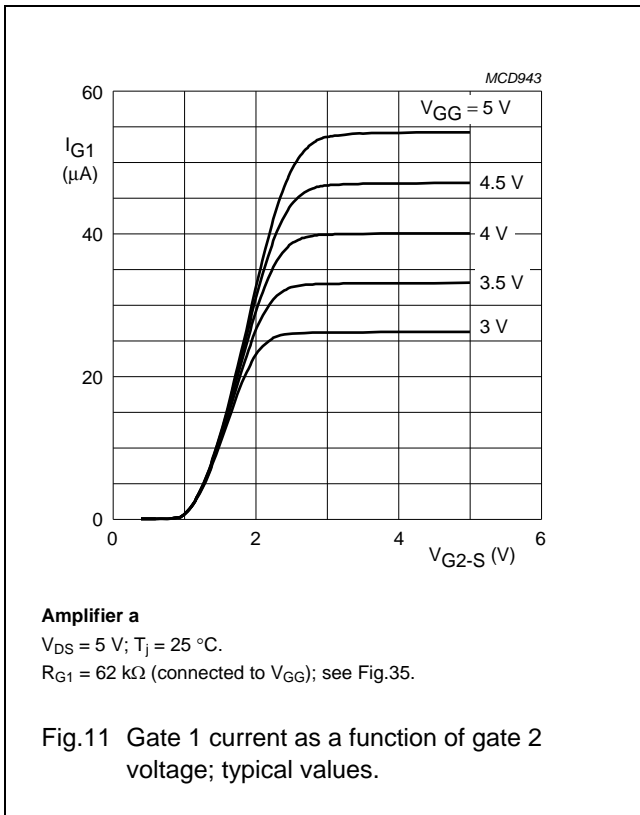
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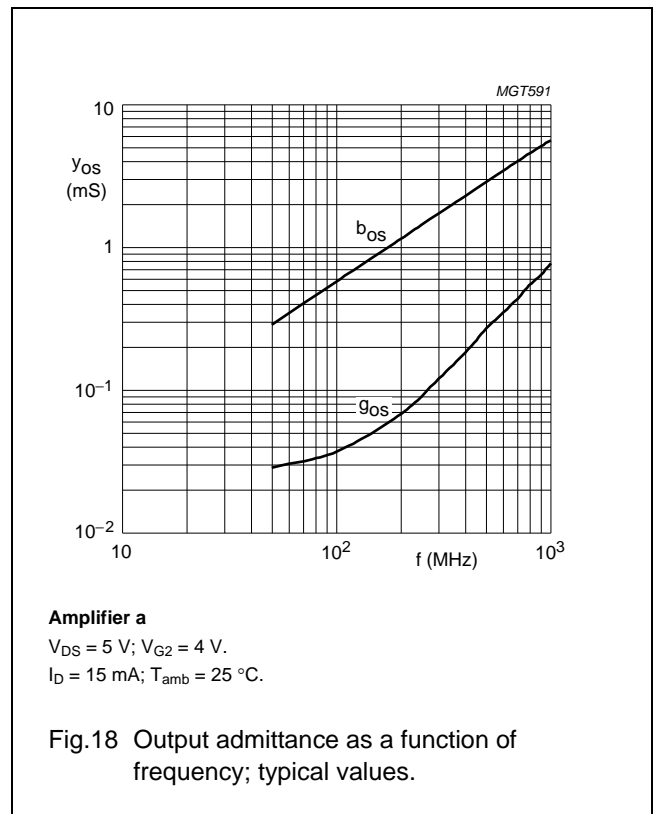
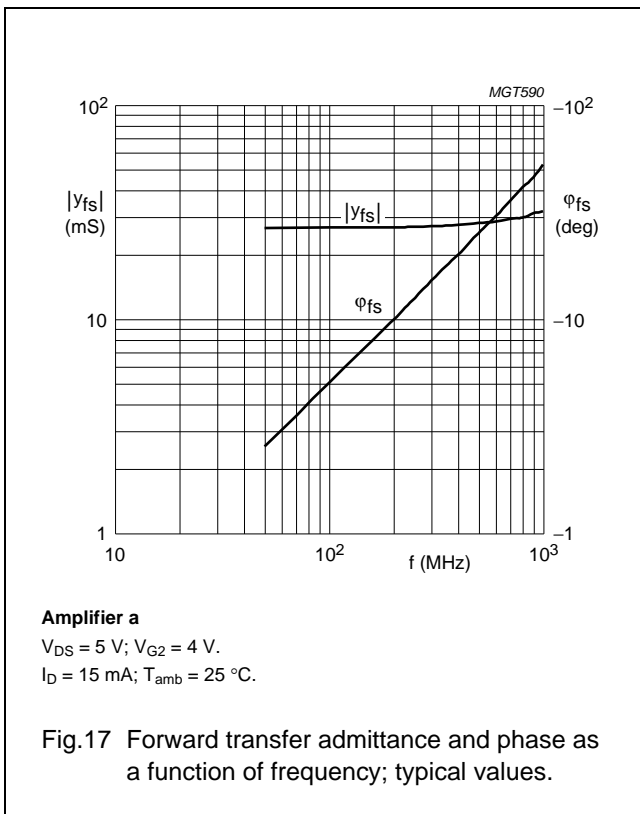
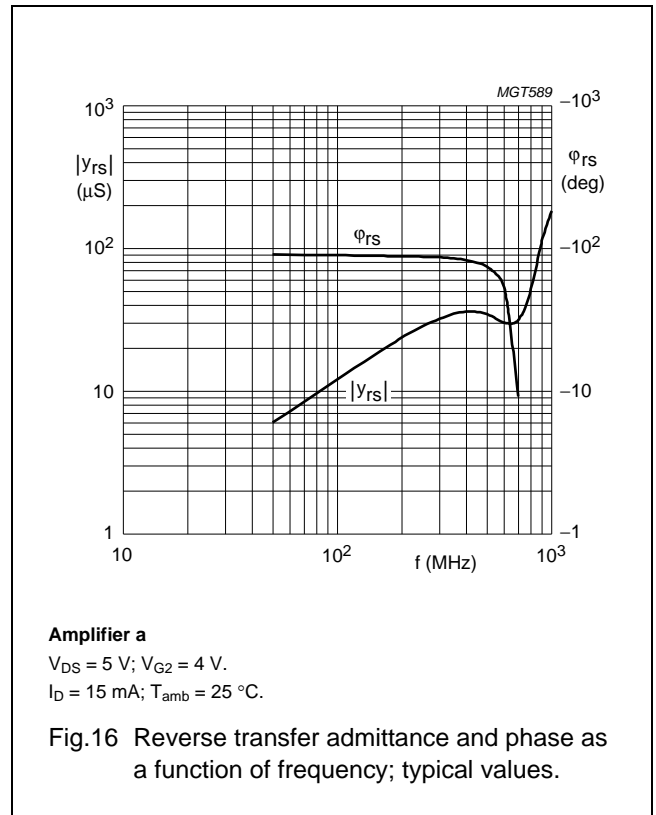
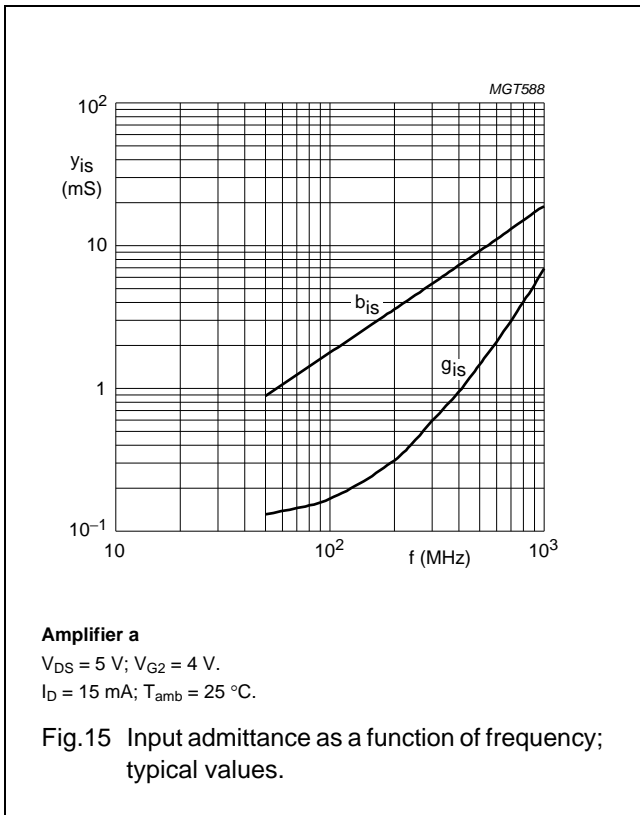
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Dual N-channel dual gate MOS-FET

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Dual N-channel dual gate MOS-FET

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Amplifier a scattering parameters

 $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ °C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.987	-5.12	2.67	174.07	0.0006	85.79	0.997	-1.72
100	0.983	-10.24	2.66	168.16	0.0012	83.27	0.996	-3.42
200	0.976	-20.37	2.61	156.64	0.0023	78.22	0.992	-6.77
300	0.946	-30.36	2.54	145.05	0.0030	73.26	0.986	-10.12
400	0.919	-40.15	2.47	134.13	0.0032	71.40	0.980	-13.33
500	0.885	-49.55	2.37	132.32	0.0029	74.34	0.972	-16.56
600	0.851	-58.50	2.26	113.25	0.0024	90.33	0.965	-19.74
700	0.815	-67.28	2.15	103.20	0.0023	129.94	0.960	-22.90
800	0.778	-75.03	2.02	93.78	0.0035	172.18	0.950	-26.05
900	0.747	-83.30	1.95	84.84	0.0070	171.55	0.951	-29.10
1000	0.710	-90.47	1.83	75.92	0.0104	172.88	0.947	-32.25

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DYNAMIC CHARACTERISTICS AMPLIFIER bCommon source; $T_{amb} = 25\text{ °C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 12\text{ mA}$; unless otherwise specified.

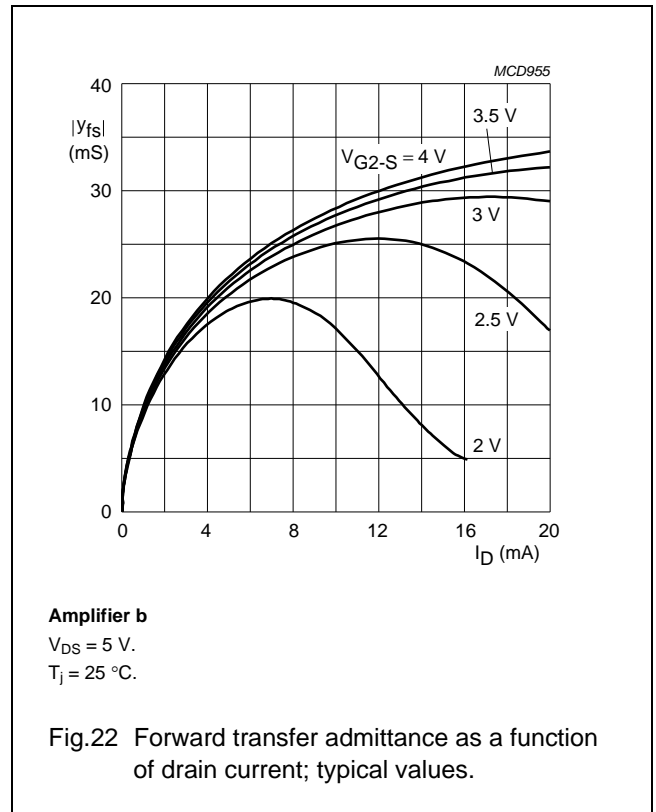
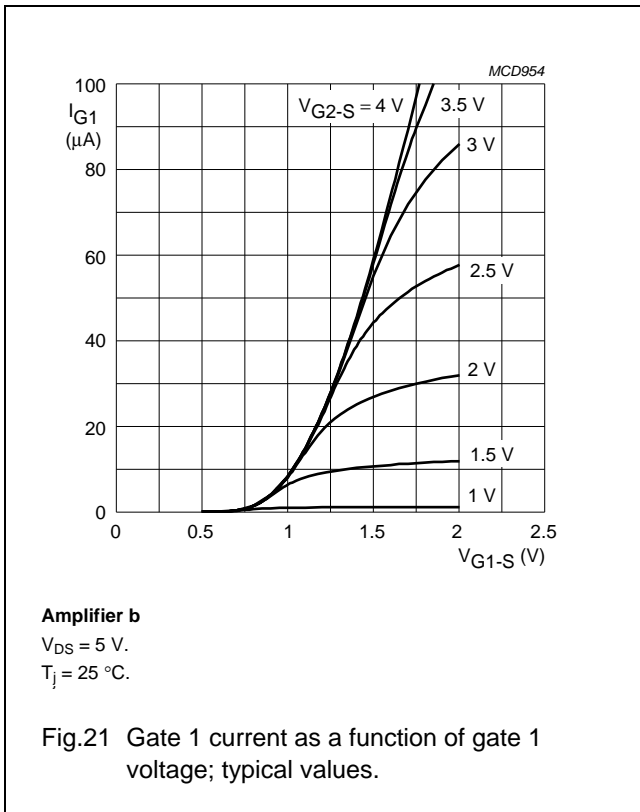
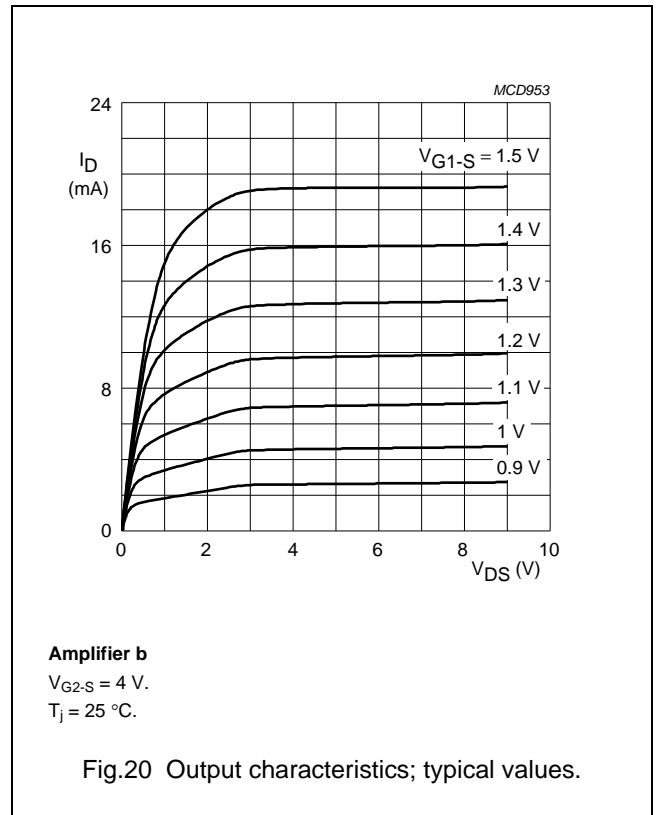
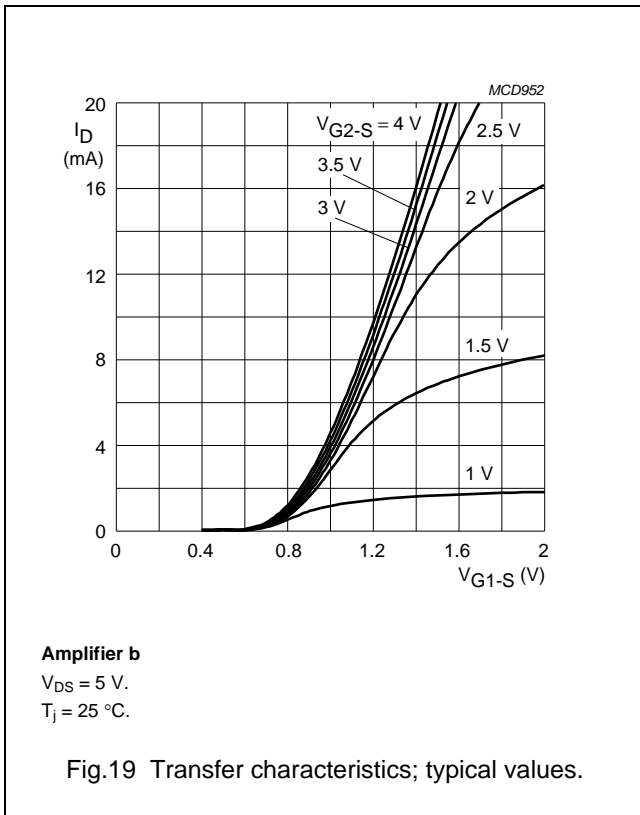
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ °C}$	25	30	40	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	1.7	2.2	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	4	–	pF
C_{oss}	output capacitance	$f = 1\text{ MHz}$	–	0.85	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	15	30	fF
F	noise figure	$f = 10.7\text{ MHz}$; $G_S = 20\text{ mS}$; $B_S = 0$	–	9	11	dB
		$f = 400\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	0.9	1.5	dB
		$f = 800\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	1.1	1.8	dB
G_{tr}	power gain	$f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 0.5\text{ mS}$; $B_L = B_{L\text{ opt}}$; note 1	–	34	–	dB
		$f = 400\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$; note 1	–	30	–	dB
		$f = 800\text{ MHz}$; $G_S = 3.3\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$; note 1	–	25	–	dB
X_{mod}	cross-modulation	input level for $k = 1\%$; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 2				
		at 0 dB AGC	90	–	–	dB μ V
		at 10 dB AGC	–	92	–	dB μ V
	at 40 dB AGC	100	105	–	dB μ V	

Notes

1. Calculated from measured s-parameters.
2. Measured in Fig.35 test circuit.

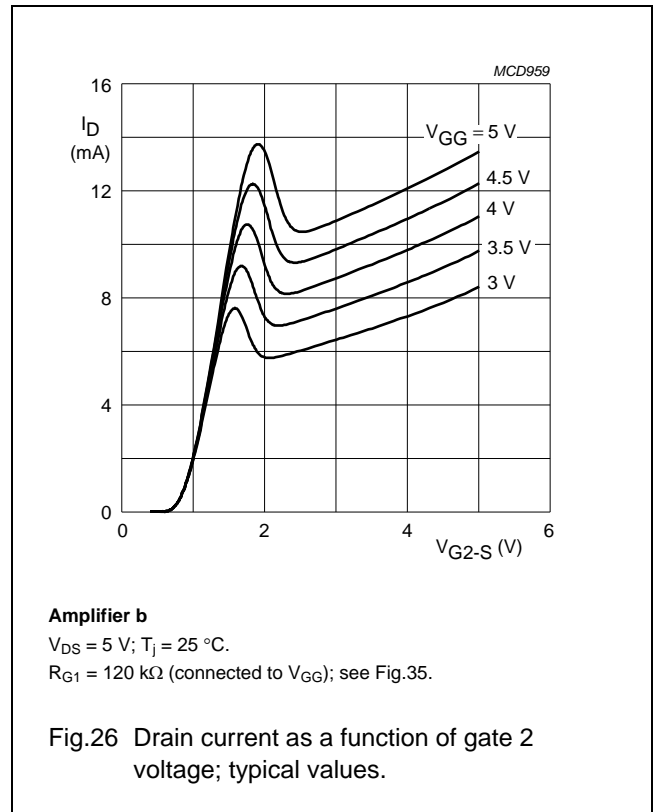
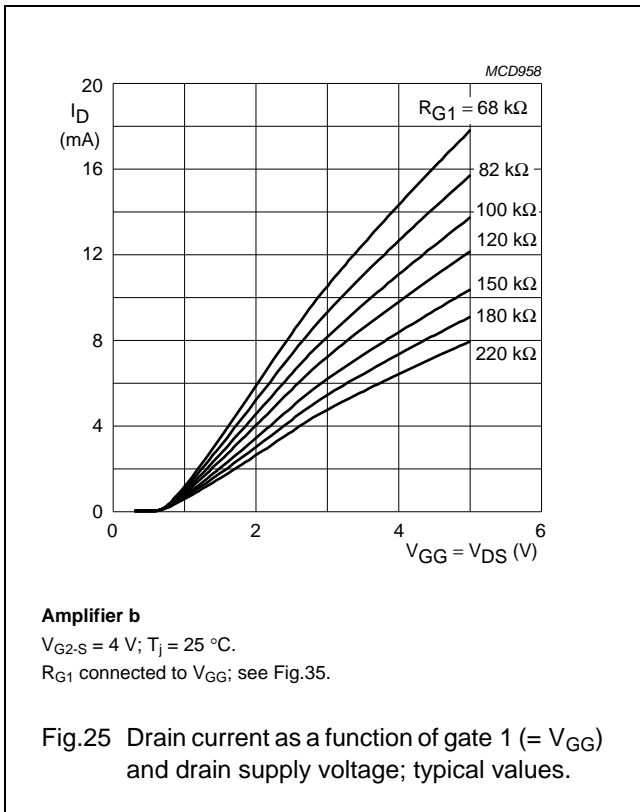
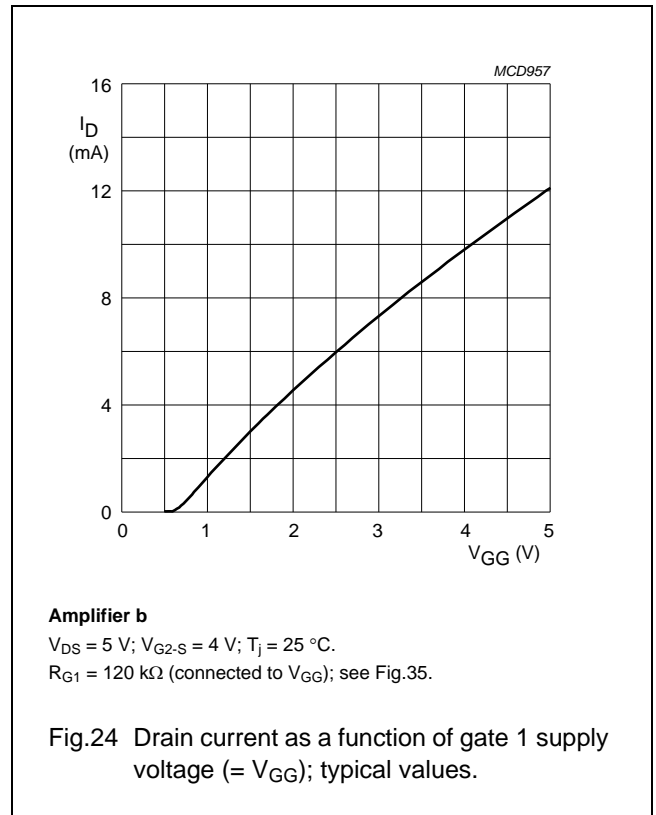
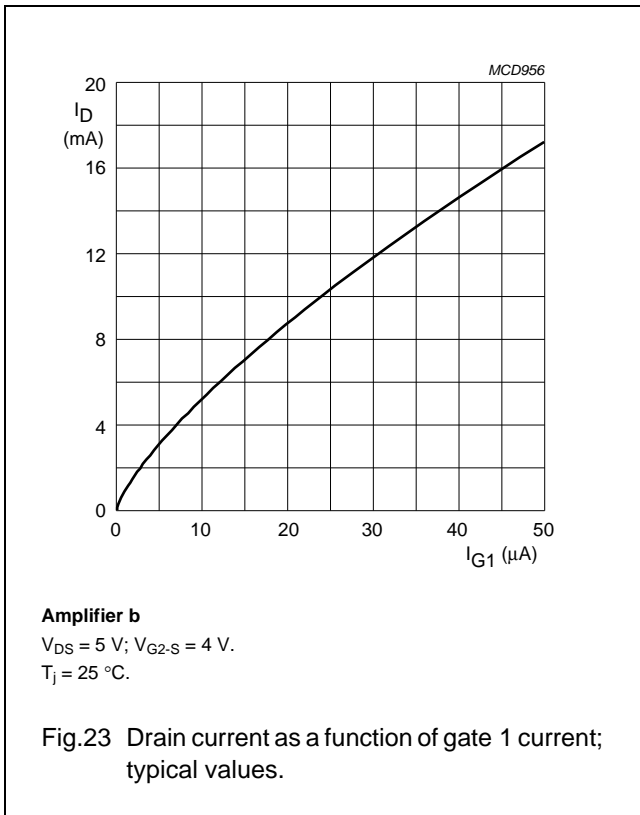
Dual N-channel dual gate MOS-FET

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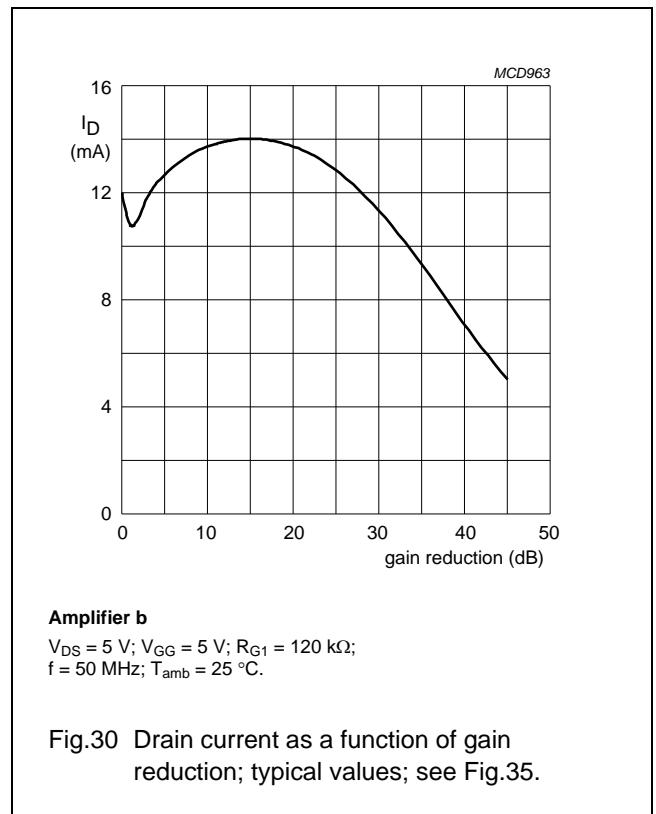
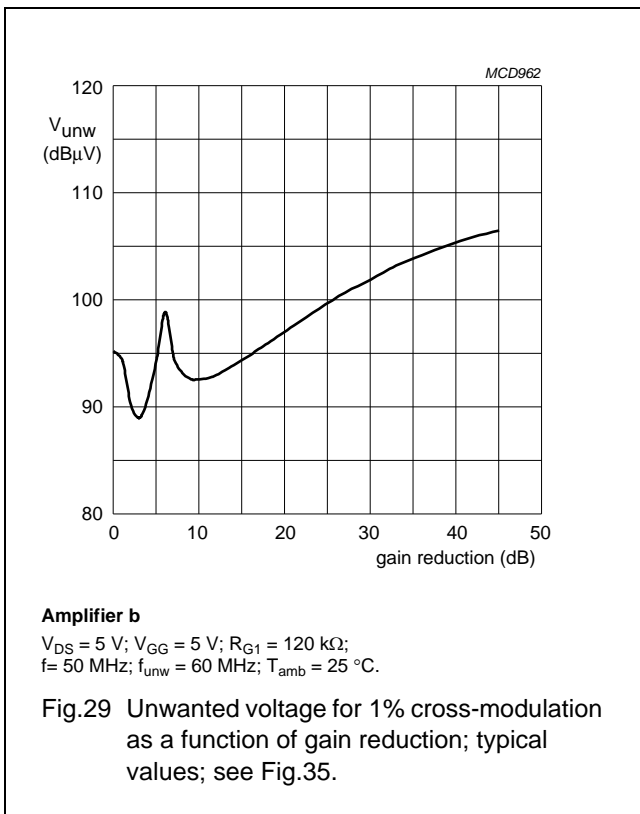
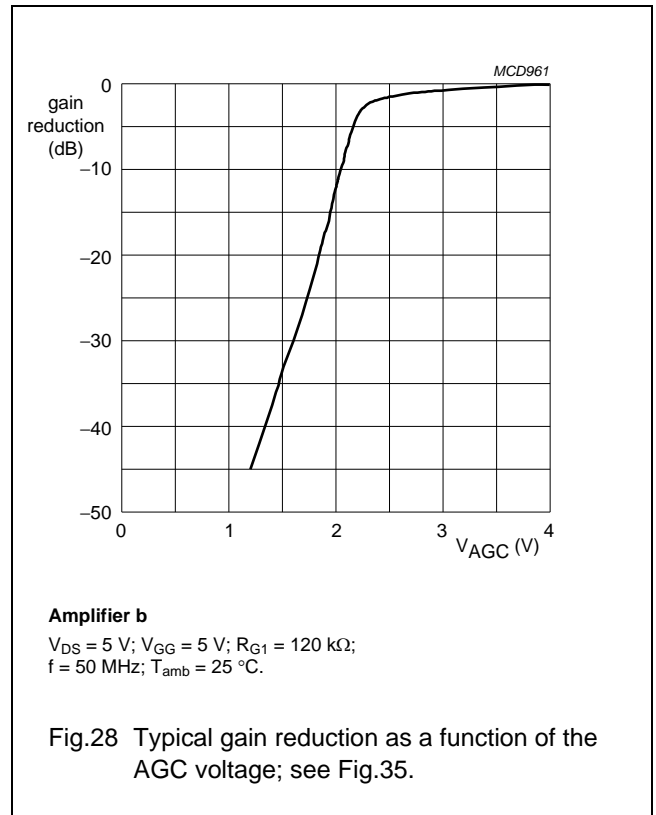
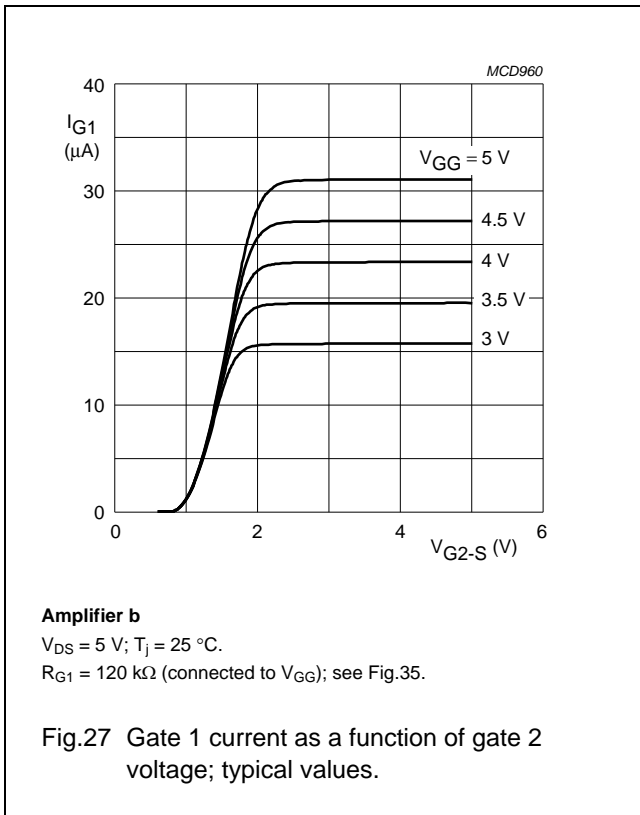
Dual N-channel dual gate MOS-FET

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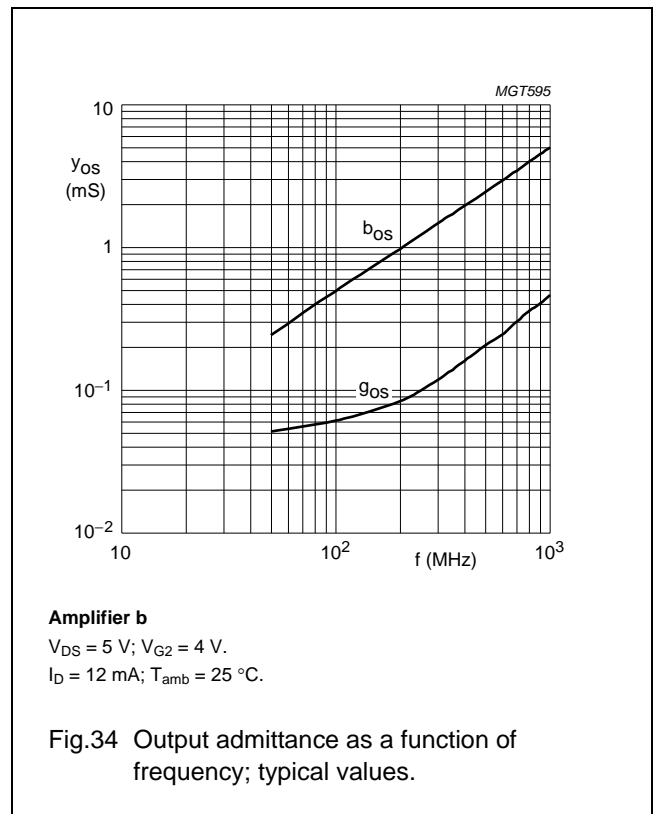
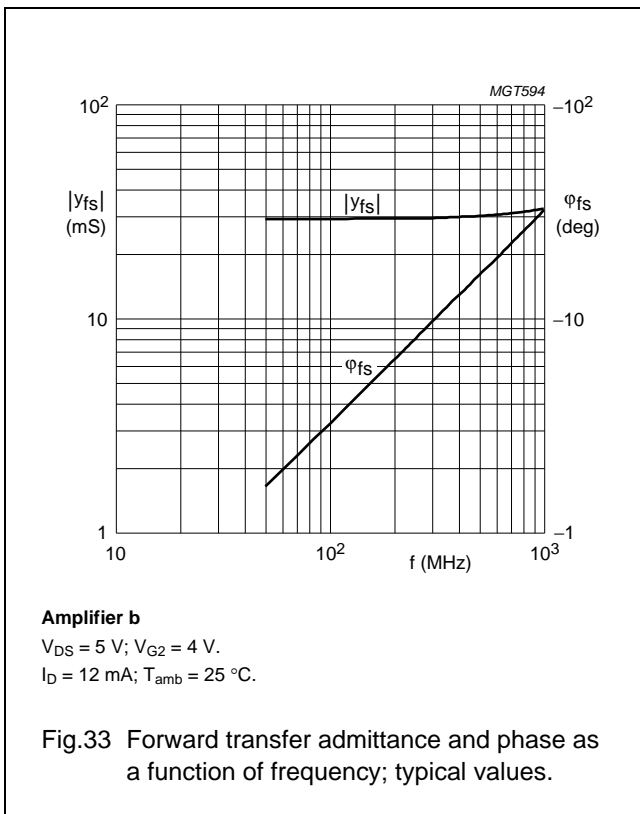
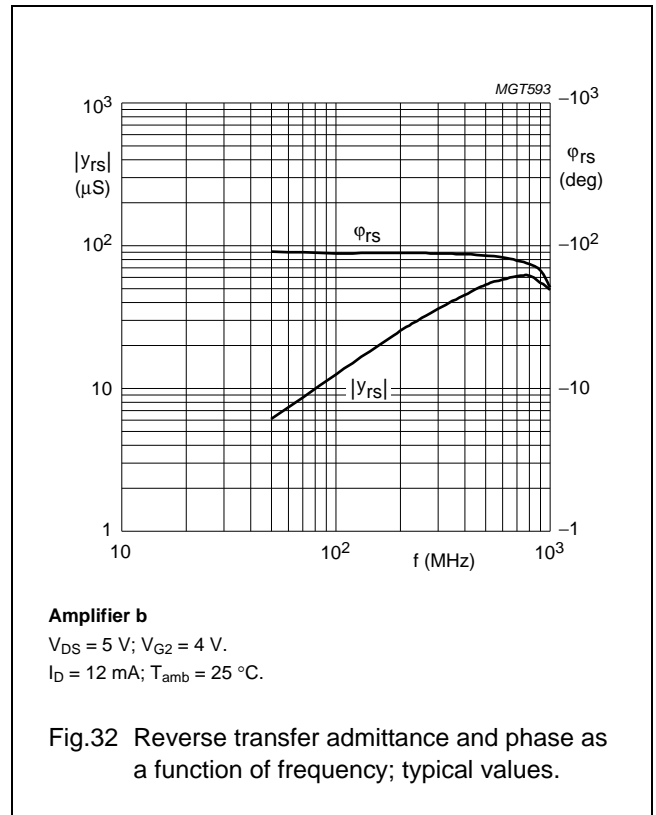
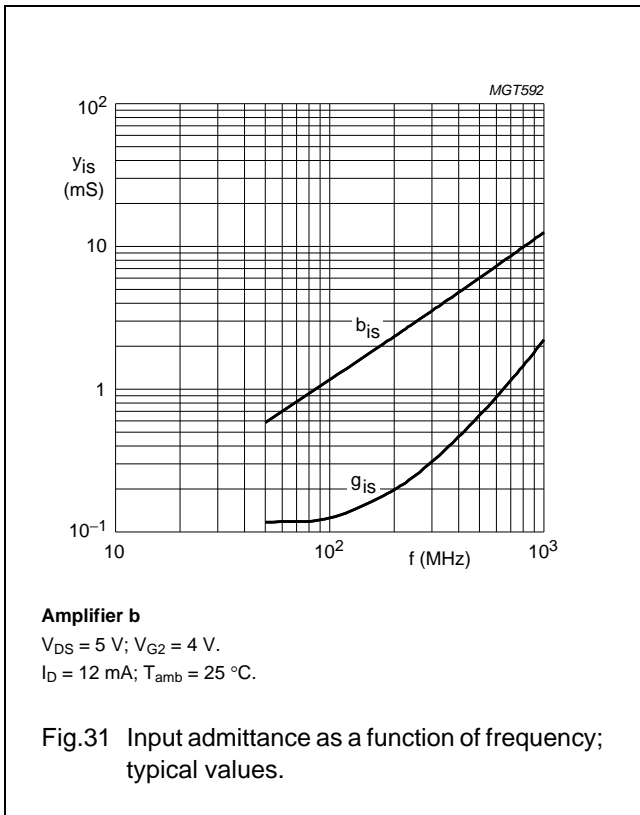
Dual N-channel dual gate MOS-FET

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Dual N-channel dual gate MOS-FET

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Dual N-channel dual gate MOS-FET

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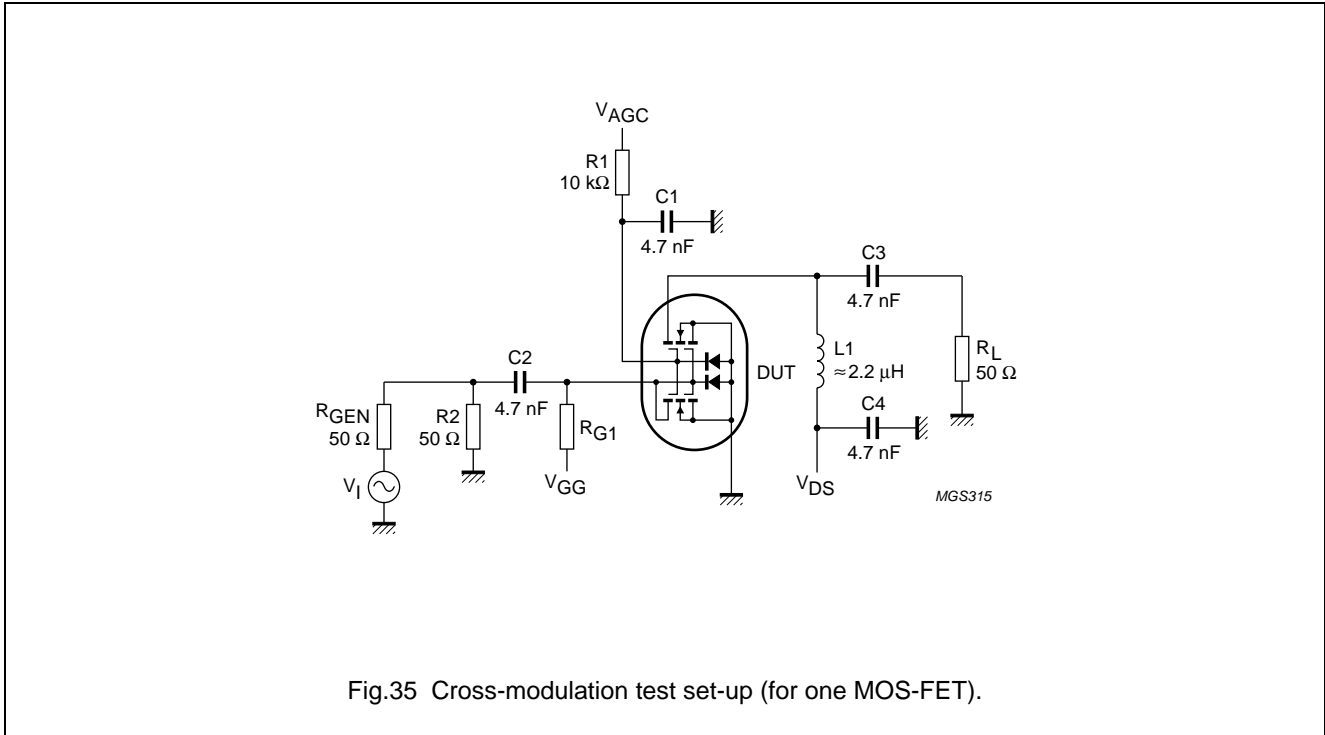


Fig.35 Cross-modulation test set-up (for one MOS-FET).

Amplifier b scattering parameters

$V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^\circ\text{C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.988	-3.30	2.93	166.05	0.0006	87.62	0.994	-1.45
100	0.987	-6.60	2.92	172.11	0.0013	86.02	0.993	-2.92
200	0.981	-13.19	2.90	164.49	0.0025	82.03	0.990	-5.72
300	0.969	-19.81	2.87	156.59	0.0036	76.76	0.986	-8.57
400	0.957	-26.42	2.84	149.17	0.0045	73.59	0.981	-11.32
500	0.941	-33.04	2.79	141.47	0.0051	71.13	0.975	-14.22
600	0.925	-39.44	2.73	134.25	0.0054	69.07	0.971	-17.04
700	0.907	-45.89	2.67	126.81	0.0055	68.03	0.966	-19.92
800	0.889	-51.93	2.60	119.56	0.0055	68.55	0.958	-22.77
900	0.827	-57.82	2.54	112.70	0.0048	69.87	0.957	-25.54
1000	0.853	-63.24	2.46	105.72	0.0042	78.19	0.954	-28.41

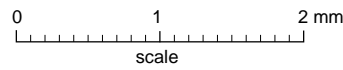
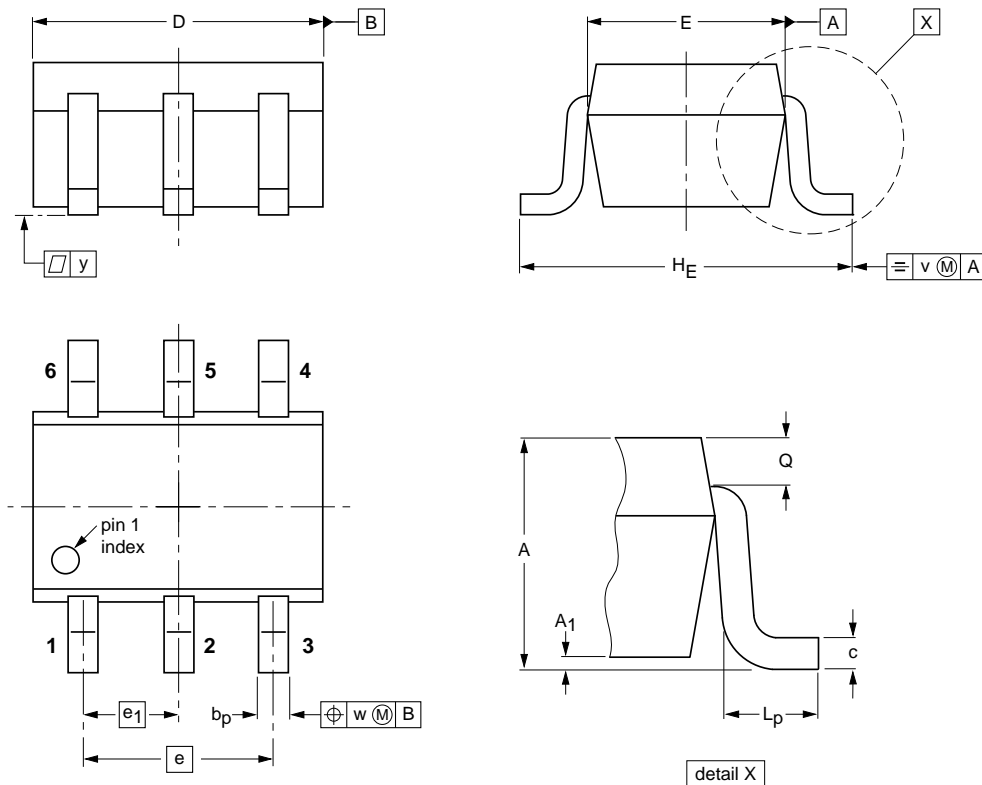
Dual N-channel dual gate MOS-FET

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PACKAGE OUTLINE

Plastic surface-mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
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Dual N-channel dual gate MOS-FET

BF1203

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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