



**THE DATASHEET OF  
NCV890101MWTXG**



# NCV890101

## Switching Regulator - Automotive, Buck

### 1.2 A, 2 MHz

The NCV890101 is a fixed-frequency, monolithic, Buck switching regulator intended for Automotive, battery-connected applications that must operate with up to a 36 V input supply. The regulator is suitable for systems with low noise and small form factor requirements often encountered in automotive driver information systems. The NCV890101 is capable of converting the typical 4.5 V to 18 V automotive input voltage range to outputs as low as 3.3 V at a constant switching frequency above the sensitive AM band, eliminating the need for costly filters and EMI countermeasures. Two pins are provided to synchronize switching to a clock, or to another NCV890101. The NCV890101 also provides several protection features expected in Automotive power supply systems such as current limit, short circuit protection, and thermal shutdown. In addition, the high switching frequency produces low output voltage ripple even when using small inductor values and an all-ceramic output filter capacitor – forming a space-efficient switching regulator solution.

#### Features

- Internal N-Channel Power Switch
- Low  $V_{IN}$  Operation Down to 4.5 V
- High  $V_{IN}$  Operation to 36 V
- Withstands Load Dump to 40 V
- 2 MHz Free-running Switching Frequency
- Auto-synchronizes with Other NCV890101 or to an External Clock
- Logic level Enable Input Can be Directly Tied to Battery
- 1.4 A (min) Cycle-by-Cycle Peak Current Limit
- Short Circuit Protection enhanced by Frequency Foldback
- $\pm 1.75\%$  Output Voltage Tolerance
- Output Voltage Adjustable Down to 0.8 V
- 1.4 Millisecond Internal Soft-Start
- Thermal Shutdown (TSD)

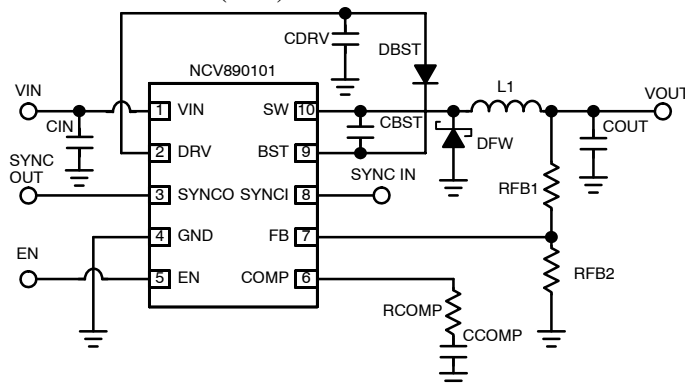


Figure 1. Typical Application



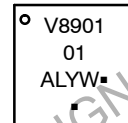
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#### MARKING DIAGRAM



DFN10  
CASE 485C



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Device

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

- Low Shutdown Current
- Wettable Flanks – DFN
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### Applications

- Audio
- Infotainment
- Safety – Vision Systems
- Instrumentation

NCV890101

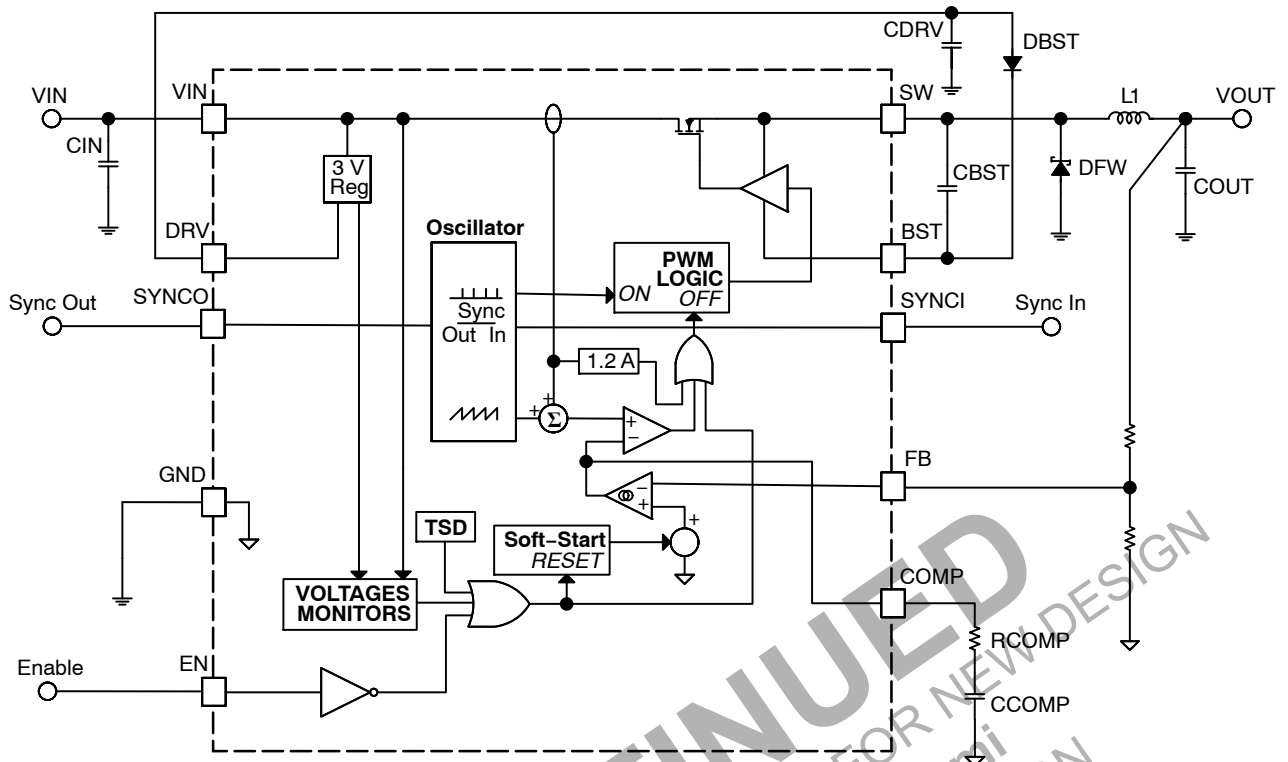


Figure 2. NCV890101 Block Diagram

**DISCONTINUED**  
 THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN.  
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 REPRESENTATIVE FOR INFORMATION

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Min/Max Voltage VIN		-0.3 to 40	V
Max Voltage VIN to SW		40	V
Min/Max Voltage SW		-0.7 to 40	V
Min Voltage SW – 20ns		-3.0	V
Min/Max Voltage BST		-0.3 to 40	
Min/Max Voltage BST to SW		-0.3 to 3.6	V
Min/Max Voltage on EN		-0.3 to 40	V
Min/Max Voltage COMP		-0.3 to 2	V
Min/Max Voltage FB		-0.3 to 18	V
Min/Max Voltage SYNCO		-0.3 to 3.6	V
Min/Max Voltage DRV		-0.3 to 3.6	V
Min/Max Voltage SYNCI		-0.3 to 6	V
Thermal Resistance, 3x3 DFN Junction-to-Ambient*	$R_{\theta JA}$	50	°C/W
Storage Temperature range		-55 to +150	°C
Operating Junction Temperature Range	$T_J$	-40 to +150	°C
ESD withstand Voltage	Human Body Model	2.0	kV
	Machine Model	200	V
	Charge Device Model	>1.0	kV
Moisture Sensitivity	MSL	Level 1	
Peak Reflow Soldering Temperature		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

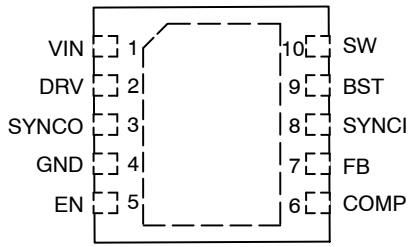
\*Mounted on 1 sq. in. of a 4-layer PCB with 1 oz. copper thickness.

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THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN

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# NCV890101



(Top View)

**Figure 3. Pin Connections**

## PIN FUNCTION DESCRIPTIONS

Pin No.	Symbol	Description
1	VIN	Input voltage from battery. Place an input filter capacitor in close proximity to this pin.
2	DRV	Output voltage to provide a regulated voltage to the Power Switch gate driver.
3	SYNCO	Synchronization output. Turn-on of the Power Switch causes the SYNCO signal to fall. SYNCO rises half a switching period later. Connecting to the SYNCI pin of another NCV890101 causes them to switch out-of-phase
4	GND	Battery return, and output voltage ground reference.
5	EN	This TTL compatible Enable input allows the direct connection of Battery as the enable signal. Grounding this input stops switching and reduces quiescent current draw to a minimum.
6	COMP	Error Amplifier output, for tailoring transient response with external compensation components.
7	FB	Feedback input pin to program output voltage, and detect pre-charged or shorted output conditions.
8	SYNCI	Synchronization input. Connecting an external clock to the SYNCI pin synchronizes switching to the rising edge of the SYNCI voltage.
9	BST	Bootstrap input provides drive voltage higher than VIN to the N-channel Power Switch for optimum switch $R_{DS(on)}$ and highest efficiency.
10	SW	Switching node of the Regulator. Connect the output inductor and cathode of the freewheeling diode to this pin.
Exposed Pad		Connect to Pin 4 (electrical ground) and to a low thermal resistance path to the ambient temperature environment.

# NCV890101

**ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 4.5\text{ V to }28\text{ V}$ ,  $V_{EN} = 5\text{ V}$ ,  $V_{BST} = V_{SW} + 3.0\text{ V}$ ,  $C_{DRV} = 0.1\text{ }\mu\text{F}$ , Min/Max values are valid for the temperature range  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$  unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
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## QUIESCENT CURRENT

Quiescent Current, shutdown	$I_{qSD}$	$V_{IN} = 13.2\text{ V}$ , $V_{EN} = 0\text{ V}$ , $T_J = 25^{\circ}\text{C}$			5	$\mu\text{A}$
Quiescent Current, enabled	$I_{qEN}$	$V_{IN} = 13.2\text{ V}$			3	mA

## UNDERVOLTAGE LOCKOUT - VIN (UVLO)

UVLO Start Threshold	$V_{UVLSTT}$	$V_{IN}$ rising	4.1		4.5	V
UVLO Stop Threshold	$V_{UVLSTP}$	$V_{IN}$ falling	3.9		4.4	V
UVLO Hysteresis	$V_{UVLOHY}$		0.1		0.2	V

## ENABLE (EN)

Logic Low	$V_{ENLO}$		0.8			V
Logic High	$V_{ENHI}$				2	V
Input Current	$I_{EN}$		8		30	$\mu\text{A}$

## SOFT-START (SS)

Soft-Start Completion Time	$t_{SS}$		0.8	1.4	2.0	ms
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## VOLTAGE REFERENCE

FB Pin Voltage during regulation	$V_{FBR}$	COMP shorted to FB	0.786	0.8	0.814	V
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## ERROR AMPLIFIER

FB Bias Current	$I_{FBBIAS}$	$V_{FB} = 0.8\text{ V}$	0.25		1	$\mu\text{A}$
Transconductance	$g_m$ $g_m(HV)$	$V_{COMP} = 1.3\text{ V}$ $4.5\text{ V} < V_{IN} < 18\text{ V}$ $20\text{ V} < V_{IN} < 28\text{ V}$	0.6 0.3	1 0.5	1.5 0.75	mmho
Output Resistance	$R_{OUT}$			1.4		$\text{M}\Omega$
COMP Source Current Limit	$I_{SOURCE}$	$V_{FB} = 0.63\text{ V}$ , $V_{COMP} = 1.3\text{ V}$ $4.5\text{ V} < V_{IN} < 18\text{ V}$ $20\text{ V} < V_{IN} < 28\text{ V}$		75 40		$\mu\text{A}$
COMP Sink Current Limit	$I_{SINK}$	$V_{FB} = 0.97\text{ V}$ , $V_{COMP} = 1.3\text{ V}$ $4.5\text{ V} < V_{IN} < 18\text{ V}$ $20\text{ V} < V_{IN} < 28\text{ V}$		75 40		$\mu\text{A}$
Minimum COMP voltage	$V_{CMPMIN}$	$V_{FB} = 0.97\text{ V}$	0.2		0.7	V

## OSCILLATOR

Frequency	$F_{SW}$ $F_{SW(HV)}$	$4.5 < V_{IN} < 18\text{ V}$ $20\text{ V} < V_{IN} < 28\text{ V}$	1.8 0.9	2.0 1.0	2.2 1.1	MHz
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## VIN FREQUENCY FOLDBACK MONITOR

Frequency Foldback Threshold $V_{IN}$ rising $V_{IN}$ falling	$V_{FLDUP}$ $V_{FLDDN}$	$V_{FB} = 0.63\text{ V}$	18.4 18		20 19.8	V
Frequency Foldback Hysteresis	$V_{FLDHY}$		0.2	0.3	0.4	V

1. Not tested in production. Limits are guaranteed by design.

# NCV890101

**ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 4.5\text{ V to }28\text{ V}$ ,  $V_{EN} = 5\text{ V}$ ,  $V_{BST} = V_{SW} + 3.0\text{ V}$ ,  $C_{DRV} = 0.1\text{ }\mu\text{F}$ , Min/Max values are valid for the temperature range  $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$  unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
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## SYNCHRONIZATION

SYNCO Output Pulse Duty Ratio	$D_{(SYNCO)}$	$C_{LOAD} = 40\text{ pF}$	40		60	%
SYNCO Output Pulse Faltime	$t_{R(SYNCO)}$	$C_{LOAD} = 40\text{ pF}$ , 90% to 10%		4		ns
SYNCO Output Pulse Risettime	$t_{F(SYNCO)}$	$C_{LOAD} = 40\text{ pF}$ , 10% to 90%		4		ns
SYNCO Input Resistance to ground	$R_{H(SYNCO)}$	$V_{SYNCO} = 5.0\text{ V}$	50		200	$k\Omega$
SYNCO Input High Threshold Voltage	$V_{HSYNCO}$				2.0	V
SYNCO Input Low Threshold Voltage	$V_{LSYNCO}$		0.8			V
SYNCO High Pulse Width	$t_{HSYNCO}$	$V_{SYNCO} > \max V_{HSYNCO}$	40			ns
SYNCO Low Pulse Width	$t_{LSYNCO}$	$V_{SYNCO} < \min V_{LSYNCO}$	40			ns
External Sync Frequency	$F_{SYNCO}$		1.8		2.5	MHz
Master Reassertion Time	$t_{I(SYNCO)}$	Time from last rising SYNCO edge to first un-synchronized turn-on.		650		ns

## SLOPE COMPENSATION

Ramp Slope (Note 1) (With respect to switch current)	$S_{ramp}$ $S_{ramp(HV)}$	$4.5 < V_{IN} < 18\text{ V}$ $20\text{ V} < V_{IN} < 28\text{ V}$	0.7 0.25		1.3 0.6	A/ $\mu\text{s}$
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## POWER SWITCH

ON Resistance	$R_{DSON}$	$V_{BST} = V_{SW} + 3.0\text{ V}$			650	$m\Omega$
Leakage current VIN to SW	$I_{LKSW}$	$V_{EN} = 0\text{ V}$ , $V_{SW} = 0$ , $V_{IN} = 18\text{ V}$			10	$\mu\text{A}$
Minimum ON Time	$t_{ONMIN}$	Measured at SW pin	45		70	ns
Minimum OFF Time	$t_{OFFMIN}$	Measured at SW pin At $F_{SW} = 2\text{ MHz}$ (normal) At $F_{SW} = 500\text{ kHz}$ (max duty cycle)	30	30 50	70	ns

## PEAK CURRENT LIMIT

Current Limit Threshold	$I_{LIM}$		1.4	1.55	1.7	A
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## SHORT CIRCUIT FREQUENCY FOLDBACK

Lowest Foldback Frequency	$F_{SWAF}$	$V_{FB} = 0\text{ V}$ , $4.5\text{ V} < V_{IN} < 18\text{ V}$	400	500	600	kHz
Lowest Foldback Frequency – High $V_{in}$	$F_{SWAFHV}$	$V_{FB} = 0\text{ V}$ , $20\text{ V} < V_{IN} < 28\text{ V}$	200	250	300	
Hiccup Mode	$F_{SWHIC}$	$V_{FB} = 0\text{ V}$	24	32	40	

## GATE VOLTAGE SUPPLY (DRV pin)

Output Voltage	$V_{DRV}$		3.1	3.3	3.5	V
DRV POR Start Threshold	$V_{DRVSTT}$		2.7	2.9	3.05	V
DRV POR Stop Threshold	$V_{DRVSTP}$		2.5	2.8	3.0	V
DRV Current Limit	$I_{DRVLIM}$	$V_{DRV} = 0\text{ V}$	16		45	mA

## OUTPUT PRECHARGE DETECTOR

Threshold Voltage	$V_{SSEN}$		20	35	50	mV
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## THERMAL SHUTDOWN

Activation Temperature (Note 1)	$T_{SD}$		150		190	$^{\circ}\text{C}$
Hysteresis (Note 1)	$T_{HYS}$		5		20	$^{\circ}\text{C}$

1. Not tested in production. Limits are guaranteed by design.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS CURVES

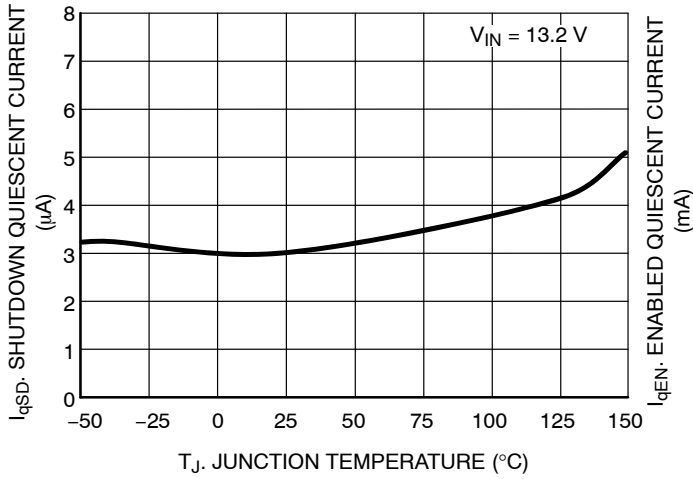


Figure 4. Shutdown Quiescent Current vs. Junction Temperature

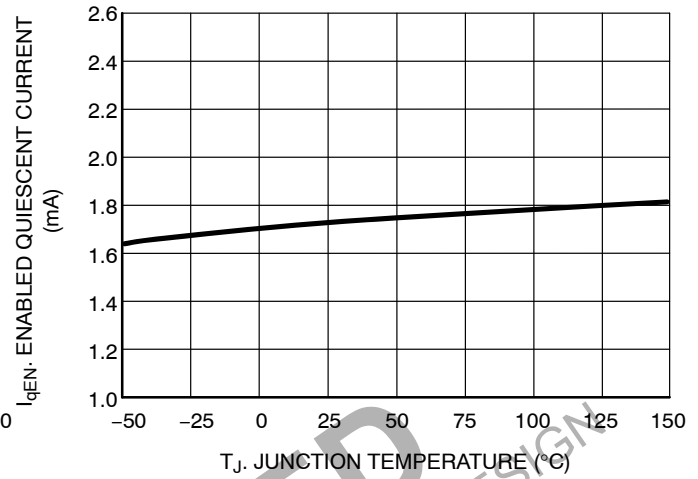


Figure 5. Enabled Quiescent Current vs. Junction Temperature

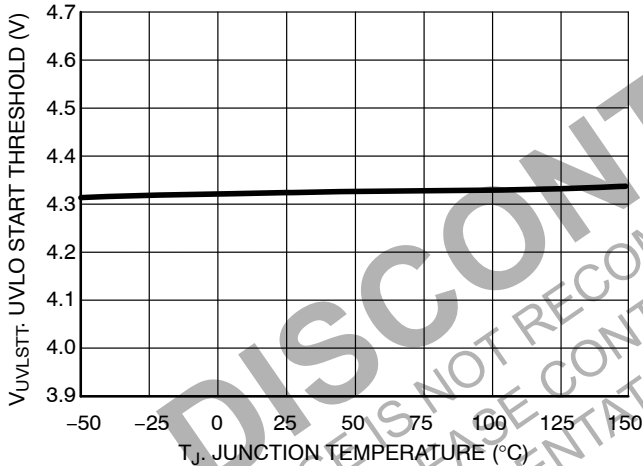


Figure 6. UVLO Start Threshold vs. Junction Temperature

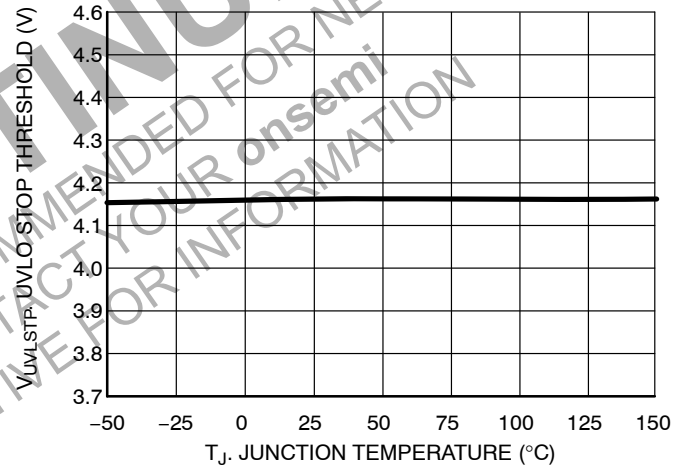


Figure 7. UVLO Stop Threshold vs. Junction Temperature

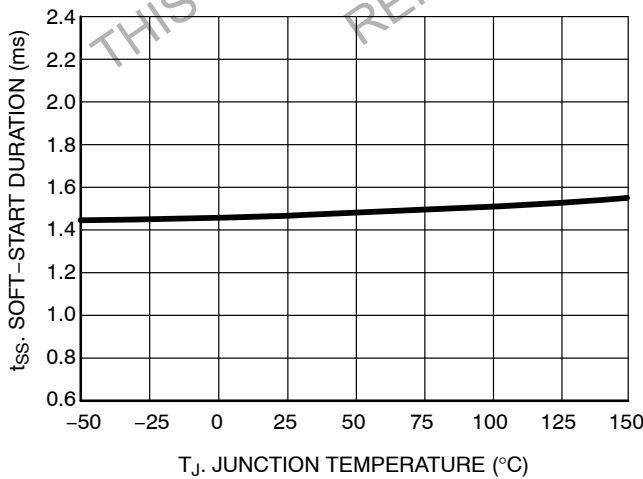


Figure 8. Soft-Start Duration vs. Junction Temperature

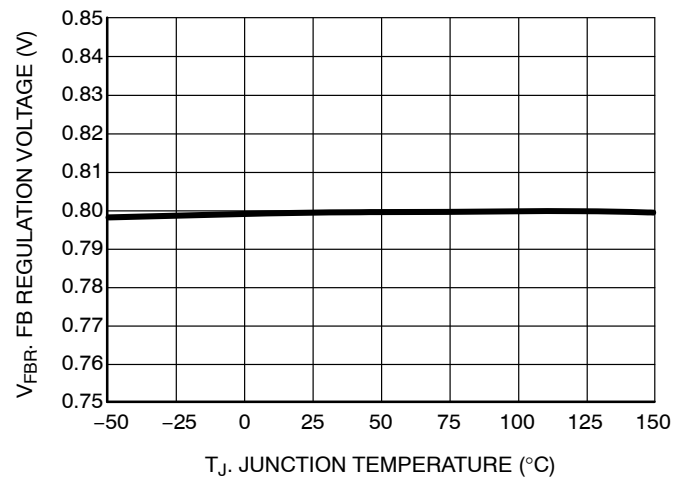


Figure 9. FB Regulation Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS CURVES

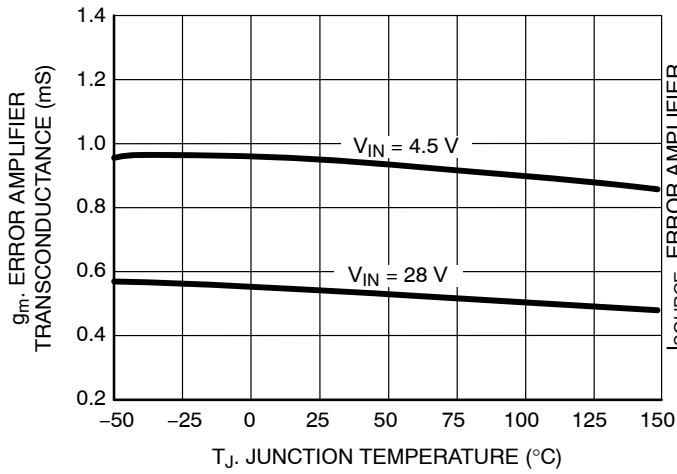


Figure 10. Error Amplifier Transconductance vs. Junction Temperature

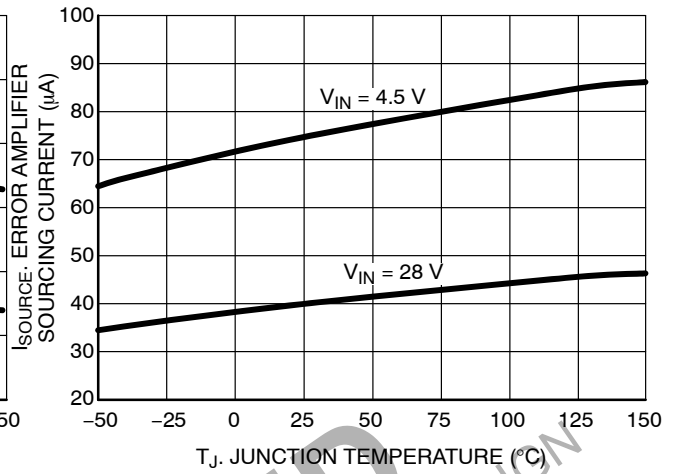


Figure 11. Error Amplifier Max Sourcing Current vs. Junction Temperature

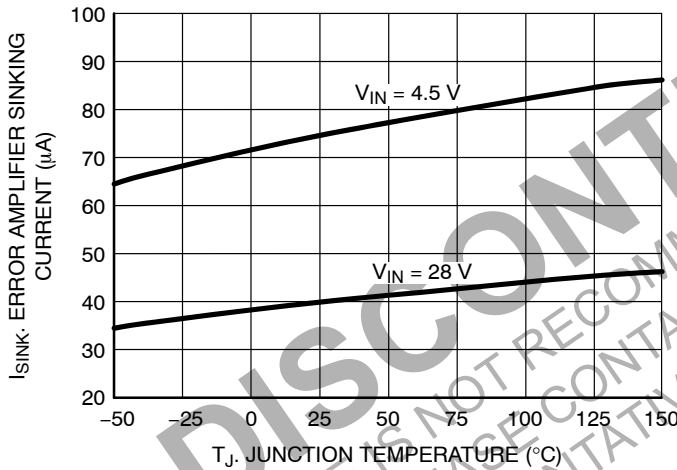


Figure 12. Error Amplifier Max Sinking Current vs. Junction Temperature

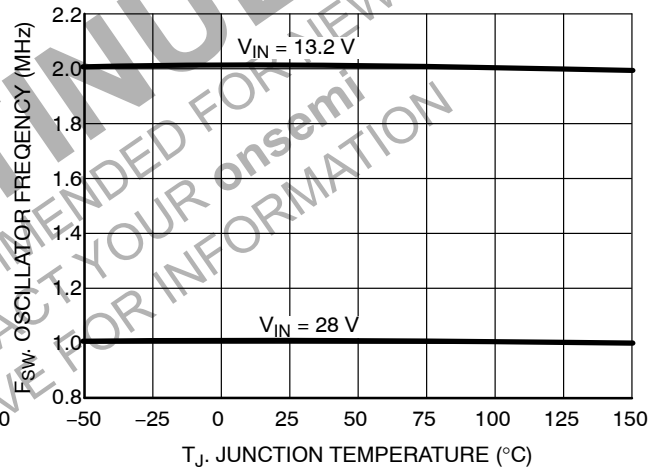


Figure 13. Oscillator Frequency vs. Junction Temperature

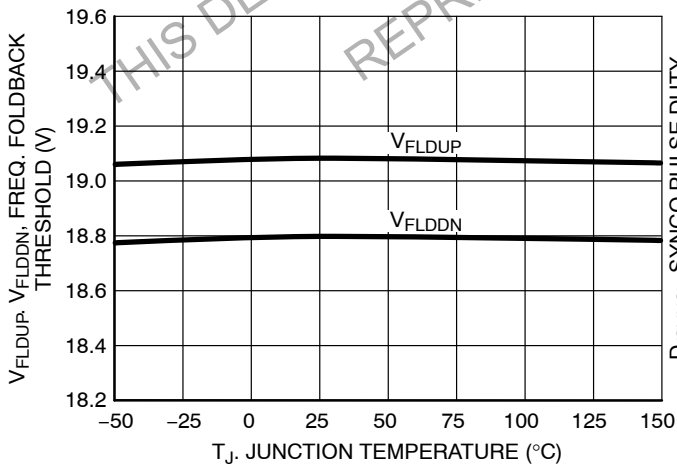


Figure 14. Rising Frequency Foldback Threshold vs. Junction Temperature

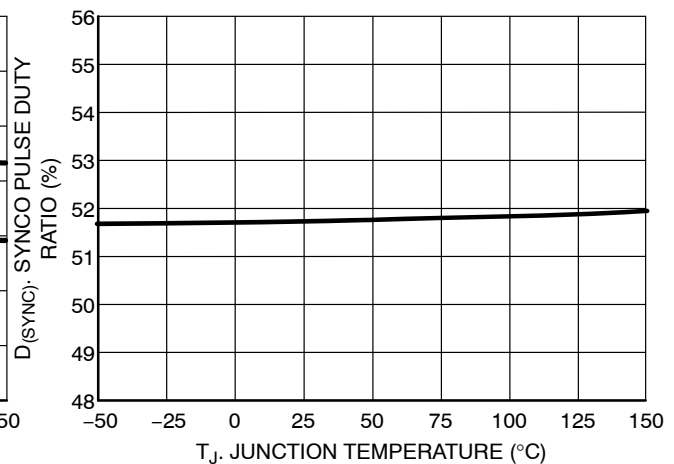


Figure 15. SYNCO Pulse Duty Ratio vs. Junction Temperature

TYPICAL CHARACTERISTICS CURVES

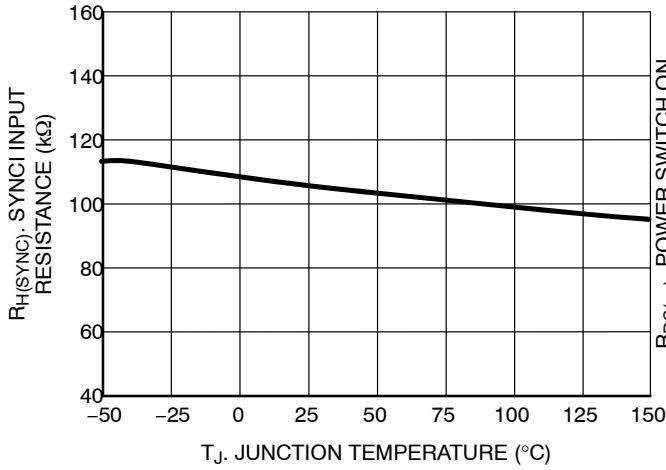


Figure 16. SYNCl Input Resistance vs. Junction Temperature

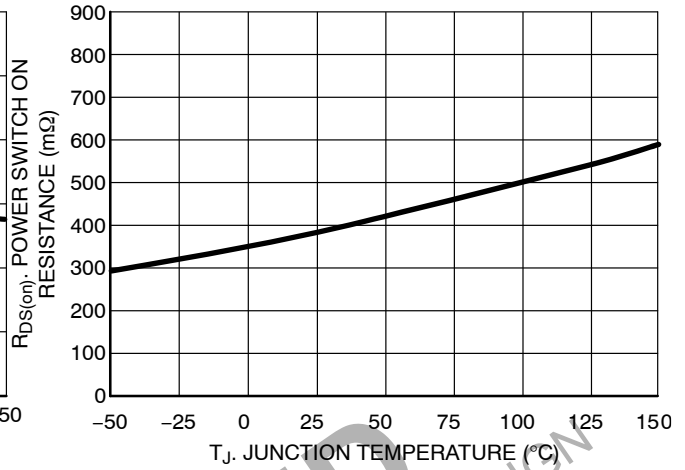


Figure 17. Power Switch R<sub>DS(on)</sub> vs. Junction Temperature

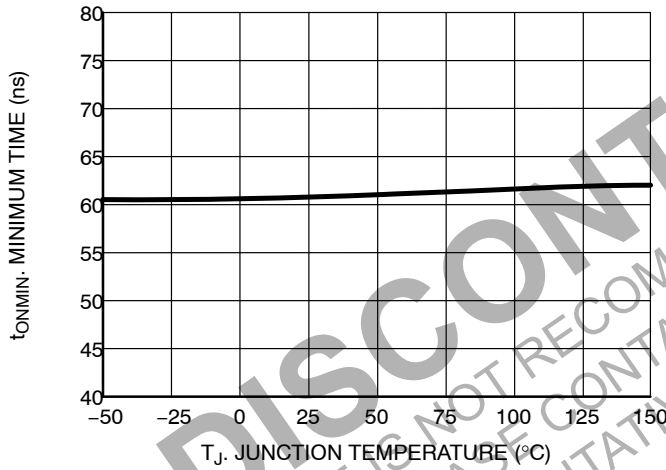


Figure 18. Minimum On Time vs. Junction Temperature

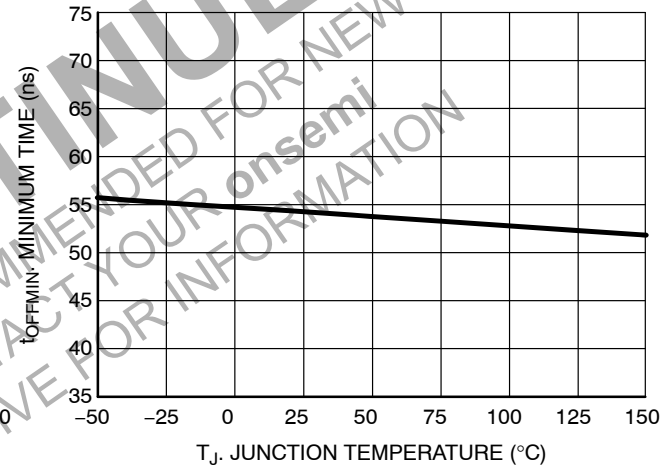


Figure 19. Minimum Off Time vs. Junction Temperature

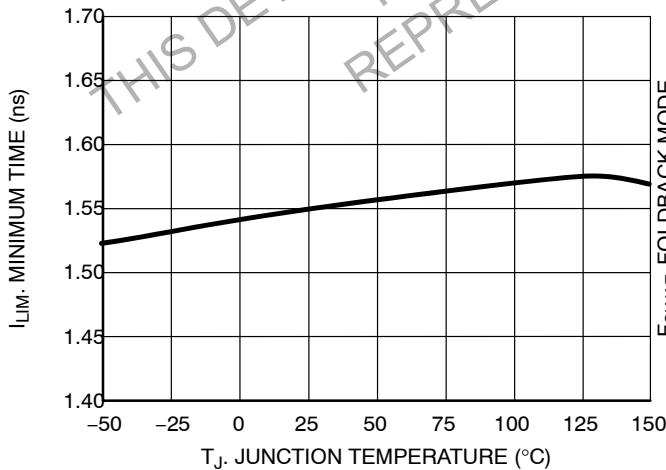


Figure 20. Current Limit Threshold vs. Junction Temperature

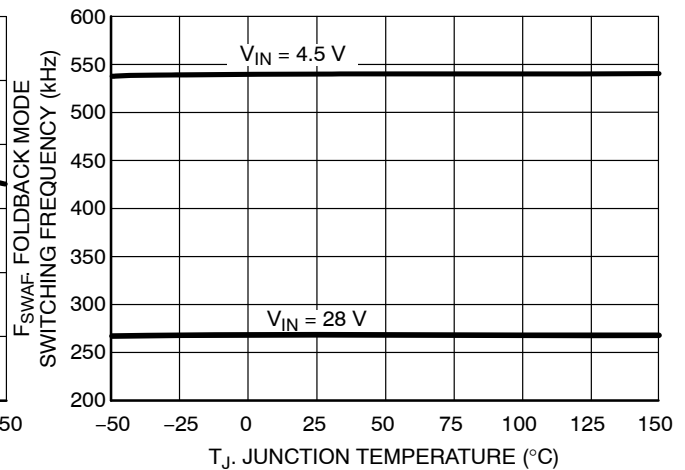


Figure 21. Short-Circuit Foldback Frequency vs. Junction Temperature

TYPICAL CHARACTERISTICS CURVES

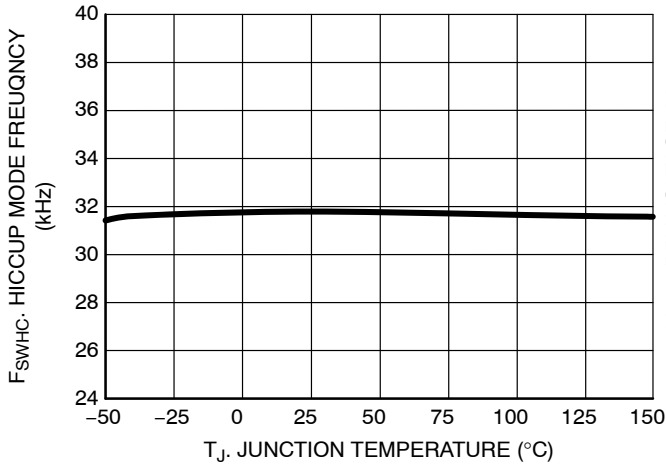


Figure 22. Hiccup Mode Switching Frequency vs. Junction Temperature

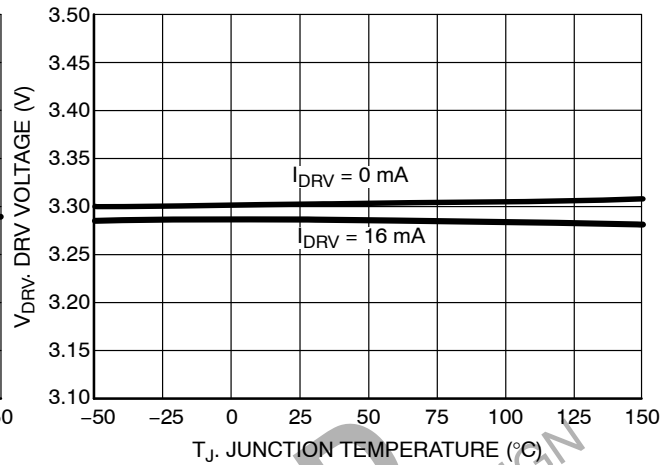


Figure 23. DRV Voltage vs. Junction Temperature

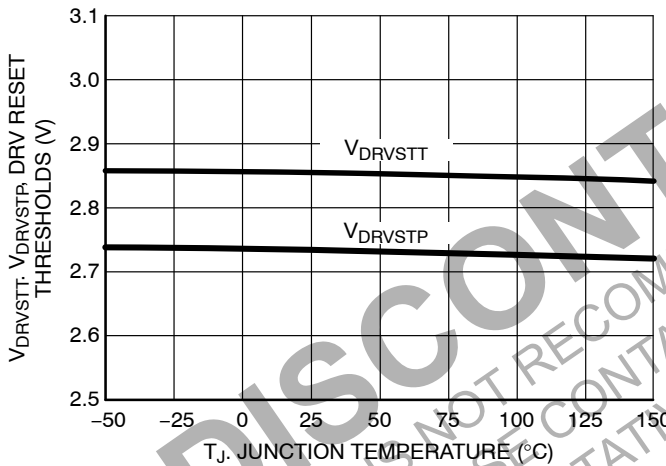


Figure 24. DRV Reset Threshold vs. Junction Temperature

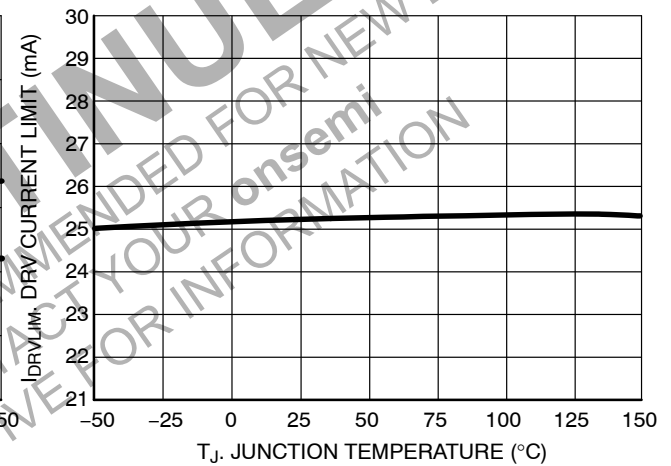


Figure 25. DRV Current Limit vs. Junction Temperature

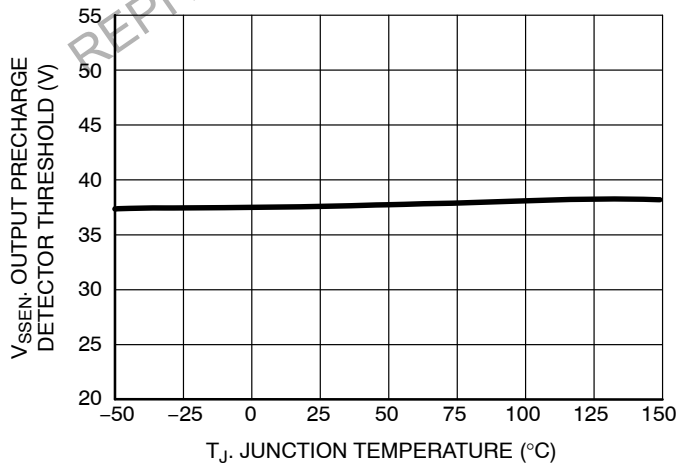


Figure 26. Output Precharge Detector Threshold vs. Junction Temperature

GENERAL INFORMATION

INPUT VOLTAGE

An Undervoltage Lockout (UVLO) circuit monitors the input, and inhibits switching and resets the Soft-start circuit if there is insufficient voltage for proper regulation. The NCV890101 can regulate a 3.3 V output with input voltages above 4.5 V and a 5.0 V output with an input above 6.5 V.

The NCV890101 withstands input voltages up to 40 V.

To limit the power lost in generating the drive voltage for the Power Switch, the switching frequency is reduced by a factor of 2 when the input voltage exceeds the  $V_{IN}$  Frequency Foldback threshold  $V_{FLDUP}$  (see Figure 27). Frequency reduction is automatically terminated when the input voltage drops back below the  $V_{IN}$  Frequency Foldback threshold  $V_{FLDDN}$ .

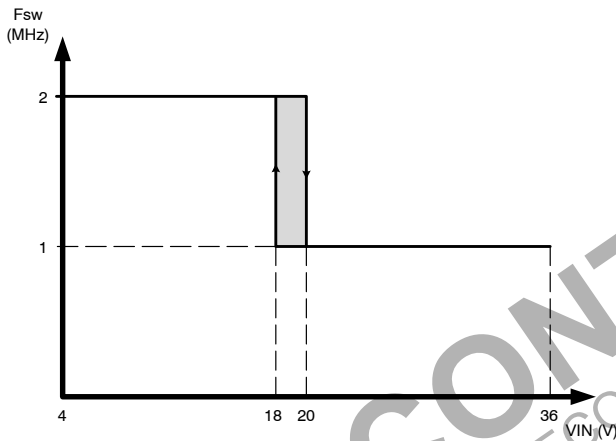


Figure 27. NCV890101 Switching Frequency Reduction at High Input Voltage

ENABLE

The NCV890101 is designed to accept either a logic level signal or battery voltage as an Enable signal. EN low induces a 'sleep mode' which shuts off the regulator and minimizes its supply current to a couple of  $\mu A$  typically ( $I_{qSD}$ ) by disabling all functions. Upon enabling, voltage is established at the DRV pin, followed by a soft-start of the switching regulator output.

SOFT-START

Upon being enabled or released from a fault condition, and after the DRV voltage is established, a soft-start circuit ramps the switching regulator error amplifier reference voltage to the final value. During soft-start, the average switching frequency is lower than its normal mode value (typically 2 MHz) until the output voltage approaches regulation.

SLOPE COMPENSATION

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50%. The fixed amplitude of the slope compensation signal requires the inductor to be greater than a minimum value, depending on output voltage, in order to avoid sub-harmonic oscillations. For 3.3 V and 5 V output voltages, the recommended inductor value is 4.7  $\mu H$ .

SHORT CIRCUIT FREQUENCY FOLDBACK

During severe output overloads or short circuits, the NCV890101 automatically reduces its switching frequency. This creates duty cycles small enough to limit the peak current in the power components, while maintaining the ability to automatically reestablish the output voltage if the overload is removed. If the current is still too high after the switching frequency folds back to 500 kHz, the regulator enters an auto-recovery burst mode that further reduces the dissipated power.

CURRENT LIMITING

Due to the ripple on the inductor current, the average output current of a buck converter is lower than the peak current setpoint of the regulator. Figure 28 shows – for a 4.7  $\mu H$  inductor – how the variation of inductor peak current with input voltage affects the maximum DC current the NCV890101 can deliver to a load.

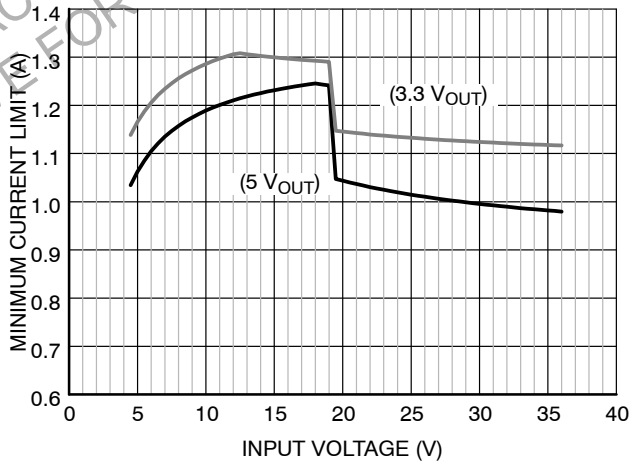


Figure 28. NCV890101 Load Current Capability with 4.7  $\mu H$  Inductor

# NCV890101

## SYNCHRONIZATION

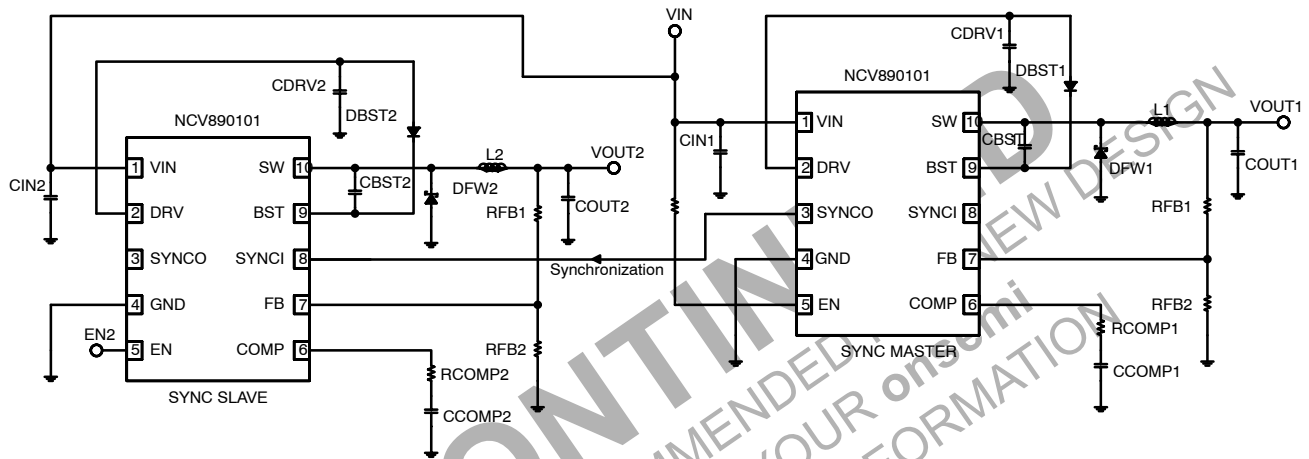
Two NCV890101 can be synchronized out-of-phase to one another by connecting the SYNCO pin of one to the SYNCI pin of the other (Figure 29). Any number of NCV890101 can also be synchronized to an external clock (Figure 30). If a part does not have its switching frequency controlled by the SYNCI input, it drives the SYNCO pin low when it turns on the power switch, and drives it high half a switching period later. When the switching frequency is controlled by the SYNCI input, the SYNCO pin is held low. Synchronization starts within 2 ms of soft-start completion.

A rising edge at the SYNCI pin causes an NCV890101 to immediately turn on the power switch. If another rising edge

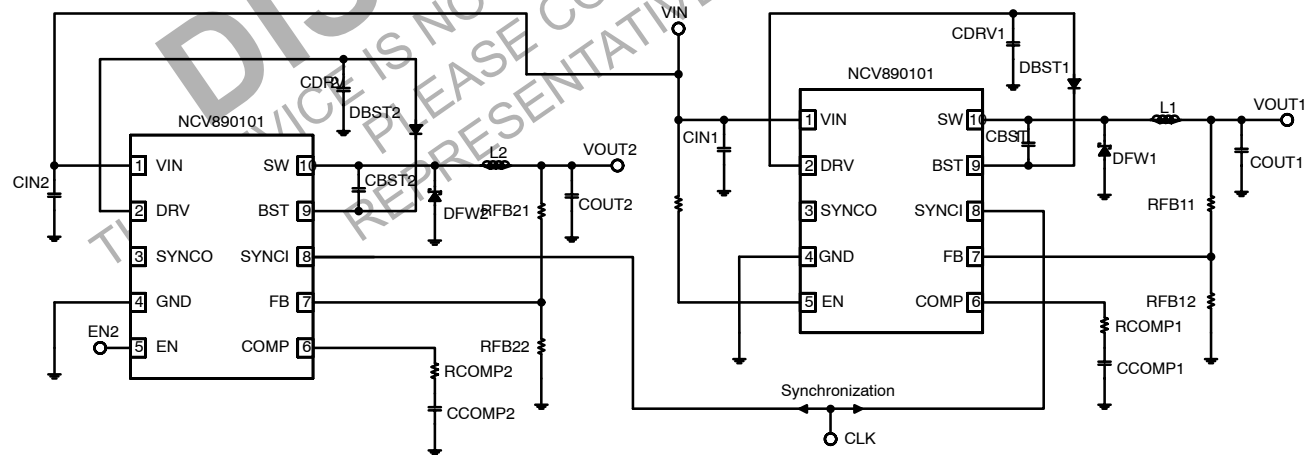
does not arrive at the SYNCI pin within the Master Reassertion Time, the NCV890101 controls its own switching frequency, allowing uninterrupted operation in the event that the clock (or controlling NCV890101) is turned off.

If internal conditions or excessive input voltage cause an NCV890101 to fold back its switching frequency, the main oscillator switching frequency is no longer derived from the frequency received at the SYNCI pin. Under these conditions, the SYNCO pin is held low.

An external pulldown resistor is not required at the SYNCI pin if it is unconnected.



**Figure 29. NCV890101s Synchronized to Each Other  
Master Enabled by Battery**

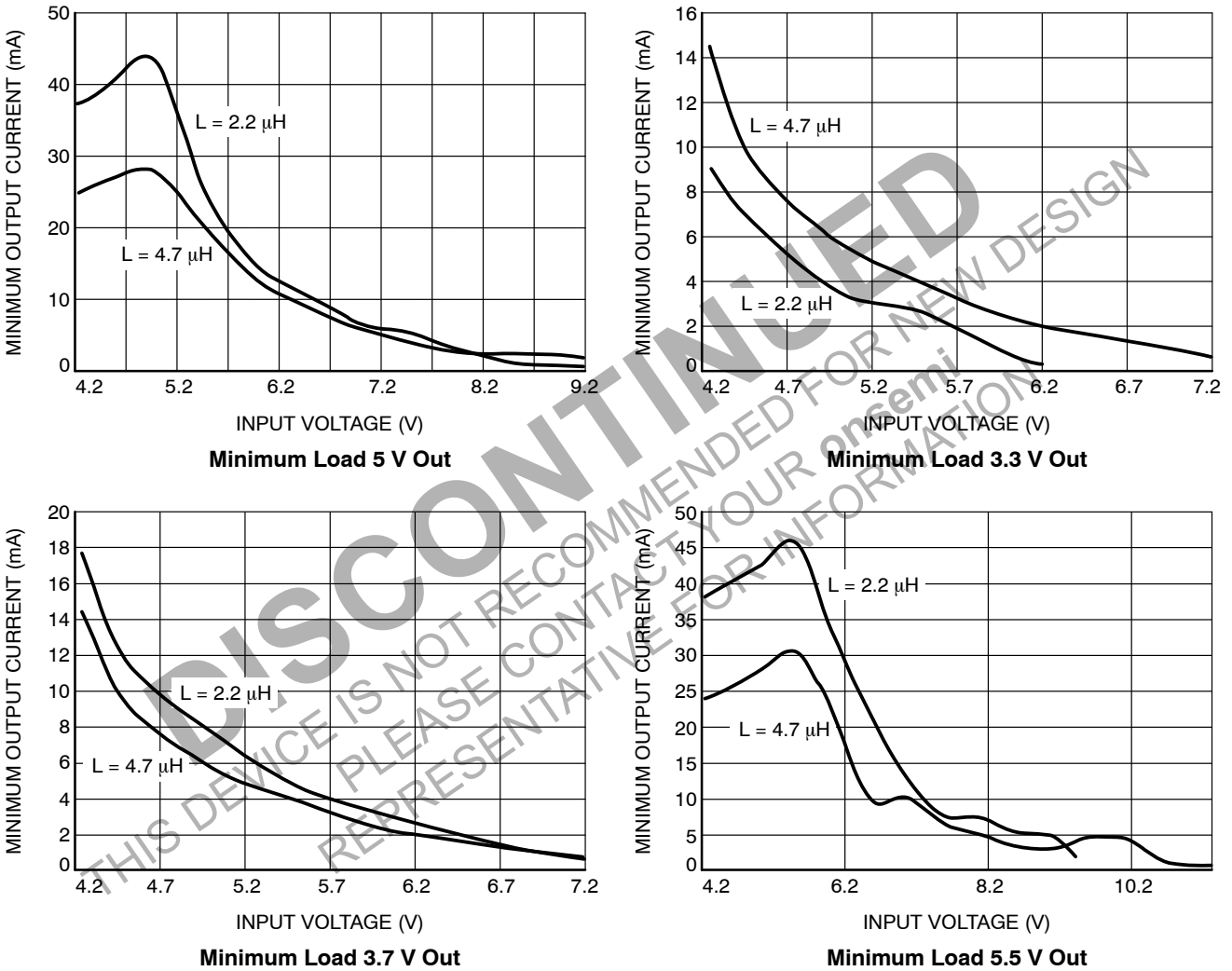


**Figure 30. Both NCV890101s Synchronized to External Clock  
#1 Enabled by Battery**

**BOOTSTRAP**

At the DRV pin an internal regulator provides a ground-referenced voltage to an external capacitor ( $C_{DRV}$ ), to allow fast recharge of the external bootstrap capacitor ( $C_{BST}$ ) used to supply power to the power switch gate driver. If the voltage at the DRV pin goes below the DRV UVLO Threshold  $V_{DRVSTB}$  switching is inhibited and the Soft-start circuit is reset, until the DRV pin voltage goes back up above  $V_{DRVSTT}$ .

In order for the bootstrap capacitor to stay charged, the Switch node needs to be pulled down to ground regularly. In very light load condition, the NCV890101 skips switching cycles to ensure the output voltage stays regulated. When the skip cycle repetition frequency gets too low, the bootstrap voltage collapses and the regulator stops switching. Practically, this means that the NCV890101 needs a minimum load to operate correctly. Figure 31 shows the minimum current requirements for different input and output voltages.



**Figure 31. Minimum Load Current with Different Input and Output Voltages**

**OUTPUT PRECHARGE DETECTION**

Prior to Soft-start, the FB pin is monitored to ensure the SW voltage is low enough to have charged the external bootstrap capacitor (C<sub>BST</sub>). If the FB pin is higher than V<sub>SSEN</sub>, restart is delayed until the output has discharged. Figure 32 shows the IC starts to switch after the voltage on FB pin reaches V<sub>SSEN</sub>, even the EN pin is high. After the IC is switching, the FB pin follows the soft starts reference to reach the final set point.

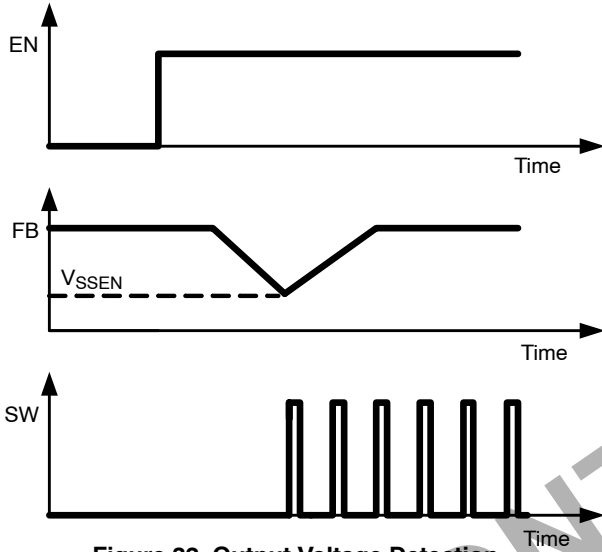


Figure 32. Output Voltage Detection

**THERMAL SHUTDOWN**

A thermal shutdown circuit inhibits switching, resets the Soft-start circuit, and removes DRV voltage if internal temperature exceeds a safe level. Switching is automatically restored when temperature returns to a safe level.

**MINIMUM DROPOUT VOLTAGE**

When operating at low input voltages, two parameters play a major role in imposing a minimum voltage drop across the regulator: the minimum off time (that sets the maximum duty cycle), and the on state resistance.

When operating in continuous conduction mode (CCM), the output voltage is equal to the input voltage multiplied by the duty ratio. Because the NCV890101 needs a sufficient bootstrap voltage to operate, its duty cycle cannot be 100%: it needs a minimum off time (t<sub>OFFmin</sub>) to periodically re-fuel the bootstrap capacitor C<sub>BST</sub>. This imposes a maximum duty ratio D<sub>MAX</sub> = 1 - t<sub>OFFmin</sub>·F<sub>SW(min)</sub>, with the switching frequency being folded back down to F<sub>SW(min)</sub> = 500 kHz to keep regulating at the lowest input voltage possible.

The drop due to the on-state resistance is simply the voltage drop across the Switch resistance R<sub>DSon</sub> at the given output current: V<sub>SWdrop</sub> = I<sub>OUT</sub>·R<sub>DSon</sub>.

Which leads to the maximum output voltage in low Vin condition: V<sub>OUT</sub> = D<sub>MAX</sub>·V<sub>IN(min)</sub> - V<sub>SWdrop</sub>

**EXPOSED PAD**

The exposed pad (EPAD) on the back of the package must be electrically connected to the electrical ground (GND pin) for proper, noise-free operation.

**DESIGN METHODOLOGY**

The NCV890101 being a fixed-frequency regulator with the switching element integrated, is optimized for one value of inductor. This value is set to 4.7 μH, and the slope compensation is adjusted for this inductor. The only components left to be designed are the input and output capacitor and the freewheeling diode. Please refer to the design spreadsheet [www.onsemi.com](http://www.onsemi.com) NCV890101 page that helps with the calculation.

Output capacitor:

The minimum output capacitor value can be calculated based on the specification for output voltage ripple:

$$C_{OUTmin} = \frac{\Delta I_L}{8 \cdot \Delta V_{OUT} \cdot F_{SW}} \quad (\text{eq. 1})$$

With

- ΔI<sub>L</sub> the inductor ripple current:

$$\Delta I_L = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \cdot F_{SW}} \quad (\text{eq. 2})$$

- ΔV<sub>OUT</sub> the desired voltage ripple.

However, the ESR of the output capacitor also contributes to the output voltage ripple, so to comply with the requirement, the ESR cannot exceed R<sub>ESRmax</sub>:

$$R_{ESRmax} = \frac{\Delta V_{OUT} \cdot L \cdot F_{SW}}{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (\text{eq. 3})$$

Finally, the output capacitor must be able to sustain the ac current (or RMS ripple current):

$$I_{OUTac} = \frac{\Delta I_L}{2\sqrt{3}} \quad (\text{eq. 4})$$

Typically, with the recommended 4.7 μH inductor, two ceramic capacitors of 10 μF each in parallel give very good results.

Freewheeling diode:

The diode must be chosen according to its maximum current and voltage ratings, and to thermal considerations.

As far as max ratings are concerned, the maximum reverse voltage the diode sees is the maximum input voltage (with some margin in case of ringing on the Switch node), and the maximum forward current the peak current limit of the NCV890101, I<sub>LIM</sub>.

The power dissipated in the diode is P<sub>Dloss</sub>:

$$P_{Dloss} = I_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot V_F + I_{DRMS} \cdot R_D \quad (\text{eq. 5})$$

with:

- $I_{OUT}$  the average (dc) output current
- $V_F$  the forward voltage of the diode
- $I_{DRMS}$  the RMS current in the diode:

$$I_{DRMS} = \sqrt{(1 - D) \left( I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right)} \quad (\text{eq. 6})$$

- $R_D$  the dynamic resistance of the diode (extracted from the V/I curve of the diode in its datasheet).

Then, knowing the thermal resistance of the package and the amount of heatsinking on the PCB, the temperature rise corresponding to this power dissipation can be estimated.

Input capacitor:

The input capacitor must sustain the RMS input ripple current  $I_{INac}$ :

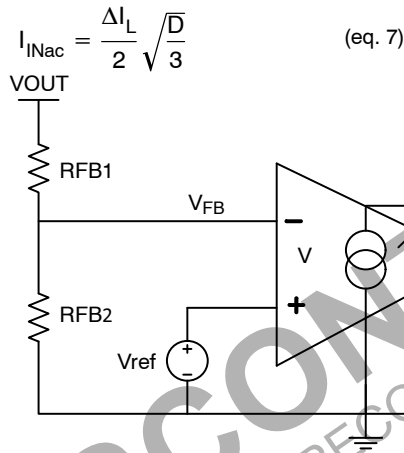


Figure 33. Feedback Compensator Network Model

The transfer function from VOUT to VCOMP is the product of the feedback voltage divider and the error amplifier.

$$G_{divider}(s) = \frac{RFB2}{RFB1 + RFB2} \quad (\text{eq. 8})$$

$$G_{err\_amp}(s) = gm \cdot Ro \cdot \frac{1 + \frac{s}{\omega Z}}{\left(1 + \frac{s}{\omega_{pl}}\right) \left(1 + \frac{s}{\omega_{ph}}\right)} \quad (\text{eq. 9})$$

$$\omega Z = \frac{1}{R_{COMP} \cdot C_{COMP}} \quad (\text{eq. 10})$$

$$\omega_{pl} = \frac{1}{Ro \cdot C_{COMP}} \quad (\text{eq. 11})$$

$$\omega_{ph} = \frac{1}{R_{COMP} \cdot C_p} \quad (\text{eq. 12})$$

The output resistor  $Ro$  of the error amplifier is 1.4 MΩ and  $gm$  is 1 mA/V. The capacitor  $Cp$  is for rejecting noise at high frequency and is integrated inside the IC with a value of 18 pF.

The power stage transfer function (from Vcomp to output) is shown below:

$$G_{ps}(s) = \frac{R_{load}}{R_i} \cdot \frac{1}{1 + \frac{R_{load} \cdot T_{sw}}{L} \cdot [Mc \cdot (1 - D) - 0.5]} \cdot \frac{1 + \frac{s}{\omega Z}}{1 + \frac{s}{\omega p}} \cdot F_h(s) \quad (\text{eq. 13})$$

$$\omega p = \frac{1}{R_{esr} \cdot C_{out}} \quad (\text{eq. 14})$$

$$\omega p = \frac{1}{R_{load} \cdot C_{out}} + \frac{Mc \cdot (1 - D) - 0.5}{L \cdot C_{out} \cdot F_{sw}} \quad (\text{eq. 15})$$

It can be designed in combination with an inductor to build an input filter to filter out the ripple current in the source, in order to reduce EMI conducted emissions.

For example, using a 4.7 μH input capacitor, it is easy to calculate that an inductor of 200 nH will ensure that the input filter has a cut-off frequency below 200 kHz (low enough to attenuate the 2 MHz ripple).

### Error Amplifier and Loop Transfer Function

The error amplifier is a transconductance type amplifier. The output voltage of the error amplifier controls the peak inductor current at which the power switch shuts off. The Current Mode control method employed allows the use of a simple, type II compensation to optimize the dynamic response according to system requirements.

Figure 33 shows the error amplifier with the compensation components and the voltage feedback divider.

where

$$M_c = 1 + \frac{S_e}{S_n} \quad (\text{eq. 16})$$

$$S_n = \frac{V_{in} - V_{out}}{L} \cdot R_i \quad (\text{eq. 17})$$

$R_i$  represents the equivalent sensing resistor which has a value of  $0.29 \Omega$ ,  $S_e$  is the compensation slope which is  $291.9 \text{ kV/S}$ ,  $S_n$  is the slope of the sensing resistor current during on time.  $F_h(s)$  represents the sampling effect from the current loop which has two poles at one half of the switching frequency:

$$F_h(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_p} + \frac{s^2}{\omega_n^2}} \quad (\text{eq. 18})$$

$$\omega_n = \pi \cdot F_{sw}$$

$$Q_p = \frac{1}{\pi \cdot [M_c \cdot (1 - D) - 0.5]} \quad (\text{eq. 19})$$

The total loop transfer function is the product of power stage and feedback compensation network.

$$G_{loop}(s) = G_{divider}(s) \cdot G_{err\_amp}(s) \cdot G_{ps}(s) \quad (\text{eq. 20})$$

The bode plots of the open loop transfer function will show the gain and phase margin of the system. The compensation network is designed to make sure the system has enough phase margin and bandwidth.

### Design of the Compensation Network

The function of the compensation network is to provide enough phase margin at crossover frequency to stabilize the system as well as to provide high gain at low frequency to eliminate the steady state error of the output voltage. Please refer to the design spreadsheet [www.onsemi.com](http://www.onsemi.com) NCV890101 page that helps with the calculation.

The design steps will be introduced through an example.

Example:

$V_{in} = 15.5 \text{ V}$ ,  $V_{out} = 3.3 \text{ V}$ ,  $R_{load} = 2.75 \Omega$ ,  $I_{out} = 1.2 \text{ A}$ ,  $L = 4.7 \mu\text{H}$ ,  $C_{out} = 20 \mu\text{F}$  ( $R_{esr} = 7 \text{ m}\Omega$ )

The reference voltage of the feedback signal is  $0.8 \text{ V}$  and to meet the minimum load requirements, select  $R_{FB1} = 100 \Omega$ ,  $R_{FB2} = 31.6 \Omega$ .

From the specification, the power stage transfer function can be plotted as below:

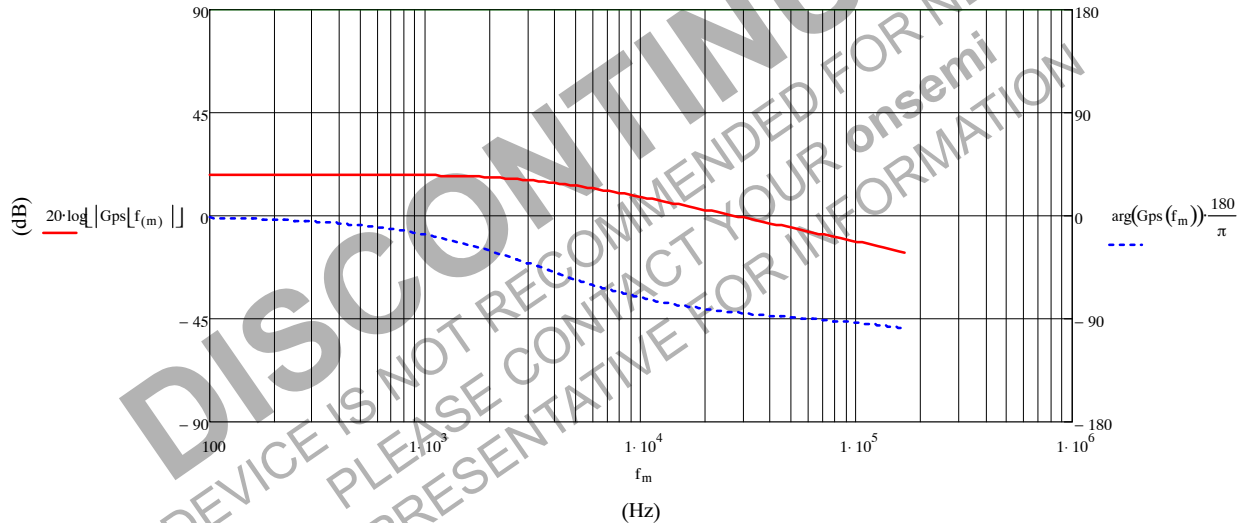


Figure 34. Power Stage Bode Plots

The crossover frequency is chosen to be  $F_c = 70 \text{ kHz}$ , the power stage gain at this frequency is  $-8 \text{ dB}$  ( $0.398$ ) from calculation. Then the gain of the feedback compensation network must be  $8 \text{ dB}$ . Next is to decide the locations of one zero and one pole of the compensator. The zero is to provide phase boost at the crossover frequency and the pole is to reject the noise of high frequency. In this example, a zero is placed at  $1/10$  of the crossover frequency and a pole is placed at  $1/5$  of the switching frequency ( $F_{sw} = 2 \text{ MHz}$ ):

$F_z = 7000 \text{ Hz}$ ,  $F_p = 400000 \text{ Hz}$ ,

$R_{COMP}$ ,  $C_{COMP}$  and  $C_p$  can be calculated from the following equations:

$$R_{COMP} = \frac{F_p \cdot g_m}{(F_p - F_z) \cdot |G_{ps}(F_c)|} \cdot \frac{V_{out}}{V_{ref}} \cdot \frac{\sqrt{1 + \left(\frac{F_c}{F_p}\right)^2}}{\sqrt{1 + \left(\frac{F_z}{F_c}\right)^2}} \quad (\text{eq. 21})$$

$$C_{COMP} = \frac{1}{2\pi \cdot F_z \cdot R_{COMP}} \quad (\text{eq. 22})$$

$$C_p = \frac{1}{2\pi \cdot F_p \cdot R_{COMP}} \quad (\text{eq. 23})$$

Note: there is an  $18 \text{ pF}$  capacitor at the output of the OTA integrated in the IC, and if a larger capacitor needs to be used, subtract this value from the calculated  $C_p$ . Figure 35 shows  $C_p$  is split into two capacitors.  $C_{int}$  is the  $18 \text{ pF}$  in the IC.  $C_{ext}$  is the extra capacitor added outside the IC.

From the calculation:

$R_{COMP} = 10.6 \text{ K}\Omega$ ,  $C_{COMP} = 2 \text{ nF}$ ,  $C_p = 37 \text{ pF}$

So the feedback compensation network is as below:

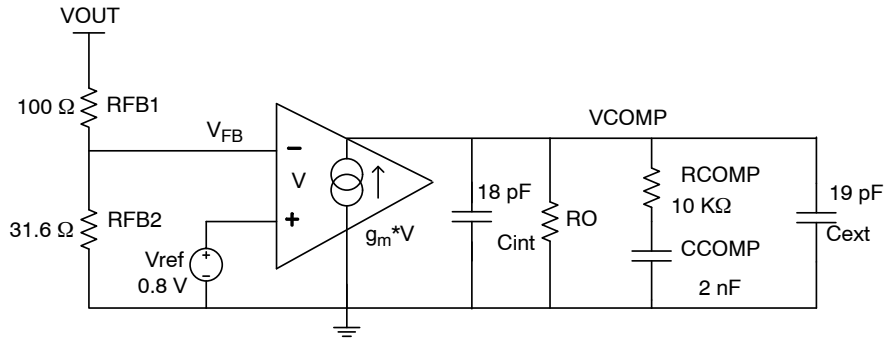


Figure 35. Example of the Feedback Compensation Network

Figure 36 shows the bode plot of the OTA compensator

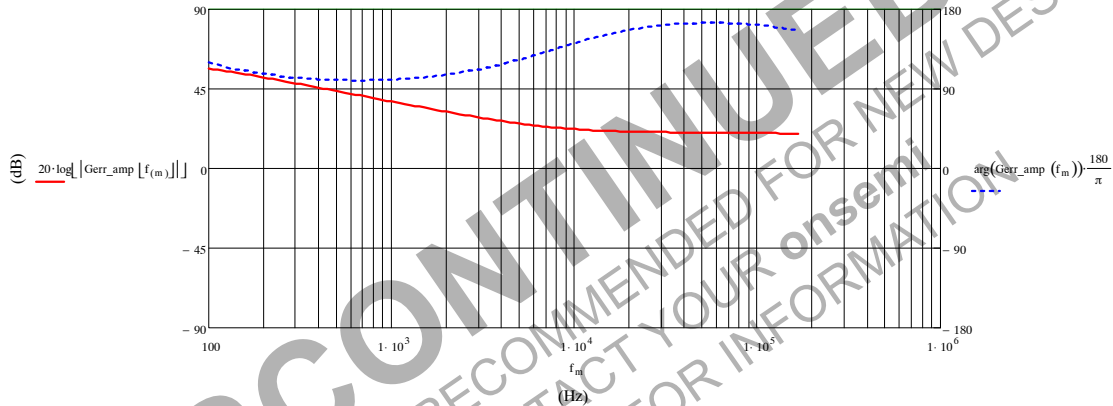


Figure 36. Bode Plot of the OTA Compensator

The total loop bode plot is as below:

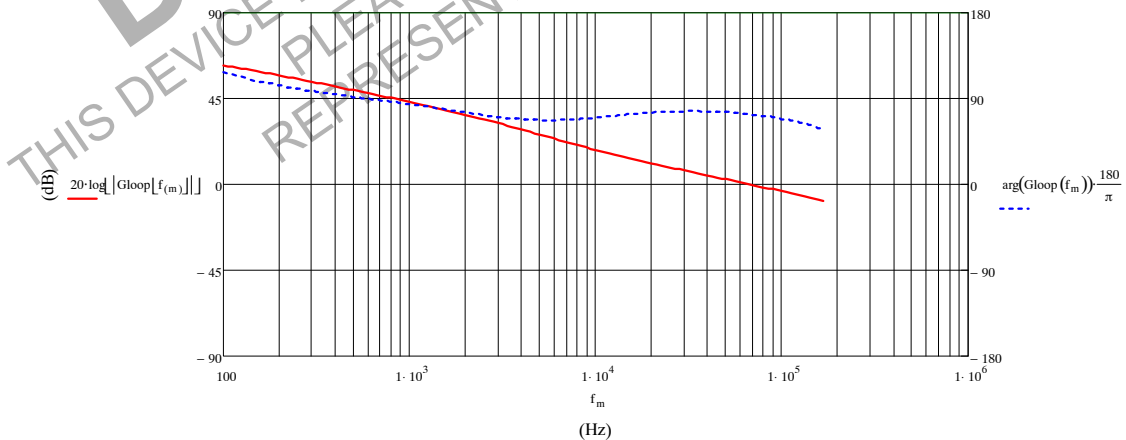


Figure 37. Bode Plot of the Total Loop

The crossover frequency is at 70 KHz and phase margin is 75 degrees.

## NCV890101

### PCB LAYOUT RECOMMENDATION

As with any switching power supplies, there are some guidelines to follow to optimize the layout of the printed circuit board for the NCV890101. However, because of the high switching frequency extra care has to be taken.

– Minimize the area of the power current loops:

- ◆ Input capacitor → NCV890101 switch → Inductor  
→ output capacitor → return through Ground

- ◆ Freewheeling diode → inductor → Output capacitor  
→ return through ground
- Minimize the length of high impedance signals, and route them far away from the power loops:
  - ◆ Feedback trace
  - ◆ Comp trace

### ORDERING INFORMATION

Device	Package	Shipping†
NCV890101MWTXG	DFN10 with wettable flanks (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**DISCONTINUED**  
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN  
PLEASE CONTACT YOUR onsemi  
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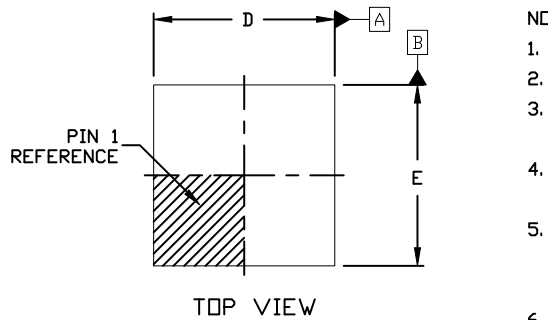
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

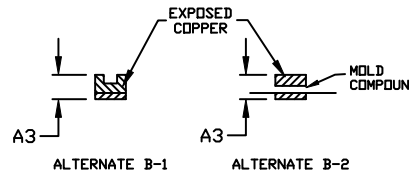
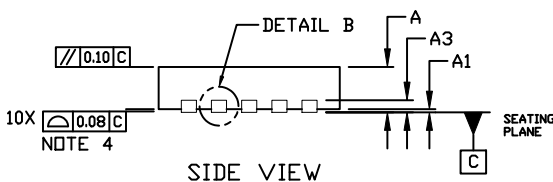
## DFN10, 3x3, 0.5P CASE 485C ISSUE F

DATE 16 DEC 2021

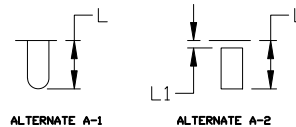
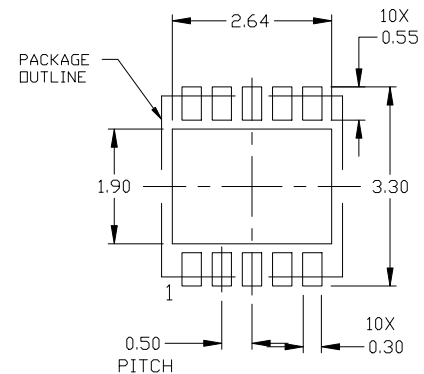
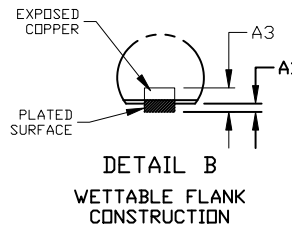
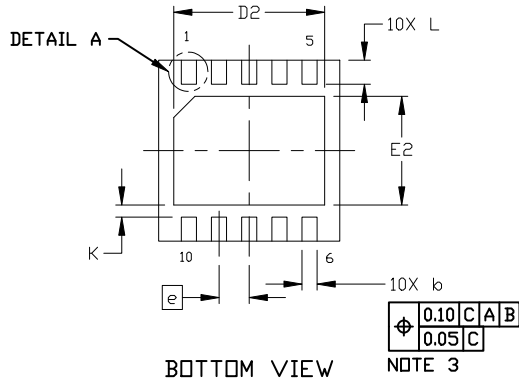


### NOTES:

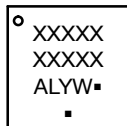
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL *b* MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
<i>b</i>	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
<i>e</i>	0.50 BSC		
K	0.20 REF		
L	0.30	0.40	0.50
L1	---	---	0.03



### GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

### RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>DFN10, 3X3 MM, 0.5 MM PITCH</b>	<b>PAGE 1 OF 1</b>

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-  Alternative Solution
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