DATA SHEET

BF1212; BF1212R; BF1212WR

N-channel dual-gate MOS-FETs

Product specification

2003 Nov 14

N-channel dual-gate MOS-FETs

BF1212; BF1212R; BF1212WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Excellent low frequency noise performance
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

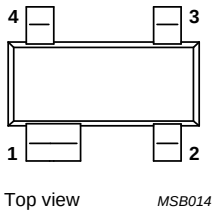
- Gain controlled low noise VHF and UHF amplifiers for 5 V digital and analog television tuner applications.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1212, BF1212R and BF1212WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

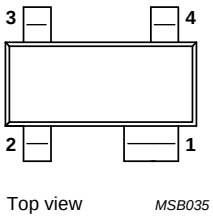
PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



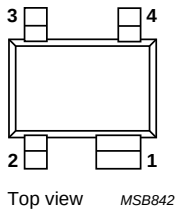
BF1212; marking code: LGp

Fig.1 Simplified outline (SOT143B).



BF1212R; marking code: LKp

Fig.2 Simplified outline (SOT143R).



BF1212WR; marking code: ML

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	6	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	180	mW
$\lvert y_{fs} \rvert$	forward transfer admittance		28	33	43	mS
C_{ig1-ss}	input capacitance at gate 1		–	1.7	2.2	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	15	30	fF
F	noise figure	f = 800 MHz	–	1.1	1.8	dB
X_{mod}	cross-modulation	input level for k = 1 % at 40 dB AGC	100	104	–	dBμV
T_j	junction temperature		–	–	150	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BF1212	–	plastic surface mounted package; 4 leads	SOT143B
BF1212R	–	plastic surface mounted package; reverse pinning; 4 leads	SOT143R
BF1212WR	–	plastic surface mounted package; reverse pinning; 4 leads	SOT343R

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

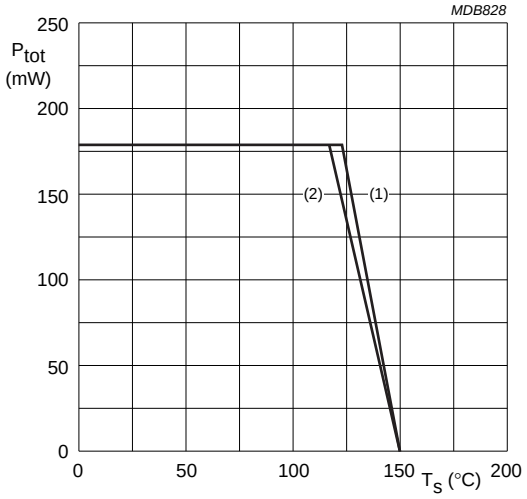
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	6	V
I_D	drain current (DC)		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation				
	BF1212; BF1212R	$T_s \leq 116$ °C; note 1	–	180	mW
	BF1212WR	$T_s \leq 122$ °C; note 1	–	180	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

Note

1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		
	BF1212; BF1212R	185	K/W
	BF1212WR	155	K/W



(1) BF1212WR.
(2) BF1212; BF1212R.

Fig.4 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$ V; $I_D = 10$ μA	6	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$ V; $I_{G1-S} = 10$ mA	6	10	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$ V; $I_{G2-S} = 10$ mA	6	10	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$ V; $I_{S-G1} = 10$ mA	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$ V; $I_{S-G2} = 10$ mA	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4$ V; $V_{DS} = 5$ V; $I_D = 100$ μA	0.3	1.0	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 5$ V; $V_{DS} = 5$ V; $I_D = 100$ μA	0.35	1.0	V
I_{DSX}	drain-source current	$V_{G2-S} = 4$ V; $V_{DS} = 5$ V; $R_{G1} = 150$ kΩ; note 1	8	16	mA
I_{G1-S}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$ V; $V_{G1-S} = 5$ V	–	50	nA
I_{G2-S}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$ V; $V_{G2-S} = 4$ V	–	20	nA

Note

1. R_{G1} connects G_1 to $V_{GG} = 5$ V.

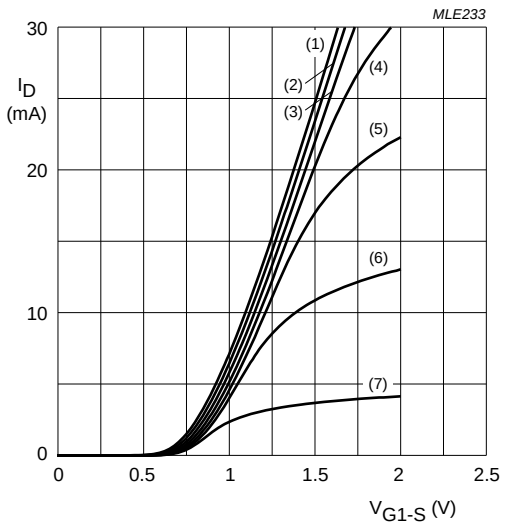
DYNAMIC CHARACTERISTICS

Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 12 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|y_{fs}\|$	forward transfer admittance	pulsed; T_j = 25 °C	28	33	43	mS
C_{ig1-ss}	input capacitance at gate 1	f = 1 MHz	–	1.7	2.2	pF
C_{ig2-ss}	input capacitance at gate 2	f = 1 MHz	–	1.1	–	pF
C_{oss}	output capacitance	f = 1 MHz	–	0.9	–	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	15	30	fF
F	noise figure	f = 11 MHz; G_S = 20 mS; B_S = 0	–	4	–	dB
		f = 400 MHz; $Y_S = Y_{S\ (opt)}$	–	0.9	1.6	dB
		f = 800 MHz; $Y_S = Y_{S\ (opt)}$	–	1.1	1.8	dB
G_{tr}	power gain	f = 200 MHz; G_S = 2 mS; $B_S = B_{S\ (opt)}$; G_L = 0.5 mS; $B_L = B_{L\ (opt)}$	–	35	–	dB
		f = 400 MHz; G_S = 2 mS; $B_S = B_{S\ (opt)}$; G_L = 1 mS; $B_L = B_{L\ (opt)}$	–	30	–	dB
		f = 800 MHz; G_S = 3.3 mS; $B_S = B_{S\ (opt)}$; G_L = 1 mS; $B_L = B_{L\ (opt)}$	–	25	–	dB
X_{mod}	cross-modulation	input level for k = 1%; f_w = 50 MHz; f_{unw} = 60 MHz; note 1				
		at 0 dB AGC	90	–	–	dBμV
		at 10 dB AGC	–	89	–	dBμV
		at 40 dB AGC	100	104	–	dBμV

Note

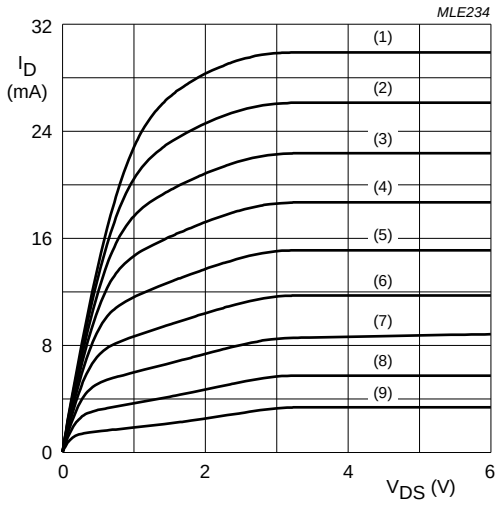
1. Measured in test circuit Fig.21.



(1) V_{G2-S} = 4 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1 V.

V_{DS} = 5 V.
T_j = 25 °C.

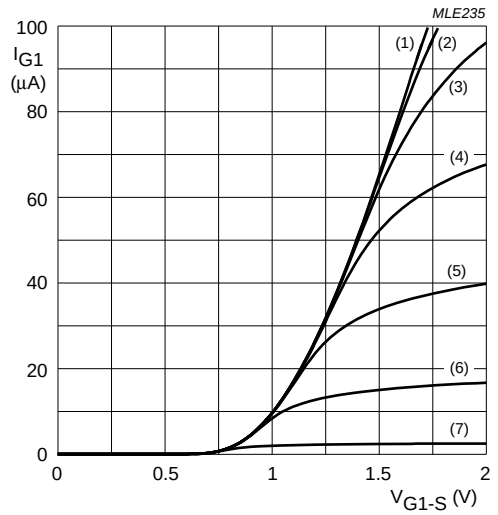
Fig.5 Transfer characteristics; typical values.



(1) V_{G1-S} = 1.6 V.
(2) V_{G1-S} = 1.5 V.
(3) V_{G1-S} = 1.4 V.
(4) V_{G1-S} = 1.3 V.
(5) V_{G1-S} = 1.2 V.
(6) V_{G1-S} = 1.1 V.
(7) V_{G1-S} = 1.0 V.
(8) V_{G1-S} = 0.9 V.
(9) V_{G1-S} = 0.8 V.

V_{G2-S} = 4 V.
T_j = 25 °C.

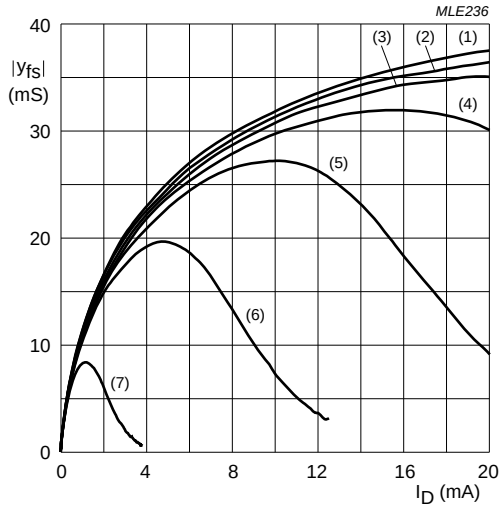
Fig.6 Output characteristics; typical values.



(1) V_{G2-S} = 4 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1 V.

V_{DS} = 5 V.
T_j = 25 °C.

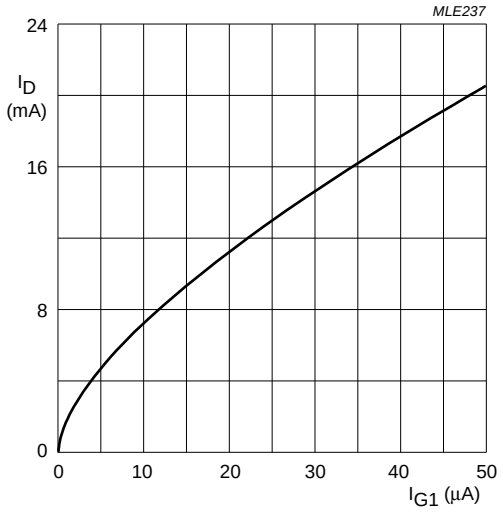
Fig.7 Gate 1 current as a function of gate 1 voltage; typical values.



(1) V_{G2-S} = 4 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1 V.

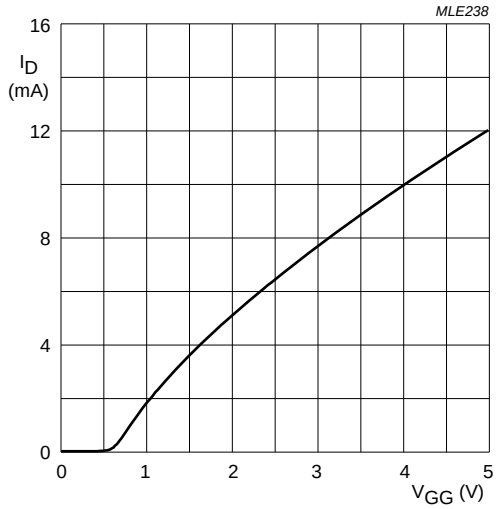
V_{DS} = 5 V.
T_j = 25 °C.

Fig.8 Forward transfer admittance as a function of drain current; typical values.



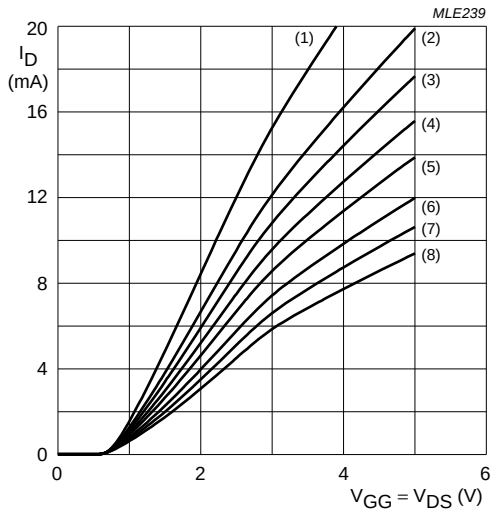
V_{DS} = 5 V; V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.9 Drain current as a function of gate 1 current; typical values.



V_{DS} = 5 V; V_{G2-S} = 4 V; T_j = 25 °C.
R_{G1} = 150 kΩ (connected to V_{GG}); see Fig.21.

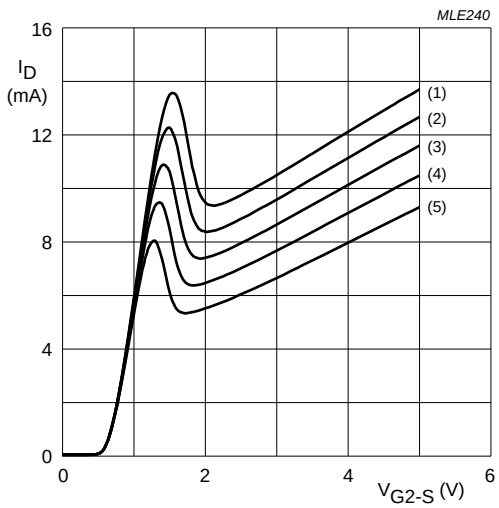
Fig.10 Drain current as a function of gate 1 supply voltage; typical values.



(1) R_{G1} = 47 kΩ.
(2) R_{G1} = 56 kΩ.
(3) R_{G1} = 82 kΩ.
(4) R_{G1} = 100 kΩ.
(5) R_{G1} = 120 kΩ.
(6) R_{G1} = 150 kΩ.
(7) R_{G1} = 180 kΩ.
(8) R_{G1} = 220 kΩ.

V_{G2-S} = 4 V; T_j = 25 °C.
R_{G1} connected to V_{GG}; see Fig.21.

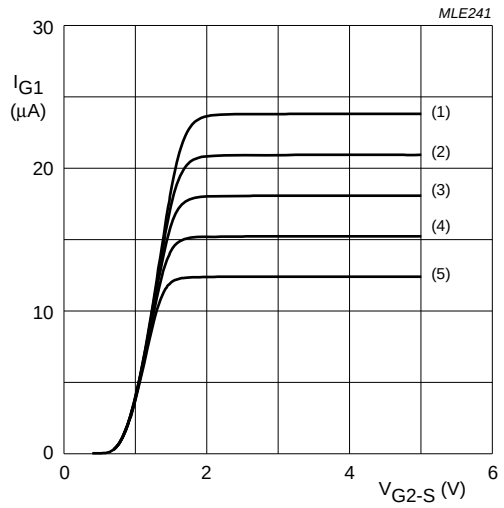
Fig.11 Drain current as a function of gate 1 and drain supply voltage; typical values.



(1) V_{GG} = 5 V.
(2) V_{GG} = 4.5 V.
(3) V_{GG} = 4 V.
(4) V_{GG} = 3.5 V.
(5) V_{GG} = 3 V.

V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 150 kΩ (connected to V_{GG}); see Fig.21.

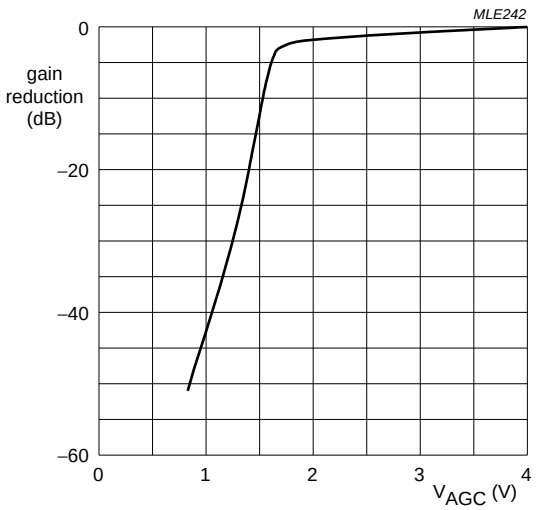
Fig.12 Drain current as a function of gate 2 voltage; typical values.



(1) V_{GG} = 5 V.
(2) V_{GG} = 4.5 V.
(3) V_{GG} = 4 V.
(4) V_{GG} = 3.5 V.
(5) V_{GG} = 3 V.

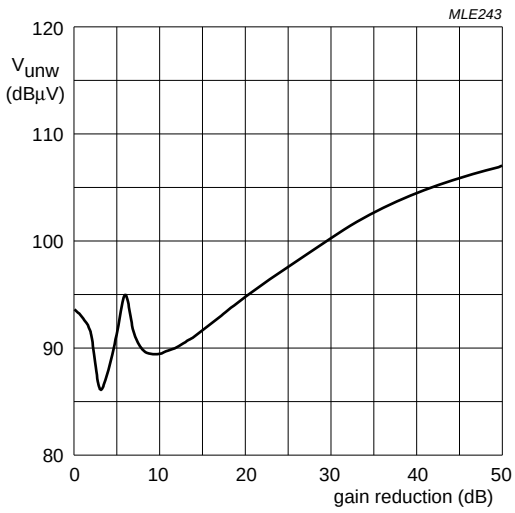
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 150 kΩ (connected to V_{GG}); see Fig.21.

Fig.13 Gate 1 current as a function of gate 2 voltage; typical values.



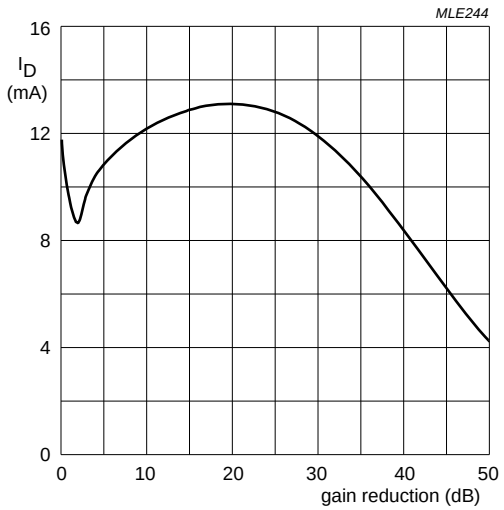
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 150 kΩ (connected to V_{GG}); see Fig.21; f = 50 MHz; T_{amb} = 25 °C.

Fig.14 Typical gain reduction as a function of AGC voltage.



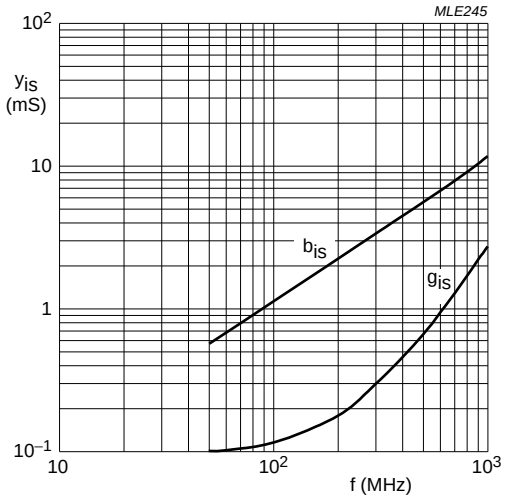
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 150 kΩ (connected to V_{GG}); see Fig.21; f= 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.15 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values.



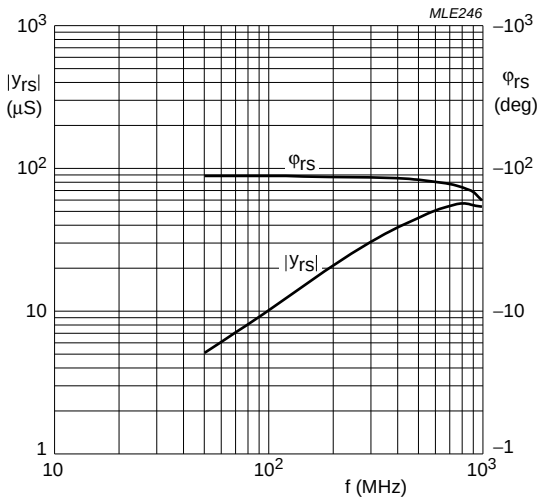
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 150 kΩ (connected to V_{GG}); see Fig.21; f= 50 MHz; T_{amb} = 25 °C.

Fig.16 Drain current as a function of gain reduction; typical values.



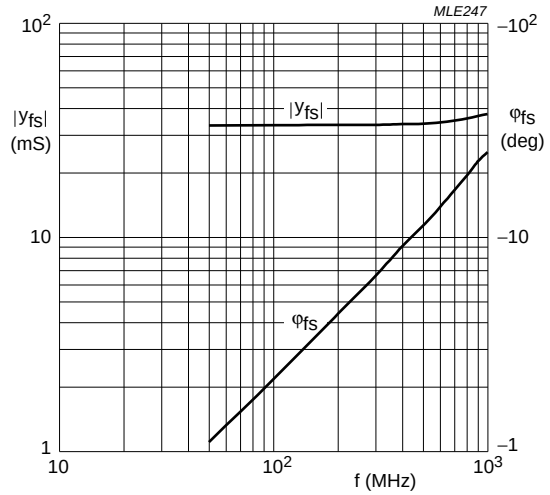
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.17 Input admittance as a function of frequency; typical values.



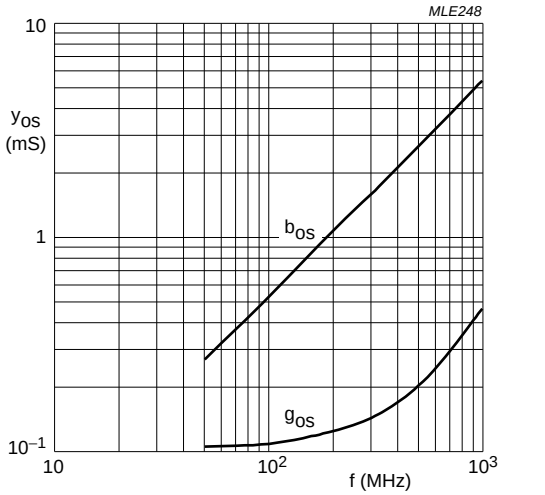
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.18 Reverse transfer admittance and phase as functions of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.19 Forward transfer admittance and phase as functions of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.20 Output admittance as a function of frequency; typical values.

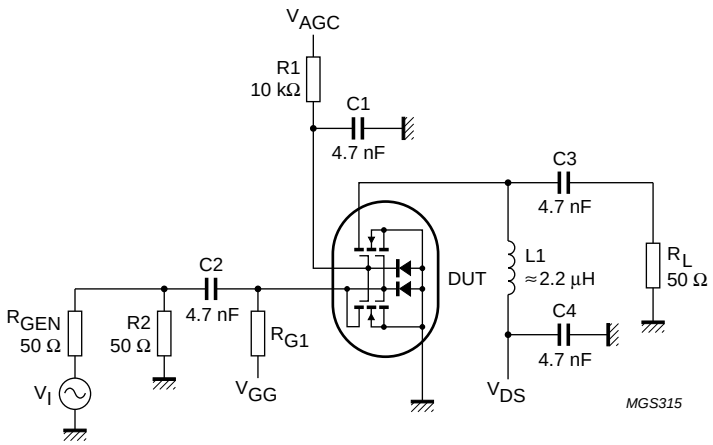


Fig.21 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 12 mA; T_{amb} = 25 °C

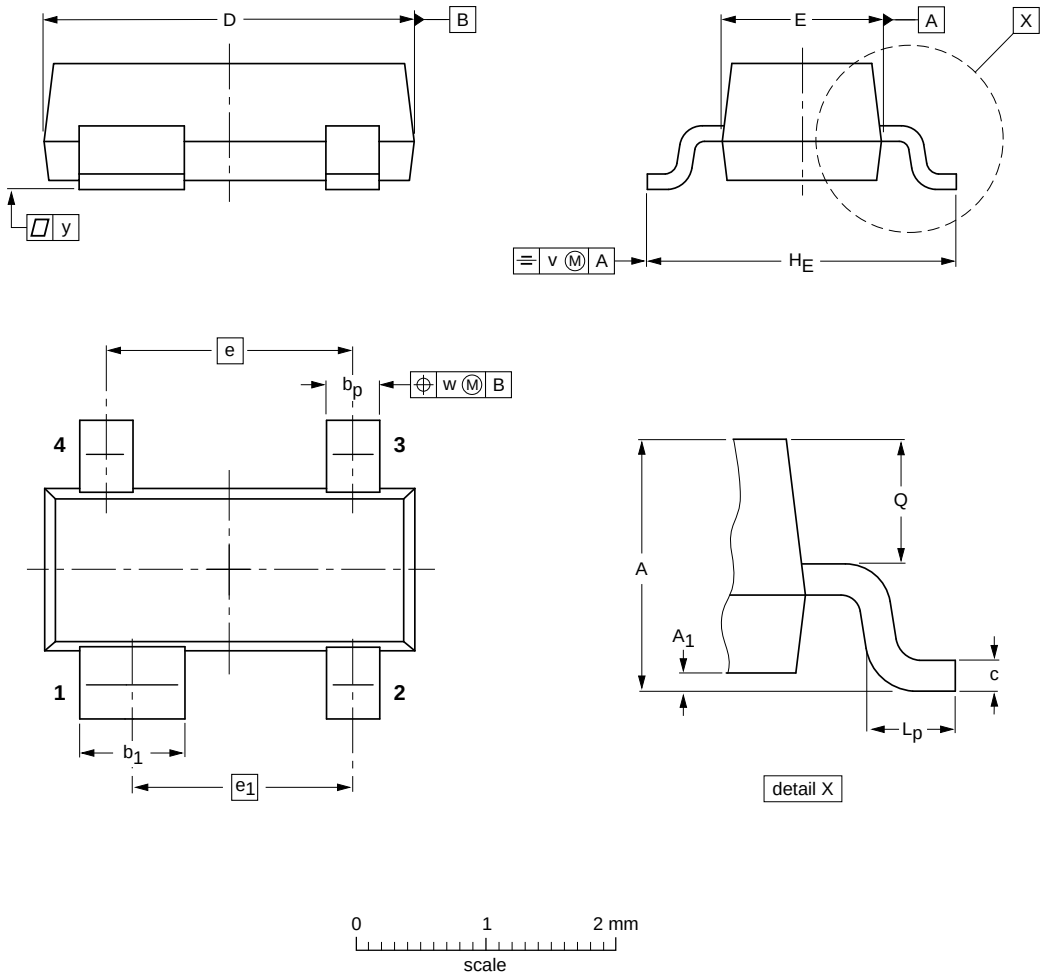
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.990	−3.39	3.288	176.5	0.0005	86.9	0.990	−1.66
100	0.988	−6.76	3.280	173.0	0.0011	85.6	0.990	−3.30
200	0.983	−13.40	3.261	166.1	0.0021	81.2	0.991	−6.62
300	0.974	−19.86	3.218	159.0	0.0030	77.5	0.991	−9.92
400	0.969	−26.46	3.205	152.6	0.0039	74.6	0.994	−13.30
500	0.958	−32.73	3.141	145.9	0.0045	72.4	0.994	−16.56
600	0.947	−38.83	3.086	139.5	0.0049	70.9	0.993	−19.77
700	0.936	−44.75	3.017	133.1	0.0051	69.5	0.991	−22.78
800	0.924	−50.51	2.949	126.9	0.0051	69.9	0.981	−25.77
900	0.910	−56.18	2.870	120.5	0.0049	69.8	0.984	−28.72
1000	0.896	−61.64	2.785	114.7	0.0045	72.7	0.980	−31.77

Table 2 Noise data: V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 12 mA; T_{amb} = 25 °C

f (MHz)	F_{min} (dB)	Γ_{opt}		R_n (Ω)
		(ratio)	(deg)	
400	0.9	0.695	13.87	28.5
800	1.1	0.634	30.30	32.85

PACKAGE OUTLINES

Plastic surface-mounted package; 4 leads **SOT143B**

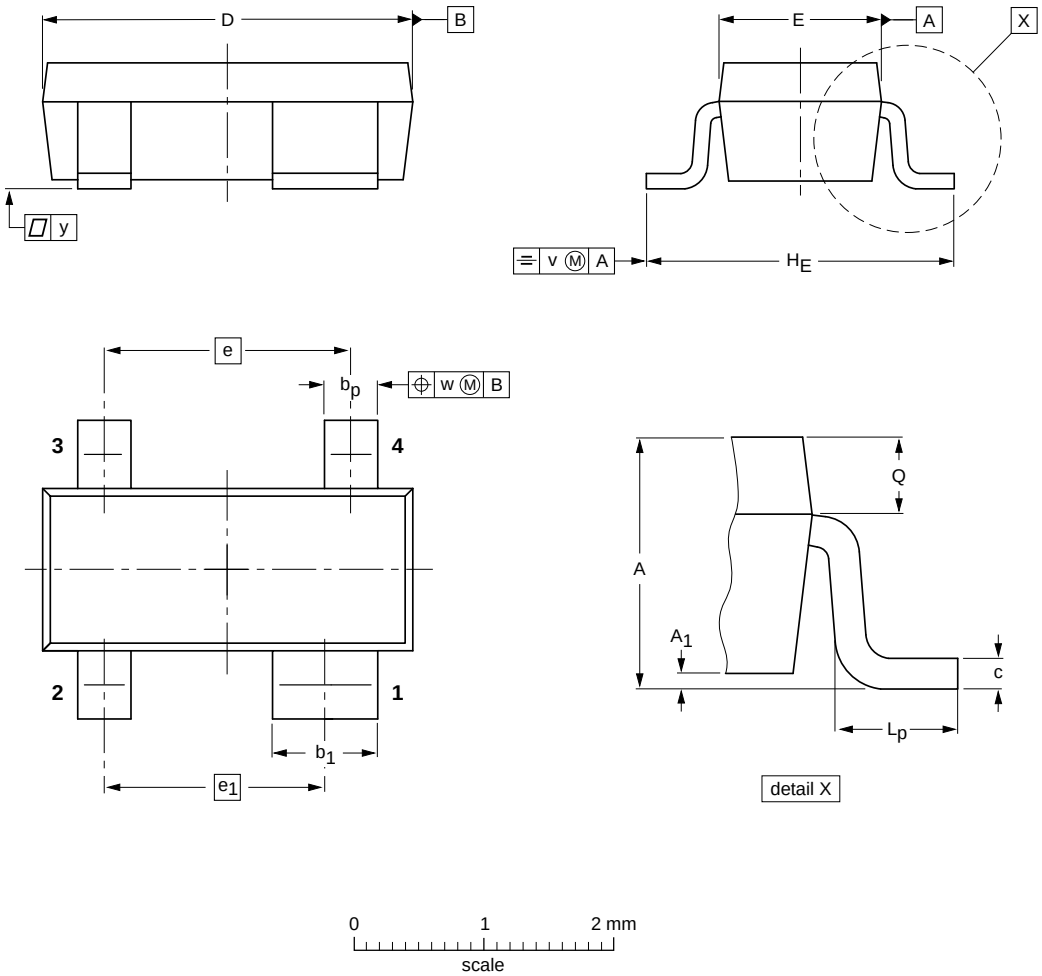


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143B						~~04-11-16~~ 06-03-16

Plastic surface-mounted package; reverse pinning; 4 leads **SOT143R**

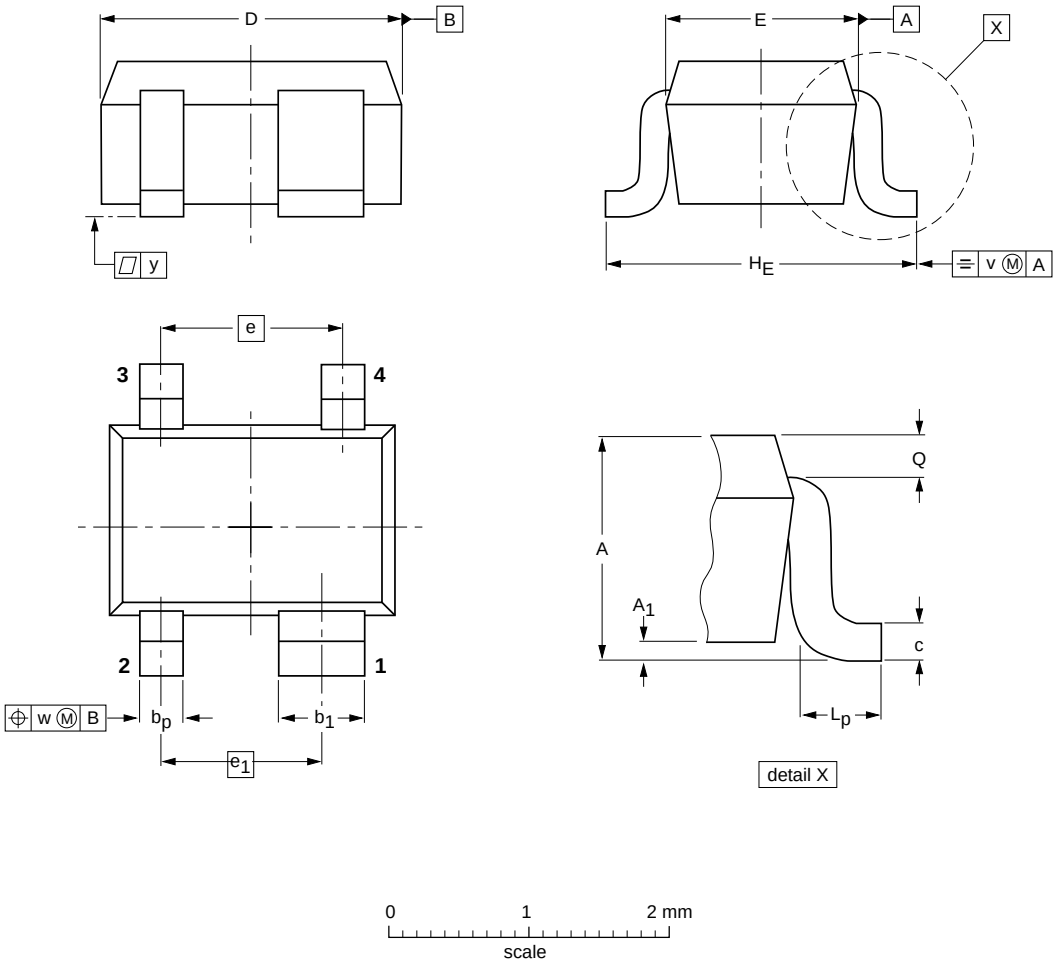


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143R			SC-61AA			~~04-11-16~~ 06-03-16

Plastic surface-mounted package; reverse pinning; 4 leads **SOT343R**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						~~97-05-21~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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