

DATA SHEET

BF1212; BF1212R; BF1212WR
N-channel dual-gate MOS-FETs

Product specification

2003 Nov 14



N-channel dual-gate MOS-FETs

BF1212; BF1212R; BF1212WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Excellent low frequency noise performance
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

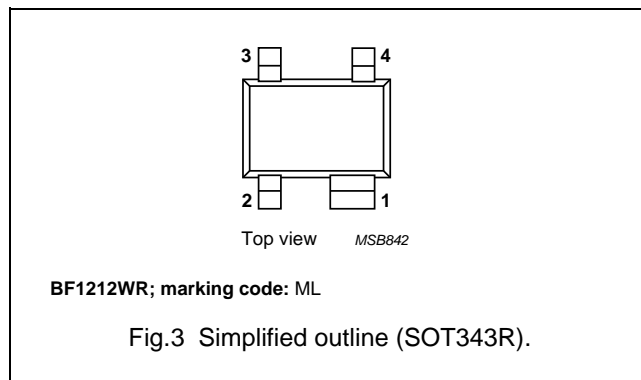
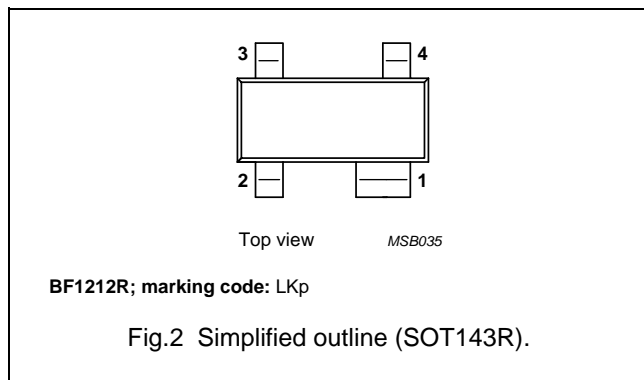
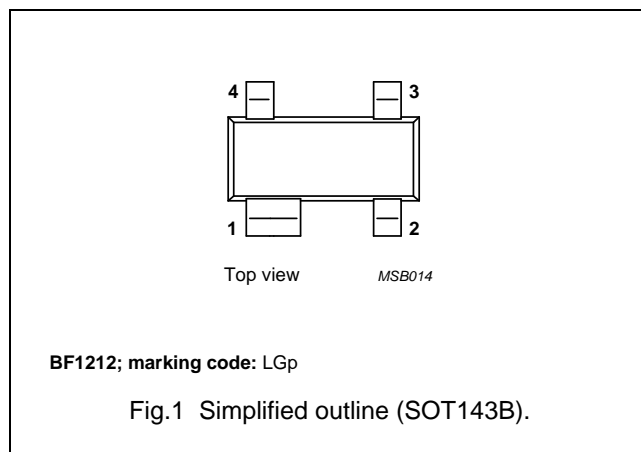
- Gain controlled low noise VHF and UHF amplifiers for 5 V digital and analog television tuner applications.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1212, BF1212R and BF1212WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | source |
| 2 | drain |
| 3 | gate 2 |
| 4 | gate 1 |



QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------|------------------------------|---|------|------|------|------------|
| V_{DS} | drain-source voltage | | – | – | 6 | V |
| I_D | drain current | | – | – | 30 | mA |
| P_{tot} | total power dissipation | | – | – | 180 | mW |
| $ y_{fs} $ | forward transfer admittance | | 28 | 33 | 43 | mS |
| C_{ig1-ss} | input capacitance at gate 1 | | – | 1.7 | 2.2 | pF |
| C_{rss} | reverse transfer capacitance | $f = 1 \text{ MHz}$ | – | 15 | 30 | fF |
| F | noise figure | $f = 800 \text{ MHz}$ | – | 1.1 | 1.8 | dB |
| X_{mod} | cross-modulation | input level for $k = 1 \%$ at 40 dB AGC | 100 | 104 | – | dB μ V |
| T_j | junction temperature | | – | – | 150 | °C |

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CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|---------|
| | NAME | DESCRIPTION | VERSION |
| BF1212 | – | plastic surface mounted package; 4 leads | SOT143B |
| BF1212R | – | plastic surface mounted package; reverse pinning; 4 leads | SOT143R |
| BF1212WR | – | plastic surface mounted package; reverse pinning; 4 leads | SOT343R |

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|-------------------------|-----------------------------------|------|----------|------|
| V_{DS} | drain-source voltage | | – | 6 | V |
| I_D | drain current (DC) | | – | 30 | mA |
| I_{G1} | gate 1 current | | – | ± 10 | mA |
| I_{G2} | gate 2 current | | – | ± 10 | mA |
| P_{tot} | total power dissipation | | | | |
| | BF1212; BF1212R | $T_s \leq 116\text{ °C}$; note 1 | – | 180 | mW |
| | BF1212WR | $T_s \leq 122\text{ °C}$; note 1 | – | 180 | mW |
| T_{stg} | storage temperature | | –65 | +150 | °C |
| T_j | junction temperature | | – | 150 | °C |

Note

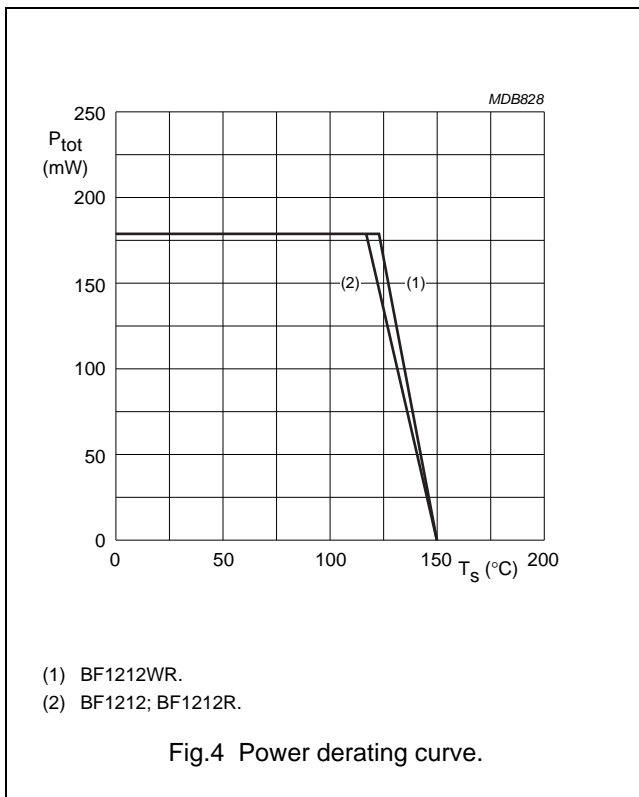
1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---------------|---|-------|------|
| $R_{th\ j-s}$ | thermal resistance from junction to soldering point | | |
| | BF1212; BF1212R | 185 | K/W |
| | BF1212WR | 155 | K/W |

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STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------------|---------------------------------|--|------|------|------|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{G1-S} = V_{G2-S} = 0\text{ V}$; $I_D = 10\text{ }\mu\text{A}$ | 6 | – | V |
| $V_{(BR)G1-SS}$ | gate 1-source breakdown voltage | $V_{G2-S} = V_{DS} = 0\text{ V}$; $I_{G1-S} = 10\text{ mA}$ | 6 | 10 | V |
| $V_{(BR)G2-SS}$ | gate 2-source breakdown voltage | $V_{G1-S} = V_{DS} = 0\text{ V}$; $I_{G2-S} = 10\text{ mA}$ | 6 | 10 | V |
| $V_{(F)S-G1}$ | forward source-gate 1 voltage | $V_{G2-S} = V_{DS} = 0\text{ V}$; $I_{S-G1} = 10\text{ mA}$ | 0.5 | 1.5 | V |
| $V_{(F)S-G2}$ | forward source-gate 2 voltage | $V_{G1-S} = V_{DS} = 0\text{ V}$; $I_{S-G2} = 10\text{ mA}$ | 0.5 | 1.5 | V |
| $V_{G1-S(th)}$ | gate 1-source threshold voltage | $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$ | 0.3 | 1.0 | V |
| $V_{G2-S(th)}$ | gate 2-source threshold voltage | $V_{G1-S} = 5\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$ | 0.35 | 1.0 | V |
| I_{DSX} | drain-source current | $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 150\text{ k}\Omega$; note 1 | 8 | 16 | mA |
| I_{G1-S} | gate 1 cut-off current | $V_{G2-S} = V_{DS} = 0\text{ V}$; $V_{G1-S} = 5\text{ V}$ | – | 50 | nA |
| I_{G2-S} | gate 2 cut-off current | $V_{G1-S} = V_{DS} = 0\text{ V}$; $V_{G2-S} = 4\text{ V}$ | – | 20 | nA |

Note

- R_{G1} connects G_1 to $V_{GG} = 5\text{ V}$.

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DYNAMIC CHARACTERISTICSCommon source; $T_{amb} = 25\text{ °C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 12\text{ mA}$; unless otherwise specified.

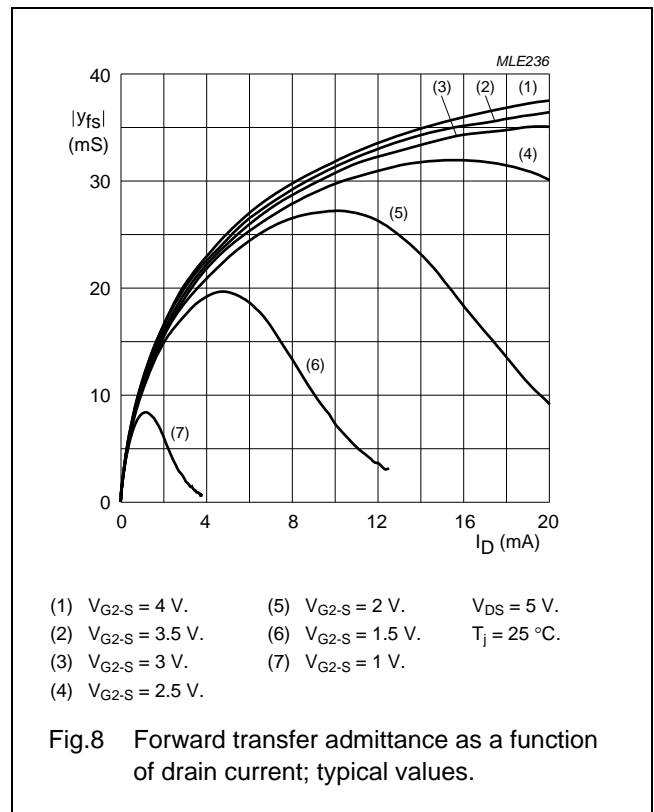
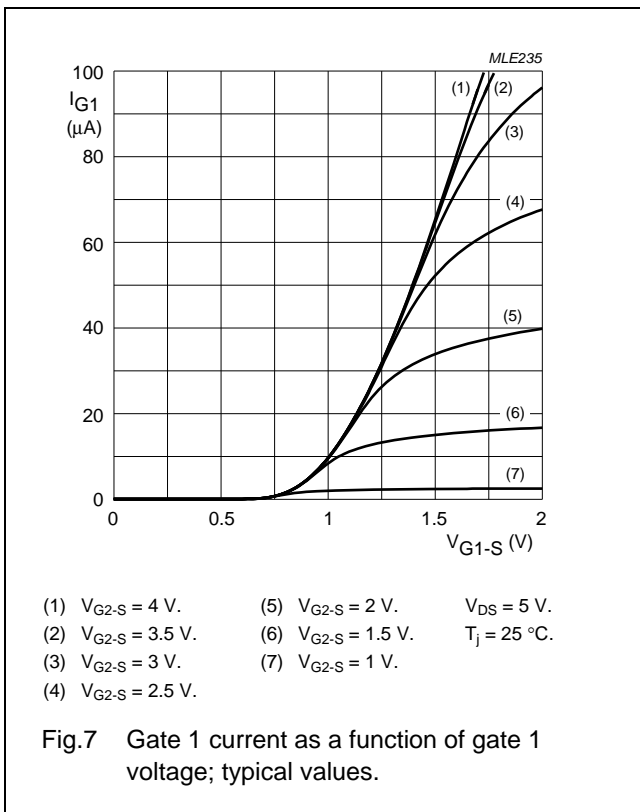
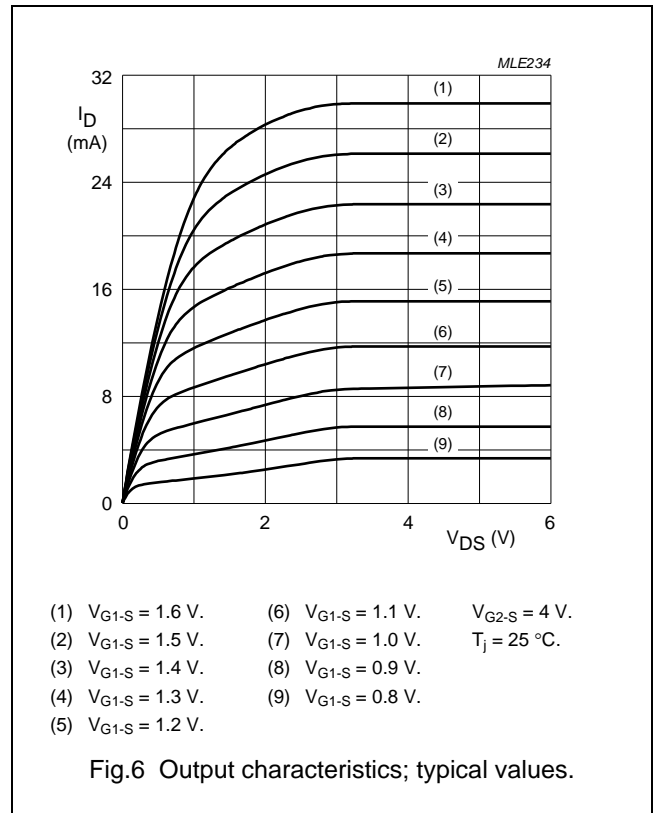
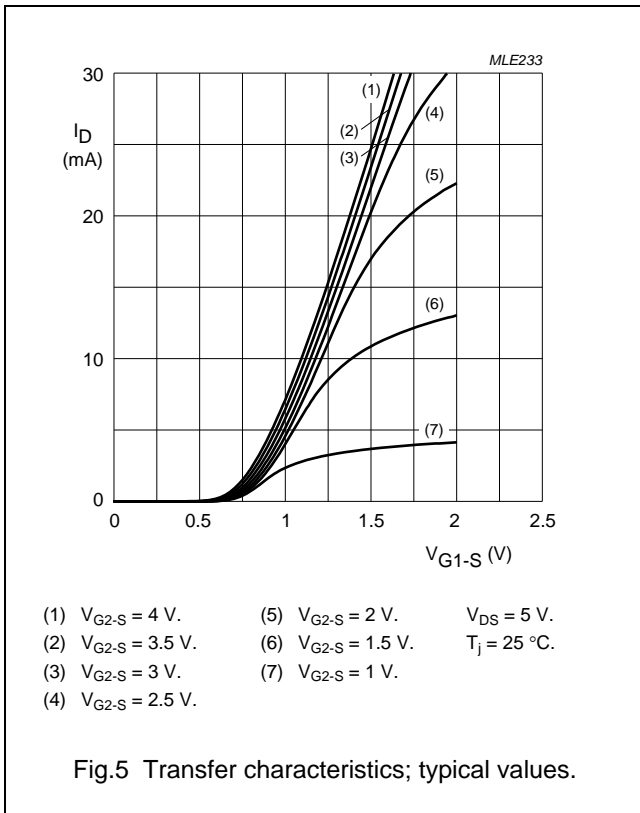
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------|------------------------------|---|------|------|------------|------------|
| $ y_{fs} $ | forward transfer admittance | pulsed; $T_j = 25\text{ °C}$ | 28 | 33 | 43 | mS |
| C_{ig1-ss} | input capacitance at gate 1 | $f = 1\text{ MHz}$ | – | 1.7 | 2.2 | pF |
| C_{ig2-ss} | input capacitance at gate 2 | $f = 1\text{ MHz}$ | – | 1.1 | – | pF |
| C_{oss} | output capacitance | $f = 1\text{ MHz}$ | – | 0.9 | – | pF |
| C_{rss} | reverse transfer capacitance | $f = 1\text{ MHz}$ | – | 15 | 30 | fF |
| F | noise figure | $f = 11\text{ MHz}$; $G_S = 20\text{ mS}$; $B_S = 0$ | – | 4 | – | dB |
| | | $f = 400\text{ MHz}$; $Y_S = Y_{S(opt)}$ | – | 0.9 | 1.6 | dB |
| | | $f = 800\text{ MHz}$; $Y_S = Y_{S(opt)}$ | – | 1.1 | 1.8 | dB |
| G_{tr} | power gain | $f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 0.5\text{ mS}$; $B_L = B_{L(opt)}$ | – | 35 | – | dB |
| | | $f = 400\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 1\text{ mS}$; $B_L = B_{L(opt)}$ | – | 30 | – | dB |
| | | $f = 800\text{ MHz}$; $G_S = 3.3\text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 1\text{ mS}$; $B_L = B_{L(opt)}$ | – | 25 | – | dB |
| X_{mod} | cross-modulation | input level for $k = 1\%$; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 1 | | | | |
| | | at 0 dB AGC | 90 | – | – | dB μ V |
| | | at 10 dB AGC | – | 89 | – | dB μ V |
| | at 40 dB AGC | 100 | 104 | – | dB μ V | |

Note

1. Measured in test circuit Fig.21.

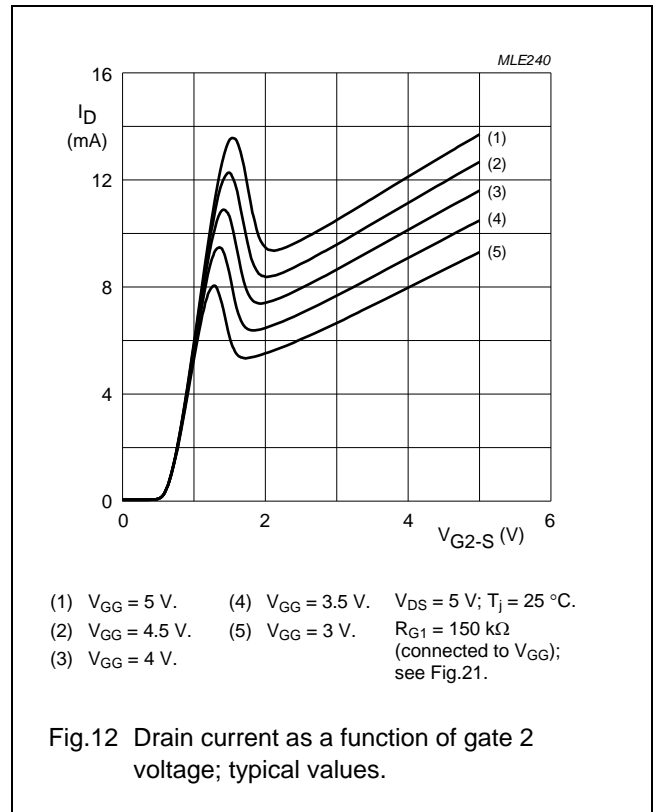
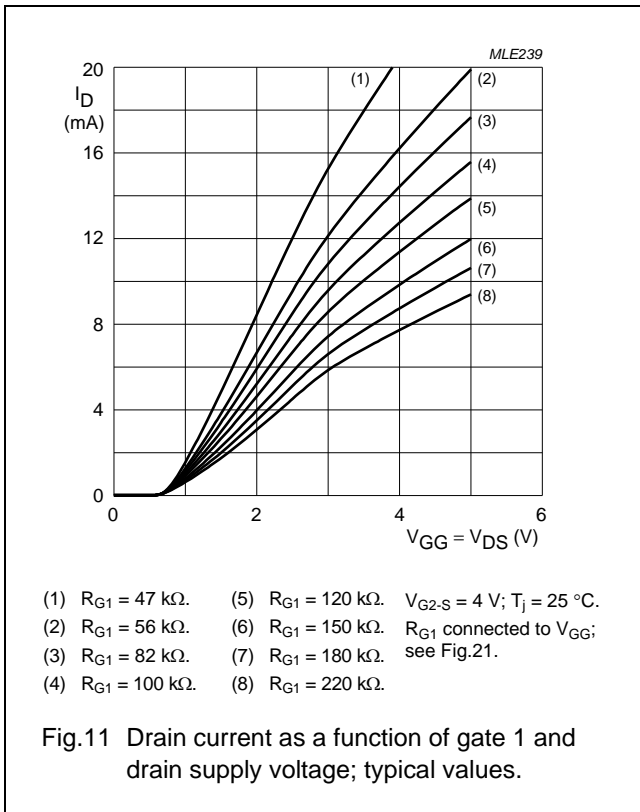
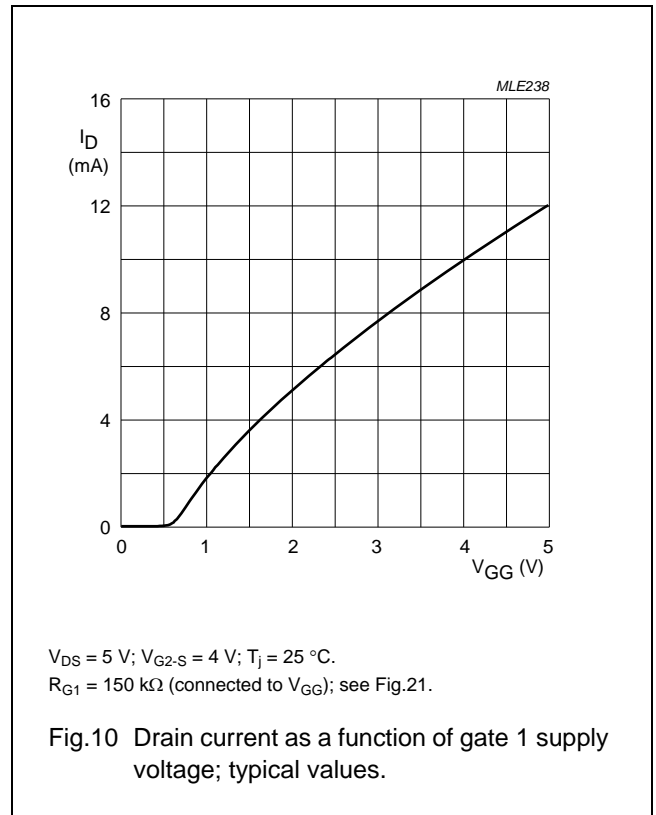
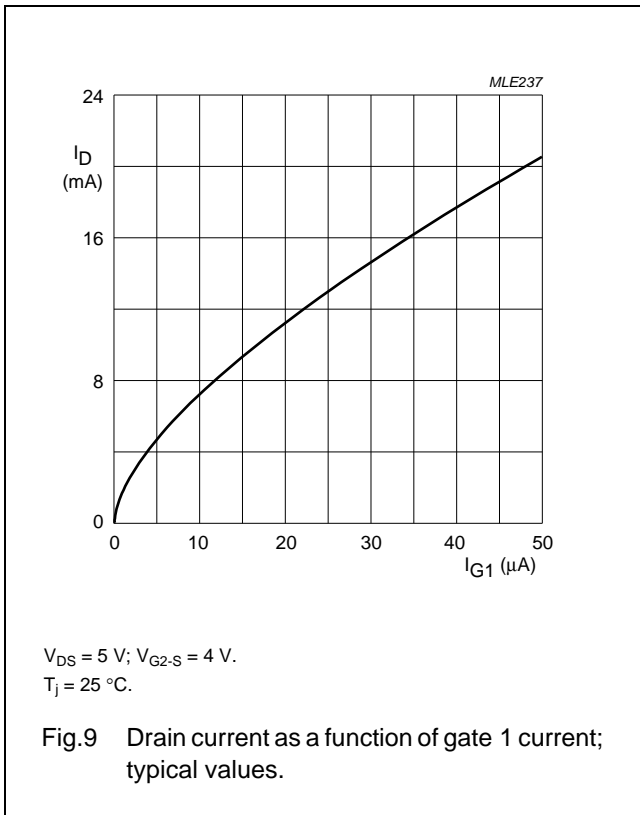
N-channel dual-gate MOS-FETs

BF1212; BF1212R; BF1212WR



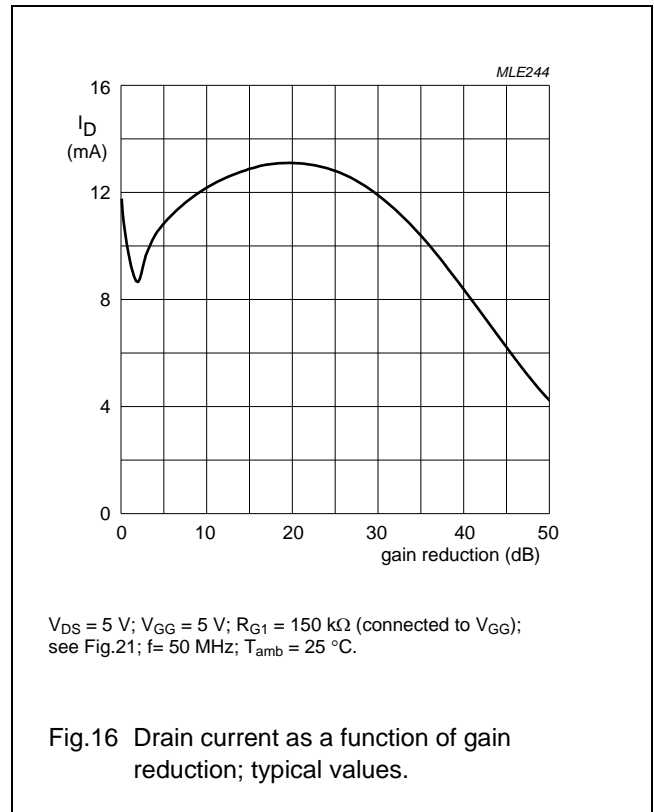
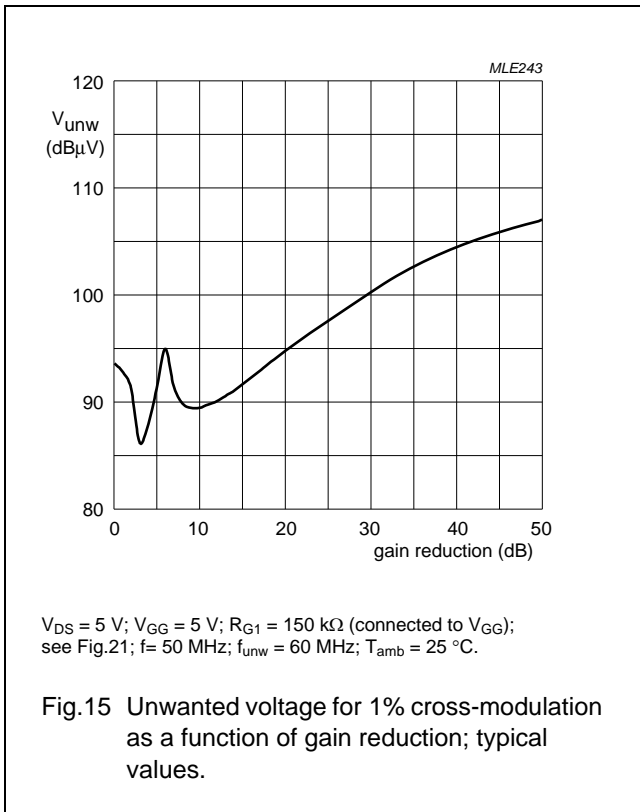
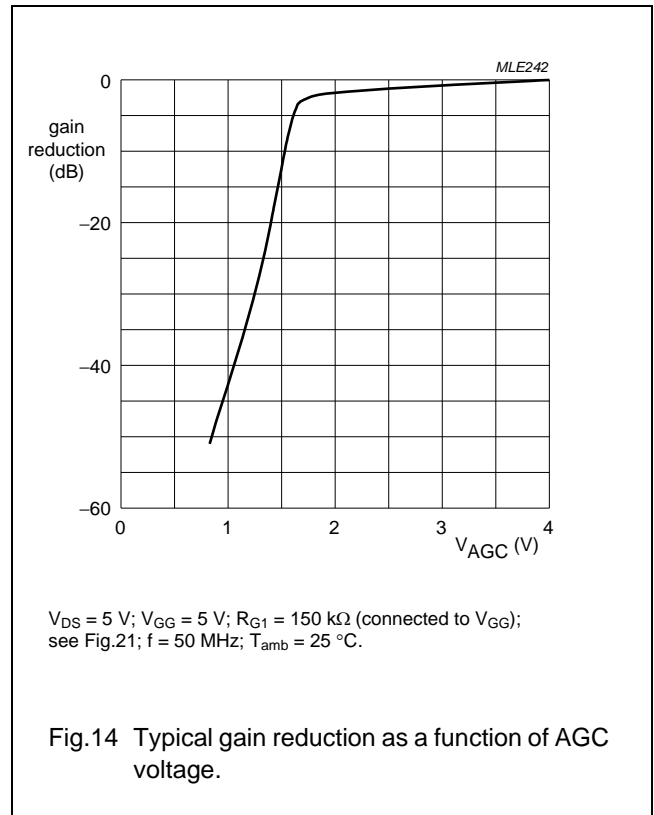
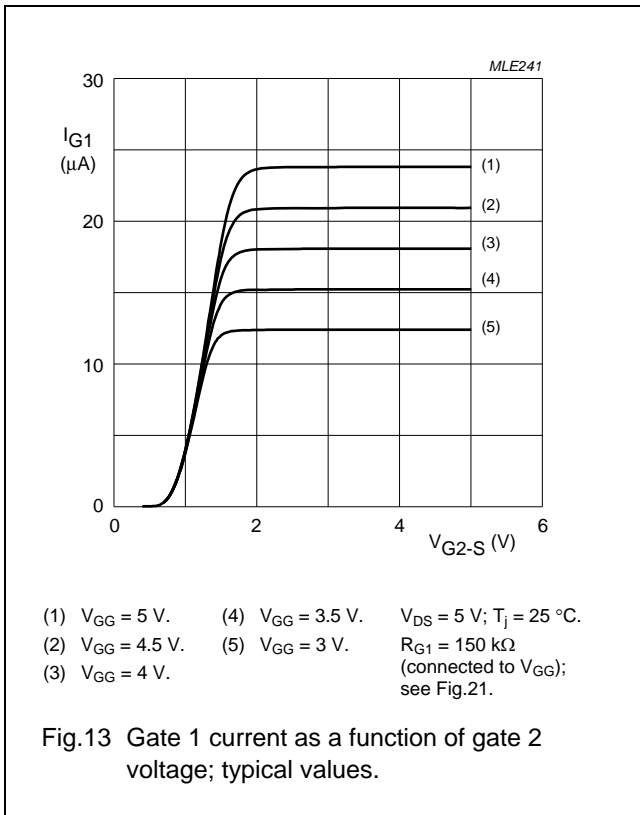
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BF1212; BF1212R; BF1212WR



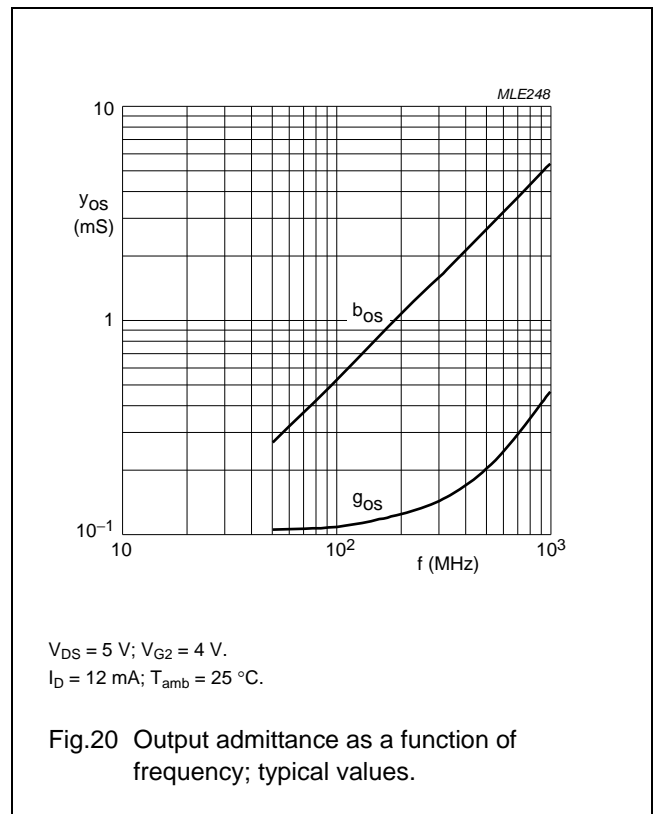
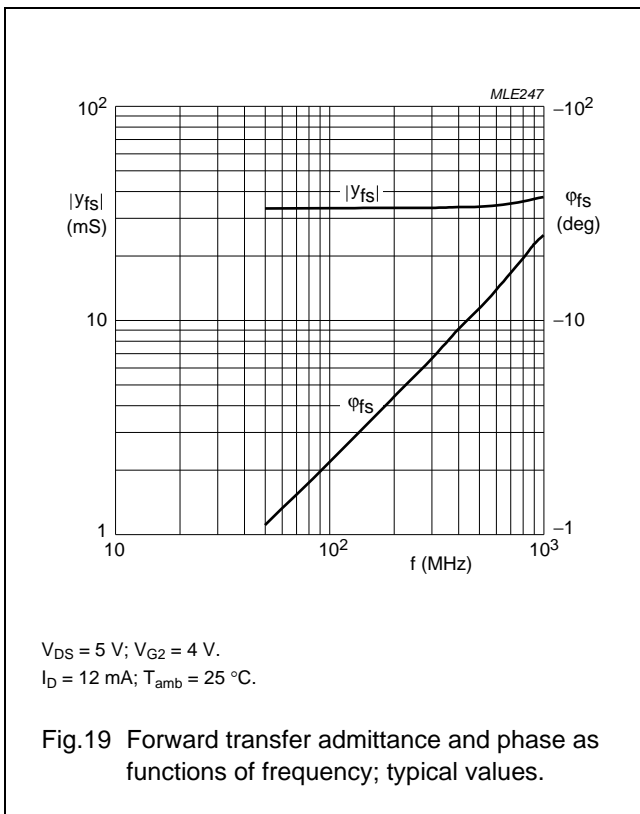
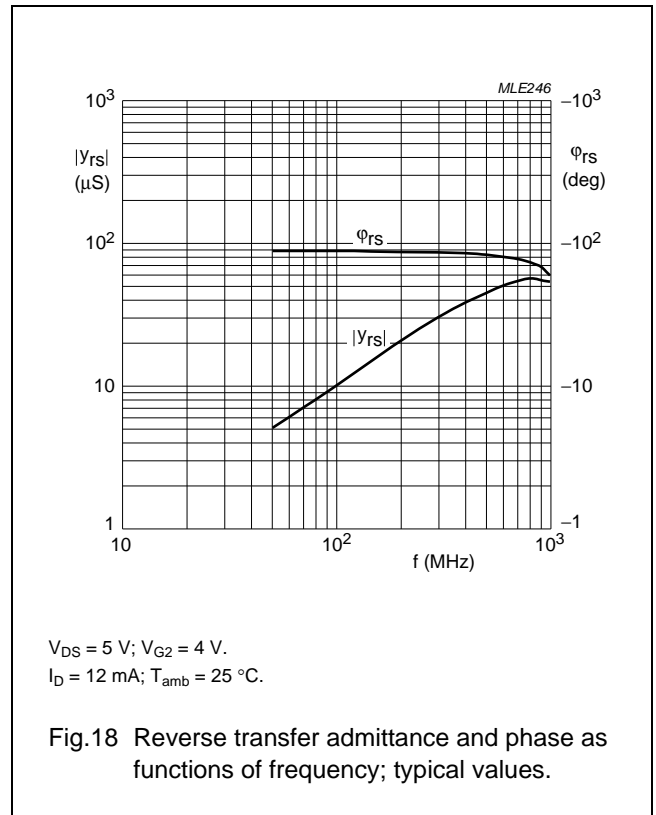
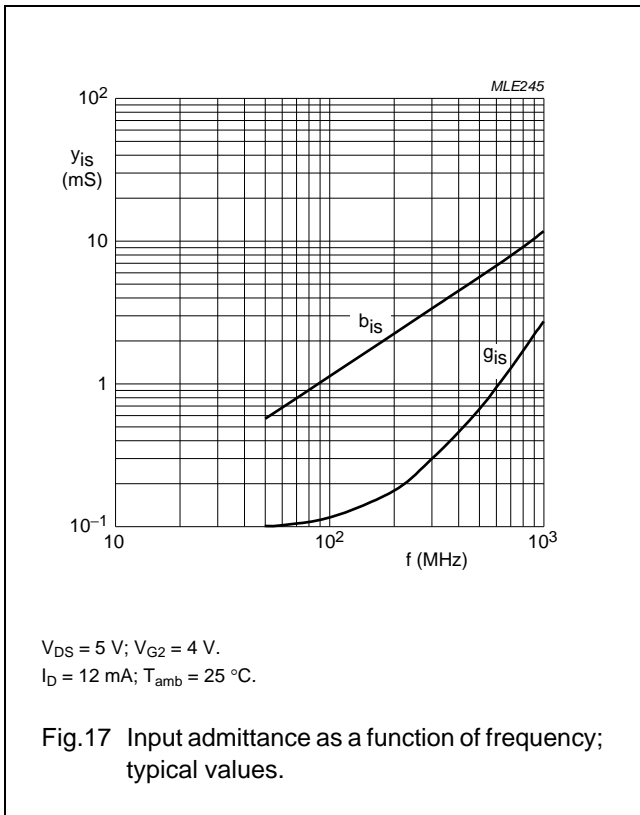
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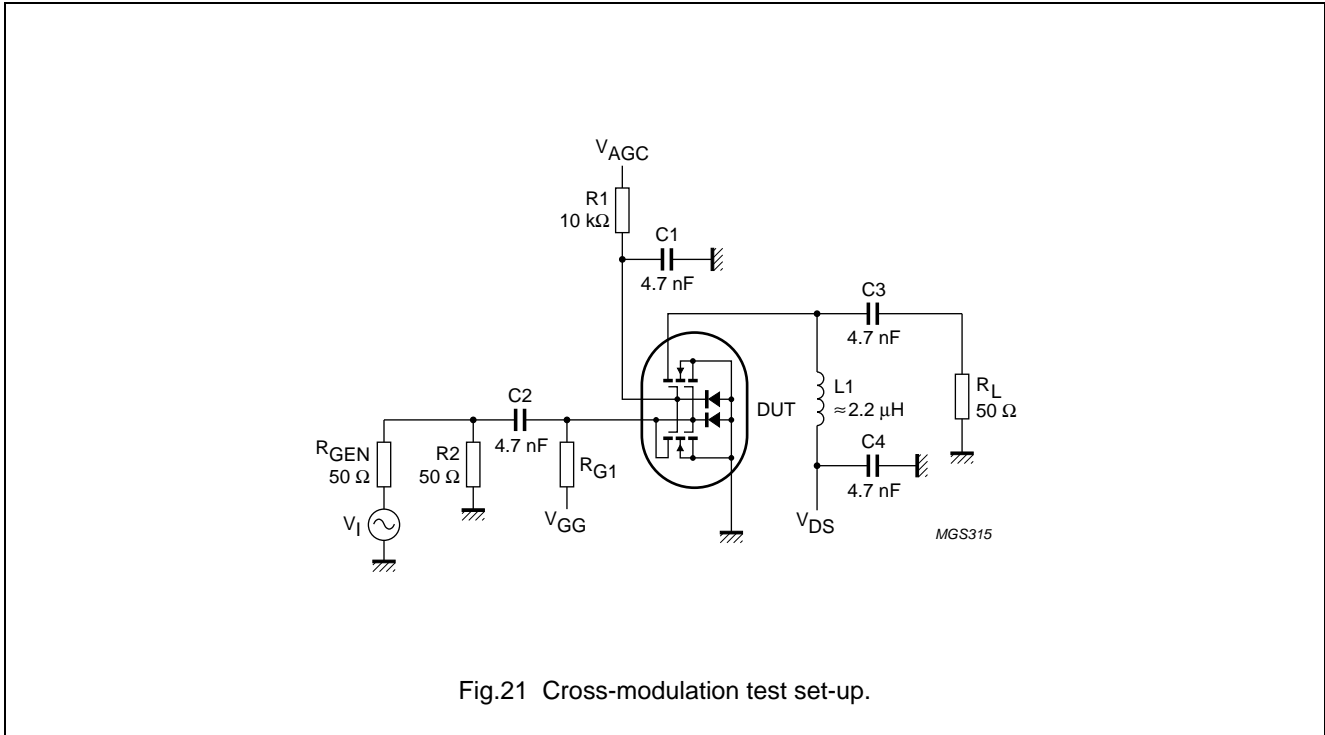


Fig.21 Cross-modulation test set-up.

Table 1 Scattering parameters: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^\circ\text{C}$

| f (MHz) | S ₁₁ | | S ₂₁ | | S ₁₂ | | S ₂₂ | |
|------------|----------------------|----------------|----------------------|----------------|----------------------|----------------|----------------------|----------------|
| | MAGNITUDE (ratio) | ANGLE (deg) | MAGNITUDE (ratio) | ANGLE (deg) | MAGNITUDE (ratio) | ANGLE (deg) | MAGNITUDE (ratio) | ANGLE (deg) |
| 50 | 0.990 | -3.39 | 3.288 | 176.5 | 0.0005 | 86.9 | 0.990 | -1.66 |
| 100 | 0.988 | -6.76 | 3.280 | 173.0 | 0.0011 | 85.6 | 0.990 | -3.30 |
| 200 | 0.983 | -13.40 | 3.261 | 166.1 | 0.0021 | 81.2 | 0.991 | -6.62 |
| 300 | 0.974 | -19.86 | 3.218 | 159.0 | 0.0030 | 77.5 | 0.991 | -9.92 |
| 400 | 0.969 | -26.46 | 3.205 | 152.6 | 0.0039 | 74.6 | 0.994 | -13.30 |
| 500 | 0.958 | -32.73 | 3.141 | 145.9 | 0.0045 | 72.4 | 0.994 | -16.56 |
| 600 | 0.947 | -38.83 | 3.086 | 139.5 | 0.0049 | 70.9 | 0.993 | -19.77 |
| 700 | 0.936 | -44.75 | 3.017 | 133.1 | 0.0051 | 69.5 | 0.991 | -22.78 |
| 800 | 0.924 | -50.51 | 2.949 | 126.9 | 0.0051 | 69.9 | 0.981 | -25.77 |
| 900 | 0.910 | -56.18 | 2.870 | 120.5 | 0.0049 | 69.8 | 0.984 | -28.72 |
| 1000 | 0.896 | -61.64 | 2.785 | 114.7 | 0.0045 | 72.7 | 0.980 | -31.77 |

Table 2 Noise data: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^\circ\text{C}$

| f (MHz) | F _{min} (dB) | Γ _{opt} | | R _n (Ω) |
|------------|--------------------------|------------------|-------|-----------------------|
| | | (ratio) | (deg) | |
| 400 | 0.9 | 0.695 | 13.87 | 28.5 |
| 800 | 1.1 | 0.634 | 30.30 | 32.85 |

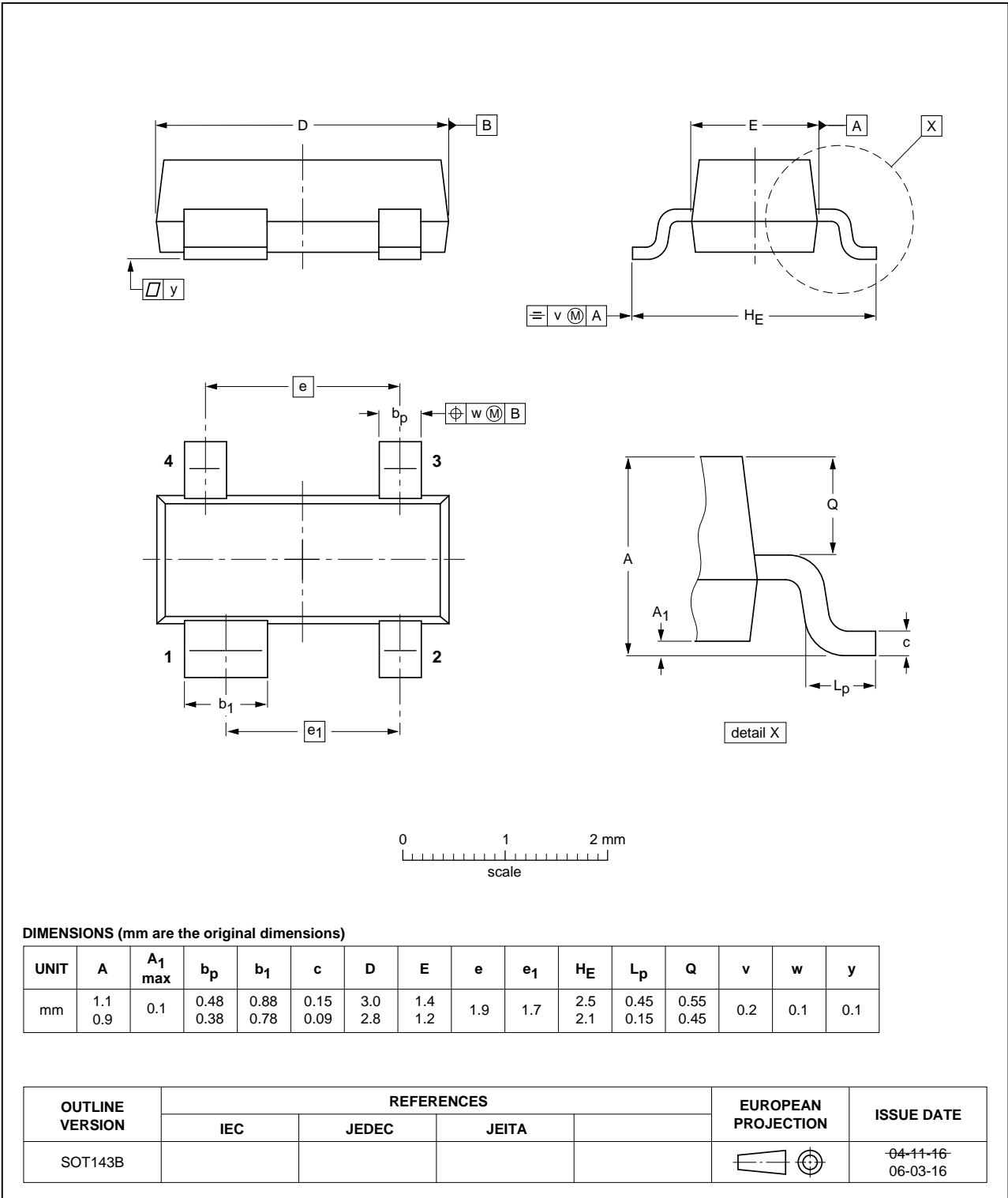
N-channel dual-gate MOS-FETs

BF1212; BF1212R; BF1212WR

PACKAGE OUTLINES

Plastic surface-mounted package; 4 leads

SOT143B

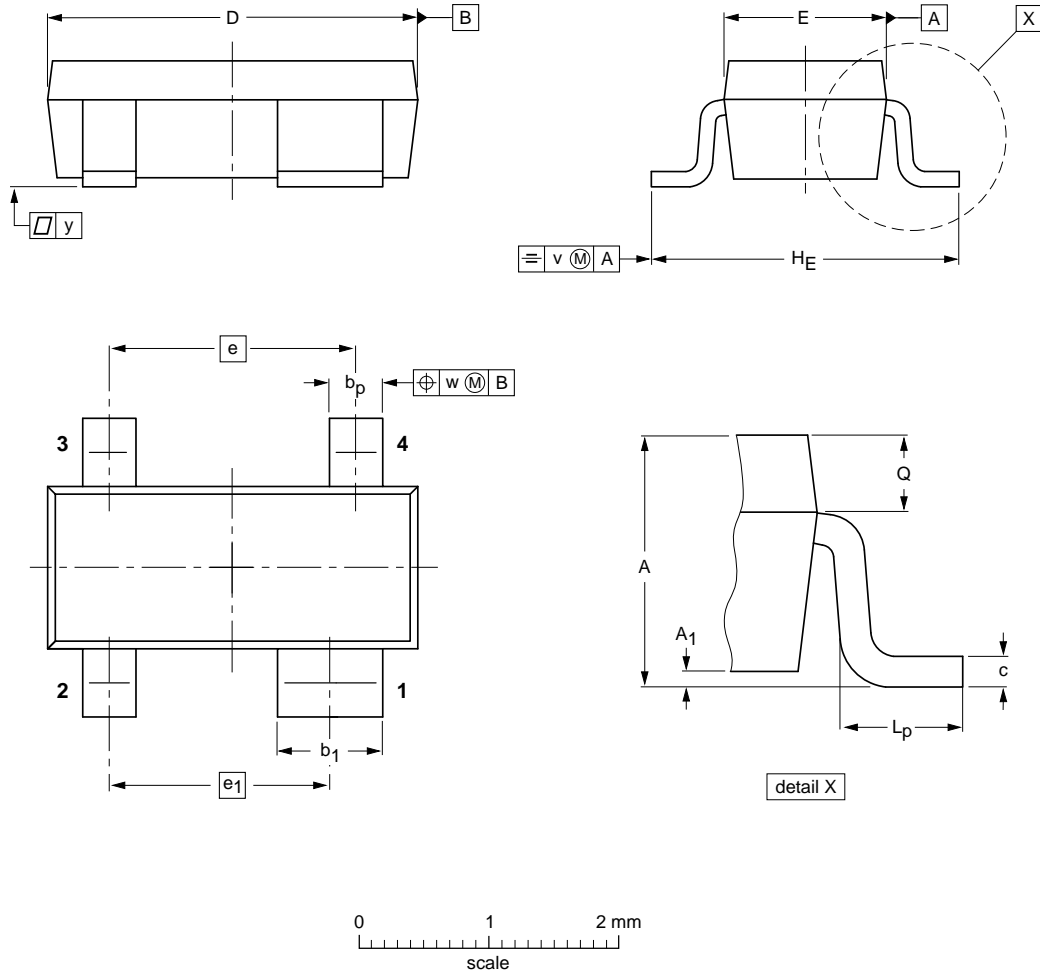


N-channel dual-gate MOS-FETs

BF1212; BF1212R; BF1212WR

Plastic surface-mounted package; reverse pinning; 4 leads

SOT143R



DIMENSIONS (mm are the original dimensions)

| UNIT | A | A ₁ max | b _p | b ₁ | c | D | E | e | e ₁ | H _E | L _p | Q | v | w | y |
|------|------------|-----------------------|----------------|----------------|--------------|------------|------------|-----|----------------|----------------|----------------|--------------|-----|-----|-----|
| mm | 1.1 0.9 | 0.1 | 0.48 0.38 | 0.88 0.78 | 0.15 0.09 | 3.0 2.8 | 1.4 1.2 | 1.9 | 1.7 | 2.5 2.1 | 0.55 0.25 | 0.45 0.25 | 0.2 | 0.1 | 0.1 |

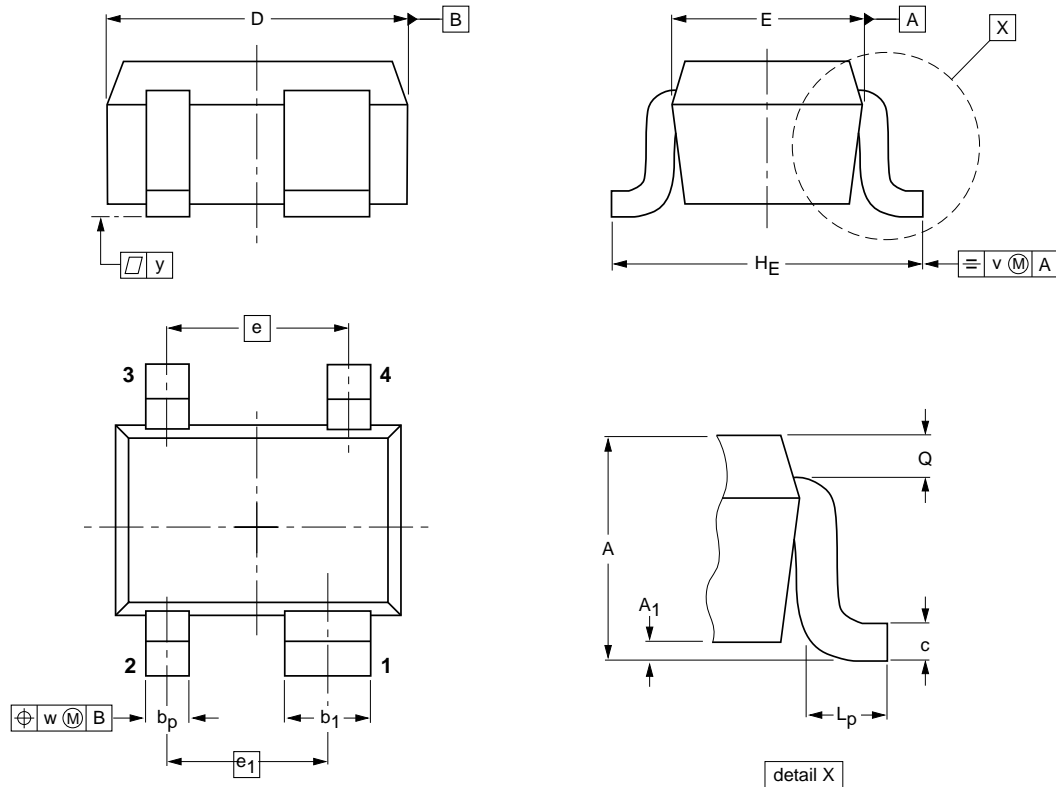
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|-----------------|------------|-------|---------|--|---------------------|----------------------|
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| SOT143R | | | SC-61AA | | | 04-11-16 06-03-16 |

N-channel dual-gate MOS-FETs

BF1212; BF1212R; BF1212WR

Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

| UNIT | A | A ₁ max | b _p | b ₁ | c | D | E | e | e ₁ | H _E | L _p | Q | v | w | y |
|------|------------|-----------------------|----------------|----------------|--------------|------------|--------------|-----|----------------|----------------|----------------|--------------|-----|-----|-----|
| mm | 1.1 0.8 | 0.1 | 0.4 0.3 | 0.7 0.5 | 0.25 0.10 | 2.2 1.8 | 1.35 1.15 | 1.3 | 1.15 | 2.2 2.0 | 0.45 0.15 | 0.23 0.13 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|------|--|------------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT343R | | | | | | 97-05-21 06-03-16 |

N-channel dual-gate MOS-FETs

BF1212; BF1212R; BF1212WR

DATA SHEET STATUS

| DOCUMENT STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾ | DEFINITION |
|--------------------------------|-------------------------------|---|
| Objective data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary data sheet | Qualification | This document contains data from the preliminary specification. |
| Product data sheet | Production | This document contains the product specification. |

Notes

1. Please consult the most recently issued document before initiating or completing a design.
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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: <http://www.nxp.com>

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