

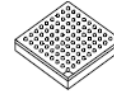


**THE DATASHEET OF
P2040NSN7KLC**



P2040

P2040 QorIQ Integrated Processor Hardware Specifications



FCPBGA-780
23 mm x 23 mm

The P2040 QorIQ integrated communication processor combines four Power Architecture® processor cores with high performance data path acceleration logic and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, base station controllers, and general-purpose embedded computing. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also greatly simplifying board design.

This chip includes the following functions and features:

- Four e500mc Power Architecture cores
 - Three levels of instructions: User, supervisor, and hypervisor
 - Independent boot and reset
 - Secure boot capability
 - CoreNet fabric supporting coherent and non-coherent transactions amongst CoreNet endpoints
 - One 1 MB CoreNet platform cache with ECC
 - CoreNet bridges between the CoreNet fabric the I/Os, data path accelerators, and high and low speed peripheral interfaces
 - Five 1-Gigabit Ethernet controllers
 - 2.5 Gbps SGMII interfaces
 - RGMII interfaces
 - One 64-bit DDR3 and DDR3L SDRAM memory controller with ECC
 - Multicore programmable interrupt controller
 - Four I²C controllers
 - Four 2-pin UARTs or two 4-pin UARTs
 - Two 4-channel DMA engines
 - Enhanced local bus controller (eLBC)
 - Three PCI Express 2.0 controllers/ports
- Two serial RapidIO® controllers/ports (sRIO port) supporting version 1.3 with features 2.1
 - Two serial ATA (SATA 2.0) controllers
 - Enhanced secure digital host controller (SD/MMC)
 - Enhanced serial peripheral interface (eSPI)
 - 2× high-speed USB 2.0 controllers with integrated PHYs

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This figure shows the major functional units within the chip.

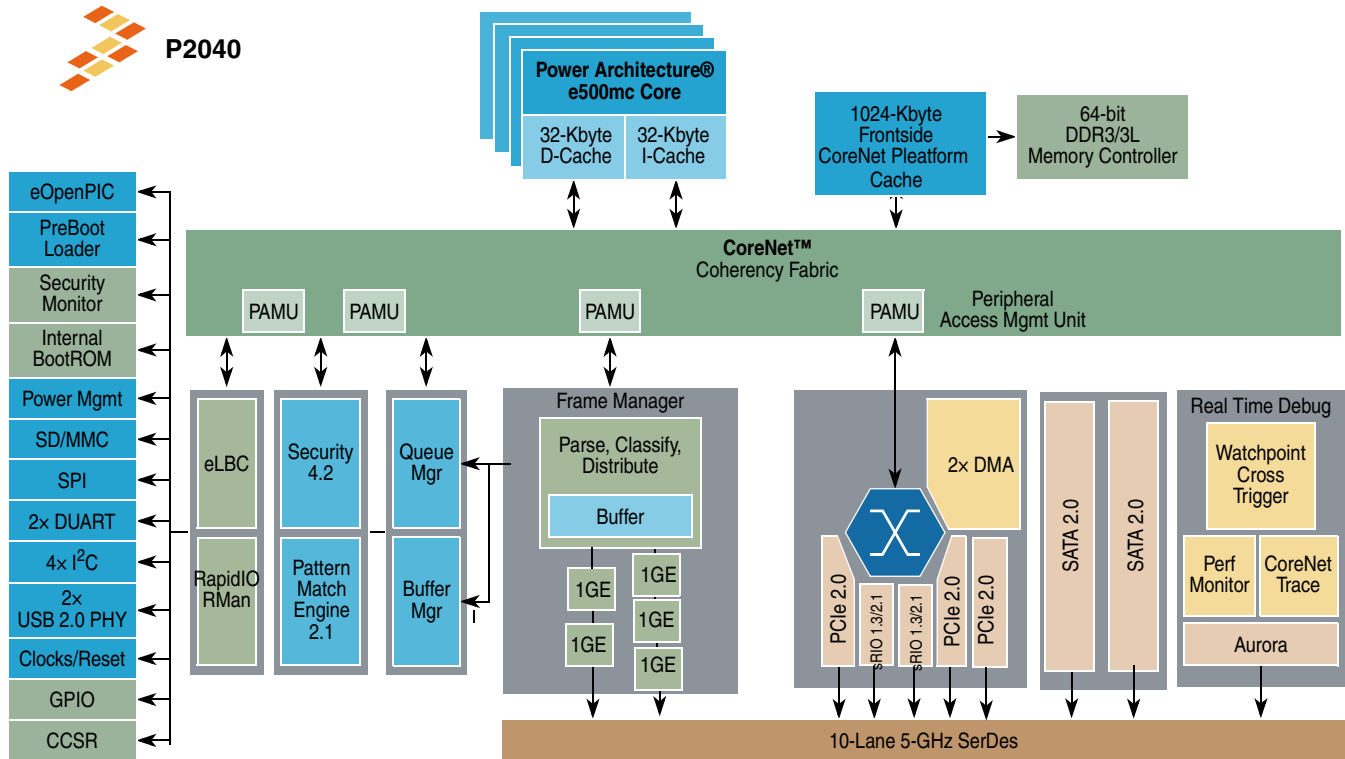


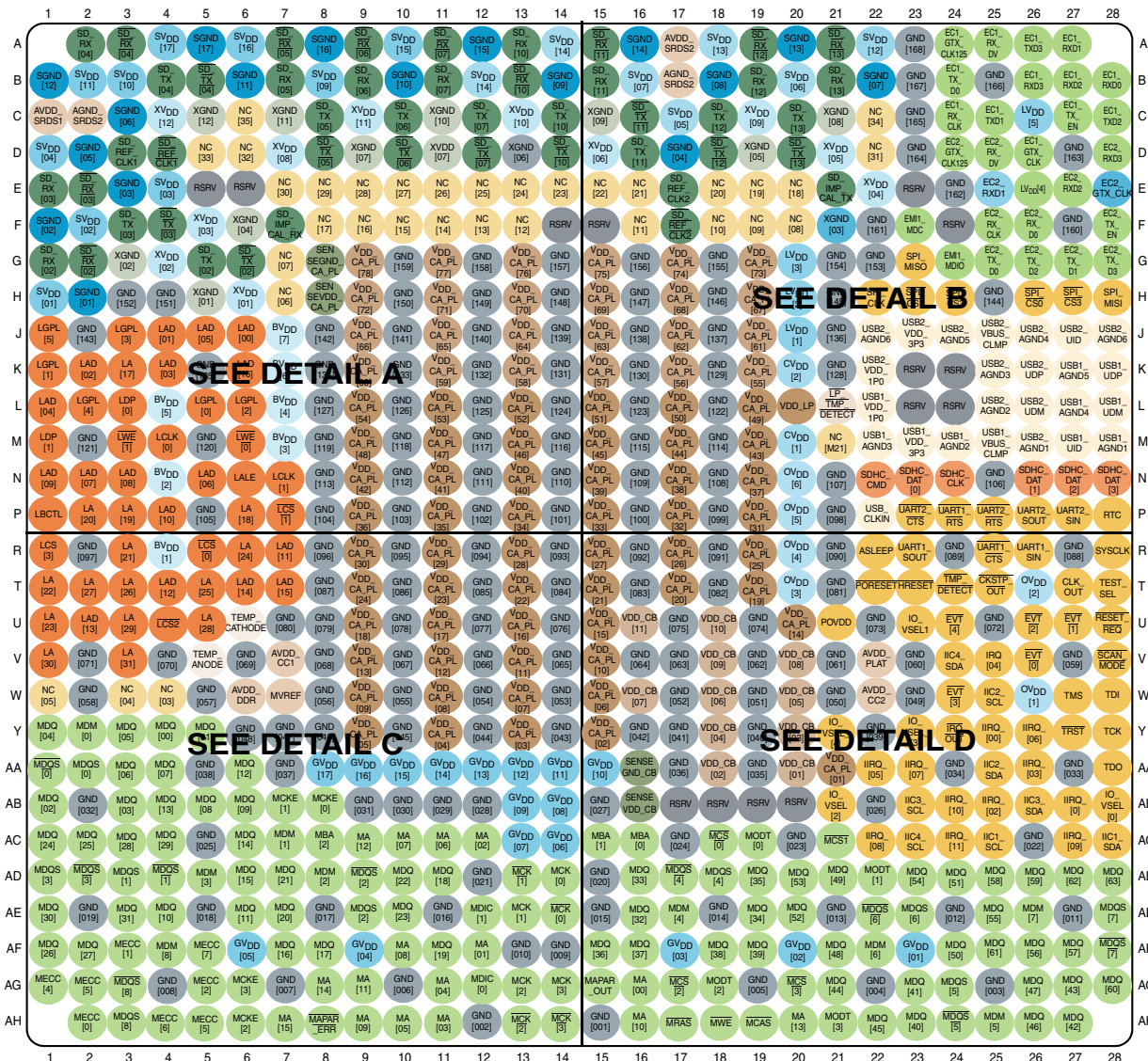
Figure 1. Block Diagram

1 Pin Assignments and Reset States

This section provides a top view of the ball layout diagram and four detailed views by quadrant. It also provides a pinout listing by bus.

1.1 780 FC-PBGA Ball Layout Diagrams

These figures show the FC-PBGA ball map diagrams.



- Signal Groups**
- **V_{DD}** I/O Supply Voltage
 - **LV_{DD}** I/O Supply Voltage
 - **GV_{DD}** DDR DRAM I/O Supply
 - **CV_{DD}** SPI Voltage Supply
 - **BV_{DD}** Local Bus I/O Supply
 - **SV_{DD}** SerDes Core Power Supply
 - **XV_{DD}** SerDes Transcvr Pad Supply
 - **VDD_PL** Platform Supply Voltage
 - **VDD_CA** Core Group A Supply Voltage
 - **VDD_CB** Core Group B Supply Voltage
 - **AVDD_SRD_{S1}** SerDes 1 PLL Supply Voltage
 - **AVDD_SRD_{S2}** SerDes 2 PLL Supply Voltage
 - **AVDD_PLAT** Platform PLL Supply Voltage
 - **AVDD_CC** Core PLL Supply Voltage
 - **SENSE_VDD_CA** Core A, B and Platform Voltage Sense
 - **SENSE_VDD_CB** Core Group B Voltage Sense
 - **RSRV** Reserved
 - **POVDD** Fuse Programming Override Supply

Figure 2. 780 BGA Ball Map Diagram (Top View)

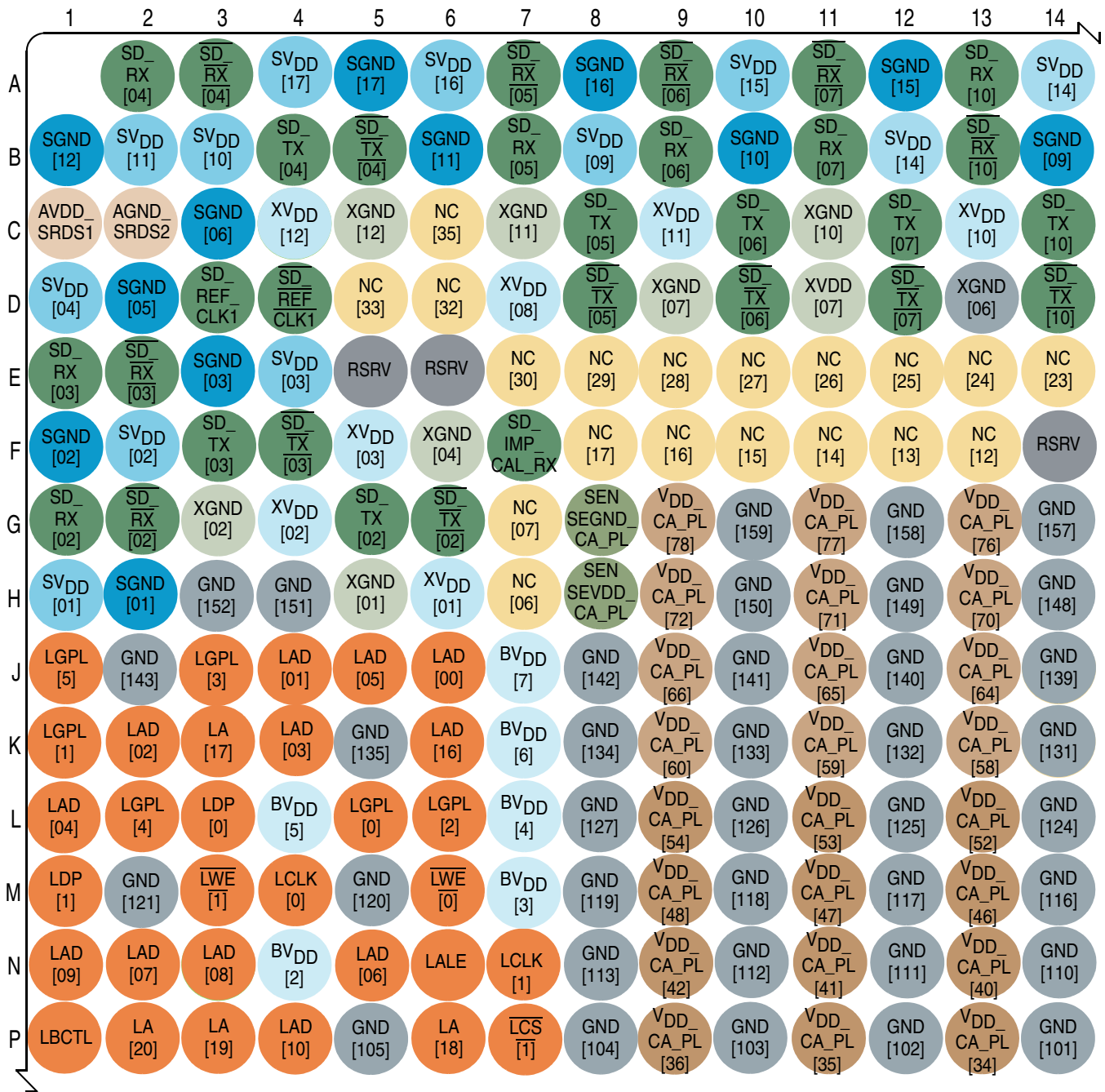


Figure 3. 780 BGA Ball Map Diagram (Detail View A)

Pin Assignments and Reset States

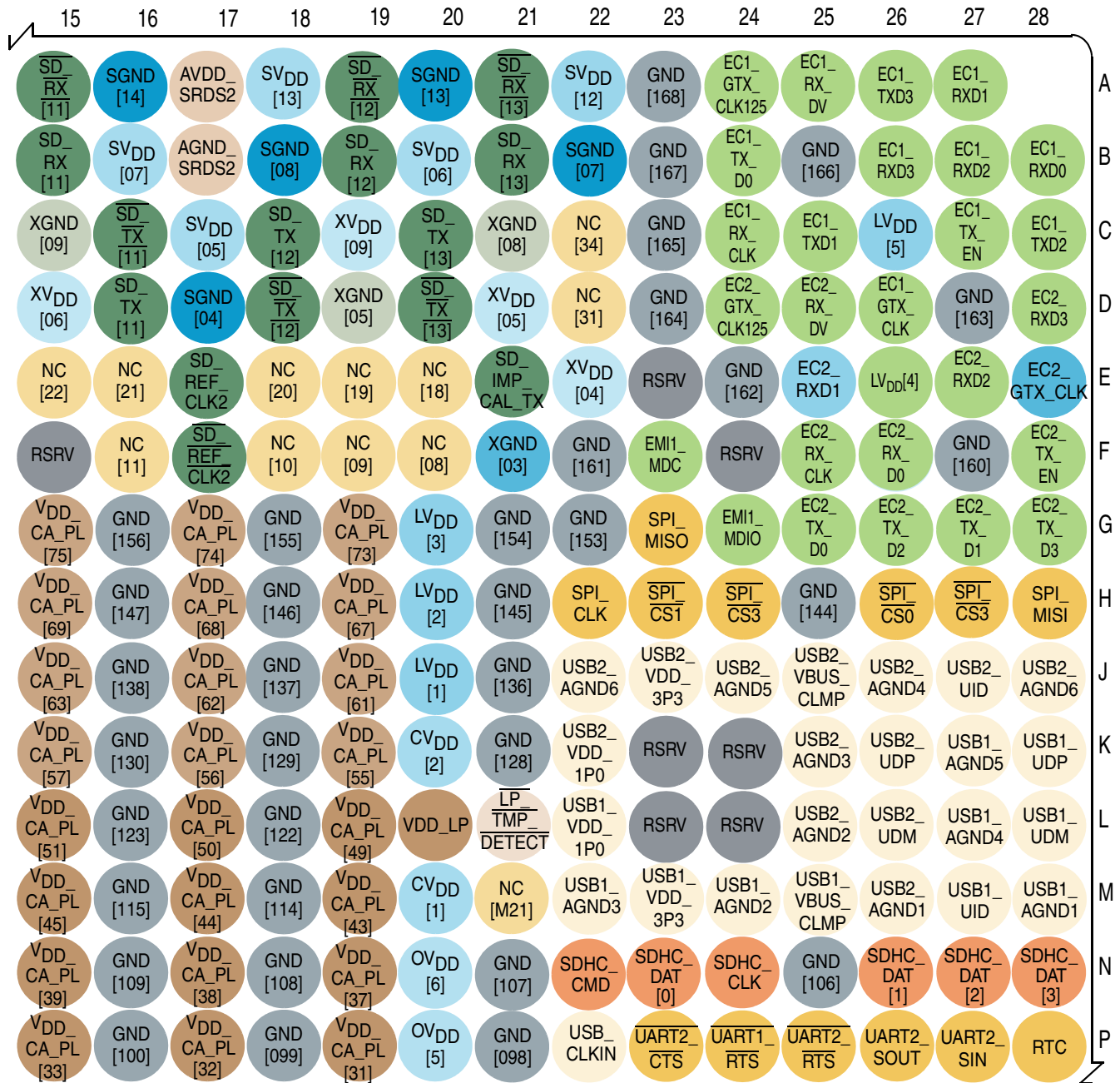


Figure 4. 780 BGA Ball Map Diagram (Detail View B)

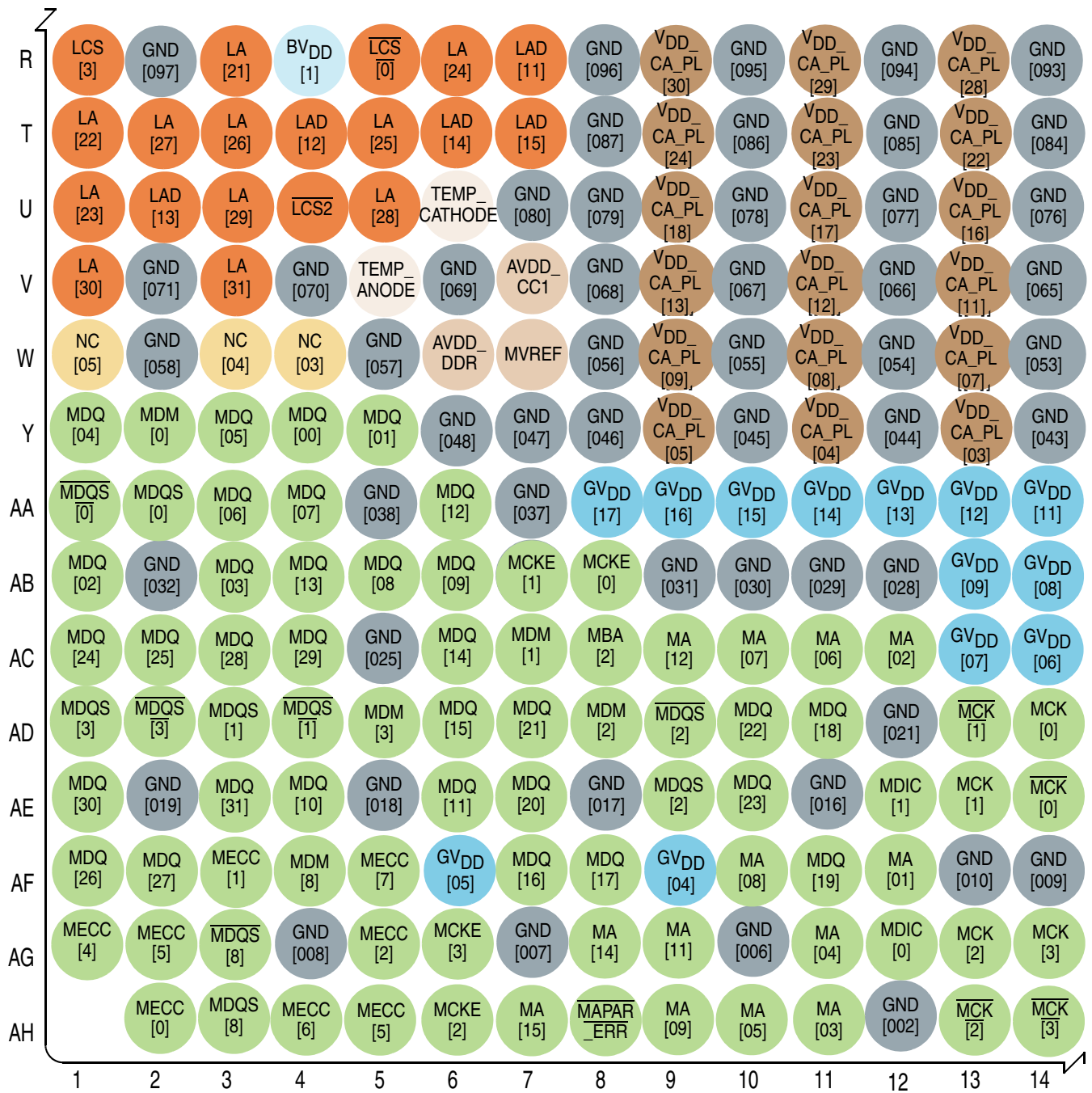


Figure 5. 780 BGA Ball Map Diagram (Detail View C)

1.2 Pinout List

This table provides the pinout listing for the 780 FC-PBGA package by bus. Pins for multiplexed signals appear in the bus group for their default status and have a corresponding note stating that they have multiple functionality depending on the mode in which they are configured.

Table 1. Pin List by Bus

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|-----------------------------------|--------------------|--------------------|----------|------------------|------|
| DDR SDRAM Memory Interface | | | | | |
| MDQ00 | Data | Y4 | I/O | GV _{DD} | — |
| MDQ01 | Data | Y5 | I/O | GV _{DD} | — |
| MDQ02 | Data | AB1 | I/O | GV _{DD} | — |
| MDQ03 | Data | AB3 | I/O | GV _{DD} | — |
| MDQ04 | Data | Y1 | I/O | GV _{DD} | — |
| MDQ05 | Data | Y3 | I/O | GV _{DD} | — |
| MDQ06 | Data | AA3 | I/O | GV _{DD} | — |
| MDQ07 | Data | AA4 | I/O | GV _{DD} | — |
| MDQ08 | Data | AB5 | I/O | GV _{DD} | — |
| MDQ09 | Data | AB6 | I/O | GV _{DD} | — |
| MDQ10 | Data | AE4 | I/O | GV _{DD} | — |
| MDQ11 | Data | AE6 | I/O | GV _{DD} | — |
| MDQ12 | Data | AA6 | I/O | GV _{DD} | — |
| MDQ13 | Data | AB4 | I/O | GV _{DD} | — |
| MDQ14 | Data | AC6 | I/O | GV _{DD} | — |
| MDQ15 | Data | AD6 | I/O | GV _{DD} | — |
| MDQ16 | Data | AF7 | I/O | GV _{DD} | — |
| MDQ17 | Data | AF8 | I/O | GV _{DD} | — |
| MDQ18 | Data | AD11 | I/O | GV _{DD} | — |
| MDQ19 | Data | AF11 | I/O | GV _{DD} | — |
| MDQ20 | Data | AE7 | I/O | GV _{DD} | — |
| MDQ21 | Data | AD7 | I/O | GV _{DD} | — |
| MDQ22 | Data | AD10 | I/O | GV _{DD} | — |
| MDQ23 | Data | AE10 | I/O | GV _{DD} | — |
| MDQ24 | Data | AC1 | I/O | GV _{DD} | — |
| MDQ25 | Data | AC2 | I/O | GV _{DD} | — |
| MDQ26 | Data | AF1 | I/O | GV _{DD} | — |
| MDQ27 | Data | AF2 | I/O | GV _{DD} | — |
| MDQ28 | Data | AC3 | I/O | GV _{DD} | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|--------------------|----------|------------------|------|
| MDQ29 | Data | AC4 | I/O | GV _{DD} | — |
| MDQ30 | Data | AE1 | I/O | GV _{DD} | — |
| MDQ31 | Data | AE3 | I/O | GV _{DD} | — |
| MDQ32 | Data | AE16 | I/O | GV _{DD} | — |
| MDQ33 | Data | AD16 | I/O | GV _{DD} | — |
| MDQ34 | Data | AE19 | I/O | GV _{DD} | — |
| MDQ35 | Data | AD19 | I/O | GV _{DD} | — |
| MDQ36 | Data | AF15 | I/O | GV _{DD} | — |
| MDQ37 | Data | AF16 | I/O | GV _{DD} | — |
| MDQ38 | Data | AF18 | I/O | GV _{DD} | — |
| MDQ39 | Data | AF19 | I/O | GV _{DD} | — |
| MDQ40 | Data | AH23 | I/O | GV _{DD} | — |
| MDQ41 | Data | AG23 | I/O | GV _{DD} | — |
| MDQ42 | Data | AH27 | I/O | GV _{DD} | — |
| MDQ43 | Data | AG27 | I/O | GV _{DD} | — |
| MDQ44 | Data | AG21 | I/O | GV _{DD} | — |
| MDQ45 | Data | AH22 | I/O | GV _{DD} | — |
| MDQ46 | Data | AH26 | I/O | GV _{DD} | — |
| MDQ47 | Data | AG26 | I/O | GV _{DD} | — |
| MDQ48 | Data | AF21 | I/O | GV _{DD} | — |
| MDQ49 | Data | AD21 | I/O | GV _{DD} | — |
| MDQ50 | Data | AF24 | I/O | GV _{DD} | — |
| MDQ51 | Data | AD24 | I/O | GV _{DD} | — |
| MDQ52 | Data | AE20 | I/O | GV _{DD} | — |
| MDQ53 | Data | AD20 | I/O | GV _{DD} | — |
| MDQ54 | Data | AD23 | I/O | GV _{DD} | — |
| MDQ55 | Data | AE25 | I/O | GV _{DD} | — |
| MDQ56 | Data | AF26 | I/O | GV _{DD} | — |
| MDQ57 | Data | AF27 | I/O | GV _{DD} | — |
| MDQ58 | Data | AD25 | I/O | GV _{DD} | — |
| MDQ59 | Data | AD26 | I/O | GV _{DD} | — |
| MDQ60 | Data | AG28 | I/O | GV _{DD} | — |
| MDQ61 | Data | AF25 | I/O | GV _{DD} | — |
| MDQ62 | Data | AD27 | I/O | GV _{DD} | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--------------------------------|-----------------------|--------------------|----------|------------------|------|
| MDQ63 | Data | AD28 | I/O | GV _{DD} | — |
| MECC0 | Error Correcting Code | AH2 | I/O | GV _{DD} | — |
| MECC1 | Error Correcting Code | AF3 | I/O | GV _{DD} | — |
| MECC2 | Error Correcting Code | AG5 | I/O | GV _{DD} | — |
| MECC3 | Error Correcting Code | AH5 | I/O | GV _{DD} | — |
| MECC4 | Error Correcting Code | AG1 | I/O | GV _{DD} | — |
| MECC5 | Error Correcting Code | AG2 | I/O | GV _{DD} | — |
| MECC6 | Error Correcting Code | AH4 | I/O | GV _{DD} | — |
| MECC7 | Error Correcting Code | AF5 | I/O | GV _{DD} | — |
| $\overline{\text{MAPAR_ERR}}$ | Address Parity Error | AH8 | I | GV _{DD} | 4 |
| MAPAR_OUT | Address Parity Out | AG15 | O | GV _{DD} | — |
| MDM0 | Data Mask | Y2 | O | GV _{DD} | — |
| MDM1 | Data Mask | AC7 | O | GV _{DD} | — |
| MDM2 | Data Mask | AD8 | O | GV _{DD} | — |
| MDM3 | Data Mask | AD5 | O | GV _{DD} | — |
| MDM4 | Data Mask | AE17 | O | GV _{DD} | — |
| MDM5 | Data Mask | AH25 | O | GV _{DD} | — |
| MDM6 | Data Mask | AF22 | O | GV _{DD} | — |
| MDM7 | Data Mask | AE26 | O | GV _{DD} | — |
| MDM8 | Data Mask | AF4 | O | GV _{DD} | — |
| MDQS0 | Data Strobe | AA2 | I/O | GV _{DD} | — |
| MDQS1 | Data Strobe | AD3 | I/O | GV _{DD} | — |
| MDQS2 | Data Strobe | AE9 | I/O | GV _{DD} | — |
| MDQS3 | Data Strobe | AD1 | I/O | GV _{DD} | — |
| MDQS4 | Data Strobe | AD18 | I/O | GV _{DD} | — |
| MDQS5 | Data Strobe | AG24 | I/O | GV _{DD} | — |
| MDQS6 | Data Strobe | AE23 | I/O | GV _{DD} | — |
| MDQS7 | Data Strobe | AE28 | I/O | GV _{DD} | — |
| MDQS8 | Data Strobe | AH3 | I/O | GV _{DD} | — |
| $\overline{\text{MDQS0}}$ | Data Strobe | AA1 | I/O | GV _{DD} | — |
| $\overline{\text{MDQS1}}$ | Data Strobe | AD4 | I/O | GV _{DD} | — |
| $\overline{\text{MDQS2}}$ | Data Strobe | AD9 | I/O | GV _{DD} | — |
| $\overline{\text{MDQS3}}$ | Data Strobe | AD2 | I/O | GV _{DD} | — |
| $\overline{\text{MDQS4}}$ | Data Strobe | AD17 | I/O | GV _{DD} | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---------------------------|-----------------------|--------------------|----------|-------------------------|------|
| $\overline{\text{MDQS5}}$ | Data Strobe | AH24 | I/O | GV_{DD} | — |
| $\overline{\text{MDQS6}}$ | Data Strobe | AE22 | I/O | GV_{DD} | — |
| $\overline{\text{MDQS7}}$ | Data Strobe | AF28 | I/O | GV_{DD} | — |
| $\overline{\text{MDQS8}}$ | Data Strobe | AG3 | I/O | GV_{DD} | — |
| MBA0 | Bank Select | AC16 | O | GV_{DD} | — |
| MBA1 | Bank Select | AC15 | O | GV_{DD} | — |
| MBA2 | Bank Select | AC8 | O | GV_{DD} | — |
| MA00 | Address | AG16 | O | GV_{DD} | — |
| MA01 | Address | AF12 | O | GV_{DD} | — |
| MA02 | Address | AC12 | O | GV_{DD} | — |
| MA03 | Address | AH11 | O | GV_{DD} | — |
| MA04 | Address | AG11 | O | GV_{DD} | — |
| MA05 | Address | AH10 | O | GV_{DD} | — |
| MA06 | Address | AC11 | O | GV_{DD} | — |
| MA07 | Address | AC10 | O | GV_{DD} | — |
| MA08 | Address | AF10 | O | GV_{DD} | — |
| MA09 | Address | AH9 | O | GV_{DD} | — |
| MA10 | Address | AH16 | O | GV_{DD} | — |
| MA11 | Address | AG9 | O | GV_{DD} | — |
| MA12 | Address | AC9 | O | GV_{DD} | — |
| MA13 | Address | AH20 | O | GV_{DD} | — |
| MA14 | Address | AG8 | O | GV_{DD} | — |
| MA15 | Address | AH7 | O | GV_{DD} | — |
| $\overline{\text{MWE}}$ | Write Enable | AH18 | O | GV_{DD} | — |
| $\overline{\text{MRAS}}$ | Row Address Strobe | AH17 | O | GV_{DD} | — |
| $\overline{\text{MCAS}}$ | Column Address Strobe | AH19 | O | GV_{DD} | — |
| $\overline{\text{MCS0}}$ | Chip Select | AC18 | O | GV_{DD} | — |
| $\overline{\text{MCS1}}$ | Chip Select | AC21 | O | GV_{DD} | — |
| $\overline{\text{MCS2}}$ | Chip Select | AG17 | O | GV_{DD} | — |
| $\overline{\text{MCS3}}$ | Chip Select | AG20 | O | GV_{DD} | — |
| MCKE0 | Clock Enable | AB8 | O | GV_{DD} | — |
| MCKE1 | Clock Enable | AB7 | O | GV_{DD} | — |
| MCKE2 | Clock Enable | AH6 | O | GV_{DD} | — |
| MCKE3 | Clock Enable | AG6 | O | GV_{DD} | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---------------------------------------|------------------------------|--------------------|----------|------------------|------|
| MCK0 | Clock | AD14 | O | GV _{DD} | — |
| MCK1 | Clock | AE13 | O | GV _{DD} | — |
| MCK2 | Clock | AG13 | O | GV _{DD} | — |
| MCK3 | Clock | AG14 | O | GV _{DD} | — |
| $\overline{\text{MCK0}}$ | Clock Complements | AE14 | O | GV _{DD} | — |
| $\overline{\text{MCK1}}$ | Clock Complements | AD13 | O | GV _{DD} | — |
| $\overline{\text{MCK2}}$ | Clock Complements | AH13 | O | GV _{DD} | — |
| $\overline{\text{MCK3}}$ | Clock Complements | AH14 | O | GV _{DD} | — |
| MODT0 | On Die Termination | AC19 | O | GV _{DD} | — |
| MODT1 | On Die Termination | AD22 | O | GV _{DD} | — |
| MODT2 | On Die Termination | AG18 | O | GV _{DD} | — |
| MODT3 | On Die Termination | AH21 | O | GV _{DD} | — |
| MDIC0 | Driver Impedance Calibration | AG12 | I/O | GV _{DD} | 16 |
| MDIC1 | Driver Impedance Calibration | AE12 | I/O | GV _{DD} | 16 |
| Local Bus Controller Interface | | | | | |
| LAD00 | Muxed Data/Address | J6 | I/O | BV _{DD} | 3 |
| LAD01 | Muxed Data/Address | J4 | I/O | BV _{DD} | 3 |
| LAD02 | Muxed Data/Address | K2 | I/O | BV _{DD} | 3 |
| LAD03 | Muxed Data/Address | K4 | I/O | BV _{DD} | 3 |
| LAD04 | Muxed Data/Address | L1 | I/O | BV _{DD} | 3 |
| LAD05 | Muxed Data/Address | J5 | I/O | BV _{DD} | 3 |
| LAD06 | Muxed Data/Address | N5 | I/O | BV _{DD} | 3 |
| LAD07 | Muxed Data/Address | N2 | I/O | BV _{DD} | 3 |
| LAD08 | Muxed Data/Address | N3 | I/O | BV _{DD} | 3 |
| LAD09 | Muxed Data/Address | N1 | I/O | BV _{DD} | 3 |
| LAD10 | Muxed Data/Address | P4 | I/O | BV _{DD} | 3 |
| LAD11 | Muxed Data/Address | R7 | I/O | BV _{DD} | 3 |
| LAD12 | Muxed Data/Address | T4 | I/O | BV _{DD} | 3 |
| LAD13 | Muxed Data/Address | U2 | I/O | BV _{DD} | 3 |
| LAD14 | Muxed Data/Address | T6 | I/O | BV _{DD} | 3 |
| LAD15 | Muxed Data/Address | T7 | I/O | BV _{DD} | 3 |
| LA16 | Address | K6 | I/O | BV _{DD} | 31 |
| LA17 | Address | K3 | I/O | BV _{DD} | 31 |
| LA18 | Address | P6 | I/O | BV _{DD} | 31 |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|--|--------------------|----------|------------------|-------|
| LA19 | Address | P3 | I/O | BV _{DD} | 31 |
| LA20 | Address | P2 | I/O | BV _{DD} | 31 |
| LA21 | Address | R3 | I/O | BV _{DD} | 31 |
| LA22 | Address | T1 | I/O | BV _{DD} | 31 |
| LA23 | Address | U1 | I/O | BV _{DD} | 3 |
| LA24 | Address | R6 | I/O | BV _{DD} | 3 |
| LA25 | Address | T5 | I/O | BV _{DD} | 31 |
| LA26 | Address | T3 | I/O | BV _{DD} | 3, 29 |
| LA27 | Address | T2 | O | BV _{DD} | — |
| LA28 | Address | U5 | I/O | BV _{DD} | — |
| LA29 | Address | U3 | I/O | BV _{DD} | — |
| LA30 | Address | V1 | I/O | BV _{DD} | — |
| LA31 | Address | V3 | I/O | BV _{DD} | — |
| LDP0 | Data Parity | L3 | I/O | BV _{DD} | — |
| LDP1 | Data Parity | M1 | I/O | BV _{DD} | — |
| $\overline{\text{LCS0}}$ | Chip Selects | R5 | O | BV _{DD} | 5 |
| $\overline{\text{LCS1}}$ | Chip Selects | P7 | O | BV _{DD} | 5 |
| $\overline{\text{LCS2}}$ | Chip Selects | U4 | O | BV _{DD} | 5 |
| $\overline{\text{LCS3}}$ | Chip Selects | R1 | O | BV _{DD} | 5 |
| $\overline{\text{LWE0}}$ | Write Enable | M6 | O | BV _{DD} | — |
| $\overline{\text{LWE1}}$ | Write Enable | M3 | O | BV _{DD} | — |
| LBCTL | Buffer Control | P1 | O | BV _{DD} | — |
| LALE | Address Latch Enable | N6 | I/O | BV _{DD} | — |
| LGPL0/LFCLE | UPM General Purpose Line 0/ LFCLE—FCM | L5 | O | BV _{DD} | 3, 4 |
| LGPL1/LFALE | UPM General Purpose Line 1/ LFALE—FCM | K1 | O | BV _{DD} | 3, 4 |
| LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$ | UPM General Purpose Line 2/ LOE_B—Output Enable | L6 | O | BV _{DD} | 3, 4 |
| LGPL3/ $\overline{\text{LFWP}}$ | UPM General Purpose Line 3/ LFWP_B—FCM | J3 | O | BV _{DD} | 3, 4 |
| LGPL4/ $\overline{\text{LGTA}}$ /LUPWAIT/LPBSE | UPM General Purpose Line 4/ LGTA_B—FCM | L2 | I/O | BV _{DD} | 36 |
| LGPL5 | UPM General Purpose Line 5 / Amux | J1 | O | BV _{DD} | 3, 4 |
| LCLK0 | Local Bus Clock | M4 | O | BV _{DD} | — |
| LCLK1 | Local Bus Clock | N7 | O | BV _{DD} | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--|-------------------------------|--------------------|----------|-------------------------------------|-------|
| DMA | | | | | |
| DMA1_DREQ0/IIC4_SCL/EVT5/M1SRCID1/LB_SRCID1/GPIO18 | DMA1 Channel 0 Request | AC23 | I | OV _{DD} | 24 |
| DMA1_DACK0/IIC3_SCL/GPIO16/SDHC_CD/M1DVAL/LB_DVAL | DMA1 Channel 0 Acknowledge | AB23 | O | OV _{DD} | 2, 14 |
| DMA1_DDONE0/IIC3_SDA/GPIO17/M1SRCID0/LB_SRCID0/SDHC_WP | DMA1 Channel 0 Done | AB26 | O | OV _{DD} | 2, 14 |
| DMA2_DREQ0/IRQ03/GPIO21 | DMA2 Channel 0 Request | AA26 | I | OV _{DD} | 24 |
| DMA2_DACK0/IRQ04/GPIO22 | DMA2 Channel 0 Acknowledge | V25 | O | OV _{DD} | 24 |
| DMA2_DDONE0/IRQ05/GPIO23 | DMA2 Channel 0 Done | AA22 | O | OV _{DD} | 24 |
| USB Host Port 1 | | | | | |
| USB1_UDP | USB1 PHY Data Plus | K28 | I/O | USB_V _{DD-3P} ₃ | — |
| USB1_UDM | USB1 PHY Data Minus | L28 | I/O | USB_V _{DD-3P} ₃ | — |
| USB1_VBUS_CLMP | USB1 PHY VBUS Divided Signals | M25 | I | USB_V _{DD-3P} ₃ | 34 |
| USB1_UID | USB1 PHY ID Detect | M27 | I | USB_V _{DD-3P} ₃ | — |
| USB_CLKIN | USB PHY Clock Input | P22 | I | OV _{DD} | — |
| USB1_DRVVBUS/GPIO24/IRQ6 | USB1 5V Supply Enable | Y26 | O | OV _{DD} | — |
| USB1_PWRFAULT/GPIO25/IRQ7 | USB Power Fault | AA23 | I | OV _{DD} | — |
| USB Host Port 2 | | | | | |
| USB2_UDP | USB2 PHY Data Plus | K26 | I/O | USB_V _{DD-3P} ₃ | — |
| USB2_UDM | USB2 PHY Data Minus | L26 | I/O | USB_V _{DD-3P} ₃ | — |
| USB2_VBUS_CLMP | USB2 PHY VBUS Divided Signals | J25 | I | USB_V _{DD-3P} ₃ | 34 |
| USB2_UID | USB2 PHY ID Detect | J27 | I | USB_V _{DD-3P} ₃ | — |
| USB2_DRVVBUS/GPIO26/IRQ8 | USB2 5V Supply Enable | AC22 | I/O | OV _{DD} | — |
| USB2_PWRFAULT/GPIO27/IRQ9 | USB2 Power Fault | AC27 | I/O | OV _{DD} | — |
| Programmable Interrupt Controller | | | | | |
| IRQ00 | External Interrupts | Y25 | I | OV _{DD} | — |
| IRQ01 | External Interrupts | AB27 | I | OV _{DD} | — |
| IRQ02 | External Interrupts | AB25 | I | OV _{DD} | — |
| IRQ03/GPIO21/DMA2_DREQ0 | External Interrupts | AA26 | I | OV _{DD} | 24 |
| IRQ04/GPIO22/DMA2_DACK0 | External Interrupts | V25 | I | OV _{DD} | 24 |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--|-------------------------|--------------------|----------|--------------------|----------|
| IRQ05/GPIO23/DMA2_DDONE0 | External Interrupts | AA22 | I | OV _{DD} | 24 |
| IRQ06/GPIO24/USB1_DRVVBUS | External Interrupts | Y26 | I | OV _{DD} | 24 |
| IRQ07/GPIO25/USB1_PWRFAULT | External Interrupts | AA23 | I | OV _{DD} | 24 |
| IRQ08/GPIO26/USB2_DRVVBUS | External Interrupts | AC22 | I | OV _{DD} | 24 |
| IRQ09/GPIO27/USB2_PWRFAULT | External Interrupts | AC27 | I | OV _{DD} | 24 |
| IRQ10/GPIO28/EVT7 | External Interrupts | AB24 | I | OV _{DD} | 24 |
| IRQ11/GPIO29/EVT8 | External Interrupts | AC24 | I | OV _{DD} | 24 |
| IRQ_OUT/EVT9 | Interrupt Output | Y24 | O | OV _{DD} | 1, 2, 24 |
| Trust | | | | | |
| TMP_DETECT | Tamper Detect | T24 | I | OV _{DD} | 25 |
| LP_TMP_DETECT | Low Power Tamper Detect | L21 | I | V _{DD_LP} | 25 |
| eSDHC | | | | | |
| SDHC_CMD | Command/Response | N22 | I/O | CV _{DD} | — |
| SDHC_DAT0 | Data | N23 | I/O | CV _{DD} | — |
| SDHC_DAT1 | Data | N26 | I/O | CV _{DD} | — |
| SDHC_DAT2 | Data | N27 | I/O | CV _{DD} | — |
| SDHC_DAT3 | Data | N28 | I/O | CV _{DD} | — |
| SDHC_DAT4/SPI_CS0/GPIO00 | Data | H26 | I/O | CV _{DD} | 24, 28 |
| SDHC_DAT5/SPI_CS1/GPIO01 | Data | H23 | I/O | CV _{DD} | 24, 28 |
| SDHC_DAT6/SPI_CS2/GPIO02 | Data | H27 | I/O | CV _{DD} | 24, 28 |
| SDHC_DAT7/SPI_CS3/GPIO03 | Data | H24 | I/O | CV _{DD} | 24, 28 |
| SDHC_CLK | Host to Card Clock | N24 | O | OV _{DD} | — |
| SDHC_CD/IIC3_SCL/GPIO16/ M1DVAL/LB_DVAL/DMA1_DACK0 | Card Detection | AB23 | I/O | OV _{DD} | 24, 28 |
| SDHC_WP/IIC3_SDA/GPIO17/ M1SRCID0/LB_SRCID0/DMA1_DDONE0 | Card Write Protection | AB26 | I | OV _{DD} | 24, 28 |
| eSPI | | | | | |
| SPI_MOSI | Master Out Slave In | H28 | I/O | CV _{DD} | — |
| SPI_MISO | Master In Slave Out | G23 | I | CV _{DD} | — |
| SPI_CLK | eSPI Clock | H22 | O | CV _{DD} | — |
| SPI_CS0/SDHC_DAT4/GPIO00 | eSPI Chip Select | H26 | O | CV _{DD} | 24 |
| SPI_CS1/SDHC_DAT5/GPIO01 | eSPI Chip Select | H23 | O | CV _{DD} | 24 |
| SPI_CS2/SDHC_DAT6/GPIO02 | eSPI Chip Select | H27 | O | CV _{DD} | 24 |
| SPI_CS3/SDHC_DAT7/GPIO03 | eSPI Chip Select | H24 | O | CV _{DD} | 24 |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--|-------------------------------|--------------------|----------|------------------|------|
| IEEE 1588 | | | | | |
| TSEC_1588_CLK_IN/EC1_RXD2 | Clock In | B27 | I | LV _{DD} | — |
| TSEC_1588_TRIG_IN1/EC1_RXD0 | Trigger In 1 | B28 | I | LV _{DD} | — |
| TSEC_1588_TRIG_IN2/EC1_RXD1 | Trigger In 2 | A27 | I | LV _{DD} | — |
| TSEC_1588_ALARM_OUT1/EC1_TXD0 | Alarm Out 1 | B24 | O | LV _{DD} | — |
| TSEC_1588_ALARM_OUT2/ EC1_TXD1/GPIO30 | Alarm Out 2 | C25 | O | LV _{DD} | 23 |
| TSEC_1588_CLK_OUT/EC1_RXD3 | Clock Out | B26 | O | LV _{DD} | — |
| TSEC_1588_PULSE_OUT1/EC1_TXD2 | Pulse Out1 | C28 | O | LV _{DD} | — |
| TSEC_1588_PULSE_OUT2/EC1_TXD3/G PIO31 | Pulse Out2 | A26 | O | LV _{DD} | 23 |
| Ethernet Management Interface 1 | | | | | |
| EMI1_MDC | Management Data Clock | F23 | O | LV _{DD} | — |
| EMI1_MDIO | Management Data In/Out | G24 | I/O | LV _{DD} | — |
| Ethernet Reference Clock | | | | | |
| EC1_GTX_CLK125/EC_XTRNL_TX_STMP 2 | Reference Clock (RGMII) | A24 | I | LV _{DD} | 25 |
| EC2_GTX_CLK125 | Reference Clock (RGMII) | D24 | I | LV _{DD} | 25 |
| Ethernet External Timestamping | | | | | |
| EC_XTRNL_TX_STMP1/EC1_TX_EN | External Timestamp Transmit 1 | C27 | I | LV _{DD} | — |
| EC_XTRNL_RX_STMP1/EC1_RX_DV | External Timestamp Receive 1 | A25 | I | LV _{DD} | — |
| EC_XTRNL_TX_STMP2/EC1_GTX_CLK12 5 | External Timestamp Transmit 2 | A24 | I | LV _{DD} | — |
| EC_XTRNL_RX_STMP2/EC1_RX_CLK | External Timestamp Receive 2 | C24 | I | LV _{DD} | — |
| Three-Speed Ethernet Controller 1 | | | | | |
| EC1_TXD3/TSEC_1588_PULSE_OUT2/G PIO31 | Transmit Data | A26 | O | LV _{DD} | — |
| EC1_TXD2/TSEC_1588_PULSE_OUT1 | Transmit Data | C28 | O | LV _{DD} | — |
| EC1_TXD1/TSEC_1588_ALARM_OUT2/G PIO30 | Transmit Data | C25 | O | LV _{DD} | — |
| EC1_TXD0/TSEC_1588_ALARM_OUT1 | Transmit Data | B24 | O | LV _{DD} | — |
| EC1_TX_EN/EC_XTRNL_TX_STMP1 | Transmit Enable | C27 | O | LV _{DD} | 15 |
| EC1_GTX_CLK | Transmit Clock Out (RGMII) | D26 | O | LV _{DD} | 24 |
| EC1_RXD3/TSEC_1588_CLK_OUT | Receive Data | B26 | I | LV _{DD} | 25 |
| EC1_RXD2/TSEC_1588_CLK_IN | Receive Data | B27 | I | LV _{DD} | 25 |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|----------------------------|--------------------|----------|------------------|--------|
| EC1_RXD1/TSEC_1588_TRIG_IN2 | Receive Data | A27 | I | LV _{DD} | 25 |
| EC1_RXD0/TSEC_1588_TRIG_IN1 | Receive Data | B28 | I | LV _{DD} | 25 |
| EC1_RX_DV/EC_XTRNL_RX_STMP1 | Receive Data Valid | A25 | I | LV _{DD} | 25 |
| EC1_RX_CLK/EC_XTRNL_RX_STMP2 | Receive Clock | C24 | I | LV _{DD} | 25 |
| Three-Speed Ethernet Controller 2 | | | | | |
| EC2_TXD3 | Transmit Data | G28 | O | LV _{DD} | — |
| EC2_TXD2 | Transmit Data | G26 | O | LV _{DD} | — |
| EC2_TXD1 | Transmit Data | G27 | O | LV _{DD} | — |
| EC2_TXD0 | Transmit Data | G25 | O | LV _{DD} | — |
| EC2_TX_EN | Transmit Enable | F28 | O | LV _{DD} | 15 |
| EC2_GTX_CLK | Transmit Clock Out (RGMII) | E28 | O | LV _{DD} | 24 |
| EC2_RXD3 | Receive Data | D28 | I | LV _{DD} | 25 |
| EC2_RXD2 | Receive Data | E27 | I | LV _{DD} | 25 |
| EC2_RXD1 | Receive Data | E25 | I | LV _{DD} | 24, 25 |
| EC2_RXD0 | Receive Data | F26 | I | LV _{DD} | 24, 25 |
| EC2_RX_DV | Receive Data Valid | D25 | I | LV _{DD} | 25 |
| EC2_RX_CLK | Receive Clock | F25 | I | LV _{DD} | 25 |
| UART | | | | | |
| UART1_SOUT/GPIO8 | Transmit Data | R23 | O | OV _{DD} | 24 |
| UART2_SOUT/GPIO9 | Transmit Data | P26 | O | OV _{DD} | 24 |
| UART1_SIN/GPIO10 | Receive Data | R26 | I | OV _{DD} | 24 |
| UART2_SIN/GPIO11 | Receive Data | P27 | I | OV _{DD} | 24 |
| UART1_RTS/UART3_SOUT/GPIO12 | Ready to Send | P24 | O | OV _{DD} | 24 |
| UART2_RTS/UART4_SOUT/GPIO13 | Ready to Send | P25 | O | OV _{DD} | 24 |
| UART1_CTS/UART3_SIN/GPIO14 | Clear to Send | R25 | I | OV _{DD} | 24 |
| UART2_CTS/UART4_SIN/GPIO15 | Clear to Send | P23 | I | OV _{DD} | 24 |
| I²C Interface | | | | | |
| IIC1_SCL | Serial Clock | AC25 | I/O | OV _{DD} | 2, 14 |
| IIC1_SDA | Serial Data | AC28 | I/O | OV _{DD} | 2, 14 |
| IIC2_SCL | Serial Clock | W25 | I/O | OV _{DD} | 2, 14 |
| IIC2_SDA | Serial Data | AA25 | I/O | OV _{DD} | 2, 14 |
| IIC3_SCL/GPIO16/M1DVAL/LB_DVAL/ DMA1_DACK0/SDHC_CD | Serial Clock | AB23 | I/O | OV _{DD} | 2, 14 |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------------|--------------------|----------|------------------|-------|
| IIC3_SDA/GPIO17/M1SRCID0/LB_SRCID0 / DMA1_DDONE0/SDHC_WP | Serial Data | AB26 | I/O | OV _{DD} | 2, 14 |
| IIC4_SCL/EVT5/M1SRCID1/LB_SRCID1/ GPIO18/DMA1_DREQ0 | Serial Clock | AC23 | I/O | OV _{DD} | 2, 14 |
| IIC4_SDA/EVT6/M1SRCID2/ LB_SRCID2/GPIO19 | Serial Data | V24 | I/O | OV _{DD} | 2, 14 |
| SerDes (x10) PCI Express, Serial RapidIO, Aurora, 10GE, 1GE | | | | | |
| SD_TX13 | Transmit Data (positive) | C20 | O | XV _{DD} | — |
| SD_TX12 | Transmit Data (positive) | C18 | O | XV _{DD} | — |
| SD_TX11 | Transmit Data (positive) | D16 | O | XV _{DD} | — |
| SD_TX10 | Transmit Data (positive) | C14 | O | XV _{DD} | — |
| SD_TX07 | Transmit Data (positive) | C12 | O | XV _{DD} | — |
| SD_TX06 | Transmit Data (positive) | C10 | O | XV _{DD} | — |
| SD_TX05 | Transmit Data (positive) | C8 | O | XV _{DD} | — |
| SD_TX04 | Transmit Data (positive) | B4 | O | XV _{DD} | — |
| SD_TX03 | Transmit Data (positive) | F3 | O | XV _{DD} | — |
| SD_TX02 | Transmit Data (positive) | G5 | O | XV _{DD} | — |
| $\overline{\text{SD_TX13}}$ | Transmit Data (negative) | D20 | O | XV _{DD} | — |
| $\overline{\text{SD_TX12}}$ | Transmit Data (negative) | D18 | O | XV _{DD} | — |
| $\overline{\text{SD_TX11}}$ | Transmit Data (negative) | C16 | O | XV _{DD} | — |
| $\overline{\text{SD_TX10}}$ | Transmit Data (negative) | D14 | O | XV _{DD} | — |
| $\overline{\text{SD_TX07}}$ | Transmit Data (negative) | D12 | O | XV _{DD} | — |
| $\overline{\text{SD_TX06}}$ | Transmit Data (negative) | D10 | O | XV _{DD} | — |
| $\overline{\text{SD_TX05}}$ | Transmit Data (negative) | D8 | O | XV _{DD} | — |
| $\overline{\text{SD_TX04}}$ | Transmit Data (negative) | B5 | O | XV _{DD} | — |
| $\overline{\text{SD_TX03}}$ | Transmit Data (negative) | F4 | O | XV _{DD} | — |
| $\overline{\text{SD_TX02}}$ | Transmit Data (negative) | G6 | O | XV _{DD} | — |
| SD_RX13 | Receive Data (positive) | B21 | I | XV _{DD} | — |
| SD_RX12 | Receive Data (positive) | B19 | I | XV _{DD} | — |
| SD_RX11 | Receive Data (positive) | B15 | I | XV _{DD} | — |
| SD_RX10 | Receive Data (positive) | A13 | I | XV _{DD} | — |
| SD_RX07 | Receive Data (positive) | B11 | I | XV _{DD} | — |
| SD_RX06 | Receive Data (positive) | B9 | I | XV _{DD} | — |
| SD_RX05 | Receive Data (positive) | B7 | I | XV _{DD} | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|--|--------------------|----------|------------------|------|
| SD_RX04 | Receive Data (positive) | A2 | I | XV _{DD} | — |
| SD_RX03 | Receive Data (positive) | E1 | I | XV _{DD} | — |
| SD_RX02 | Receive Data (positive) | G1 | I | XV _{DD} | — |
| $\overline{\text{SD_RX13}}$ | Receive Data (negative) | A21 | I | XV _{DD} | — |
| $\overline{\text{SD_RX12}}$ | Receive Data (negative) | A19 | I | XV _{DD} | — |
| $\overline{\text{SD_RX11}}$ | Receive Data (negative) | A15 | I | XV _{DD} | — |
| $\overline{\text{SD_RX10}}$ | Receive Data (negative) | B13 | I | XV _{DD} | — |
| $\overline{\text{SD_RX07}}$ | Receive Data (negative) | A11 | I | XV _{DD} | — |
| $\overline{\text{SD_RX06}}$ | Receive Data (negative) | A9 | I | XV _{DD} | — |
| $\overline{\text{SD_RX05}}$ | Receive Data (negative) | A7 | I | XV _{DD} | — |
| $\overline{\text{SD_RX04}}$ | Receive Data (negative) | A3 | I | XV _{DD} | — |
| $\overline{\text{SD_RX03}}$ | Receive Data (negative) | E2 | I | XV _{DD} | — |
| $\overline{\text{SD_RX02}}$ | Receive Data (negative) | G2 | I | XV _{DD} | — |
| SD_REF_CLK1 | SerDes Bank 1 PLL Reference Clock | D3 | I | XV _{DD} | — |
| $\overline{\text{SD_REF_CLK1}}$ | SerDes Bank 1 PLL Reference Clock Complement | D4 | I | XV _{DD} | — |
| SD_REF_CLK2 | SerDes Bank 2 PLL Reference Clock | E17 | I | XV _{DD} | — |
| $\overline{\text{SD_REF_CLK2}}$ | SerDes Bank 2 PLL Reference Clock Complement | F17 | I | XV _{DD} | — |
| General-Purpose Input/Output | | | | | |
| GPIO00/ $\overline{\text{SPI_CS0}}$ /SDHC_DATA4 | General Purpose Input/Output | H26 | I/O | CV _{DD} | — |
| GPIO01/ $\overline{\text{SPI_CS1}}$ /SDHC_DATA5 | General Purpose Input/Output | H23 | I/O | CV _{DD} | — |
| GPIO02/ $\overline{\text{SPI_CS2}}$ /SDHC_DATA6 | General Purpose Input/Output | H27 | I/O | CV _{DD} | — |
| GPIO03/ $\overline{\text{SPI_CS3}}$ /SDHC_DATA7 | General Purpose Input/Output | H24 | I/O | CV _{DD} | — |
| GPIO08/UART1_SOUT | General Purpose Input/Output | R23 | I/O | OV _{DD} | — |
| GPIO09/UART2_SOUT | General Purpose Input/Output | P26 | I/O | OV _{DD} | — |
| GPIO10/UART1_SIN | General Purpose Input/Output | R26 | I/O | OV _{DD} | — |
| GPIO11/UART2_SIN | General Purpose Input/Output | P27 | I/O | OV _{DD} | — |
| GPIO12/ $\overline{\text{UART1_RTS}}$ /UART3_SOUT | General Purpose Input/Output | P24 | I/O | OV _{DD} | — |
| GPIO13/ $\overline{\text{UART2_RTS}}$ /UART4_SOUT | General Purpose Input/Output | P25 | I/O | OV _{DD} | — |
| GPIO14/ $\overline{\text{UART1_CTS}}$ /UART3_SIN | General Purpose Input/Output | R25 | I/O | OV _{DD} | — |
| GPIO15/ $\overline{\text{UART2_CTS}}$ /UART4_SIN | General Purpose Input/Output | P23 | I/O | OV _{DD} | — |
| GPIO16/IIC3_SCL/M1DVAL/LB_DVAL/ $\overline{\text{DMA1_DACK0}}$ /SDHC_CD | General Purpose Input/Output | AB23 | I/O | OV _{DD} | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---|------------------------------|--------------------|----------|------------------|------|
| GPIO17/IIC3_SDA/M1SRCID0/LB_SRCID0 / DMA1_DDONE0/SDHC_WP | General Purpose Input/Output | AB26 | I/O | OV _{DD} | — |
| GPIO18/IIC4_SCL/EVT5/M1SRCID1/ LB_SRCID1/DMA1_DREQ0 | General Purpose Input/Output | AC23 | I/O | OV _{DD} | — |
| GPIO19/IIC4_SDA/EVT6/M1SRCID2/ LB_SRCID2 | General Purpose Input/Output | V24 | I/O | OV _{DD} | — |
| GPIO21/IRQ3/DMA2_DREQ0 | General Purpose Input/Output | AA26 | I/O | OV _{DD} | — |
| GPIO22/IRQ4/DMA2_DACK0 | General Purpose Input/Output | V25 | I/O | OV _{DD} | — |
| GPIO23/IRQ5/DMA2_DDONE0 | General Purpose Input/Output | AA22 | I/O | OV _{DD} | — |
| GPIO24/IRQ6/USB1_DRVVBUS | General Purpose Input/Output | Y26 | I/O | OV _{DD} | — |
| GPIO25/IRQ7/USB1_PWRFAULT | General Purpose Input/Output | AA23 | I/O | OV _{DD} | — |
| GPIO26/IRQ8/USB2_DRVVBUS | General Purpose Input/Output | AC22 | I/O | OV _{DD} | — |
| GPIO27/IRQ9/USB2_PWRFAULT | General Purpose Input/Output | AC27 | I/O | OV _{DD} | — |
| GPIO28/IRQ10/EVT7 | General Purpose Input/Output | AB24 | I/O | OV _{DD} | — |
| GPIO29/IRQ11/EVT8 | General Purpose Input/Output | AC24 | I/O | OV _{DD} | — |
| GPIO30/EC1_TXD1/TSEC_1588_ALARM_OUT2 | General Purpose Input/Output | C25 | I/O | LV _{DD} | 23 |
| GPIO31/EC1_TXD3/TSEC_1588_PULSE_OUT2 | General Purpose Input/Output | A26 | I/O | LV _{DD} | 23 |
| System Control | | | | | |
| PORESET | Power On Reset | T22 | I | OV _{DD} | — |
| HRESET | Hard Reset | T23 | I/O | OV _{DD} | 1, 2 |
| RESET_REQ | Reset Request | U28 | O | OV _{DD} | 31 |
| CKSTP_OUT | Checkstop Out | T25 | O | OV _{DD} | 1, 2 |
| Debug | | | | | |
| EVT0 | Event 0 | V26 | I/O | OV _{DD} | 18 |
| EVT1 | Event 1 | U27 | I/O | OV _{DD} | — |
| EVT2 | Event 2 | U26 | I/O | OV _{DD} | — |
| EVT3 | Event 3 | W24 | I/O | OV _{DD} | — |
| EVT4 | Event 4 | U24 | I/O | OV _{DD} | — |
| EVT5/IIC4_SCL/M1SRCID1/LB_SRCID1/ GPIO18/DMA1_DREQ0 | Event 5 | AC23 | I/O | OV _{DD} | — |
| EVT6/IIC4_SDA/M1SRCID2/ LB_SRCID2/GPIO19 | Event 6 | V24 | I/O | OV _{DD} | — |
| EVT7/GPIO28/IRQ10 | Event 7 | AB24 | I/O | OV _{DD} | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------|--------------------|----------|------------------|--------|
| $\overline{\text{EVT8}}$ /GPIO29/IRQ11 | Event 8 | AC24 | I/O | OV _{DD} | — |
| $\overline{\text{EVT9}}$ /IRQ_OUT | Event 9 | Y24 | I/O | OV _{DD} | — |
| M1DVAL/LB_DVAL/IIC3_SCL/GPIO16/ SDHC_CD/DMA1_DACK0 | Debug Data Valid | AB23 | O | OV _{DD} | — |
| MSRCID0/LB_SRCID0/IIC3_SDA/GPIO17/ DMA_DDONE0/SDHC_WP | Debug Source ID 0 | AB26 | O | OV _{DD} | 4, 31 |
| MSRCID1/LB_MSRCID1/ $\overline{\text{EVT5}}$ /IIC4_SCL/ LB_SRCID1/GPIO18/DMA1_DREQ0 | Debug Source ID 1 | AC23 | O | OV _{DD} | — |
| MSRCID2/LB_SRCID2/ $\overline{\text{EVT6}}$ /IIC4_SDA/ LB_SRCID2/GPIO19 | Debug Source ID 2 | V24 | O | OV _{DD} | — |
| CLK_OUT | Clock Out | T27 | O | OV _{DD} | 6 |
| Clock | | | | | |
| RTC | Real Time Clock | P28 | I | OV _{DD} | — |
| SYSCLK | System Clock | R28 | I | OV _{DD} | — |
| JTAG | | | | | |
| TCK | Test Clock | Y28 | I | OV _{DD} | — |
| TDI | Test Data In | W28 | I | OV _{DD} | 7 |
| TDO | Test Data Out | AA28 | O | OV _{DD} | 6 |
| TMS | Test Mode Select | W27 | I | OV _{DD} | 7 |
| $\overline{\text{TRST}}$ | Test Reset | Y27 | I | OV _{DD} | 7 |
| DFT | | | | | |
| $\overline{\text{SCAN_MODE}}$ | Scan Mode | V28 | I | OV _{DD} | 35 |
| TEST_SEL | Test Mode Select | T28 | I | OV _{DD} | 12, 26 |
| Power Management | | | | | |
| ASLEEP | Asleep | R22 | O | OV _{DD} | 31 |
| Input /Output Voltage Select | | | | | |
| IO_VSEL0 | I/O Voltage Select | AB28 | I | OV _{DD} | 27 |
| IO_VSEL1 | I/O Voltage Select | U23 | I | OV _{DD} | 27 |
| IO_VSEL2 | I/O Voltage Select | AB21 | I | OV _{DD} | 27 |
| IO_VSEL3 | I/O Voltage Select | Y23 | I | OV _{DD} | 27 |
| IO_VSEL4 | I/O Voltage Select | Y21 | I | OV _{DD} | 27 |
| Power and Ground Signals | | | | | |
| GND168 | Ground | A23 | — | — | — |
| GND167 | Ground | B23 | — | — | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|--------------------|----------|--------------|------|
| GND166 | Ground | B25 | — | — | — |
| GND165 | Ground | C23 | — | — | — |
| GND164 | Ground | D23 | — | — | — |
| GND163 | Ground | D27 | — | — | — |
| GND162 | Ground | E24 | — | — | — |
| GND161 | Ground | F22 | — | — | — |
| GND160 | Ground | F27 | — | — | — |
| GND159 | Ground | G10 | — | — | — |
| GND158 | Ground | G12 | — | — | — |
| GND157 | Ground | G14 | — | — | — |
| GND156 | Ground | G16 | — | — | — |
| GND155 | Ground | G18 | — | — | — |
| GND154 | Ground | G21 | — | — | — |
| GND153 | Ground | G22 | — | — | — |
| GND152 | Ground | H3 | — | — | — |
| GND151 | Ground | H4 | — | — | — |
| GND150 | Ground | H10 | — | — | — |
| GND149 | Ground | H12 | — | — | — |
| GND148 | Ground | H14 | — | — | — |
| GND147 | Ground | H16 | — | — | — |
| GND146 | Ground | H18 | — | — | — |
| GND145 | Ground | H21 | — | — | — |
| GND144 | Ground | H25 | — | — | — |
| GND143 | Ground | J2 | — | — | — |
| GND142 | Ground | J8 | — | — | — |
| GND141 | Ground | J10 | — | — | — |
| GND140 | Ground | J12 | — | — | — |
| GND139 | Ground | J14 | — | — | — |
| GND138 | Ground | J16 | — | — | — |
| GND137 | Ground | J18 | — | — | — |
| GND136 | Ground | J21 | — | — | — |
| GND135 | Ground | K5 | — | — | — |
| GND134 | Ground | K8 | — | — | — |
| GND133 | Ground | K10 | — | — | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|--------------------|----------|--------------|------|
| GND132 | Ground | K12 | — | — | — |
| GND131 | Ground | K14 | — | — | — |
| GND130 | Ground | K16 | — | — | — |
| GND129 | Ground | K18 | — | — | — |
| GND128 | Ground | K21 | — | — | — |
| GND127 | Ground | L8 | — | — | — |
| GND126 | Ground | L10 | — | — | — |
| GND125 | Ground | L12 | — | — | — |
| GND124 | Ground | L14 | — | — | — |
| GND123 | Ground | L16 | — | — | — |
| GND122 | Ground | L18 | — | — | — |
| GND121 | Ground | M2 | — | — | — |
| GND120 | Ground | M5 | — | — | — |
| GND119 | Ground | M8 | — | — | — |
| GND118 | Ground | M10 | — | — | — |
| GND117 | Ground | M12 | — | — | — |
| GND116 | Ground | M14 | — | — | — |
| GND115 | Ground | M16 | — | — | — |
| GND114 | Ground | M18 | — | — | — |
| GND113 | Ground | N8 | — | — | — |
| GND112 | Ground | N10 | — | — | — |
| GND111 | Ground | N12 | — | — | — |
| GND110 | Ground | N14 | — | — | — |
| GND109 | Ground | N16 | — | — | — |
| GND108 | Ground | N18 | — | — | — |
| GND107 | Ground | N21 | — | — | — |
| GND106 | Ground | N25 | — | — | — |
| GND105 | Ground | P5 | — | — | — |
| GND104 | Ground | P8 | — | — | — |
| GND103 | Ground | P10 | — | — | — |
| GND102 | Ground | P12 | — | — | — |
| GND101 | Ground | P14 | — | — | — |
| GND100 | Ground | P16 | — | — | — |
| GND099 | Ground | P18 | — | — | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|--------------------|----------|--------------|------|
| GND098 | Ground | P21 | — | — | — |
| GND097 | Ground | R2 | — | — | — |
| GND096 | Ground | R8 | — | — | — |
| GND095 | Ground | R10 | — | — | — |
| GND094 | Ground | R12 | — | — | — |
| GND093 | Ground | R14 | — | — | — |
| GND092 | Ground | R16 | — | — | — |
| GND091 | Ground | R18 | — | — | — |
| GND090 | Ground | R21 | — | — | — |
| GND089 | Ground | R24 | — | — | — |
| GND088 | Ground | R27 | — | — | — |
| GND087 | Ground | T8 | — | — | — |
| GND086 | Ground | T10 | — | — | — |
| GND085 | Ground | T12 | — | — | — |
| GND084 | Ground | T14 | — | — | — |
| GND083 | Ground | T16 | — | — | — |
| GND082 | Ground | T18 | — | — | — |
| GND081 | Ground | T21 | — | — | — |
| GND080 | Ground | U7 | — | — | — |
| GND079 | Ground | U8 | — | — | — |
| GND078 | Ground | U10 | — | — | — |
| GND077 | Ground | U12 | — | — | — |
| GND076 | Ground | U14 | — | — | — |
| GND075 | Ground | U17 | — | — | — |
| GND074 | Ground | U19 | — | — | — |
| GND073 | Ground | U22 | — | — | — |
| GND072 | Ground | U25 | — | — | — |
| GND071 | Ground | V2 | — | — | — |
| GND070 | Ground | V4 | — | — | — |
| GND069 | Ground | V6 | — | — | — |
| GND068 | Ground | V8 | — | — | — |
| GND067 | Ground | V10 | — | — | — |
| GND066 | Ground | V12 | — | — | — |
| GND065 | Ground | V14 | — | — | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|--------------------|----------|--------------|------|
| GND064 | Ground | V16 | — | — | — |
| GND063 | Ground | V17 | — | — | — |
| GND062 | Ground | V19 | — | — | — |
| GND061 | Ground | V21 | — | — | — |
| GND060 | Ground | V23 | — | — | — |
| GND059 | Ground | V27 | — | — | — |
| GND058 | Ground | W2 | — | — | — |
| GND057 | Ground | W5 | — | — | — |
| GND056 | Ground | W8 | — | — | — |
| GND055 | Ground | W10 | — | — | — |
| GND054 | Ground | W12 | — | — | — |
| GND053 | Ground | W14 | — | — | — |
| GND052 | Ground | W17 | — | — | — |
| GND051 | Ground | W19 | — | — | — |
| GND050 | Ground | W21 | — | — | — |
| GND049 | Ground | W23 | — | — | — |
| GND048 | Ground | Y6 | — | — | — |
| GND047 | Ground | Y7 | — | — | — |
| GND046 | Ground | Y8 | — | — | — |
| GND045 | Ground | Y10 | — | — | — |
| GND044 | Ground | Y12 | — | — | — |
| GND043 | Ground | Y14 | — | — | — |
| GND042 | Ground | Y16 | — | — | — |
| GND041 | Ground | Y17 | — | — | — |
| GND040 | Ground | Y19 | — | — | — |
| GND039 | Ground | Y22 | — | — | — |
| GND038 | Ground | AA5 | — | — | — |
| GND037 | Ground | AA7 | — | — | — |
| GND036 | Ground | AA17 | — | — | — |
| GND035 | Ground | AA19 | — | — | — |
| GND034 | Ground | AA24 | — | — | — |
| GND033 | Ground | AA27 | — | — | — |
| GND032 | Ground | AB2 | — | — | — |
| GND031 | Ground | AB9 | — | — | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--------|------------------------|--------------------|----------|--------------|------|
| GND030 | Ground | AB10 | — | — | — |
| GND029 | Ground | AB11 | — | — | — |
| GND028 | Ground | AB12 | — | — | — |
| GND027 | Ground | AB15 | — | — | — |
| GND026 | Ground | AB22 | — | — | — |
| GND025 | Ground | AC5 | — | — | — |
| GND024 | Ground | AC17 | — | — | — |
| GND023 | Ground | AC20 | — | — | — |
| GND022 | Ground | AC26 | — | — | — |
| GND021 | Ground | AD12 | — | — | — |
| GND020 | Ground | AD15 | — | — | — |
| GND019 | Ground | AE2 | — | — | — |
| GND018 | Ground | AE5 | — | — | — |
| GND017 | Ground | AE8 | — | — | — |
| GND016 | Ground | AE11 | — | — | — |
| GND015 | Ground | AE15 | — | — | — |
| GND014 | Ground | AE18 | — | — | — |
| GND013 | Ground | AE21 | — | — | — |
| GND012 | Ground | AE24 | — | — | — |
| GND011 | Ground | AE27 | — | — | — |
| GND010 | Ground | AF13 | — | — | — |
| GND009 | Ground | AF14 | — | — | — |
| GND008 | Ground | AG4 | — | — | — |
| GND007 | Ground | AG7 | — | — | — |
| GND006 | Ground | AG10 | — | — | — |
| GND005 | Ground | AG19 | — | — | — |
| GND004 | Ground | AG22 | — | — | — |
| GND003 | Ground | AG25 | — | — | — |
| GND002 | Ground | AH12 | — | — | — |
| GND001 | Ground | AH15 | — | — | — |
| XGND12 | SerDes Transceiver GND | C5 | — | — | — |
| XGND11 | SerDes Transceiver GND | C7 | — | — | — |
| XGND10 | SerDes Transceiver GND | C11 | — | — | — |
| XGND09 | SerDes Transceiver GND | C15 | — | — | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|----------------|-------------------------------------|--------------------|----------|--------------|------|
| XGND08 | SerDes Transceiver GND | C21 | — | — | — |
| XGND07 | SerDes Transceiver GND | D9 | — | — | — |
| XGND06 | SerDes Transceiver GND | D13 | — | — | — |
| XGND05 | SerDes Transceiver GND | D19 | — | — | — |
| XGND04 | SerDes Transceiver GND | F6 | — | — | — |
| XGND03 | SerDes Transceiver GND | F21 | — | — | — |
| XGND02 | SerDes Transceiver GND | G3 | — | — | — |
| XGND01 | SerDes Transceiver GND | H5 | — | — | — |
| SGND17 | SerDes Core Logic GND | A5 | — | — | — |
| SGND16 | SerDes Core Logic GND | A8 | — | — | — |
| SGND15 | SerDes Core Logic GND | A12 | — | — | — |
| SGND14 | SerDes Core Logic GND | A16 | — | — | — |
| SGND13 | SerDes Core Logic GND | A20 | — | — | — |
| SGND12 | SerDes Core Logic GND | B1 | — | — | — |
| SGND11 | SerDes Core Logic GND | B6 | — | — | — |
| SGND10 | SerDes Core Logic GND | B10 | — | — | — |
| SGND09 | SerDes Core Logic GND | B14 | — | — | — |
| SGND08 | SerDes Core Logic GND | B18 | — | — | — |
| SGND07 | SerDes Core Logic GND | B22 | — | — | — |
| SGND06 | SerDes Core Logic GND | C3 | — | — | — |
| SGND05 | SerDes Core Logic GND | D2 | — | — | — |
| SGND04 | SerDes Core Logic GND | D17 | — | — | — |
| SGND03 | SerDes Core Logic GND | E3 | — | — | — |
| SGND02 | SerDes Core Logic GND | F1 | — | — | — |
| SGND01 | SerDes Core Logic GND | H2 | — | — | — |
| AGND_SRDS1 | SerDes PLL1 GND | C2 | — | — | — |
| AGND_SRDS2 | SerDes PLL2 GND | B17 | — | — | — |
| SENSEGND_CA_PL | Core Group A and Platform GND Sense | G8 | — | — | 8 |
| SENSEGND_CB | Core Group B GND Sense | AA16 | — | — | 8 |
| USB1_AGND06 | USB1 PHY Transceiver GND | J28 | — | — | — |
| USB1_AGND05 | USB1 PHY Transceiver GND | K27 | — | — | — |
| USB1_AGND04 | USB1 PHY Transceiver GND | L27 | — | — | — |
| USB1_AGND03 | USB1 PHY Transceiver GND | M22 | — | — | — |
| USB1_AGND02 | USB1 PHY Transceiver GND | M24 | — | — | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|-------------|--------------------------|--------------------|----------|------------------|------|
| USB1_AGND01 | USB1 PHY Transceiver GND | M28 | — | — | — |
| USB2_AGND06 | USB2 PHY Transceiver GND | J22 | — | — | — |
| USB2_AGND05 | USB2 PHY Transceiver GND | J24 | — | — | — |
| USB2_AGND04 | USB2 PHY Transceiver GND | J26 | — | — | — |
| USB2_AGND03 | USB2 PHY Transceiver GND | K25 | — | — | — |
| USB2_AGND02 | USB2 PHY Transceiver GND | L25 | — | — | — |
| USB2_AGND01 | USB2 PHY Transceiver GND | M26 | — | — | — |
| OVDD06 | General I/O Supply | N20 | — | OV _{DD} | — |
| OVDD05 | General I/O Supply | P20 | — | OV _{DD} | — |
| OVDD04 | General I/O Supply | R20 | — | OV _{DD} | — |
| OVDD03 | General I/O Supply | T20 | — | OV _{DD} | — |
| OVDD02 | General I/O Supply | T26 | — | OV _{DD} | — |
| OVDD01 | General I/O Supply | W26 | — | OV _{DD} | — |
| CVDD2 | eSPI and eSDHC Supply | K20 | — | CV _{DD} | — |
| CVDD1 | eSPI and eSDHC Supply | M20 | — | CV _{DD} | — |
| GVDD17 | DDR Supply | AA8 | — | GV _{DD} | — |
| GVDD16 | DDR Supply | AA9 | — | GV _{DD} | — |
| GVDD15 | DDR Supply | AA10 | — | GV _{DD} | — |
| GVDD14 | DDR Supply | AA11 | — | GV _{DD} | — |
| GVDD13 | DDR Supply | AA12 | — | GV _{DD} | — |
| GVDD12 | DDR Supply | AA13 | — | GV _{DD} | — |
| GVDD11 | DDR Supply | AA14 | — | GV _{DD} | — |
| GVDD10 | DDR Supply | AA15 | — | GV _{DD} | — |
| GVDD09 | DDR Supply | AB13 | — | GV _{DD} | — |
| GVDD08 | DDR Supply | AB14 | — | GV _{DD} | — |
| GVDD07 | DDR Supply | AC13 | — | GV _{DD} | — |
| GVDD06 | DDR Supply | AC14 | — | GV _{DD} | — |
| GVDD05 | DDR Supply | AF6 | — | GV _{DD} | — |
| GVDD04 | DDR Supply | AF9 | — | GV _{DD} | — |
| GVDD03 | DDR Supply | AF17 | — | GV _{DD} | — |
| GVDD02 | DDR Supply | AF20 | — | GV _{DD} | — |
| GVDD01 | DDR Supply | AF23 | — | GV _{DD} | — |
| BVDD07 | Local Bus Supply | J7 | — | BV _{DD} | — |
| BVDD06 | Local Bus Supply | K7 | — | BV _{DD} | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--------|---------------------------|--------------------|----------|------------------|------|
| BVDD05 | Local Bus Supply | L4 | — | BV _{DD} | — |
| BVDD04 | Local Bus Supply | L7 | — | BV _{DD} | — |
| BVDD03 | Local Bus Supply | M7 | — | BV _{DD} | — |
| BVDD02 | Local Bus Supply | N4 | — | BV _{DD} | — |
| BVDD01 | Local Bus Supply | R4 | — | BV _{DD} | — |
| SVDD17 | SerDes Core Logic Supply | A4 | — | SV _{DD} | — |
| SVDD16 | SerDes Core Logic Supply | A6 | — | SV _{DD} | — |
| SVDD15 | SerDes Core Logic Supply | A10 | — | SV _{DD} | — |
| SVDD14 | SerDes Core Logic Supply | A14 | — | SV _{DD} | — |
| SVDD13 | SerDes Core Logic Supply | A18 | — | SV _{DD} | — |
| SVDD12 | SerDes Core Logic Supply | A22 | — | SV _{DD} | — |
| SVDD11 | SerDes Core Logic Supply | B2 | — | SV _{DD} | — |
| SVDD10 | SerDes Core Logic Supply | B3 | — | SV _{DD} | — |
| SVDD09 | SerDes Core Logic Supply | B8 | — | SV _{DD} | — |
| SVDD08 | SerDes Core Logic Supply | B12 | — | SV _{DD} | — |
| SVDD07 | SerDes Core Logic Supply | B16 | — | SV _{DD} | — |
| SVDD06 | SerDes Core Logic Supply | B20 | — | SV _{DD} | — |
| SVDD05 | SerDes Core Logic Supply | C17 | — | SV _{DD} | — |
| SVDD04 | SerDes Core Logic Supply | D1 | — | SV _{DD} | — |
| SVDD03 | SerDes Core Logic Supply | E4 | — | SV _{DD} | — |
| SVDD02 | SerDes Core Logic Supply | F2 | — | SV _{DD} | — |
| SVDD01 | SerDes Core Logic Supply | H1 | — | SV _{DD} | — |
| XVDD12 | SerDes Transceiver Supply | C4 | — | XV _{DD} | — |
| XVDD11 | SerDes Transceiver Supply | C9 | — | XV _{DD} | — |
| XVDD10 | SerDes Transceiver Supply | C13 | — | XV _{DD} | — |
| XVDD09 | SerDes Transceiver Supply | C19 | — | XV _{DD} | — |
| XVDD08 | SerDes Transceiver Supply | D7 | — | XV _{DD} | — |
| XVDD07 | SerDes Transceiver Supply | D11 | — | XV _{DD} | — |
| XVDD06 | SerDes Transceiver Supply | D15 | — | XV _{DD} | — |
| XVDD05 | SerDes Transceiver Supply | D21 | — | XV _{DD} | — |
| XVDD04 | SerDes Transceiver Supply | E22 | — | XV _{DD} | — |
| XVDD03 | SerDes Transceiver Supply | F5 | — | XV _{DD} | — |
| XVDD02 | SerDes Transceiver Supply | G4 | — | XV _{DD} | — |
| XVDD01 | SerDes Transceiver Supply | H6 | — | XV _{DD} | — |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|-------------|------------------------------------|--------------------|----------|-----------------------|------|
| LVDD05 | Ethernet Controller 1 and 2 Supply | C26 | — | LV _{DD} | — |
| LVDD04 | Ethernet Controller 1 and 2 Supply | E26 | — | LV _{DD} | — |
| LVDD03 | Ethernet Controller 1 and 2 Supply | G20 | — | LV _{DD} | — |
| LVDD02 | Ethernet Controller 1 and 2 Supply | H20 | — | LV _{DD} | — |
| LVDD01 | Ethernet Controller 1 and 2 Supply | J20 | — | LV _{DD} | — |
| POVDD | Fuse Programming Override Supply | U21 | — | POV _{DD} | 30 |
| VDD_CA_PL78 | Core Group A and Platform Supply | G9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL77 | Core Group A and Platform Supply | G11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL76 | Core Group A and Platform Supply | G13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL75 | Core Group A and Platform Supply | G15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL74 | Core Group A and Platform Supply | G17 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL73 | Core Group A and Platform Supply | G19 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL72 | Core Group A and Platform Supply | H9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL71 | Core Group A and Platform Supply | H11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL70 | Core Group A and Platform Supply | H13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL69 | Core Group A and Platform Supply | H15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL68 | Core Group A and Platform Supply | H17 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL67 | Core Group A and Platform Supply | H19 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL66 | Core Group A and Platform Supply | J9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL65 | Core Group A and Platform Supply | J11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL64 | Core Group A and Platform Supply | J13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL63 | Core Group A and Platform Supply | J15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL62 | Core Group A and Platform Supply | J17 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL61 | Core Group A and Platform Supply | J19 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL60 | Core Group A and Platform Supply | K9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL59 | Core Group A and Platform Supply | K11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL58 | Core Group A and Platform Supply | K13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL57 | Core Group A and Platform Supply | K15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL56 | Core Group A and Platform Supply | K17 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL55 | Core Group A and Platform Supply | K19 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL54 | Core Group A and Platform Supply | L9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL53 | Core Group A and Platform Supply | L11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL52 | Core Group A and Platform Supply | L13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL51 | Core Group A and Platform Supply | L15 | — | V _{DD_CA_PL} | 37 |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|-------------|----------------------------------|--------------------|----------|-----------------------|------|
| VDD_CA_PL50 | Core Group A and Platform Supply | L17 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL49 | Core Group A and Platform Supply | L19 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL48 | Core Group A and Platform Supply | M9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL47 | Core Group A and Platform Supply | M11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL46 | Core Group A and Platform Supply | M13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL45 | Core Group A and Platform Supply | M15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL44 | Core Group A and Platform Supply | M17 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL43 | Core Group A and Platform Supply | M19 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL42 | Core Group A and Platform Supply | N9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL41 | Core Group A and Platform Supply | N11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL40 | Core Group A and Platform Supply | N13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL39 | Core Group A and Platform Supply | N15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL38 | Core Group A and Platform Supply | N17 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL37 | Core Group A and Platform Supply | N19 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL36 | Core Group A and Platform Supply | P9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL35 | Core Group A and Platform Supply | P11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL34 | Core Group A and Platform Supply | P13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL33 | Core Group A and Platform Supply | P15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL32 | Core Group A and Platform Supply | P17 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL31 | Core Group A and Platform Supply | P19 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL30 | Core Group A and Platform Supply | R9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL29 | Core Group A and Platform Supply | R11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL28 | Core Group A and Platform Supply | R13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL27 | Core Group A and Platform Supply | R15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL26 | Core Group A and Platform Supply | R17 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL25 | Core Group A and Platform Supply | R19 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL24 | Core Group A and Platform Supply | T9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL23 | Core Group A and Platform Supply | T11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL22 | Core Group A and Platform Supply | T13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL21 | Core Group A and Platform Supply | T15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL20 | Core Group A and Platform Supply | T17 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL19 | Core Group A and Platform Supply | T19 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL18 | Core Group A and Platform Supply | U9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL17 | Core Group A and Platform Supply | U11 | — | V _{DD_CA_PL} | 37 |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|-------------|-----------------------------------|--------------------|----------|-----------------------|------|
| VDD_CA_PL16 | Core Group A and Platform Supply | U13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL15 | Core Group A and Platform Supply | U15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL14 | Core Group A and Platform Supply | U20 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL13 | Core Group A and Platform Supply | V9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL12 | Core Group A and Platform Supply | V11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL11 | Core Group A and Platform Supply | V13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL10 | Core Group A and Platform Supply | V15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL09 | Core Group A and Platform Supply | W9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL08 | Core Group A and Platform Supply | W11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL07 | Core Group A and Platform Supply | W13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL06 | Core Group A and Platform Supply | W15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL05 | Core Group A and Platform Supply | Y9 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL04 | Core Group A and Platform Supply | Y11 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL03 | Core Group A and Platform Supply | Y13 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL02 | Core Group A and Platform Supply | Y15 | — | V _{DD_CA_PL} | 37 |
| VDD_CA_PL01 | Core Group A and Platform Supply | AA21 | — | V _{DD_CA_PL} | 37 |
| VDD_CB11 | Core Group B Supply | U16 | — | V _{DD_CB} | 37 |
| VDD_CB10 | Core Group B Supply | U18 | — | V _{DD_CB} | 37 |
| VDD_CB09 | Core Group B Supply | V18 | — | V _{DD_CB} | 37 |
| VDD_CB08 | Core Group B Supply | V20 | — | V _{DD_CB} | 37 |
| VDD_CB07 | Core Group B Supply | W16 | — | V _{DD_CB} | 37 |
| VDD_CB06 | Core Group B Supply | W18 | — | V _{DD_CB} | 37 |
| VDD_CB05 | Core Group B Supply | W20 | — | V _{DD_CB} | 37 |
| VDD_CB04 | Core Group B Supply | Y18 | — | V _{DD_CB} | 37 |
| VDD_CB03 | Core Group B Supply | Y20 | — | V _{DD_CB} | 37 |
| VDD_CB02 | Core Group B Supply | AA18 | — | V _{DD_CB} | 37 |
| VDD_CB01 | Core Group B Supply | AA20 | — | V _{DD_CB} | 37 |
| VDD_LP | Low Power Security Monitor Supply | L20 | — | V _{DD_LP} | 25 |
| AVDD_CC1 | Core Cluster PLL1 Supply | V7 | — | — | 13 |
| AVDD_CC2 | Core Cluster PLL2 Supply | W22 | — | — | 13 |
| AVDD_PLAT | Platform PLL Supply | V22 | — | — | 13 |
| AVDD_DDR | DDR PLL Supply | W6 | — | — | 13 |
| AVDD_SRDS1 | SerDes PLL1 Supply | C1 | — | — | 13 |
| AVDD_SRDS2 | SerDes PLL2 Supply | A17 | — | — | 13 |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---------------------------|--|--------------------|----------|--|------|
| SENSEVDD_CA_PL | Core Group A and Platform Vdd Sense | H8 | — | — | 8 |
| SENSEVDD_CB | Core Group B Vdd Sense | AB16 | — | — | 8 |
| USB1_VDD_3P3 | USB1 PHY Transceiver 3.3 V Supply | M23 | — | — | — |
| USB2_VDD_3P3 | USB2 PHY Transceiver 3.3 V Supply | J23 | — | — | — |
| USB1_VDD_1P0 | USB1 PHY PLL 1.0 V Supply | L22 | — | — | — |
| USB2_VDD_1P0 | USB2 PHY PLL 1.0 V Supply | K22 | — | — | — |
| Analog Signals | | | | | |
| MVREF | SSTL_1.5/1.35 Reference Voltage | W7 | I | $GV_{DD}/2$ | — |
| SD_IMP_CAL_TX | SerDes Tx Impedance Calibration | E21 | I | 200Ω ($\pm 1\%$) to XV_{DD} | 21 |
| SD_IMP_CAL_RX | SerDes Rx Impedance Calibration | F7 | I | 200Ω ($\pm 1\%$) to SV_{DD} | 22 |
| TEMP_ANODE | Temperature Diode Anode | V5 | — | internal diode | 9 |
| TEMP_CATHODE | Temperature Diode Cathode | U6 | — | internal diode | 9 |
| USB2_IBIAS_REXT | USB PHY2 Reference Bias Current Generation | K23 | — | GND | 32 |
| USB1_IBIAS_REXT | USB PHY1 Reference Bias Current Generation | L23 | — | GND | 32 |
| USB2_VDD_1P8_DECAP | USB2 PHY 1.8 V Output to External Decap | K24 | — | GND | 33 |
| USB1_VDD_1P8_DECAP | USB1 PHY 1.8 V Output to External Decap | L24 | — | GND | 33 |
| No Connection Pins | | | | | |
| NC03 | No Connection | W4 | — | — | 11 |
| NC04 | No Connection | W3 | — | — | 11 |
| NC05 | No Connection | W1 | — | — | 11 |
| NC06 | No Connection | H7 | — | — | 11 |
| NC07 | No Connection | G7 | — | — | 11 |
| NC08 | No Connection | F20 | — | — | 11 |
| NC09 | No Connection | F19 | — | — | 11 |
| NC10 | No Connection | F18 | — | — | 11 |
| NC11 | No Connection | F16 | — | — | 11 |
| NC12 | No Connection | F13 | — | — | 11 |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|----------------------|--------------------|--------------------|----------|--------------|------|
| NC13 | No Connection | F12 | — | — | 11 |
| NC14 | No Connection | F11 | — | — | 11 |
| NC15 | No Connection | F10 | — | — | 11 |
| NC16 | No Connection | F9 | — | — | 11 |
| NC17 | No Connection | F8 | — | — | 11 |
| NC18 | No Connection | E20 | — | — | 11 |
| NC19 | No Connection | E19 | — | — | 11 |
| NC20 | No Connection | E18 | — | — | 11 |
| NC21 | No Connection | E16 | — | — | 11 |
| NC22 | No Connection | E15 | — | — | 11 |
| NC23 | No Connection | E14 | — | — | 11 |
| NC24 | No Connection | E13 | — | — | 11 |
| NC25 | No Connection | E12 | — | — | 11 |
| NC26 | No Connection | E11 | — | — | 11 |
| NC27 | No Connection | E10 | — | — | 11 |
| NC28 | No Connection | E9 | — | — | 11 |
| NC29 | No Connection | E8 | — | — | 11 |
| NC30 | No Connection | E7 | — | — | 11 |
| NC31 | No Connection | D22 | — | — | 11 |
| NC32 | No Connection | D6 | — | — | 11 |
| NC33 | No Connection | D5 | — | — | 11 |
| NC34 | No Connection | C22 | — | — | 11 |
| NC35 | No Connection | C6 | — | — | 11 |
| NC_M21 | No Connection | M21 | — | — | 11 |
| Reserved Pins | | | | | |
| Reserve | — | F24 | — | 1.2 V | 20 |
| Reserve | — | E23 | — | 1.2 V | 20 |
| Reserve | — | E5 | — | — | 11 |
| Reserve | — | E6 | — | — | 11 |
| Reserve | — | F14 | — | — | 11 |
| Reserve | — | F15 | — | — | 11 |
| Reserve | — | AB17 | — | GND | 19 |
| Reserve | — | AB18 | — | GND | 19 |
| Reserve | — | AB19 | — | GND | 19 |

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|---------|--------------------|--------------------|----------|--------------|------|
| Reserve | — | AB20 | — | GND | 19 |

Note:

1. Recommend that a weak pull-up resistor (2–10 k Ω) be placed on this pin to OV_{DD} .
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k Ω resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, then a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend that a weak pull-up resistor (2–10 k Ω) be placed on this pin to BV_{DD} in order to ensure no random chip select assertion due to possible noise, etc.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
8. These pins are connected to the corresponding power and ground nets internally. They may be connected as a differential pair to be used by the voltage regulators with remote sense function. For Rev1.1 silicon, the better solution is to use the far sense pins relative to the power supply location, the other pair can be left as no connected. The DC power simulation should be done during the board layout process to approve the selected solution.
9. These pins may be connected to a thermal diode monitoring device such as the ADT7461A. If a thermal diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.
10. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
11. Do not connect.
12. These are test signals for factory use only and must be pulled low (1 K Ω –2 k Ω) to ground (GND) for normal machine operation.
13. Independent supplies derived from board $V_{DD_CA_CB_PL}$ (core clusters, platform, DDR) or SV_{DD} (SerDes).
14. Recommend that a pull-up resistor (1 K Ω) be placed on this pin to OV_{DD} if I²C interface is used.
15. This pin requires an external 1 K Ω pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR3 and DDR3L, $Dn_MDIC[0]$ is grounded through an 20- Ω (full-strength mode) or 40.2- Ω (half-strength mode) precision 1% resistor and $Dn_MDIC[1]$ is connected to GV_{DD} through an 20- Ω (full-strength mode) or 40.2- Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 and DDR3L I/Os.
17. These pins must be pulled up to 1.2 V through a 180 $\Omega \pm 1\%$ resistor for EM2_MDC and a 330 $\Omega \pm 1\%$ resistor for EM2_MDIO.
18. Pin has a weak internal pull-up.
19. These pins must be pulled to ground (GND).
20. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
21. This pin requires a 200- Ω pull-up to XV_{DD} .
22. This pin requires a 200- Ω pull-up to SV_{DD} .
23. This GPIO pin is on LV_{DD} power plane, not OV_{DD} .
24. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.
25. See [Section 3.6, “Connection Recommendations,”](#) for additional details on this signal.

Table 1. Pin List by Bus (continued)

| Signal | Signal Description | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|--------------------|----------|--------------|------|
|--------|--------------------|--------------------|----------|--------------|------|

26. For reduced core (core 2 and 3 disabled) mode, this signal must be pulled high (100 Ω –1 k Ω) to OVDD.
27. Warning, incorrect voltage select settings can lead to irreversible device damage. This pin has an internal 2 k Ω pull-down resistor, to pull it high, a pull-up resistor of less than 1 k Ω to OVDD should be used. See [Section 3.2, “Supply Power Default Setting.”](#)
28. SDHC_DAT[4:7] require $V_{DD} = 3.3$ V when muxed extended SDHC data signals are enabled via the RCW[SPI] field.
29. The *cfg_xvdd_sel* (LA[26]) reset configuration pin must select the correct voltage that is being supplied on the XVDD pin. Incorrect voltage select settings can lead to irreversible device damage.
30. See [Section 2.2, “Power Up Sequencing,”](#) and [Section 5, “Security Fuse Processor,”](#) for additional details on this signal.
31. Pin must NOT be pulled down during power-on reset.
32. This pin must be connected to GND through a 10 k Ω \pm 0.1% resistor for bias generation.
33. A 1 μ F to 1.5 μ F capacitor connected to GND is required on this signal. [Section 3.6.4.2, “USBn_VDD_1P8_DECAP Capacitor Options,”](#) provides a list of recommended capacitors.
34. A divider network is required on this signal. See [Section 3.6.4.1, “USB Divider Network.”](#)
35. These are test signals for factory use only and must be pulled up (100 Ω –1 k Ω) to OVDD for normal machine operation.
36. For systems which boot from Local Bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull-up on LGPL4 is required.
37. Core Group A and Platform supply ($V_{DD_CA_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but they are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section describes the ratings, conditions, and other electrical characteristics.

2.1.1 Absolute Maximum Ratings

Table 2. Absolute Operating Conditions¹

| Parameter | Symbol | Max Value | Unit | Note |
|--|----------------------|--------------|------|-------|
| Core Group A (cores 0–1) and platform supply voltage (Silicon Rev 1.0) | $V_{DD_CA_PL}$ | –0.3 to 1.1 | V | 9, 10 |
| Core Group B (cores 2–3) supply voltage (Silicon Rev 1.0) | V_{DD_CB} | –0.3 to 1.1 | V | 9, 10 |
| Core Group A (cores 0–1), Core Group B (cores 2–3) and platform supply voltage (Silicon Rev 1.1) | $V_{DD_CA_CB_PL}$ | –0.3 to 1.1 | V | 9, 10 |
| PLL supply voltage (core, platform, DDR) | AV_{DD} | –0.3 to 1.1 | V | — |
| PLL supply voltage (SerDes, filtered from SV_{DD}) | AV_{DD_SRDS} | –0.3 to 1.1 | V | — |
| Fuse programming override supply | POV_{DD} | –0.3 to 1.65 | V | 1 |
| DUART, I ² C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage | OV_{DD} | –0.3 to 3.63 | V | — |

Table 2. Absolute Operating Conditions¹ (continued)

| Parameter | | Symbol | Max Value | Unit | Note |
|--|--|--------------------|--|------|------|
| eSPI, eSHDC, GPIO | | CV_{DD} | -0.3 to 3.63 -0.3 to 2.75 -0.3 to 1.98 | V | — |
| DDR3 and DDR3L DRAM I/O voltage | | GV_{DD} | -0.3 to 1.65 | V | — |
| Enhanced local bus I/O voltage | | BV_{DD} | -0.3 to 3.63 -0.3 to 2.75 -0.3 to 1.98 | V | — |
| SerDes core logic supply and receivers | | SV_{DD} | -0.3 to 1.1 | V | — |
| Pad power supply for SerDes transceivers | | XV_{DD} | -0.3 to 1.98 -0.3 to 1.65 | V | — |
| Ethernet I/O, Ethernet management interface 1 (EMI1), 1588, GPIO | | LV_{DD} | -0.3 to 3.63 -0.3 to 2.75 | V | 3 |
| USB PHY transceiver supply voltage | | $USB_V_{DD_3P3}$ | -0.3 to 3.63 | V | — |
| USB PHY PLL supply voltage | | $USB_V_{DD_1P0}$ | -0.3 to 1.1 | V | — |
| Low Power Security Monitor Supply | | V_{DD_LP} | -0.3 to 1.1 | V | — |
| Input voltage ⁷ | DDR3 and DDR3L DRAM signals | MV_{IN} | -0.3 to ($GV_{DD} + 0.3$) | V | 2, 7 |
| | DDR3 and DDR3L DRAM reference | MV_{REF}^n | -0.3 to ($GV_{DD}/2 + 0.3$) | V | 2, 7 |
| | Ethernet signals, GPIO | LV_{IN} | -0.3 to ($LV_{DD} + 0.3$) | V | 3, 7 |
| | eSPI, eSHDC, GPIO | CV_{IN} | -0.3 to ($CV_{DD} + 0.3$) | V | 4, 7 |
| | Enhanced local bus signals | BV_{IN} | -0.3 to ($BV_{DD} + 0.3$) | V | 5, 7 |
| | DUART, I ² C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage | OV_{IN} | -0.3 to ($OV_{DD} + 0.3$) | V | 6, 7 |
| | SerDes signals | XV_{IN} | -0.4 to ($XV_{DD} + 0.3$) | V | 7 |
| | USB PHY transceiver signals | $USB_V_{IN_3P3}$ | -0.3 to ($USB_V_{DD_3P3} + 0.3$) | V | 7 |
| Storage junction temperature range | | T_{stg} | -55 to 150 | °C | — |

Table 2. Absolute Operating Conditions¹ (continued)

| Parameter | Symbol | Max Value | Unit | Note |
|-----------|--------|-----------|------|------|
|-----------|--------|-----------|------|------|

Note:

- Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only; functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- (C,X,B,G,L,O) V_{IN} may overshoot (for V_{IH}) or undershoot (for V_{IL}) to the voltages and maximum duration shown in Figure 7.
- Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
- Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
- Core Group A and Platform supply ($V_{DD_CA_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

| Parameter | Symbol | Recommended Value | Unit | Note |
|--|----------------------|---|------|------|
| Core Group A (cores 0–1) and platform supply voltage (Silicon Rev 1.0) | $V_{DD_CA_PL}$ | 1.0 ± 50 mV | V | 4, 5 |
| Core Group B (cores 2–3) supply voltage (Silicon Rev 1.0) | V_{DD_CB} | 1.0 ± 50 mV | V | 4, 5 |
| Core Group A (cores 0–1), Core Group B (cores 2–3) and platform supply voltage (Silicon Rev 1.1) | $V_{DD_CA_CB_PL}$ | 1.0 ± 50 mV | V | 4, 5 |
| PLL supply voltage (core, platform, DDR) | AV_{DD} | 1.0 ± 50 mV | V | — |
| PLL supply voltage (SerDes) | AV_{DD_SRDS} | 1.0 ± 50 mV | V | — |
| Fuse programming override supply | POV_{DD} | 1.5 ± 75 mV | V | 2 |
| DUART, I ² C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage | OV_{DD} | 3.3 ± 165 mV | V | — |
| eSPI, eSDHC, GPIO | CV_{DD} | 3.3 ± 165 mV 2.5 ± 125 mV 1.8 ± 90 mV | V | — |
| DDR DRAM I/O voltage | GV_{DD} | 1.5 ± 75 mV 1.35 ± 67 mV | V | — |
| | DDR3 DDR3L | | | |

Electrical Characteristics

Table 3. Recommended Operating Conditions (continued)

| Parameter | | Symbol | Recommended Value | Unit | Note |
|--|--|--------------------|---|---|------|
| Enhanced local bus I/O voltage | | BV_{DD} | 3.3 ± 165 mV 2.5 ± 125 mV 1.8 ± 90 mV | V | — |
| SerDes core logic supply and transceivers | | SV_{DD} | 1.0 ± 50 mV | V | — |
| Pad power supply for SerDes transceivers | | XV_{DD} | 1.8 ± 90 mV 1.5 ± 75 mV | V | — |
| Ethernet I/O, Ethernet management interface 1 (EMI1), 1588, GPIO | | LV_{DD} | 3.3 ± 165 mV 2.5 ± 125 mV | V | 3 |
| USB PHY transceiver supply voltage | | $USB_V_{DD_3P3}$ | 3.3 ± 165 mV | V | — |
| USB PHY PLL supply voltage | | $USB_V_{DD_1P0}$ | 1.0 ± 50 mV | V | — |
| Low Power Security Monitor Supply | | V_{DD_LP} | 1.0 ± 50 mV | V | — |
| Input voltage | DDR3 and DDR3L DRAM signals | MV_{IN} | GND to GV_{DD} | V | — |
| | DDR3 and DDR3L DRAM reference | MV_{REF} | $GV_{DD}/2 \pm 1\%$ | V | — |
| | Ethernet signals, GPIO | LV_{IN} | GND to LV_{DD} | V | — |
| | eSPI, eSHDC, GPIO | CV_{IN} | GND to CV_{DD} | V | — |
| | Enhanced Local Bus signals | BV_{IN} | GND to BV_{DD} | V | — |
| | DUART, I ² C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage | OV_{IN} | GND to OV_{DD} | V | — |
| | SerDes signals | XV_{IN} | GND to XV_{DD} | V | — |
| | USB PHY Transceiver signals | $USB_V_{IN_3P3}$ | GND to $USB_V_{DD_3P3}$ | V | — |
| | Operating Temperature range | Normal Operation | T_A , T_J | $T_A = 0$ (min) to $T_J = 105$ (max) | °C |
| Extended Operation | | T_A , T_J | $T_A = -40$ (min) to $T_J = 105$ (max) | °C | — |
| Secure Boot Fuse Programming | | T_A , T_J | $T_A = 0$ (min) to $T_J = 70$ (max) | °C | 1 |

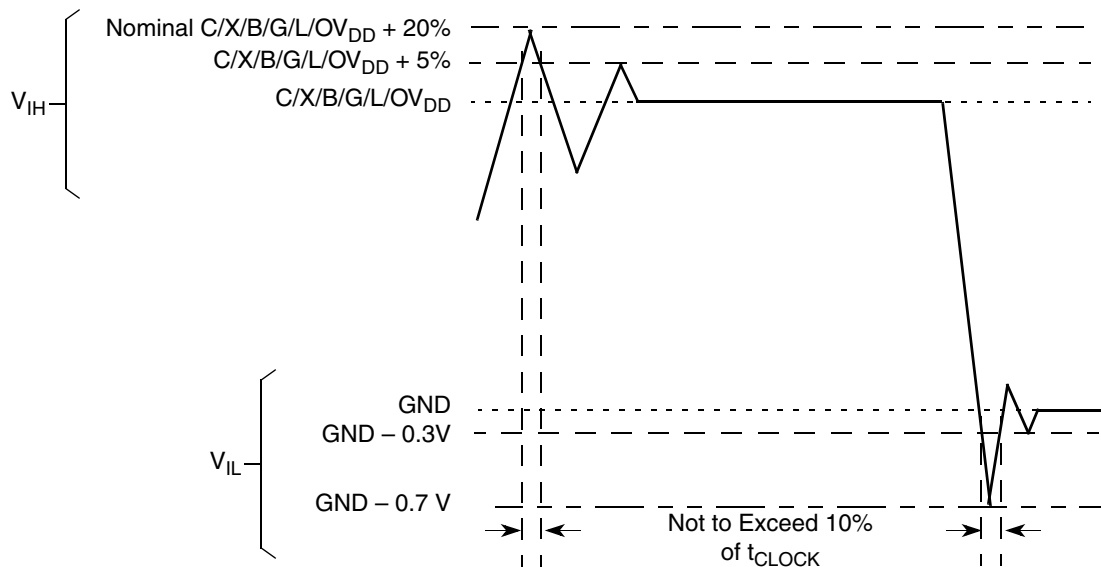
Table 3. Recommended Operating Conditions (continued)

| Parameter | Symbol | Recommended Value | Unit | Note |
|-----------|--------|-------------------|------|------|
|-----------|--------|-------------------|------|------|

Note:

1. POV_{DD} must be supplied 1.5 V and the device must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power Up Sequencing."
2. Selecting RGMII limits LV_{DD} to 2.5 V.
3. Unless otherwise stated in an interface's DC specifications, the maximum allowed input capacitance in this table is a general recommendation for signals.
4. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
5. Core Group A and Platform supply ($V_{DD_CA_PL}$) and Core Group B supply (V_{DD_CB}) were separate supplies in Rev1.0, they are tied together in Rev1.1.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.

**Notes:**

t_{CLOCK} refers to the clock period associated with the respective interface:

- For I^2C , t_{CLOCK} refers to $SYSCLK$.
- For DDR GV_{DD} , t_{CLOCK} refers to Dn_MCK .
- For eSPI CV_{DD} , t_{CLOCK} refers to SPI_CLK .
- For eLBC BV_{DD} , t_{CLOCK} refers to $LCLK$.
- For SerDes XV_{DD} , t_{CLOCK} refers to SD_REF_CLK .
- For dTSEC LV_{DD} , t_{CLOCK} refers to EC_GTX_CLK125 .
- For JTAG OV_{DD} , t_{CLOCK} refers to TCK .

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}$

The core and platform voltages must always be provided at nominal 1.0 V. See Table 3 for the actual recommended core voltage conditions. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. CV_{DD} , BV_{DD} , OV_{DD} , and LV_{DD} -based receivers are simple CMOS I/O circuits and satisfy appropriate LVC MOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied MV_{REF}^n signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.5/SSTL_1.35 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output Driver Characteristics

This table provides information about the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

| Driver Type | Output Impedance (Ω) | (Nominal) Supply Voltage | Note |
|---------------------------------------|--|--|------|
| Local Bus interface utilities signals | 45 45 45 | $BV_{DD} = 3.3\text{ V}$ $BV_{DD} = 2.5\text{ V}$ $BV_{DD} = 1.8\text{ V}$ | — |
| DDR3 signal | 20 (full-strength mode) 40 (half-strength mode) | $GV_{DD} = 1.5\text{ V}$ | 1 |
| DDR3L signal | 20 (full-strength mode) 40 (half-strength mode) | $GV_{DD} = 1.35\text{ V}$ | 1 |
| eTSEC/10/100 signals | 45 45 | $LV_{DD} = 3.3\text{ V}$ $LV_{DD} = 2.5\text{ V}$ | — |
| DUART, system control, JTAG | 45 | $OV_{DD} = 3.3\text{ V}$ | — |
| I ² C | 45 | $OV_{DD} = 3.3\text{ V}$ | — |
| eSPI, eSDHC | 45 45 45 | $CV_{DD} = 3.3\text{ V}$ $CV_{DD} = 2.5\text{ V}$ $CV_{DD} = 1.8\text{ V}$ | — |

Note:

1. The drive strength of the DDR3 or DDR3L interface in half-strength mode is at $T_j = 105\text{ }^\circ\text{C}$ and at GV_{DD} (min).

2.2 Power Up Sequencing

The device requires that its power rails be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. Bring up OV_{DD} , LV_{DD} , BV_{DD} , CV_{DD} , and $USB_V_{DD_3P3}$. Drive $POV_{DD} = \text{GND}$.
 - $\overline{\text{PORESET}}$ input must be driven asserted and held during this step.
 - IO_VSEL inputs must be driven during this step and held stable during normal operation.
 - $USB_V_{DD_3P3}$ rise time (10% to 90%) has a minimum of 350 μs .
2. Bring up $V_{DD_CA_CB_PL}$, SV_{DD} , AV_{DD} (cores, platform, SerDes) and $USB_V_{DD_1P0}$. $V_{DD_CA_CB_PL}$ and $USB_V_{DD_1P0}$ must be ramped up simultaneously.
3. Bring up GV_{DD} (DDR) and XV_{DD} .
4. Negate $\overline{\text{PORESET}}$ input as long as the required assertion/hold time has been met per [Table 17](#).
5. For secure boot fuse programming: After negation of $\overline{\text{PORESET}}$, drive $POV_{DD} = 1.5\text{ V}$ after a required minimum delay per [Table 5](#). After fuse programming is completed, it is required to return $POV_{DD} = \text{GND}$ before the system is power cycled ($\overline{\text{PORESET}}$ assertion) or powered down ($V_{DD_CA_CB_PL}$ ramp down) per the required timing specified in [Table 5](#). See [Section 5](#), “Security Fuse Processor,” for additional details.

WARNING

Only two secure boot fuse programming events are permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while $POV_{DD} = \text{GND}$.

While VDD is ramping, current may be supplied from VDD through the chip to GVDD. Nevertheless, GVDD from an external supply should follow the sequencing described above.

WARNING

Only 100,000 POR cycles are permitted per lifetime of a device.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

This figure provides the POV_{DD} timing diagram.

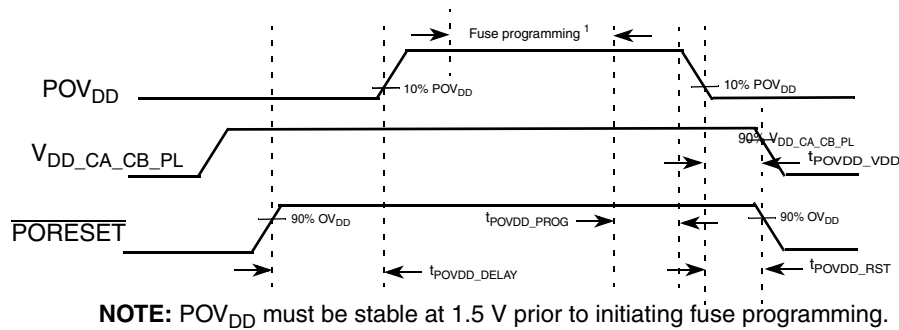


Figure 8. POV_{DD} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD} .

Table 5. POV_{DD} Timing⁵

| Driver Type | Min | Max | Unit | Note |
|--------------------|-----|-----|---------|------|
| t_{POVDD_DELAY} | 100 | — | SYSCLKs | 1 |
| t_{POVDD_PROG} | 0 | — | μ s | 2 |
| t_{POVDD_VDD} | 0 | — | μ s | 3 |
| t_{POVDD_RST} | 0 | — | μ s | 4 |

Note:

1. Delay required from the negation of $\overline{PORESET}$ to driving POV_{DD} ramp up. Delay measured from $\overline{PORESET}$ negation at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while $POV_{DD} = GND$. After fuse programming is completed, it is required to return $POV_{DD} = GND$.
3. Delay required from POV_{DD} ramp down complete to $V_{DD_CA_CB_PL}$ ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before $V_{DD_CA_CB_PL}$ is at 90% V_{DD} .
4. Delay required from POV_{DD} ramp down complete to $\overline{PORESET}$ assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before $\overline{PORESET}$ assertion reaches 90% OV_{DD} .
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

To guarantee MCKE low during power up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, the sequencing for GV_{DD} is not required.

WARNING

Incorrect voltage select settings can lead to irreversible device damage. See [Section 3.2](#), “Supply Power Default Setting.”

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the $V_{DD_CA_CB_PL}$ supplies, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power Down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per [Section 2.2](#), “Power Up Sequencing,” it is required that $POV_{DD} = GND$ before the system is power cycled (PORESET assertion) or powered down ($V_{DD_CA_CB_PL}$ ramp down) per the required timing specified in [Table 5](#).

$V_{DD_CA_CB_PL}$ and $USB_V_{DD_1P0}$ must be ramped down simultaneously. $USB_V_{DD_1P8_DECAP}$ should start ramping down only after $USB_V_{DD_3P3}$ is below 1.65 V.

2.4 Power Characteristics

This table shows the power dissipations of the $V_{DD_CA_CB_PL}$ supply for various operating platform clock frequencies versus the core and DDR clock frequencies.

Table 6. Device Power Dissipation

| Power Mode | Core Freq (MHz) | Plat Freq (MHz) | DDR Data Rate (MT/s) | FM Freq (MHz) | $V_{DD_CA_CB_PL}$ (V) | Junction Temp (°C) | Core & Platform Power ¹ (W) | $V_{DD_CA_CB_PL}$ Power (W) | Core & Platform Power ¹ (W) | $V_{DD_CA_CB_PL}$ Power (W) | SV _{DD} Power (W) | Note |
|------------|-----------------|-----------------|----------------------|---------------|--------------------------|--------------------|--|--------------------------------|--|--------------------------------|----------------------------|------|
| | | | | | | | Quad Cores | | Dual Cores | | | |
| Typical | 1200 | 600 | 1200 | 500 | 1.0 | 65 | 10.3 | — | 9.8 | — | — | 2, 3 |
| Thermal | | | | | | 105 | 14.2 | — | 13.8 | — | — | 5, 7 |
| Maximum | | | | | | 14.8 | 13.5 | 14.0 | 12.8 | 1.4 | 4, 6, 7 | |
| Typical | 1000 | 533 | 1067 | 467 | 1.0 | 65 | 9.2 | — | 8.6 | — | — | 2, 3 |
| Thermal | | | | | | 105 | 12.5 | — | 12.1 | — | — | 5, 7 |
| Maximum | | | | | | 13.0 | 11.7 | 12.3 | 11.0 | 1.4 | 4, 6, 7 | |
| Typical | 800 | 534 | 1067 | 467 | 1.0 | 65 | 9.0 | — | 8.4 | — | — | 2, 3 |
| Thermal | | | | | | 105 | 12.2 | — | 12.0 | — | — | 5, 7 |
| Maximum | | | | | | 12.6 | 11.4 | 12.1 | 10.9 | 1.4 | 4, 6, 7 | |

Table 6. Device Power Dissipation (continued)

| Power Mode | Core Freq (MHz) | Plat Freq (MHz) | DDR Data Rate (MT/s) | FM Freq (MHz) | V _{DD_CA_CB_PL} (V) | Junction Temp (°C) | Core & Platform Power ¹ (W) | | V _{DD_CA_CB_PL} Power (W) | | SV _{DD} Power (W) | Note |
|------------|-----------------|-----------------|----------------------|---------------|------------------------------|--------------------|--|------|------------------------------------|------|----------------------------|---------|
| | | | | | | | Quad Cores | | Dual Cores | | | |
| Typical | 667 | 534 | 1067 | 467 | 1.0 | 65 | 8.7 | — | 8.2 | — | — | 2, 3 |
| Thermal | | | | | | 105 | 12.0 | — | 11.8 | — | — | 5, 7 |
| Maximum | | | | | | | 12.3 | 11.1 | 11.9 | 10.6 | 1.4 | 4, 6, 7 |

Note:

1. Combined power of V_{DD_CA_CB_PL}, SV_{DD} with the DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% on all cores and executing DMA on the platform with 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 70% on all four cores, 80% on two cores and executing DMA on the platform with 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the all I/O power supply estimated values.

Table 7. P2040 I/O Power Supply Estimated Values

| Interface | Parameter | Symbol | Typical | Maximum | Unit | Notes |
|--|------------------------------|-------------|---------|---------|------|---------|
| DDR3 64 Bits Per Controller | 667 MT/s data rate | GVdd (1.5V) | 0.705 | 1.764 | W | 1,2,5,6 |
| | 800 MT/s data rate | | 0.714 | 1.785 | | |
| | 1066 MT/s data rate | | 0.731 | 1.827 | | |
| | 1200 MT/s data rate | | 0.739 | 1.848 | | |
| | 1333 MT/s data rate | | 0.747 | 1.869 | | |
| HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI | x1, 1.25 G-baud | XVdd (1.5V) | 0.078 | 0.087 | W | 1, 7 |
| | x2, 1.25 G-baud | | 0.119 | 0.134 | | |
| | x4, 1.25 G-baud | | 0.202 | 0.226 | | |
| | x8, 1.25 G-baud | | 0.367 | 0.411 | | |
| | x1, 2.5/3.0/3.125/5.0 G-baud | | 0.088 | 0.099 | | |
| | x2, 2.5/3.0/3.125/5.0 G-baud | | 0.139 | 0.156 | | |
| | x4, 2.5/3.0/3.125/5.0 G-baud | | 0.241 | 0.270 | | |
| | x8, 2.5/3.0/3.125/5.0 G-baud | | 0.447 | 0.501 | | |
| dTSEC Per Controller | RGMII | LVdd (2.5V) | 0.075 | 0.100 | W | 1,3,6 |

Table 7. P2040 I/O Power Supply Estimated Values (continued)

| | | | | | | |
|---|----------------|-------------|-------|-------|---|---------|
| IEEE 1588 | — | LVdd (2.5V) | 0.004 | 0.005 | W | 1,3,6 |
| eLBC | 32-bit, 100Mhz | BVdd (1.8V) | 0.048 | 0.120 | W | 1,3,6 |
| | | BVdd (2.5V) | 0.072 | 0.193 | | |
| | | BVdd (3.3V) | 0.120 | 0.277 | | |
| | 16-bit, 100Mhz | BVdd (1.8V) | 0.021 | 0.030 | W | 1,3,6 |
| | | BVdd (2.5V) | 0.036 | 0.046 | | |
| | | BVdd (3.3V) | 0.057 | 0.076 | | |
| eSDHC | — | Ovdd (3.3V) | 0.014 | 0.150 | W | 1,3,6 |
| eSPI | — | CVdd (1.8V) | 0.004 | 0.005 | W | 1,3,6 |
| | | CVdd (2.5V) | 0.006 | 0.008 | | |
| | | CVdd (3.3V) | 0.010 | 0.013 | | |
| USB | — | USB_Vdd_3P3 | 0.012 | 0.015 | W | 1,3,6 |
| I2C | — | OVdd (3.3V) | 0.002 | 0.003 | W | 1,3,6 |
| DUART | — | OVdd (3.3V) | 0.006 | 0.008 | W | 1,3,6 |
| GPIO | x8 | OVdd (1.8V) | 0.005 | 0.006 | W | 1,3,4,6 |
| | | OVdd (2.5V) | 0.007 | 0.009 | | |
| | | OVdd (3.3V) | 0.009 | 0.011 | | |
| Others (Reset, System Clock, JTAG & Misc) | — | OVdd (3.3V) | 0.003 | 0.015 | W | 1,3,4,6 |

Note:

1. The typical values are estimates and based on simulations at 65 °C.
2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization.
3. Assuming 15 pF total capacitance load.
4. GPIO's are supported on 1.8 V, 2.5 V and 3.3 V rails as specified in the hardware specification.
5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.
6. The maximum values are estimated and they are based on simulations at 105 °C. The values are not intended to be used as the maximum guaranteed current.
7. The total power numbers of XVDD is dependent on customer application use case. This table lists all the SerDes configuration combination possible for the device. To get the XVDD power numbers, the user should add the combined lanes to match to the total SerDes lanes used, not simply multiply the power numbers by the number of lanes.

This table shows the estimated power dissipation on the AV_{DD} and AV_{DD_SRDS} supplies for the device PLLs, at allowable voltage levels.

Table 8. Device AV_{DD} Power Dissipation

| AV_{DDs} | Typical | Maximum | Unit | Note |
|--------------------|---------|---------|------|------|
| AV_{DD_DDR} | 5 | 15 | mW | 1 |
| AV_{DD_CC1} | | | | |
| AV_{DD_CC2} | | | | |
| AV_{DD_PLAT} | | | | |
| AV_{DD_SRDS1} | — | 36 | mW | 2 |
| AV_{DD_SRDS2} | | | | |
| $USB_V_{DD_1P0}$ | — | 10 | mW | 3 |

Note:

- $V_{DD_CA_CB_PL}$, $T_A = 80^\circ\text{C}$, $T_J = 105^\circ\text{C}$
- $SV_{DD} = 1.0\text{ V}$, $T_A = 80^\circ\text{C}$, $T_J = 105^\circ\text{C}$
- $USB_V_{DD_1P0} = 1.0\text{V}$, $T_A = 80^\circ\text{C}$, $T_J = 105^\circ\text{C}$

This table shows the estimated power dissipation on the POV_{DD} supply for the chip at allowable voltage levels.

Table 9. POV_{DD} Power Dissipation

| Supply | Maximum | Unit | Notes |
|------------|---------|------|-------|
| POV_{DD} | 450 | mW | 1 |

Note:

- To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per [Table 3](#).

This table shows the estimated power dissipation on the V_{DD_LP} supply for the device, at allowable voltage levels.

Table 10. V_{DD_LP} Power Dissipation

| Supply | Maximum | Unit | Notes |
|--------------------------------|---------|---------------|-------|
| V_{DD_LP} (Device on, 105C) | 1.5 | mW | 1 |
| V_{DD_LP} (Device off, 70C) | 195 | μW | 2 |
| V_{DD_LP} (Device off, 40C) | 132 | μW | 2 |

Note:

- $V_{DD_LP} = 1.0\text{ V}$, $T_J = 105^\circ\text{C}$.
- When the device is off, V_{DD_LP} may be supplied by battery power to retain the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC, which switches V_{DD_LP} to battery when the SoC is powered down. See the Trust Architecture chapter in the device reference manual for more information.

2.5 Thermal

Table 11. Package Thermal Characteristics ⁶

| Rating | Board | Symbol | Value | Unit | Note |
|---|-------------------------|-----------------|-------|--------------------|------|
| Junction to ambient, natural convection | Single-layer board (1s) | $R_{\theta JA}$ | 21 | $^\circ\text{C/W}$ | 1, 2 |
| Junction to ambient, natural convection | Four-layer board (2s2p) | $R_{\theta JA}$ | 15 | $^\circ\text{C/W}$ | 1, 3 |

Table 11. Package Thermal Characteristics (continued)⁶

| Rating | Board | Symbol | Value | Unit | Note |
|---------------------------------------|-------------------------|--------------------|-------|---------------|------|
| Junction to ambient (at 200 ft./min.) | Single-layer board (1s) | $R_{\theta JMA}$ | 15 | $^{\circ}C/W$ | 1, 2 |
| Junction to ambient (at 200 ft./min.) | Four-layer board (2s2p) | $R_{\theta JMA}$ | 11 | $^{\circ}C/W$ | 1, 2 |
| Junction to board | — | $R_{\theta JB}$ | 6 | $^{\circ}C/W$ | 3 |
| Junction to case top | — | $R_{\theta JCtop}$ | .53 | $^{\circ}C/W$ | 4 |
| Junction to lid top | — | $R_{\theta JClid}$ | .16 | $^{\circ}C/W$ | 5 |

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51–3 and JESD51-6 with the board (JESD51–9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51–8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Junction-to-lid-top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.
6. Reference [Section 3.8, “Thermal Management Information,”](#) for additional details.

2.6 Input Clocks

2.6.1 System Clock (SYSCLK) Timing Specifications

This table shows the SYSCLK DC electrical characteristics.

Table 12. SYSCLK DC Electrical Characteristics ($OV_{DD} = 3.3 V$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|--|----------|-----|---------|-----------|---------|------|
| Input high voltage | V_{IH} | 2.0 | — | — | V | 1 |
| Input low voltage | V_{IL} | — | — | 0.8 | V | 1 |
| Input capacitance | C_{IN} | — | — | 15 | pf | — |
| Input current ($OV_{IN} = 0 V$ or $OV_{IN} = OV_{DD}$) | I_{IN} | — | — | ± 50 | μA | 2 |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in [Table 3](#).
2. The symbol OV_{IN} , in this case, represents the OV_{IN} symbol referenced in [Section 2.1.2, “Recommended Operating Conditions.”](#)

This table shows the SYSCLK AC timing specifications.

Table 13. SYSCLK AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|------------------------------------|-----|-----|------|------|------|
| SYSCLK frequency | f_{SYSCLK} | 67 | — | 133 | MHz | 1, 2 |
| SYSCLK cycle time | t_{SYSCLK} | 7.5 | — | 15 | ns | 1, 2 |
| SYSCLK duty cycle | $t_{\text{KHK}}/t_{\text{SYSCLK}}$ | 40 | — | 60 | % | 2 |
| SYSCLK slew rate | — | 1 | — | 4 | V/ns | 3 |
| SYSCLK peak period jitter | — | — | — | ±150 | ps | — |
| SYSCLK jitter phase noise at – 56dBc | — | — | — | 500 | KHz | 4 |
| AC Input Swing Limits at 3.3 V OV_{DD} | ΔV_{AC} | 1.9 | — | — | V | — |

Note:

- Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency, do not exceed their respective maximum or minimum operating frequencies.
- Measured at the rising edge and/or the falling edge at $OV_{\text{DD}} \div 2$.
- Slew rate as measured from $\pm 0.3 \Delta V_{\text{AC}}$ at center of peak to peak voltage at clock input.
- Phase noise is calculated as FFT of TIE jitter.

2.6.2 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the device input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the device is compatible with spread spectrum sources if the recommendations listed in this table are observed.

Table 14. Spread Spectrum Clock Source Recommendations

For recommended operating conditions, see [Table 3](#).

| Parameter | Min | Max | Unit | Note |
|----------------------|-----|-----|------|------|
| Frequency modulation | — | 60 | kHz | — |
| Frequency spread | — | 1.0 | % | 1, 2 |

Note:

- SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in [Table 13](#).
- Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

2.6.3 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the e500mc; there is no need for jitter specification. The minimum pulse width of the RTC signal must be greater than 16× the period of the platform clock. That is, minimum clock high time is 8× (platform clock), and minimum clock low time is 8× (platform clock). There is no minimum RTC frequency; RTC may be grounded if not needed.

2.6.4 dTSEC Gigabit Ethernet Reference Clock Timing

This table provides the dTSEC gigabit reference clocks DC electrical characteristics.

Table 15. EC_GTX_CLK125 DC Timing Specifications

| Parameter | Symbol | Min | Max | Unit | Note |
|--|----------|-----|-----|------|------|
| High-level input voltage | V_{IH} | 2 | — | V | 1 |
| Low-level input voltage | V_{IL} | — | 0.7 | V | 1 |
| Input current ($LV_{IN} = 0$ V or $LV_{IN} = LV_{DD}$) | I_{IN} | — | ±40 | μA | 2 |

Note:

1. The max V_{IH} , and min V_{IL} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
2. The symbol LV_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 3](#).

This table provides the dTSEC gigabit reference clocks AC timing specifications.

Table 16. EC_GTX_CLK125 AC Timing Specifications

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Note |
|--|-----------------------|-----|---------|-------------|------|------|
| EC_GTX_CLK125 frequency | t_{G125} | — | 125 | — | MHz | — |
| EC_GTX_CLK125 cycle time | t_{G125} | — | 8 | — | ns | — |
| EC_GTX_CLK125 rise and fall time $LV_{DD} = 2.5$ V $LV_{DD} = 3.3$ V | t_{G125R}/t_{G125F} | — | — | 0.75 1.0 | ns | 1 |
| EC_GTX_CLK125 duty cycle 1000Base-T for RGMII | t_{G125H}/t_{G125} | 47 | — | 53 | % | 2 |
| EC_GTX_CLK125 jitter | — | — | — | ± 150 | ps | 2 |

Note:

1. Rise and fall times for EC_GTX_CLK125 are measured from 20% to 80% (rise time) and 80% to 20% (fall time) of LV_{DD} .
2. EC_GTX_CLK125 is used to generate the GTX clock for the dTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the dTSEC GTX_CLK. See [Section 2.12.2.2, “RGMII AC Timing Specifications,”](#) for duty cycle for 10Base-T and 100Base-T reference clock.

2.6.5 Other Input Clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information on the input clock requirements of functional blocks sourced external of the device, such as SerDes, Ethernet Management, eSDHC, Local Bus, see the specific interface section.

2.7 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table provides the RESET initialization AC timing specifications.

Table 17. RESET Initialization Timing Specifications

| Parameter | Min | Max | Unit ¹ | Note |
|--|-----|-----|-------------------|------|
| Required assertion time of $\overline{\text{PORESET}}$ | 1 | — | ms | 3 |
| Required input assertion time of $\overline{\text{HRESET}}$ | 32 | — | SYCLKs | 1, 2 |
| Input setup time for POR configs with respect to negation of $\overline{\text{PORESET}}$ | 4 | — | SYCLKs | 1 |
| Input hold time for all POR configs with respect to negation of $\overline{\text{PORESET}}$ | 2 | — | SYCLKs | 1 |
| Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{PORESET}}$ | — | 5 | SYCLKs | 1 |

Note:

1. SYCLK is the primary clock input for the device.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of $\overline{\text{HRESET}}$ negation is documented in Section 4.4.1, “Power-On Reset Sequence,” in the chip reference manual.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up. Refer to Section 2.2, “Power Up Sequencing.”

Table 18. PLL Lock Times

| Parameter | Min | Max | Unit | Note |
|----------------|-----|-----|------|------|
| PLL lock times | — | 100 | μs | — |

2.8 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 19. Power Supply Ramp Rate

| Parameter | Min | Max | Unit | Note |
|---|-----|-------|------|------|
| Required ramp rate for all voltage supplies (including $\text{OV}_{\text{DD}}/\text{CV}_{\text{DD}}/\text{GV}_{\text{DD}}/\text{BV}_{\text{DD}}/\text{SV}_{\text{DD}}/\text{XV}_{\text{DD}}/\text{LV}_{\text{DD}}$ all V_{DD} supplies, MVREF and all AV_{DD} supplies.) | — | 36000 | V/s | 1, 2 |

Note:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (For example exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.9 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required $\text{GV}_{\text{DD}}(\text{typ})$ voltage is 1.5 V when interfacing to DDR3 SDRAM and $\text{GV}_{\text{DD}}(\text{typ})$ voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.9.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 20. DDR3 SDRAM Interface DC Electrical Characteristics ($GV_{DD} = 1.5\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|-----------------------|-------------|-----------------------|-----------------------|---------------|------------|
| I/O reference voltage | MV_{REFn} | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V | 1, 2, 3, 4 |
| Input high voltage | V_{IH} | $MV_{REFn} + 0.100$ | GV_{DD} | V | 5 |
| Input low voltage | V_{IL} | GND | $MV_{REFn} - 0.100$ | V | 5 |
| I/O leakage current | I_{OZ} | -50 | 50 | μA | 6 |

Note:

- GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
- MV_{REFn} is expected to be equal to $0.5 \times GV_{DD}$ and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REFn} may not exceed the MV_{REFn} DC level by more than $\pm 1\%$ of the DC value (that is, $\pm 15\text{mV}$).
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REFn} with a min value of $MV_{REFn} - 0.04$ and a max value of $MV_{REFn} + 0.04$. V_{TT} should track variations in the DC level of MV_{REFn} .
- The voltage regulator for MV_{REFn} must meet the specifications stated in [Table 23](#).
- Input capacitance load for DQ, DQS, and \overline{DQS} are available in the IBIS models.
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 21. DDR3L SDRAM Interface DC Electrical Characteristics ($GV_{DD} = 1.35\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|--|-------------|-----------------------|-----------------------|---------------|------------|
| I/O reference voltage | MV_{REFn} | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V | 1, 2, 3, 4 |
| Input high voltage | V_{IH} | $MV_{REFn} + 0.090$ | GV_{DD} | V | 5 |
| Input low voltage | V_{IL} | GND | $MV_{REFn} - 0.090$ | V | 5 |
| I/O leakage current | I_{OZ} | -50 | 50 | μA | 6 |
| Output high current ($V_{OUT} = 0.641\text{ V}$) | I_{OH} | — | -23.8 | mA | 7, 8 |
| Output low current ($V_{OUT} = 0.641\text{ V}$) | I_{OL} | 23.8 | — | mA | 7, 8 |

Table 21. DDR3L SDRAM Interface DC Electrical Characteristics ($GV_{DD} = 1.35\text{ V}$) (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|-----------|--------|-----|-----|------|------|
|-----------|--------|-----|-----|------|------|

Note:

- GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
- MV_{REFn} is expected to be equal to $0.5 \times GV_{DD}$ and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REFn} may not exceed the MV_{REFn} DC level by more than $\pm 1\%$ of the DC value (that is, $\pm 13.5\text{ mV}$).
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REFn} with a min value of $MV_{REFn} - 0.04$ and a max value of $MV_{REFn} + 0.04$. V_{TT} should track variations in the DC level of MV_{REFn} .
- The voltage regulator for MV_{REFn} must meet the specifications stated in [Table 23](#).
- Input capacitance load for DQ, DQS, and \overline{DQS} are available in the IBIS models.
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.
- Refer to the IBIS model for the complete output IV curve characteristics.
- I_{OH} and I_{OL} are measured at $GV_{DD} = 1.283\text{ V}$

This table provides the DDR controller interface capacitance for DDR3 and DDR3L.

Table 22. DDR3 and DDR3L SDRAM Capacitance

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|-----------|-----|-----|------|------|
| Input/output capacitance: DQ, DQS, \overline{DQS} | C_{IO} | 6 | 8 | pF | 1, 2 |
| Delta input/output capacitance: DQ, DQS, \overline{DQS} | C_{DIO} | — | 0.5 | pF | 1, 2 |

Note:

- This parameter is sampled. $GV_{DD} = 1.5\text{ V} \pm 0.075\text{ V}$ (for DDR3), $f = 1\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$, $V_{OUT} = GV_{DD} \div 2$, V_{OUT} (peak-to-peak) = 0.150 V.
- This parameter is sampled. $GV_{DD} = 1.35\text{ V} - 0.067\text{ V} \div + 0.100\text{ V}$ (for DDR3L), $f = 1\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$, $V_{OUT} = GV_{DD} \div 2$, V_{OUT} (peak-to-peak) = 0.167 V.

This table provides the current draw characteristics for MV_{REFn} .

Table 23. Current Draw Characteristics for MV_{REFn}

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|--|-------------|-----|-----|---------------|------|
| Current draw for DDR3 SDRAM for MV_{REFn} | MV_{REFn} | — | 500 | μA | — |
| Current draw for DDR3L SDRAM for MV_{REFn} | MV_{REFn} | — | 500 | μA | — |

2.9.2 DDR3 and DDR3L SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required $GV_{DD}(\text{typ})$ voltage is 1.5 V when interfacing to DDR3 SDRAM and the required $GV_{DD}(\text{typ})$ voltage is 1.35 V when interfacing to DDR3L SDRAM.

Electrical Characteristics

2.9.2.1 DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 24. DDR3 SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | | Symbol | Min | Max | Unit | Note |
|-----------------------|-----------------------|------------|-------------------|-------------------|------|------|
| AC input low voltage | > 1200 MT/s data rate | V_{ILAC} | — | $MVREF_n - 0.150$ | V | — |
| | ≤ 1200 MT/s data rate | | | $MVREF_n - 0.175$ | | |
| AC input high voltage | > 1200 MT/s data rate | V_{IHAC} | $MVREF_n + 0.150$ | — | V | — |
| | ≤ 1200 MT/s data rate | | $MVREF_n + 0.175$ | | | |

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 25. DDR3L SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | | Symbol | Min | Max | Unit | Note |
|-----------------------|-----------------------|------------|-------------------|-------------------|------|------|
| AC input low voltage | > 1200 MT/s data rate | V_{ILAC} | — | $MVREF_n - 0.135$ | V | — |
| | ≤ 1200 MT/s data rate | | | $MVREF_n - 0.160$ | | |
| AC input high voltage | > 1200 MT/s data rate | V_{IHAC} | $MVREF_n + 0.135$ | — | V | — |
| | ≤ 1200 MT/s data rate | | $MVREF_n + 0.160$ | | | |

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 26. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|-----------------------------------|--------------|------|-----|------|------|
| Controller Skew for MDQS—MDQ/MECC | t_{CISKEW} | -142 | 142 | ps | 1 |
| 1200 MT/s data rate | | | | | |
| 1066 MT/s data rate | | | | | |
| 800 MT/s data rate | | | | | |
| Tolerated Skew for MDQS—MDQ/MECC | t_{DISKEW} | -275 | 275 | ps | 2 |
| 1200 MT/s data rate | | | | | |
| 1066 MT/s data rate | | | | | |
| 800 MT/s data rate | | | | | |

Note:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

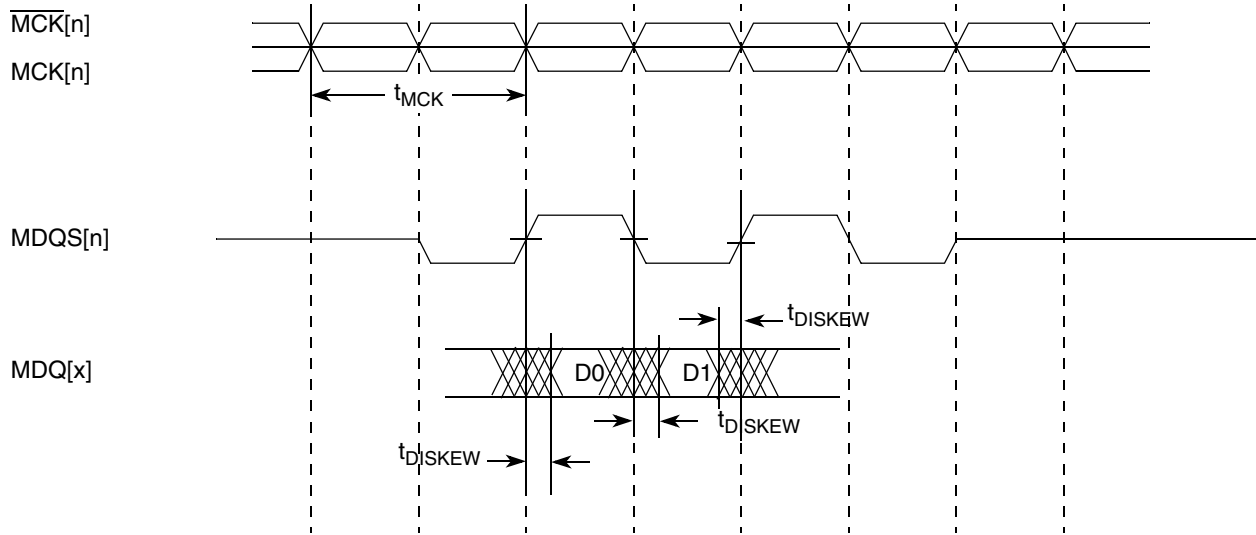


Figure 9. DDR3 and DDR3L SDRAM Interface Input Timing Diagram

2.9.2.2 DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

This table provides the DDR3/DDR3L SDRAM output AC timing specifications.

Table 27. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

For recommended operating conditions, see Table 3.

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|--|---------------------|-------|-----|------|------|
| MCK[n] cycle time | t_{MCK} | 1.67 | 2.5 | ns | 2 |
| ADDR/CMD output setup with respect to MCK | t_{DDKHAS} | | | ns | 3 |
| 1200 MT/s data rate | | 0.675 | — | | |
| 1066 MT/s data rate | | 0.744 | — | | |
| 800 MT/s data rate | | 0.917 | — | | |
| ADDR/CMD output hold with respect to MCK | t_{DDKHAX} | | | ns | 3 |
| 1200 MT/s data rate | | 0.675 | — | | |
| 1066 MT/s data rate | | 0.744 | — | | |
| 800 MT/s data rate | | 0.917 | — | | |
| $\overline{MCS}[n]$ output setup with respect to MCK | t_{DDKHCS} | | | ns | 3 |
| 1200 MT/s data rate | | 0.675 | — | | |
| 1066 MT/s data rate | | 0.744 | — | | |
| 800 MT/s data rate | | 0.917 | — | | |
| $\overline{MCS}[n]$ output hold with respect to MCK | t_{DDKHCX} | | | ns | 3 |
| 1200 MT/s data rate | | 0.675 | — | | |
| 1066 MT/s data rate | | 0.744 | — | | |
| 800 MT/s data rate | | 0.917 | — | | |

Electrical Characteristics

Table 27. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|--|--------------------------------|----------------------|----------------------|------|------|
| MCK to MDQS Skew | t_{DDKHMH} | | | ns | 4 |
| ≥ 1066 MT/s data rate | | -0.245 | 0.245 | | 4, 6 |
| 800 MT/s data rate | | -0.375 | 0.375 | | 4 |
| MDQ/MECC/MDM output setup with respect to MDQS | t_{DDKHDS} , t_{DDKLDS} | | | ps | 5 |
| 1200 MT/s data rate | | 275 | — | | |
| 1066 MT/s data rate | | 300 | — | | |
| 800 MT/s data rate | | 375 | — | | |
| MDQ/MECC/MDM output hold with respect to MDQS | t_{DDKHDX} , t_{DDKLDX} | | | ps | 5 |
| 1200 MT/s data rate | | 275 | — | | |
| 1066 MT/s data rate | | 300 | — | | |
| 800 MT/s data rate | | 375 | — | | |
| MDQS preamble | t_{DDKHMP} | $0.9 \times t_{MCK}$ | — | ns | — |
| MDQS postamble | t_{DDKHME} | $0.4 \times t_{MCK}$ | $0.6 \times t_{MCK}$ | ns | — |

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/ \overline{MCK} and MDQS/ \overline{MDQS} referenced measurements are made from the crossing of the two signals.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/ \overline{MCK} , \overline{MCS} , and MDQ/MECC/MDM/MDQS.
- Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
- Note that for 1200/1333 frequencies it is required to program the start value of the DQS adjust for write leveling.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 27](#), it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

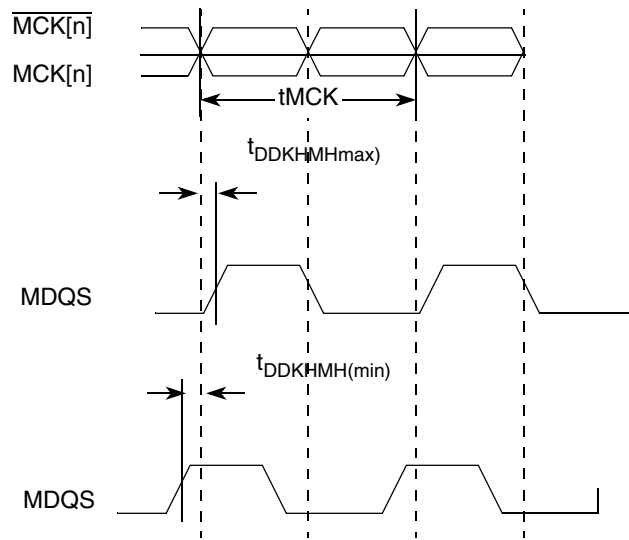


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

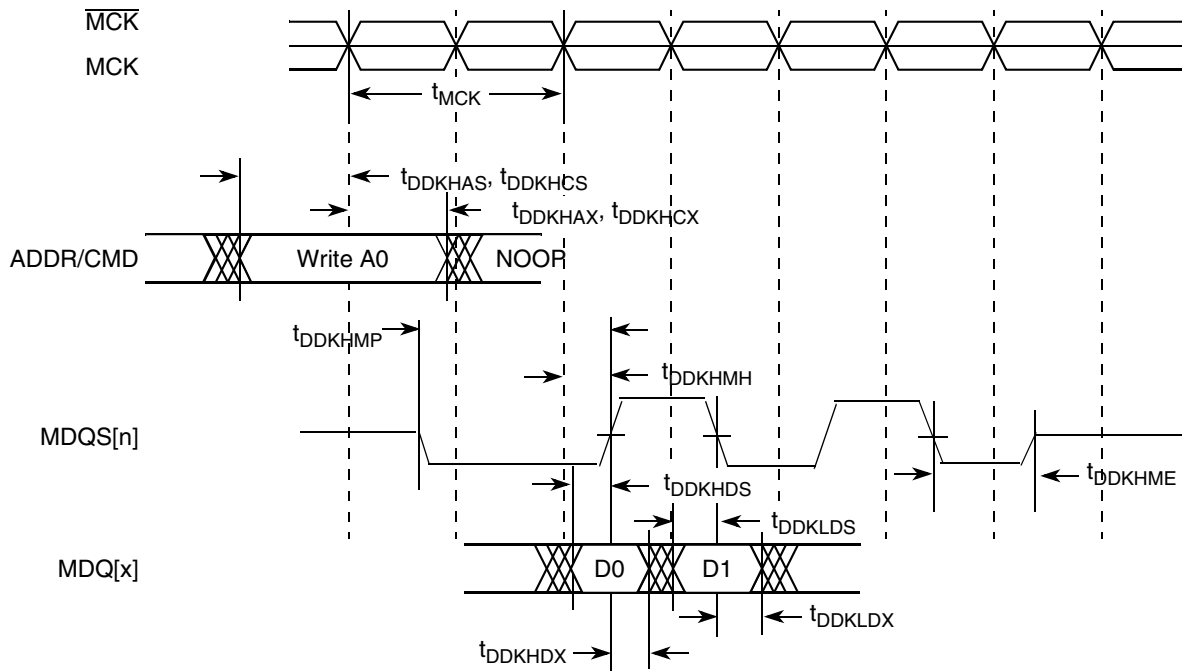


Figure 11. DDR3 and DDR3L Output Timing Diagram

Electrical Characteristics

This figure provides the AC test load for the DDR3 and DDR3L controller bus.

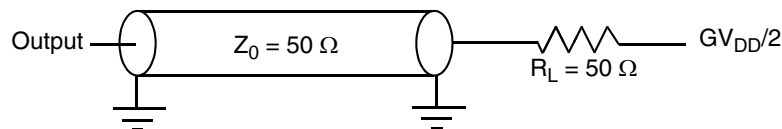


Figure 12. DDR3 and DDR3L Controller Bus AC Test Load

2.9.2.3 DDR3 and DDR3L SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 and DDR3L SDRAM controller interface. This figure shows the differential timing specification.

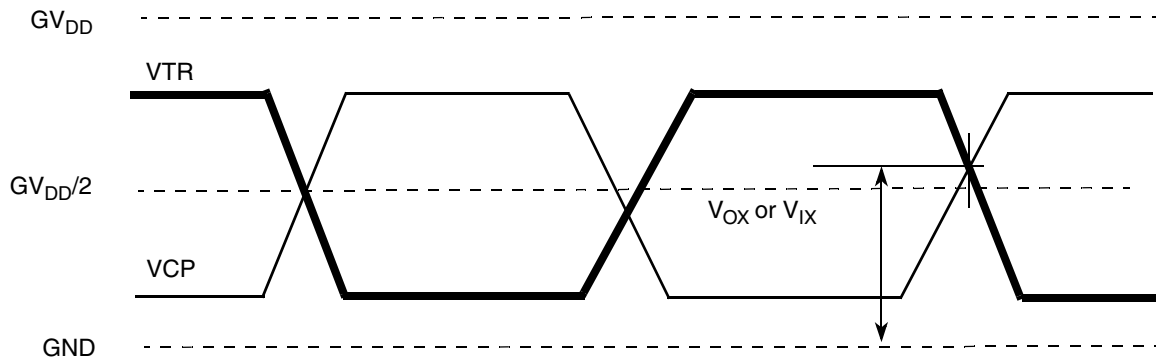


Figure 13. DDR3 and DDR3L SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

This table provides the DDR3 differential specifications for the differential signals MDQS/ $\overline{\text{MDQS}}$ and MCK/ $\overline{\text{MCK}}$.

Table 28. DDR3 SDRAM Differential Electrical Characteristics¹

| Parameter | Symbol | Min | Max | Unit | Note |
|--|------------|------------------------------|------------------------------|------|------|
| Input AC Differential Cross-Point Voltage | V_{IXAC} | $0.5 \times GV_{DD} - 0.150$ | $0.5 \times GV_{DD} + 0.150$ | V | — |
| Output AC Differential Cross-Point Voltage | V_{OXAC} | $0.5 \times GV_{DD} - 0.115$ | $0.5 \times GV_{DD} + 0.115$ | V | — |

Note:

- I/O drivers are calibrated before making measurements.

This table provides the DDR3L differential specifications for the differential signals MDQS/ $\overline{\text{MDQS}}$ and MCK/ $\overline{\text{MCK}}$.

Table 29. DDR3L SDRAM Differential Electrical Characteristics¹

| Parameter | Symbol | Min | Max | Unit | Note |
|--|------------|------------------------------|------------------------------|------|------|
| Input AC differential cross-point voltage | V_{IXAC} | $0.5 \times GV_{DD} - 0.135$ | $0.5 \times GV_{DD} + 0.135$ | V | — |
| Output AC differential cross-point voltage | V_{OXAC} | $0.5 \times GV_{DD} - 0.105$ | $0.5 \times GV_{DD} + 0.105$ | V | — |

Note:

- I/O drivers are calibrated before making measurements.

2.10 eSPI

This section describes the DC and AC electrical specifications for the eSPI interface.

2.10.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at $CV_{DD} = 3.3$ V.

Table 30. eSPI DC Electrical Characteristics ($CV_{DD} = 3.3$ V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|----------|-----|----------|---------|------|
| Input high voltage | V_{IH} | 2.0 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($V_{IN} = 0$ V or $V_{IN} = CV_{DD}$) | I_{IN} | — | ± 40 | μ A | 2 |
| Output high voltage ($CV_{DD} = \text{min}$, $I_{OH} = -2$ mA) | V_{OH} | 2.4 | — | V | — |
| Output low voltage ($CV_{DD} = \text{min}$, $I_{OL} = 2$ mA) | V_{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the CV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

This table provides the DC electrical characteristics for the eSPI interface operating at $CV_{DD} = 2.5$ V.

Table 31. eSPI DC Electrical Characteristics ($CV_{DD} = 2.5$ V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|----------|-----|----------|---------|------|
| Input high voltage | V_{IH} | 1.7 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.7 | V | 1 |
| Input current ($V_{IN} = 0$ V or $V_{IN} = CV_{DD}$) | I_{IN} | — | ± 40 | μ A | 2 |
| Output high voltage ($CV_{DD} = \text{min}$, $I_{OH} = -1$ mA) | V_{OH} | 2.0 | — | V | — |
| Output low voltage ($CV_{DD} = \text{min}$, $I_{OL} = 1$ mA) | V_{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the CV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

This table provides the DC electrical characteristics for the eSPI interface operating at $CV_{DD} = 1.8$ V.

Table 32. eSPI DC Electrical Characteristics ($CV_{DD} = 1.8$ V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|--------------------|----------|------|-----|------|------|
| Input high voltage | V_{IH} | 1.25 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.6 | V | 1 |

Electrical Characteristics

Table 32. eSPI DC Electrical Characteristics (CV_{DD} = 1.8 V) (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|--|-----------------|------|-----|------|------|
| Input current (V _{IN} = 0 V or V _{IN} = CV _{DD}) | I _{IN} | — | ±40 | μA | 2 |
| Output high voltage (CV _{DD} = min, I _{OH} = -0.5 mA) | V _{OH} | 1.35 | — | V | — |
| Output low voltage (CV _{DD} = min, I _{OL} = 0.5 mA) | V _{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in [Table 3](#).
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in [Section 2.1.2, “Recommended Operating Conditions.”](#)

2.10.2 eSPI AC Timing Specifications

This table provides the eSPI input and output AC timing specifications.

Table 33. eSPI AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|---|--|---|--|------|------|
| SPI_MOSI output—Master data (internal clock) hold time | t _{NIKHOX} | 2 + (t _{PLATFORM_CLK} *SPMO DE[HO_ADJ]) | — — | ns | 2, 3 |
| SPI_MOSI output—Master data (internal clock) delay | t _{NIKHOV} t _{NIKHOV} | — | 5.68+(t _{PLATFORM_CLK} *S PMODE[HO_ADJ]) | ns | 2, 3 |
| SPI_CS outputs—Master data (internal clock) hold time | t _{NIKHOX2} | 0 | — | ns | 2 |
| SPI_CS outputs—Master data (internal clock) delay | t _{NIKHOV2} | — | 6.0 | ns | 2 |
| eSPI inputs—Master data (internal clock) input setup time | t _{NIIVKH} | 7 | — | ns | — |
| eSPI inputs—Master data (internal clock) input hold time | t _{NIIXKH} | 0 | — | ns | — |

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. The greater of the two output timings for t_{NIKHOX} and t_{NIKHOV} are used when SPCOM[RxDelay] of the eSPI command register is set. For example, the t_{NIKHOX} is 4.0 and t_{NIKHOV} is 7.0 if SPCOM[RxDelay] is set to be 1.

This figure provides the AC test load for the eSPI.

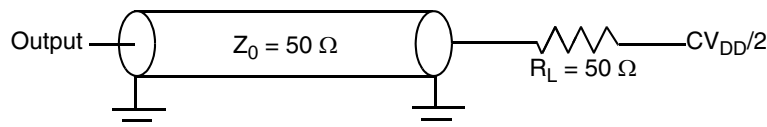


Figure 14. eSPI AC Test Load

This figure represents the AC timing from [Table 33](#) in master mode (internal clock). Note that although timing specifications generally refer to the rising edge of the clock, this figure also applies when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

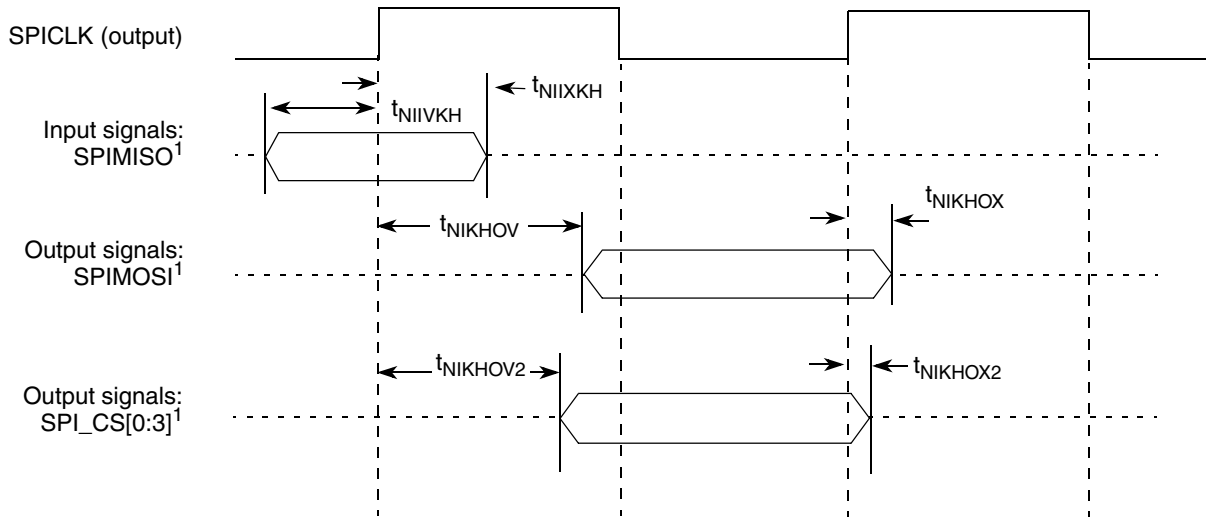


Figure 15. eSPI AC Timing in Master Mode (Internal Clock) Diagram

2.11 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

2.11.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 34. DUART DC Electrical Characteristics ($OV_{DD} = 3.3\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|--|----------|-----|----------|---------------|------|
| Input high voltage | V_{IH} | 2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($OV_{IN} = 0\text{ V}$ or $OV_{IN} = OV_{DD}$) | I_{IN} | — | ± 40 | μA | 2 |
| Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2\text{ mA}$) | V_{OH} | 2.4 | — | V | — |
| Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2\text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

1. The symbol OV_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 3](#).
2. The symbol OV_{IN} , in this case, represents the OV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

Electrical Characteristics

2.11.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 35. DUART AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Value | Unit | Note |
|-------------------|--|------|------|
| Minimum baud rate | $f_{\text{PLAT}}/(2 \times 1,048,576)$ | baud | 1 |
| Maximum baud rate | $f_{\text{PLAT}}/(2 \times 16)$ | baud | 1, 2 |
| Oversample rate | 16 | — | 3 |

Note:

1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled every 16th sample.

2.12 Ethernet: Data path Three-Speed Ethernet (dTSEC), Management Interface, IEEE Std 1588

This section provides the AC and DC electrical characteristics for the data path three-speed Ethernet controller, the Ethernet Management Interface, and the IEEE Std 1588 interface.

2.12.1 SGMII Timing Specifications

See [Section 2.20.8, “SGMII Interface.”](#)

2.12.2 RGMII Timing Specifications

This section discusses the electrical characteristics for the MII and RGMII interfaces.

2.12.2.1 RGMII DC Electrical Characteristics

This table shows the RGMII DC electrical characteristics when operating at $LV_{\text{DD}} = 2.5 \text{ V}$ supply.

Table 36. RGMII DC Electrical Characteristics ($LV_{\text{DD}} = 2.5 \text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|-----------------|------|----------|---------------|------|
| Input high voltage | V_{IH} | 1.70 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.70 | V | 1 |
| Input current ($LV_{\text{IN}} = 0 \text{ V}$ or $LV_{\text{IN}} = LV_{\text{DD}}$) | I_{IH} | — | ± 40 | μA | 2 |
| Output high voltage ($LV_{\text{DD}} = \text{min}$, $I_{\text{OH}} = -1.0 \text{ mA}$) | V_{OH} | 2.00 | — | V | — |
| Output low voltage ($LV_{\text{DD}} = \text{min}$, $I_{\text{OL}} = 1.0 \text{ mA}$) | V_{OL} | — | 0.40 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the LV_{IN} symbols referenced in [Table 2](#) and [Table 3](#).

2.12.2.2 RGMII AC Timing Specifications

This table shows the RGMII AC timing specifications.

Table 37. RGMII AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter/Condition | Symbol ¹ | Min | Typ | Max | Unit | Note |
|--|---------------------|------|-----|------|------|------|
| Data to clock output skew (at transmitter) | t_{SKRGT_TX} | -500 | 0 | 500 | ps | 5 |
| Data to clock input skew (at receiver) | t_{SKRGT_RX} | 1.0 | — | 2.8 | ns | 2 |
| Clock period duration | t_{RGT} | 7.2 | 8.0 | 8.8 | ns | 3 |
| Duty cycle for 10BASE-T and 100BASE-TX | t_{RGTH}/t_{RGT} | 40 | 50 | 60 | % | 3, 4 |
| Duty cycle for Gigabit | t_{RGTH}/t_{RGT} | 45 | 50 | 55 | % | — |
| Rise time (20%–80%) | t_{RGTR} | — | — | 0.75 | ns | — |
| Fall time (20%–80%) | t_{RGTF} | — | — | 0.75 | ns | — |

Note:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of GTX_CLK125 by more than 300ppm.

Electrical Characteristics

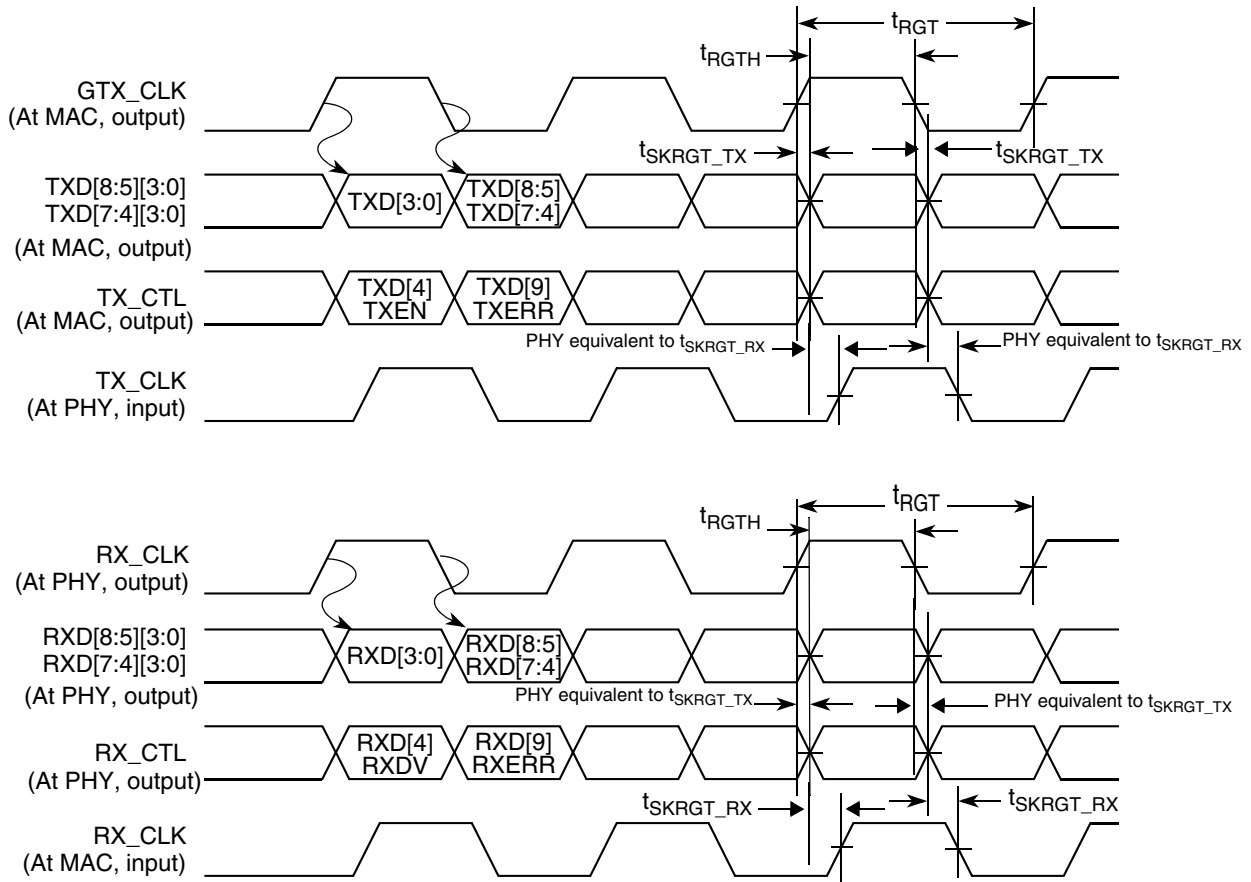


Figure 16. RGMII AC Timing and Multiplexing Diagrams

2.12.3 Ethernet Management Interface

This section discusses the electrical characteristics for the EMI1 interfaces. EMI1 is the PHY management interface controlled by the MDIO controller associated with Frame Manager 1 1GMAC-1.

2.12.3.1 Ethernet Management Interface DC Electrical Characteristics

The Ethernet management interface is defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for the Ethernet management interface is provided in this table.

Table 38. Ethernet Management Interface DC Electrical Characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|-----------------|------|-----|------|------|
| Input high voltage | V _{IH} | 2.0 | — | V | 2 |
| Input low voltage | V _{IL} | — | 0.9 | V | 2 |
| Input high current (LV _{DD} = Max, V _{IN} = 2.1 V) | I _{IH} | — | 40 | μA | 1 |
| Input low current (LV _{DD} = Max, V _{IN} = 0.5 V) | I _{IL} | -600 | — | μA | 1 |
| Output high voltage (LV _{DD} = Min, I _{OH} = -1.0 mA) | V _{OH} | 2.4 | — | V | — |
| Output low voltage (LV _{DD} = Min, I _{OL} = 1.0 mA) | V _{OL} | — | 0.4 | V | — |

Table 38. Ethernet Management Interface DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|-----------|--------|-----|-----|------|------|
|-----------|--------|-----|-----|------|------|

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in [Table 2](#) and [Table 3](#).
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in [Table 3](#).

The Ethernet management interface is defined to operate at a supply voltage of 2.5 V. The DC electrical characteristics for the Ethernet management interface is provided in this table.

Table 39. Ethernet Management Interface DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|--|-----------------|-----|-----|------|------|
| Input high voltage | V _{IH} | 1.7 | — | V | 1 |
| Input low voltage | V _{IL} | — | 0.7 | V | 1 |
| Input current (LV _{IN} = 0 V or LV _{IN} = LV _{DD}) | I _{IH} | — | ±40 | μA | 2 |
| Output high voltage (LV _{DD} = Min, I _{OH} = -1.0 mA) | V _{OH} | 2.0 | — | V | — |
| Output low voltage (LV _{DD} = Min, I _{OL} = 1.0 mA) | V _{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

2.12.3.2 Ethernet Management Interface AC Timing Specifications

This table provides the Ethernet management interface AC timing specifications.

Table 40. Ethernet Management Interface AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol ¹ | Min | Typ | Max | Unit | Note |
|----------------------------|---------------------|----------------------------------|-----|----------------------------------|------|------|
| MDC frequency | f _{MDC} | — | — | 2.5 | MHz | 2 |
| MDC clock pulse width high | t _{MDCH} | 160 | — | — | ns | — |
| MDC to MDIO delay | t _{MDKHDX} | (16 × t _{plb_clk}) - 6 | — | (16 × t _{plb_clk}) + 6 | ns | 3, 4 |
| MDIO to MDC setup time | t _{MDDVKH} | 10 | — | — | ns | — |
| MDIO to MDC hold time | t _{MDDXKH} | 0 | — | — | ns | — |

Electrical Characteristics

Table 40. Ethernet Management Interface AC Timing Specifications (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol ¹ | Min | Typ | Max | Unit | Note |
|-----------|---------------------|-----|-----|-----|------|------|
|-----------|---------------------|-----|-----|-----|------|------|

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ± 3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. $t_{\text{plb_clk}}$ is the frame manager clock period.

This figure shows the Ethernet management interface timing diagram

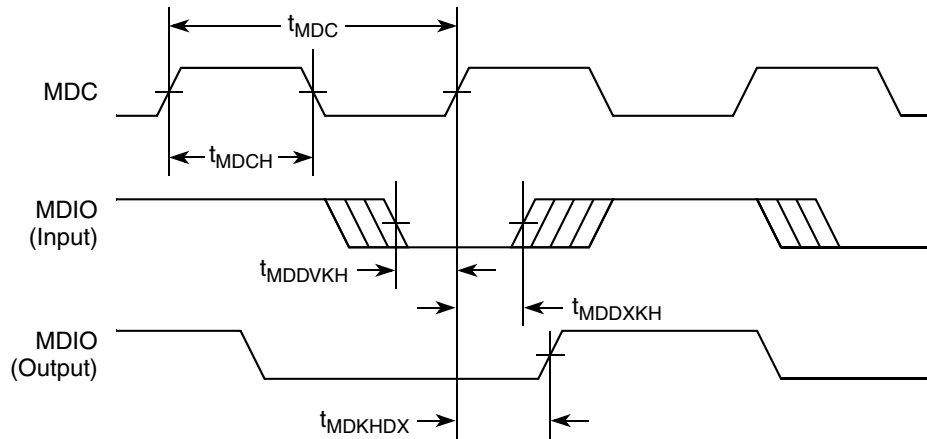


Figure 17. Ethernet Management Interface Timing Diagram

2.12.4 eTSEC IEEE Std 1588 DC Specifications

This table shows the eTSEC IEEE 1588 DC electrical characteristics when operating at $V_{\text{DD}} = 3.3$ V supply.

Table 41. IEEE 1588 DC Electrical Characteristics ($V_{\text{DD}} = 3.3$ V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|-----------------|------|-----|---------------|------|
| Input high voltage | V_{IH} | 2.0 | — | V | 2 |
| Input low voltage | V_{IL} | — | 0.9 | V | 2 |
| Input high current ($V_{\text{DD}} = \text{Max}$, $V_{\text{IN}} = 2.1$ V) | I_{IH} | — | 40 | μA | 1 |
| Input low current ($V_{\text{DD}} = \text{Max}$, $V_{\text{IN}} = 0.5$ V) | I_{IL} | -600 | — | μA | 1 |
| Output high voltage ($V_{\text{DD}} = \text{Min}$, $I_{\text{OH}} = -1.0$ mA) | V_{OH} | 2.4 | — | V | — |

Table 41. IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|-----------------|-----|-----|------|------|
| Output low voltage (LV _{DD} = Min, I _{OL} = 1.0 mA) | V _{OL} | — | 0.4 | V | — |

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in [Table 2](#) and [Table 3](#).
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in [Table 3](#).

This table shows the eTSEC IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.**Table 42. IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)**For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|--|-----------------|------|------|------|------|
| Input high voltage | V _{IH} | 1.70 | — | V | 1 |
| Input low voltage | V _{IL} | — | 0.70 | V | 1 |
| Input current (LV _{IN} = 0 V or LV _{IN} = LV _{DD}) | I _{IH} | — | ±40 | μA | 2 |
| Output high voltage (LV _{DD} = min, I _{OH} = -1.0 mA) | V _{OH} | 2.00 | — | V | — |
| Output low voltage (LV _{DD} = min, I _{OL} = 1.0 mA) | V _{OL} | — | 0.40 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in [Table 2](#) and [Table 3](#).

2.12.5 eTSEC IEEE Std 1588 AC Specifications

This table provides the eTSEC IEEE 1588 AC timing specifications.

Table 43. eTSEC IEEE 1588 AC Timing SpecificationsFor recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|------------------------------------|--|-------------------------------|-----|-------------------------|------|------|
| TSEC_1588_CLK clock period | t _{T1588CLK} | 6.4 | — | T _{RX_CLK} × 7 | ns | 1, 2 |
| TSEC_1588_CLK duty cycle | t _{T1588CLKH} / t _{T1588CLK} | 40 | 50 | 60 | % | 3 |
| TSEC_1588_CLK peak-to-peak jitter | t _{T1588CLKINJ} | — | — | 250 | ps | — |
| Rise time eTSEC_1588_CLK (20%–80%) | t _{T1588CLKINR} | 1.0 | — | 2.0 | ns | — |
| Fall time eTSEC_1588_CLK (80%–20%) | t _{T1588CLKINF} | 1.0 | — | 2.0 | ns | — |
| TSEC_1588_CLK_OUT clock period | t _{T1588CLKOUT} | 2 × t _{T1588CLK} | — | — | ns | — |
| TSEC_1588_CLK_OUT duty cycle | t _{T1588CLKOTH} / t _{T1588CLKOUT} | 30 | 50 | 70 | % | — |
| TSEC_1588_PULSE_OUT | t _{T1588OV} | 0.5 | — | 3.5 | ns | — |
| TSEC_1588_TRIG_IN pulse width | t _{T1588TRIGH} | 2 × t _{T1588CLK_MAX} | — | — | ns | 2 |

Electrical Characteristics

Table 43. eTSEC IEEE 1588 AC Timing Specifications (continued)

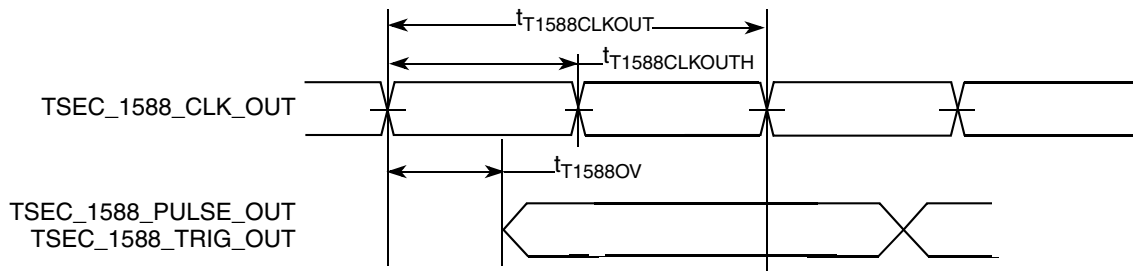
For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|-----------|--------|-----|-----|-----|------|------|
|-----------|--------|-----|-----|-----|------|------|

Note:

1. T_{RX_CLK} is the maximum clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK} , but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns, respectively.
3. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is noninverting. Otherwise, it is counted starting at the falling edge.

Figure 18. eTSEC IEEE 1588 Output AC Timing

This figure shows the data and command input AC timing diagram.

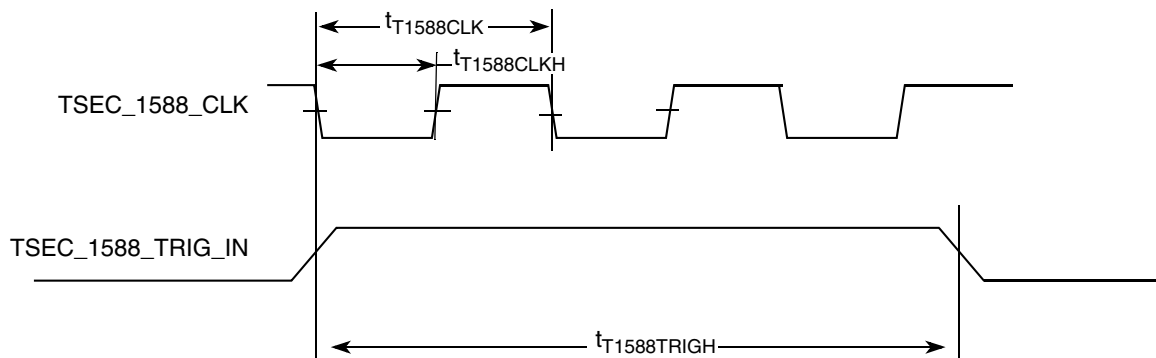


Figure 19. eTSEC IEEE 1588 Input AC Timing

2.13 USB

This section provides the AC and DC electrical specifications for the USB interface.

2.13.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface at USB_VDD_3P3 = 3.3 V.

Table 44. USB DC Electrical Characteristics (USB_VDD_3P3 = 3.3 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|--|----------|-----|-----|------|------|
| Input high voltage ¹ | V_{IH} | 2.0 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current (USB_VIN_3P3 = 0 V or USB_VIN_3P3 = USB_VDD_3P3) | I_{IN} | — | ±40 | μA | 2 |
| Output high voltage (USB_VDD_3P3 = min, $I_{OH} = -2$ mA) | V_{OH} | 2.8 | — | V | |
| Output low voltage (USB_VDD_3P3 = min, $I_{OL} = 2$ mA) | V_{OL} | — | 0.3 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max USB_VIN_3P3 values found in [Table 3](#).
2. The symbol USB_VIN_3P3, in this case, represents the USB_VIN_3P3 symbol referenced in [Section 2.1.2](#), “Recommended Operating Conditions.”

2.13.2 USB AC Electrical Specifications

This table provides the USB clock input (USBn_CLKIN) AC timing specifications.

Table 45. USB_CLK_IN AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Condition | Symbol | Min | Typ | Max | Unit | Note |
|--|---|--------------------|--------|-----|-------|------|------|
| Frequency range | — | $f_{USB_CLK_IN}$ | — | 24 | — | MHz | — |
| Rise/Fall time | Measured between 10% and 90% | t_{USRF} | — | — | 6 | ns | 1 |
| Clock frequency tolerance | — | t_{CLK_TOL} | -0.005 | 0 | 0.005 | % | — |
| Reference clock duty cycle | Measured at 1.6 V | t_{CLK_DUTY} | 40 | 50 | 60 | % | — |
| Total input jitter/time interval error | RMS value measured with a second-order, high-pass filter of 500-kHz bandwidth | t_{CLK_PJ} | — | — | 5 | ps | — |

Note:

1. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

2.14 Enhanced Local Bus Interface

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.14.1 Enhanced Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at $BV_{DD} = 3.3\text{ V}$.

Table 46. Enhanced Local Bus DC Electrical Characteristics ($BV_{DD} = 3.3\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|----------|-----|----------|---------------|------|
| Input high voltage | V_{IH} | 2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($V_{IN} = 0\text{ V}$ or $V_{IN} = BV_{DD}$) | I_{IN} | — | ± 40 | μA | 2 |
| Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -2\text{ mA}$) | V_{OH} | 2.4 | — | V | — |
| Output low voltage ($BV_{DD} = \text{min}$, $I_{OL} = 2\text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

This table provides the DC electrical characteristics for the enhanced local bus interface operating at $BV_{DD} = 2.5\text{ V}$.

Table 47. Enhanced Local Bus DC Electrical Characteristics ($BV_{DD} = 2.5\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|----------|-----|----------|---------------|------|
| Input high voltage | V_{IH} | 1.7 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.7 | V | 1 |
| Input current ($V_{IN} = 0\text{ V}$ or $V_{IN} = BV_{DD}$) | I_{IN} | — | ± 40 | μA | 2 |
| Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -1\text{ mA}$) | V_{OH} | 2.0 | — | V | — |
| Output low voltage ($BV_{DD} = \text{min}$, $I_{OL} = 1\text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

This table provides the DC electrical characteristics for the enhanced local bus interface operating at $BV_{DD} = 1.8\text{ V}$.

Table 48. Enhanced Local Bus DC Electrical Characteristics ($BV_{DD} = 1.8\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|----------|------|----------|---------------|------|
| Input high voltage | V_{IH} | 1.25 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.6 | V | 1 |
| Input current ($V_{IN} = 0\text{ V}$ or $V_{IN} = BV_{DD}$) | I_{IN} | — | ± 40 | μA | 2 |
| Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -0.5\text{ mA}$) | V_{OH} | 1.35 | — | V | — |
| Output low voltage ($BV_{DD} = \text{min}$, $I_{OL} = 0.5\text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Section 2.1.2](#), “Recommended Operating Conditions.”

2.14.2 Enhanced Local Bus AC Timing Specifications

This section describes the AC timing specifications for the enhanced local bus interface.

This figure shows the eLBC AC test load.

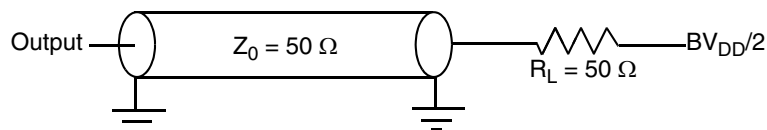


Figure 20. Enhanced Local Bus AC Test Load

2.14.2.1 Local Bus AC Timing Specification

All output signal timings are relative to the falling edge of any LCLKs. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

This table provides the eLBC timing specifications.

Table 49. Enhanced Local Bus Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|---|---------------------|-----|-----|------|------|
| Local bus cycle time | t_{LBK} | 15 | — | ns | — |
| Local bus duty cycle | t_{LBKH}/t_{LBK} | 45 | 55 | % | — |
| LCLK[n] skew to LCLK[m] | $t_{LBKSKEW}$ | — | 150 | ps | 2 |
| Input setup (except LGTA/LUPWAIT/LFRB) | t_{LBIVKH} | 6 | — | ns | — |
| Input hold (except LGTA/LUPWAIT/LFRB) | t_{LBIXKH} | 1 | — | ns | — |

Electrical Characteristics

Table 49. Enhanced Local Bus Timing Specifications (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|---|---------------------|---|-----|------|------|
| Input setup (for LGTA/LUPWAIT/LFRB) | t_{LBIVKL} | 6 | — | ns | — |
| Input hold (for LGTA/LUPWAIT/LFRB) | t_{LBIXKL} | 1 | — | ns | — |
| Output delay (Except LALE) | t_{LBKLOV} | — | 2.0 | ns | — |
| Output hold (Except LALE) | t_{LBKLOX} | -3.5 | — | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | t_{LBKLOZ} | — | 2 | ns | 3 |
| LALE output negation to LAD/LDP output transition (LATCH hold time) | t_{LBONOT} | 2 platform clock cycles - 1 ns (LBCR[AHD] = 1) | — | ns | 4 |
| | | 4 platform clock cycles - 2 ns (LBCR[AHD] = 0) | — | | |

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew is measured between different LCLKs at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. After power on reset, LBCR[AHD] defaults to 0.
5. Output hold is negative, meaning that the output transition happens earlier than the falling edge of LCLK.

This figure shows the AC timing diagram of the local bus interface.

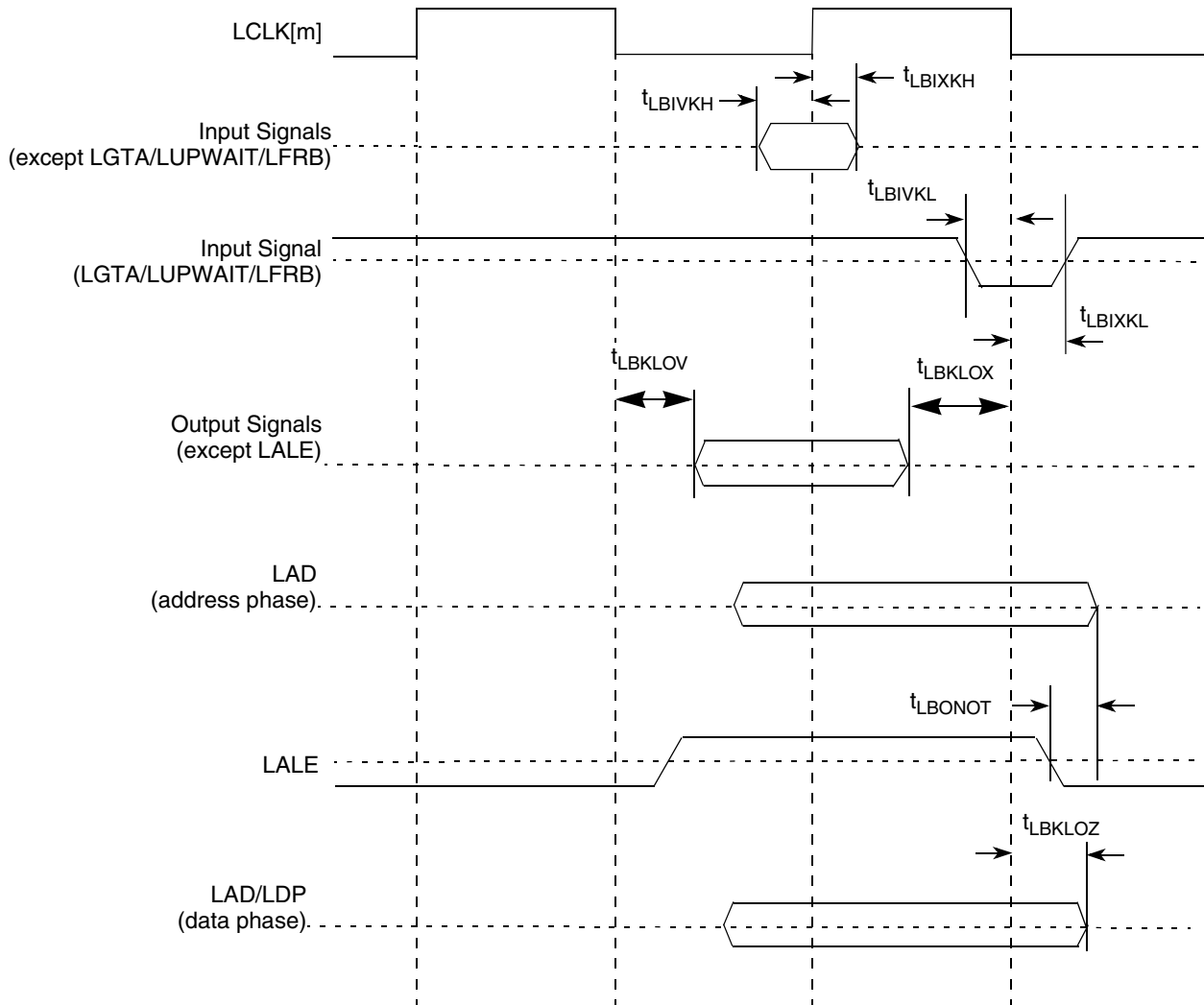


Figure 21. Enhanced Local Bus Signals

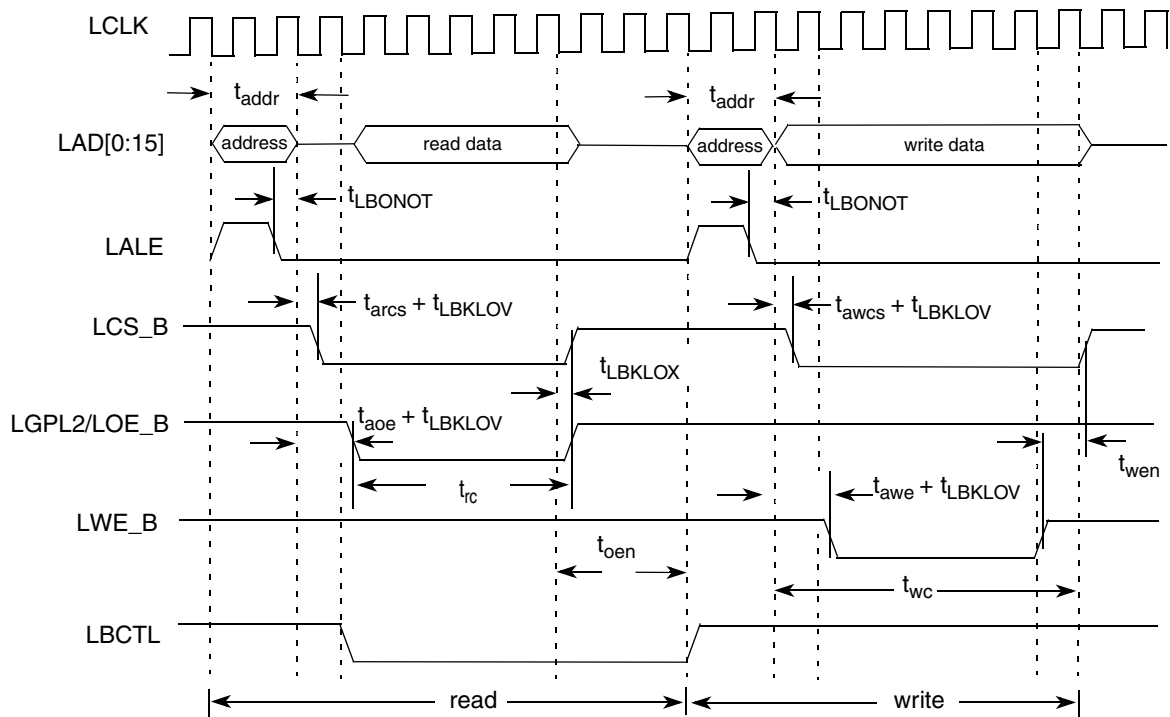
Figure 22 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, 1/4, 1/2, 1, 1 + 1/4, 1 + 1/2, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKLOV}$.

Electrical Characteristics

This figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



¹ t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

² t_{arcs} , t_{awcs} , t_{aoe} , t_{rc} , t_{oen} , t_{awe} , t_{wc} , t_{wen} are determined by ORx. See the chip reference manual.

Figure 22. GPCM Output Timing Diagram

2.15 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

2.15.1 eSDHC DC Electrical Characteristics

This table provides the eSDHC electrical characteristics.

Table 50. eSDHC Interface DC Electrical Characteristics

For recommended operating conditions, see Table 3.

| Characteristic | Symbol | Condition | Min | Max | Unit | Note |
|------------------------------|-----------------|--|------------------------|-----------------------|---------|------|
| Input high voltage | V_{IH} | — | $0.625 \times CV_{DD}$ | — | V | 1 |
| Input low voltage | V_{IL} | — | — | $0.25 \times CV_{DD}$ | V | 1 |
| Input/output leakage current | I_{IN}/I_{OZ} | — | -50 | 50 | μA | — |
| Output high voltage | V_{OH} | $I_{OH} = -100 \mu A$ at CV_{DD} min | $0.75 \times CV_{DD}$ | — | V | — |

Table 50. eSDHC Interface DC Electrical Characteristics (continued)For recommended operating conditions, see [Table 3](#).

| Characteristic | Symbol | Condition | Min | Max | Unit | Note |
|---------------------|----------|---|-----------------|------------------------|------|------|
| Output low voltage | V_{OL} | $I_{OL} = 100\mu\text{A}$ at CV_{DD} min | — | $0.125 \times CV_{DD}$ | V | — |
| Output high voltage | V_{OH} | $I_{OH} = -100\mu\text{A}$ at CV_{DD} min | $CV_{DD} - 0.2$ | — | V | 2 |
| Output low voltage | V_{OL} | $I_{OL} = 2\text{ mA}$ at CV_{DD} min | — | 0.3 | V | 2 |

Note:

- The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in [Table 3](#).
- Open drain mode for MMC cards only.

2.15.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in [Figure 23](#) and [Figure 24](#).**Table 51. eSDHC AC Timing Specifications**For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|---|-------------------------------|------|----------------|------|------|
| SD_CLK clock frequency: SD/SDIO full-speed/high-speed mode MMC full-speed/high-speed mode | f_{SHSCK} | 0 | 25/50 20/52 | MHz | 2, 4 |
| SD_CLK clock low time—full-speed/high-speed mode | t_{SHSCKL} | 10/7 | — | ns | 4 |
| SD_CLK clock high time—full-speed/high-speed mode | t_{SHSCKH} | 10/7 | — | ns | 4 |
| SD_CLK clock rise and fall times | $t_{SHSCKR}/$ t_{SHSCKF} | — | 3 | ns | 4 |
| Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK | $t_{SHSIVKH}$ | 2.5 | — | ns | 4 |
| Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK | $t_{SHSIXKH}$ | 2.5 | — | ns | 3,4 |
| Output delay time: SD_CLK to SD_CMD, SD_DATx valid | $t_{SHSKHOV}$ | -3 | 3 | ns | 4 |

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first three letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- In full-speed mode, the clock frequency value can be 0–25 MHz for an SD/SDIO card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–50 MHz for an SD/SDIO card and 0–52 MHz for an MMC card.
- To satisfy setup timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.
- $C_{CARD} \leq 10\text{ pF}$, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40\text{ pF}$

Electrical Characteristics

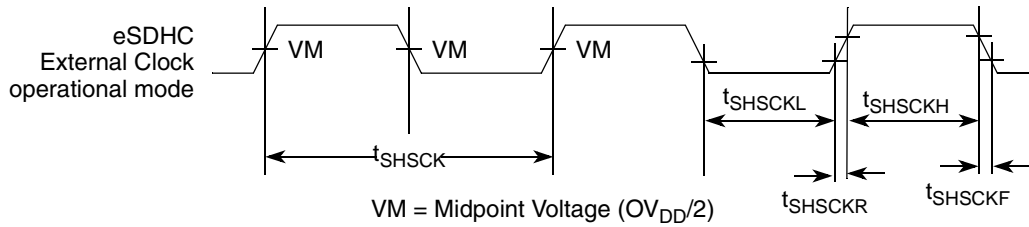
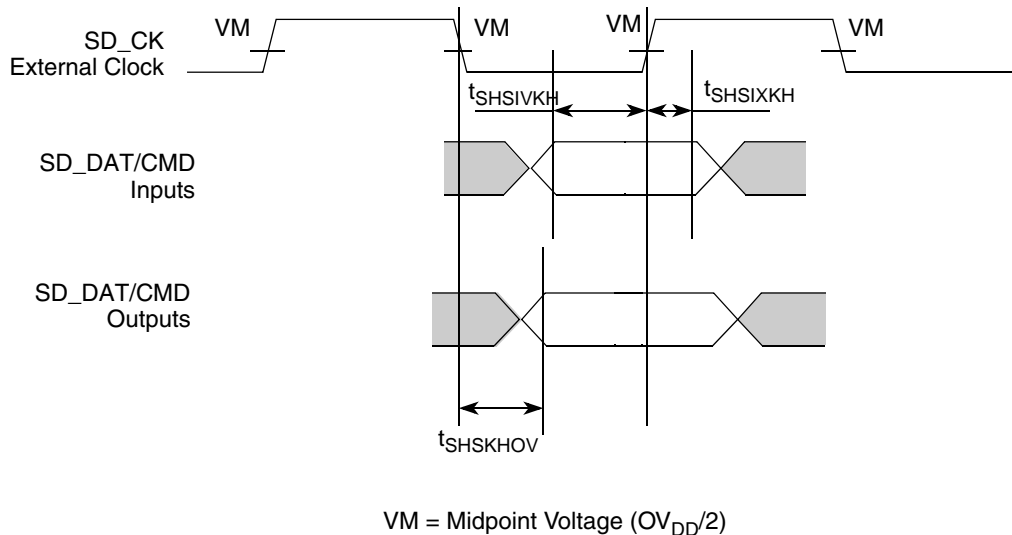


Figure 23. eSDHC Clock Input Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 24. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.16 Multicore Programmable Interrupt Controller (MPIC) Specifications

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

2.16.1 MPIC DC specifications

This table provides the DC electrical characteristics for the MPIC interface.

Table 52. MPIC DC Electrical Characteristics ($OV_{DD} = 3.3\text{ V}$)

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|--|----------|-----|----------|---------------|------|
| Input high voltage | V_{IH} | 2.0 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($OV_{IN} = 0\text{ V}$ or $OV_{IN} = OV_{DD}$) | I_{IN} | — | ± 40 | μA | 2 |
| Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2\text{ mA}$) | V_{OH} | 2.4 | — | V | — |
| Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2\text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Table 52. MPIC DC Electrical Characteristics ($OV_{DD} = 3.3\text{ V}$) (continued)For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|-----------|--------|-----|-----|------|------|
|-----------|--------|-----|-----|------|------|

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in [Table 3](#).
2. The symbol OV_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 3](#).

2.16.2 MPIC AC Timing Specifications

This table provides the MPIC input and output AC timing specifications.

Table 53. MPIC Input AC Timing SpecificationsFor recommended operating conditions, see [Table 3](#).

| Characteristic | Symbol | Min | Max | Unit | Note |
|----------------------------------|-------------|-----|-----|--------|------|
| MPIC inputs—minimum pulse width | t_{PIWID} | 3 | — | SYCLKs | 1 |
| Trust inputs—minimum pulse width | t_{TIWID} | 3 | — | SYCLKs | 2 |

Note:

1. MPIC inputs and outputs are asynchronous to any visible clock. MPIC outputs must be synchronized before use by any external synchronous logic. MPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.
2. Trust inputs are asynchronous to any visible clock. Trust inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation when working in edge triggered mode. For low power trust input pin LP_TMP_DETECT, the voltage is V_{DD_LP} and see [Table 3](#) for the voltage requirement.

2.17 JTAG Controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

2.17.1 JTAG DC Electrical Characteristics

This table provides the JTAG DC electrical characteristics.

Table 54. JTAG DC Electrical Characteristics ($OV_{DD} = 3.3\text{ V}$)For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|--|----------|-----|----------|---------------|------|
| Input high voltage | V_{IH} | 2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($OV_{IN} = 0\text{ V}$ or $OV_{IN} = OV_{DD}$) | I_{IN} | — | ± 40 | μA | 2 |
| Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2\text{ mA}$) | V_{OH} | 2.4 | — | V | — |
| Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2\text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the OV_{IN} symbol found in [Table 3](#).

2.17.2 JTAG AC Timing Specifications

This table provides the JTAG AC timing specifications as defined in Figure 25 through Figure 28.

Table 55. JTAG AC Timing Specifications

For recommended operating conditions, see Table 3.

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|--|---------------------|-----|------|------|------|
| JTAG external clock frequency of operation | f_{JTG} | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | t_{JTG} | 30 | — | ns | — |
| JTAG external clock pulse width measured at OVDD/2 V | t_{JTKHKL} | 15 | — | ns | — |
| JTAG external clock rise and fall times | t_{JTGR}/t_{JTGF} | 0 | 2 | ns | — |
| \overline{TRST} assert time | t_{TRST} | 25 | — | ns | 2 |
| Input setup times | | | | ns | — |
| Boundary-scan USB only | t_{JTDVKH} | 14 | — | | |
| Boundary (except USB) | | 4 | | | |
| TDI, TMS | | 4 | | | |
| Input hold times | t_{JTDXKH} | 10 | — | ns | — |
| Output valid times | | | | | |
| Boundary-scan data | t_{JTKLDV} | — | 15 | ns | 3 |
| TDO | | | 10 | | |
| Output hold times | t_{JTKLDX} | 0 | — | ns | 3 |

Note:

- The symbols used for timing specifications follow the pattern $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- \overline{TRST} is an asynchronous level sensitive signal. The setup time is for test purposes only.
- All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

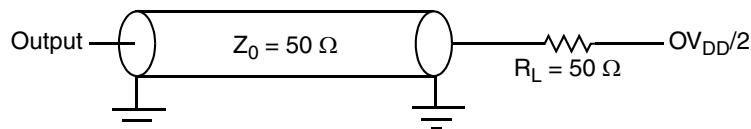


Figure 25. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

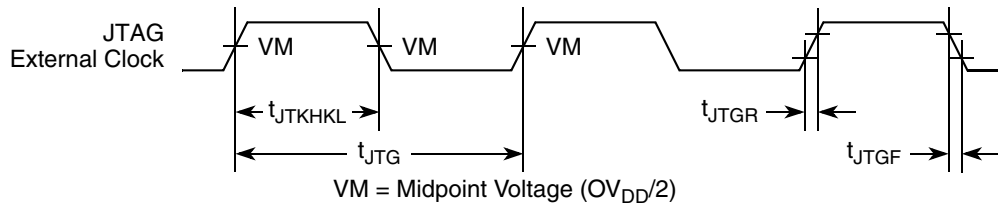


Figure 26. JTAG Clock Input Timing Diagram

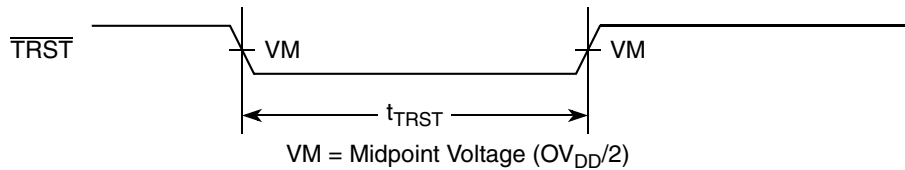


Figure 27. $\overline{\text{TRST}}$ Timing Diagram

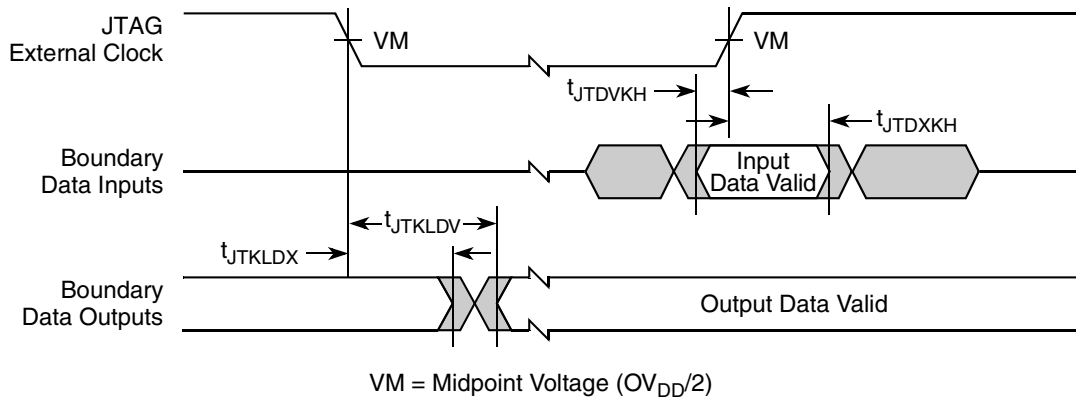


Figure 28. Boundary-Scan Timing Diagram

2.18 I²C

This section describes the DC and AC electrical characteristics for the I²C interface.

2.18.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interfaces.

Table 56. I²C DC Electrical Characteristics ($OV_{DD} = 3.3 \text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|----------|-----|-----|------|------|
| Input high voltage | V_{IH} | 2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2 \text{ mA}$) | V_{OL} | 0 | 0.4 | V | 2 |

Electrical Characteristics

Table 56. I²C DC Electrical Characteristics (OV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---------------------|-----|-----|------|------|
| Pulse width of spikes which must be suppressed by the input filter | t _{I2KHKL} | 0 | 50 | ns | 3 |
| Input current each I/O pin (input voltage is between 0.1 × OV _{DD} and 0.9 × OV _{DD} (max)) | I _I | -40 | 40 | μA | 4 |
| Capacitance for each I/O pin | C _I | — | 10 | pF | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in [Table 3](#).
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.18.2 I²C AC Electrical Specifications

This table provides the I²C AC timing specifications.

Table 57. I²C AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|--|---------------------|--------|--------|------|------|
| SCL clock frequency | f _{I2C} | 0 | 400 | kHz | 2 |
| Low period of the SCL clock | t _{I2CL} | 1.3 | — | μs | — |
| High period of the SCL clock | t _{I2CH} | 0.6 | — | μs | — |
| Setup time for a repeated START condition | t _{I2SVKH} | 0.6 | — | μs | — |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | t _{I2SXKL} | 0.6 | — | μs | — |
| Data setup time | t _{I2DVKH} | 100 | — | ns | — |
| Data input hold time: CBUS compatible masters I ² C bus devices | t _{I2DXKL} | — 0 | — — | μs | 3 |
| Data output delay time | t _{I2OVKL} | — | 0.9 | μs | 4 |
| Setup time for STOP condition | t _{I2PVKH} | 0.6 | — | μs | — |
| Bus free time between a STOP and START condition | t _{I2KHDX} | 1.3 | — | μs | — |

Table 57. I²C AC Timing Specifications (continued)

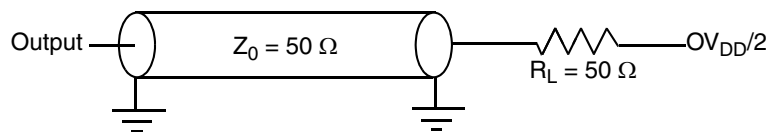
For recommended operating conditions, see Table 3.

| Parameter | Symbol ¹ | Min | Max | Unit | Note |
|---|---------------------|----------------------|-----|------|------|
| Noise margin at the LOW level for each connected device (including hysteresis) | V_{NL} | $0.1 \times OV_{DD}$ | — | V | — |
| Noise margin at the HIGH level for each connected device (including hysteresis) | V_{NH} | $0.2 \times OV_{DD}$ | — | V | — |
| Capacitive load for each bus line | Cb | — | 400 | pF | — |

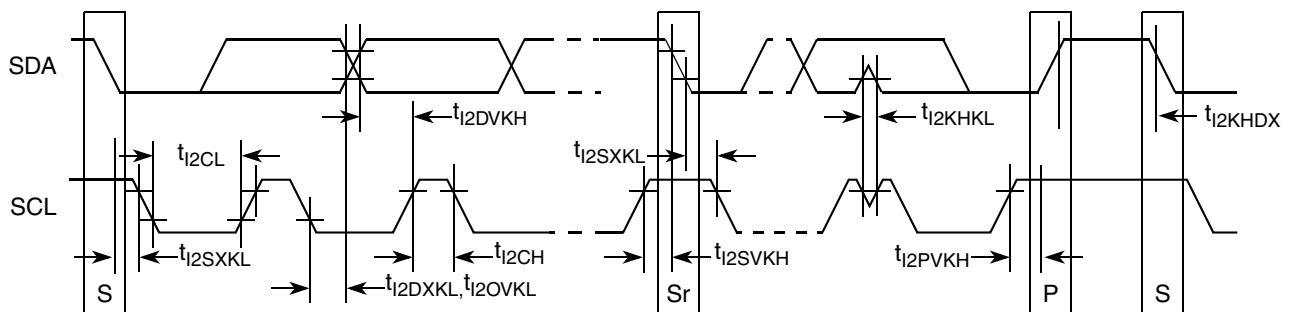
Note:

- The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
- The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, "Determining the I2C Frequency Divider Ratio for SCL."
- As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the device acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the device as transmitter, application note AN2919 referred to in note 2 above is recommended.
- The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

Figure 29. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

Figure 30. I²C Bus AC Timing Diagram

2.19 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD} , LV_{DD} or $OV_{DD} = 3.3$ V.

Table 58. GPIO DC Electrical Characteristics (CV_{DD} , LV_{DD} or $OV_{DD} = 3.3$ V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|--|----------|-----|----------|---------|------|
| Input high voltage | V_{IH} | 2.0 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($OV_{IN} = 0$ V or $OV_{IN} = OV_{DD}$) | I_{IN} | — | ± 40 | μ A | 2 |
| Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2$ mA) | V_{OH} | 2.4 | — | V | — |
| Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2$ mA) | V_{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max L/OV_{IN} respective values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the L/OV_{IN} symbol referenced in [Section 2.1.2, “Recommended Operating Conditions.”](#)

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD} or $LV_{DD} = 2.5$ V.

Table 59. GPIO DC Electrical Characteristics (CV_{DD} or $LV_{DD} = 2.5$ V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|----------|-----|----------|---------|------|
| Input high voltage | V_{IH} | 1.7 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.7 | V | 1 |
| Input current ($V_{IN} = 0$ V or $V_{IN} = LV_{DD}$) | I_{IN} | — | ± 40 | μ A | 2 |
| Output high voltage ($LV_{DD} = \text{min}$, $I_{OH} = -2$ mA) | V_{OH} | 2.0 | — | V | — |
| Output low voltage ($LV_{DD} = \text{min}$, $I_{OH} = 2$ mA) | V_{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Section 2.1.2, “Recommended Operating Conditions.”](#)

2.19.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 60. GPIO Input AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Unit | Note |
|---------------------------------|-------------|-----|------|------|
| GPIO inputs—minimum pulse width | t_{PIWID} | 20 | ns | 1 |

Note:

- GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

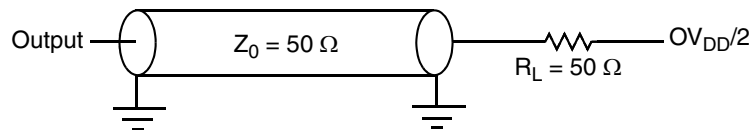


Figure 31. GPIO AC Test Load

2.20 High-Speed Serial Interfaces (HSSI)

The device features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, Serial RapidIO, Aurora, and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Electrical Characteristics

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TXn and $\overline{SD_TXn}$) or a receiver input (SD_RXn and $\overline{SD_RXn}$). Each signal swings between A volts and B volts where $A > B$.

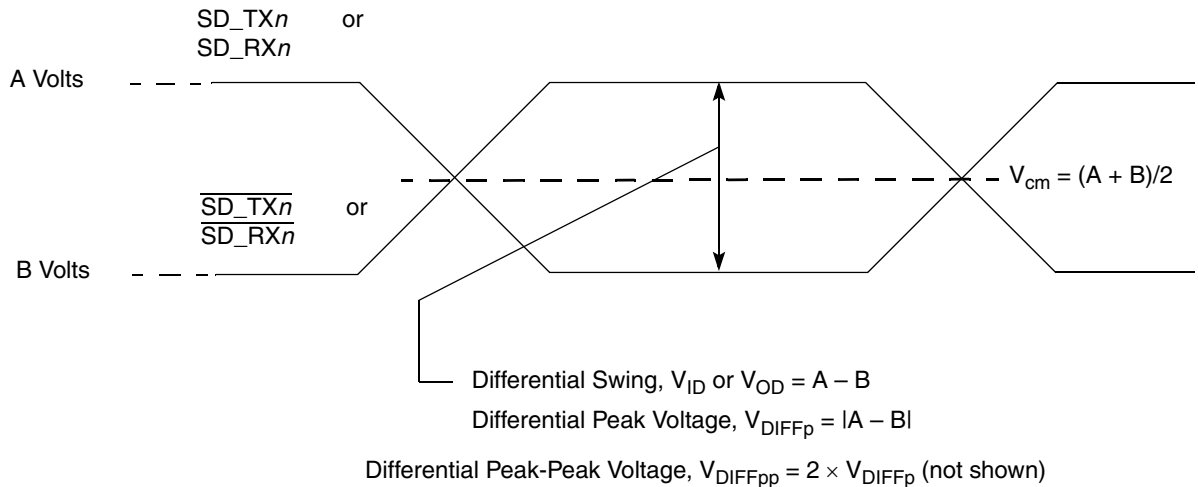


Figure 32. Differential Voltage Definitions for Transmitter or Receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing The transmitter output signals and the receiver input signals SD_TXn , $\overline{SD_TXn}$, SD_RXn and $\overline{SD_RXn}$ each have a peak-to-peak swing of $A - B$ volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing):

The differential output voltage (or swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SD_TXn} - V_{\overline{SD_TXn}}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing):

The differential input voltage (or swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SD_RXn} - V_{\overline{SD_RXn}}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{SD_TXn}$, for example) from the non-inverting signal (SD_TXn , for example) within a differential pair. There is

only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See [Figure 37](#) as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SD_TXn} + V_{\overline{SD_TXn}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and \overline{TD} . If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or \overline{TD}) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.20.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK1 and $\overline{SD_REF_CLK1}$ for SerDes bank1 and SD_REF_CLK2 and $\overline{SD_REF_CLK2}$ for SerDes bank2.

SerDes banks 1–2 may be used for various combinations of the following IP blocks based on the RCW configuration field $SRDS_PRTCL$:

- SerDes bank 1: PCI Express 1/2/3, sRIO1/2, SGMII (1.25 Gbps only).
- SerDes bank 2: PCI Express3, SGMII (1.25 or 3.125 GBaud), SATA or Aurora.

The following sections describe the SerDes reference clock requirements and provide application information.

2.20.2.1 SerDes Reference Clock Receiver Characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

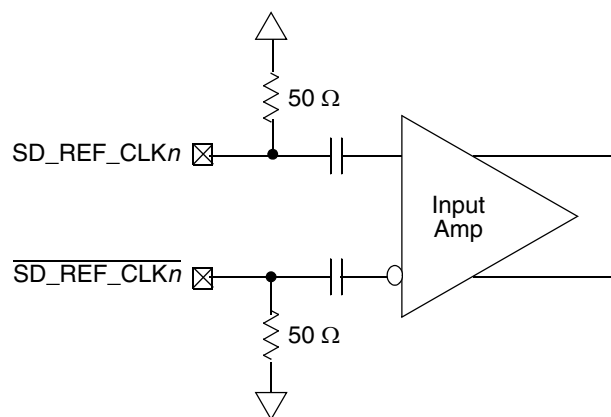


Figure 33. Receiver of SerDes Reference Clocks

Electrical Characteristics

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements (SV_{DD}) are as specified in [Section 2.1.2, “Recommended Operating Conditions.”](#)
- The SerDes reference clock receiver reference circuit structure is as follows:
 - The SD_REF_CLKn and $\overline{SD_REF_CLKn}$ are internally AC-coupled differential inputs as shown in [Figure 33](#). Each differential clock input (SD_REF_CLKn or $\overline{SD_REF_CLKn}$) has on-chip 50- Ω termination to SGND followed by on-chip AC-coupling.
 - The external reference clock driver must be able to drive this termination.
 - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
 - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
 - This current limitation sets the maximum common mode input voltage to be less than 0.4 V ($0.4\text{ V} \div 50 = 8\text{ mA}$) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
 - If the device driving the SD_REF_CLKn and $\overline{SD_REF_CLKn}$ inputs cannot drive 50 Ω to SGND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
 - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
 - For an external DC-coupled connection, as described in [Section 2.20.2.1, “SerDes Reference Clock Receiver Characteristics,”](#) the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. This figure shows the SerDes reference clock input requirement for DC-coupled connection scheme.

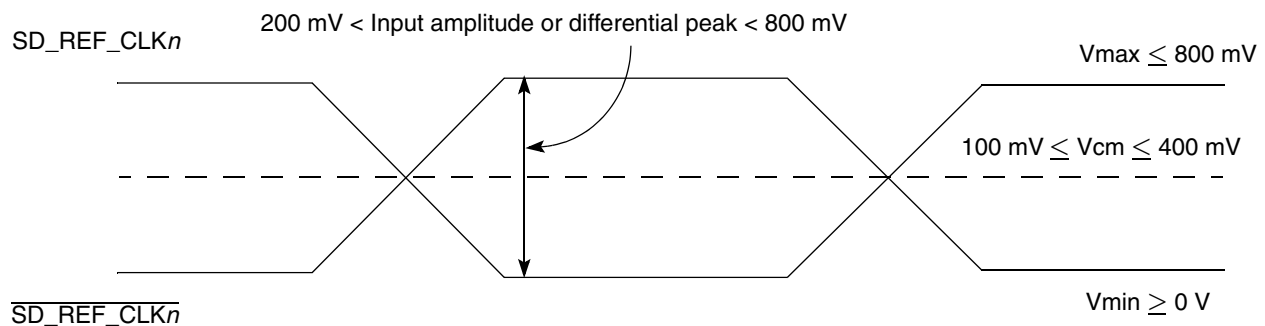


Figure 34. Differential Reference Clock Input DC Requirements (External DC-Coupled)

- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND). This figure shows the SerDes reference clock input requirement for AC-coupled connection scheme.

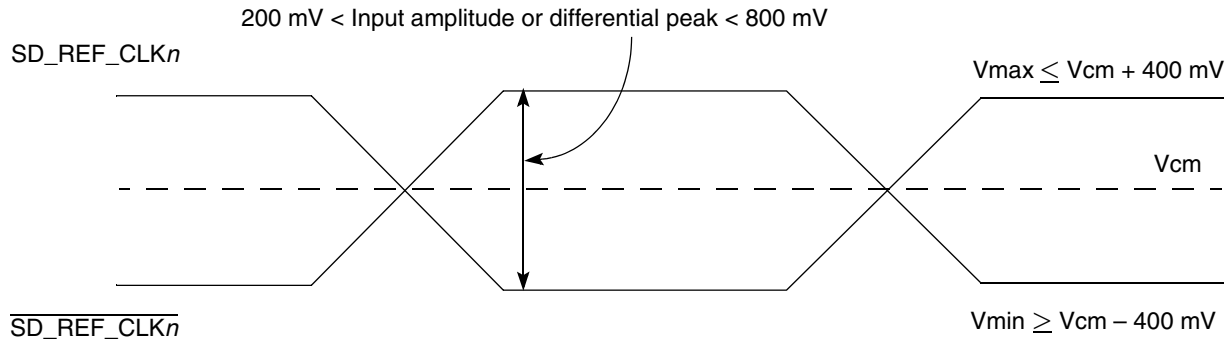


Figure 35. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
 - The reference clock can also be single-ended. The SD_REF_CLKn input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD_REF_CLKn}}$ either left unconnected or tied to ground.
 - The SD_REF_CLKn input average voltage must be between 200 and 400 mV. Figure 36 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD_REF_CLKn}}$) through the same source impedance as the clock input (SD_REF_CLKn) in use.

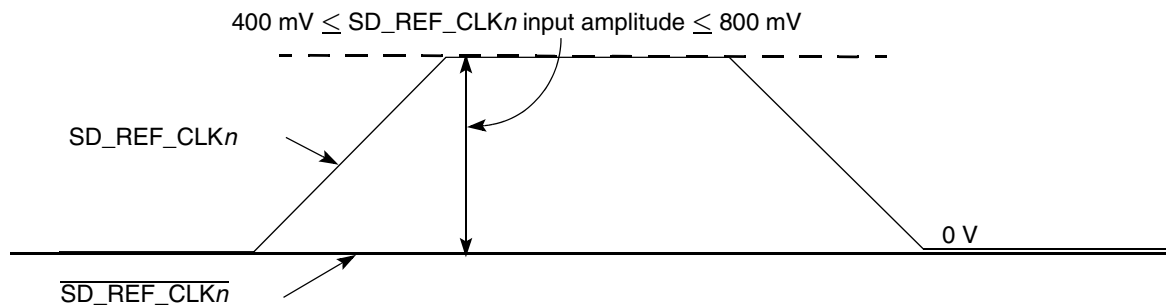


Figure 36. Single-Ended Reference Clock Input DC Requirements

2.20.2.3 AC Requirements for SerDes Reference Clocks

This table lists AC requirements for the PCI Express, SGMII, Serial RapidIO, SATA and Aurora SerDes reference clocks to be guaranteed by the customer's application design.

Table 61. SD_REF_CLK n and $\overline{\text{SD_REF_CLK}}_n$ Input Clock Requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|------|----------------|------|------|------|
| SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ frequency range | t _{CLK_REF} | — | 100/125/156.25 | — | MHz | 1 |
| SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ clock frequency tolerance | t _{CLK_TOL} | -350 | — | 350 | ppm | — |
| SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ reference clock duty cycle | t _{CLK_DUTY} | 40 | 50 | 60 | % | 4 |
| SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ max deterministic peak-peak jitter at 10 ⁻⁶ BER | t _{CLK_DJ} | — | — | 42 | ps | — |
| SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ total reference clock jitter at 10 ⁻⁶ BER (peak-to-peak jitter at refClk input) | t _{CLK_TJ} | — | — | 86 | ps | 2 |
| SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ rising/falling edge rate | t _{CLKRRR} /t _{CLKFR} | 1 | — | 4 | V/ns | 3 |
| Differential input high voltage | V _{IH} | 200 | — | — | mV | 4 |
| Differential input low voltage | V _{IL} | — | — | -200 | mV | 4 |
| Rising edge rate (SD_REF_CLK n) to falling edge rate ($\overline{\text{SD_REF_CLK}}_n$) matching | Rise-Fall Matching | — | — | 20 | % | 5, 6 |

Note:

- Caution:** Only 100, 125 and 156.25 have been tested. In-between values do not work correctly with the rest of the system.
- Limits from PCI Express CEM Rev 2.0
- Measured from -200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK n minus $\overline{\text{SD_REF_CLK}}_n$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See [Figure 37](#).
- Measurement taken from differential waveform
- Measurement taken from single-ended waveform
- Matching applies to rising edge for SD_REF_CLK n and falling edge rate for $\overline{\text{SD_REF_CLK}}_n$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK n rising meets $\overline{\text{SD_REF_CLK}}_n$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK n must be compared to the fall edge rate of $\overline{\text{SD_REF_CLK}}_n$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See [Figure 38](#).

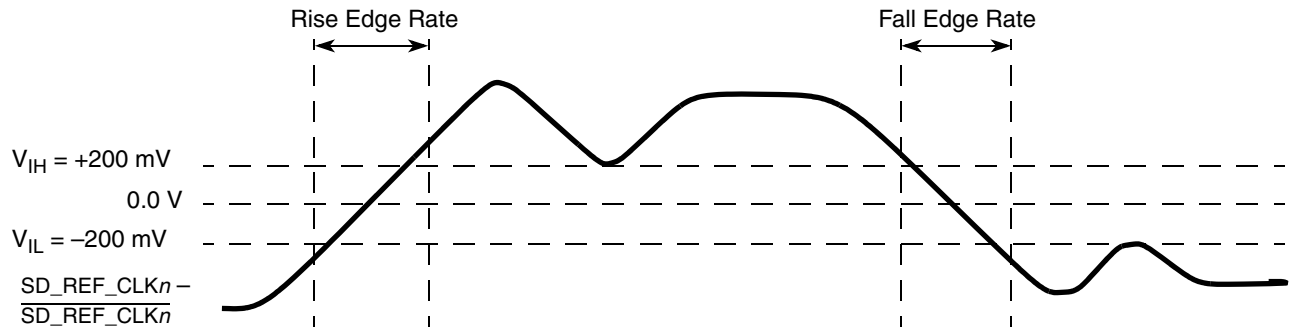


Figure 37. Differential Measurement Points for Rise and Fall Time

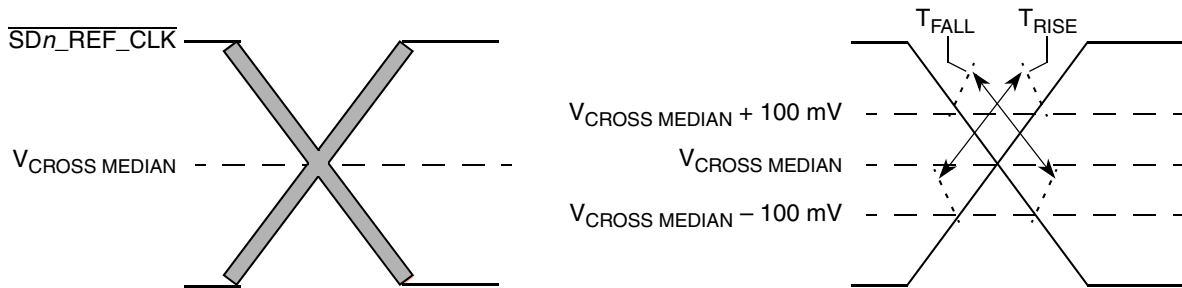


Figure 38. Single-Ended Measurement Points for Rise and Fall Time Matching

2.20.2.4 Spread Spectrum Clock

$\overline{SD_REF_CLK1}/SD_REF_CLK1$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

$\overline{SD_REF_CLK2}/SD_REF_CLK2$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and the industry protocol specifications supports it. For better results, a source without significant unintended modulation must be used.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane’s transmitter and receiver.

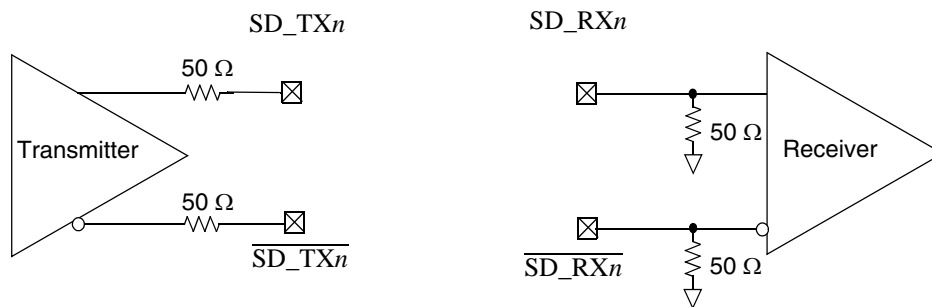


Figure 39. SerDes Transmitter and Receiver Reference Circuits

Electrical Characteristics

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- [Section 2.20.4, “PCI Express”](#)
- [Section 2.20.5, “Serial RapidIO \(sRIO\)”](#)
- [Section 2.20.6, “Aurora”](#)
- [Section 2.20.7, “Serial ATA \(SATA\)”](#)
- [Section 2.20.8, “SGMII Interface”](#)

2.20.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

2.20.4.1 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

2.20.4.2 PCI Express Clocking Requirements for $\overline{\text{SD_REF_CLK}}_n$ and SD_REF_CLK_n

SerDes banks 1–2 ($\text{SD_REF_CLK}[1:2]$ and $\overline{\text{SD_REF_CLK}}[1:2]$) may be used for various SerDes PCI Express configurations based on the RCW configuration field SRDS_PRTCL .

For more information on these specifications, see [Section 2.20.2, “SerDes Reference Clocks.”](#)

2.20.4.3 PCI Express DC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.3.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 62. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output DC Specifications
($XV_{DD} = 1.5 \text{ V or } 1.8 \text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|--------------------------|-----|---------|------|----------|--|
| Differential peak-to-peak output voltage | $V_{\text{TX-DIFFp-p}}$ | 800 | — | 1200 | mV | $V_{\text{TX-DIFFp-p}} = 2 \times V_{\text{TX-D+}} - V_{\text{TX-D-}} $ See Note 1. |
| De-emphasized differential output voltage (ratio) | $V_{\text{TX-DE-RATIO}}$ | 3.0 | 3.5 | 4.0 | dB | Ratio of the $V_{\text{TX-DIFFp-p}}$ of the second and following bits after a transition divided by the $V_{\text{TX-DIFFp-p}}$ of the first bit after a transition. See Note 1. |
| DC differential Tx impedance | $Z_{\text{TX-DIFF-DC}}$ | 80 | 100 | 120 | Ω | Tx DC differential mode low Impedance |

Table 62. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output DC Specifications
($XV_{DD} = 1.5\text{ V}$ or 1.8 V) (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|--------------------------|-------------|-----|---------|-----|----------|---|
| Transmitter DC impedance | Z_{TX-DC} | 40 | 50 | 60 | Ω | Required Tx D+ as well as D– DC Impedance during all states |

Note:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 63. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output DC Specifications
($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|--|-------------------------|-----|---------|------|----------|--|
| Differential peak-to-peak output voltage | $V_{TX-DIFFp-p}$ | 800 | — | 1200 | mV | $V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $ See Note 1. |
| Low power differential peak-to-peak output voltage | $V_{TX-DIFFp-p_low}$ | 400 | 500 | 1200 | mV | $V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $ See Note 1. |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO-3.5dB}$ | 3.0 | 3.5 | 4.0 | dB | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1. |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO-6.0dB}$ | 5.5 | 6.0 | 6.5 | dB | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1. |
| DC differential Tx impedance | $Z_{TX-DIFF-DC}$ | 80 | 100 | 120 | Ω | Tx DC differential mode low impedance |
| Transmitter DC Impedance | Z_{TX-DC} | 40 | 50 | 60 | Ω | Required Tx D+ as well as D– DC impedance during all states |

Note:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2.20.4.4 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications 2.5 GT/s, and 5 GT/s.

Electrical Characteristics

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 64. PCI Express 2.0 (2.5 GT/s) Differential Receiver (Rx) Input DC Specifications ($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---------------------------|------|-----|------|----------|--|
| Differential input peak-to-peak voltage | $V_{RX-DIFFp-p}$ | 120 | — | 1200 | mV | $V_{RX-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ See Note 1. |
| DC differential input impedance | $Z_{RX-DIFF-DC}$ | 80 | 100 | 120 | Ω | Rx DC differential mode impedance. See Note 2 |
| DC input impedance | Z_{RX-DC} | 40 | 50 | 60 | Ω | Required Rx D+ as well as D- DC Impedance ($50 \pm 20\%$ tolerance). See Notes 1 and 2. |
| Powered down DC input impedance | $Z_{RX-HIGH-IMP-DC}$ | 50 k | — | — | Ω | Required Rx D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3. |
| Electrical idle detect threshold | $V_{RX-IDLE-DET-DIFFp-p}$ | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the receiver |

Note:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 65. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input DC Specifications ($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|----------------------|-----|-----|------|------------|---|
| Differential input peak-to-peak voltage | $V_{RX-DIFFp-p}$ | 120 | — | 1200 | V | $V_{RX-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ See Note 1. |
| DC differential input impedance | $Z_{RX-DIFF-DC}$ | 80 | 100 | 120 | Ω | Rx DC Differential mode impedance. See Note 2 |
| DC input impedance | Z_{RX-DC} | 40 | 50 | 60 | Ω | Required Rx D+ as well as D- DC Impedance ($50 \pm 20\%$ tolerance). See Notes 1 and 2. |
| Powered down DC input impedance | $Z_{RX-HIGH-IMP-DC}$ | 50 | — | — | k Ω | Required Rx D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 3. |

Table 65. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input DC Specifications ($V_{DD} = 1.5 \text{ V}$ or 1.8 V) (continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|----------------------------------|---------------------------|-----|-----|-----|------|--|
| Electrical idle detect threshold | $V_{RX-IDLE-DET-DIFFp-p}$ | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the receiver |

Note:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

2.20.4.5 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.5.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 66. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output AC Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|-----------------------------------|--------|-----|--------|------|--|
| Unit interval | UI | 399.88 | 400 | 400.12 | ps | Each UI is $400 \text{ ps} \pm 300 \text{ ppm}$. UI does not account for spread spectrum clock dictated variations. See note 1. |
| Minimum Tx eye width | T_{TX-EYE} | 0.75 | — | — | UI | The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25 \text{ UI}$. Does not include spread spectrum or RefCLK jitter. Includes device random jitter at 10^{-12} . See notes 2 and 3. |
| Maximum time between the jitter median and maximum deviation from the median | $T_{TX-EYE-MEDIAN-TO-MAX-JITTER}$ | — | — | 0.125 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0 \text{ V}$) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3. |
| AC coupling capacitor | C_{TX} | 75 | — | 200 | nF | All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4. |

Electrical Characteristics

Table 66. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output AC Specifications (continued)

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|-----------|--------|-----|-----|-----|------|------|
|-----------|--------|-----|-----|-----|------|------|

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 40 and measured over any 250 consecutive Tx UIs.
3. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 67. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output AC Specifications

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------------------|-------------------|--------|--------|--------|------|---|
| Unit interval | UI | 199.94 | 200.00 | 200.06 | ps | Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1. |
| Minimum Tx eye width | T_{TX-EYE} | 0.75 | — | — | UI | The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See Notes 2 and 3. |
| Tx RMS deterministic jitter > 1.5 MHz | $T_{TX-HF-DJ-DD}$ | — | — | 0.15 | ps | — |
| Tx RMS deterministic jitter < 1.5 MHz | $T_{TX-LF-RMS}$ | — | 3.0 | — | ps | Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps |
| AC coupling capacitor | C_{TX} | 75 | — | 200 | nF | All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4. |

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 40 and measured over any 250 consecutive Tx UIs.
3. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

2.20.4.5.2 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications 2.5 GT/s and 5 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 68. PCI Express 2.0 (2.5 GT/s) Differential Receiver (Rx) Input AC Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|-----------------------------------|--------|--------|--------|------|---|
| Unit Interval | UI | 399.88 | 400.00 | 400.12 | ps | Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1. |
| Minimum receiver eye width | T_{RX-EYE} | 0.4 | — | — | UI | The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3. |
| Maximum time between the jitter median and maximum deviation from the median. | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | — | — | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See Notes 2, 3, and 4. |

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in [Figure 40](#) must be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 69. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input AC Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|----------------|--------|--------|--------|------|---|
| Unit Interval | UI | 199.40 | 200.00 | 200.06 | ps | Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1. |
| Max Rx inherent timing error | $T_{RX-TJ-CC}$ | — | — | 0.4 | UI | The maximum inherent total timing error for common RefClk Rx architecture |
| Maximum time between the jitter median and maximum deviation from the median | $T_{RX-TJ-DC}$ | — | — | 0.34 | UI | Max Rx inherent total timing error |

Electrical Characteristics

Table 69. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input AC Specifications (continued)

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|-------------------|-----|-----|------|------|---|
| Max Rx inherent deterministic timing error | $T_{RX-DJ-DD-CC}$ | — | — | 0.30 | UI | The maximum inherent deterministic timing error for common RefClk Rx architecture |
| Max Rx inherent deterministic timing error | $T_{RX-DJ-DD-DC}$ | — | — | 0.24 | UI | The maximum inherent deterministic timing error for common RefClk Rx architecture |

Note:

1. No test load is necessarily associated with this value.

2.20.4.6 Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in this figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

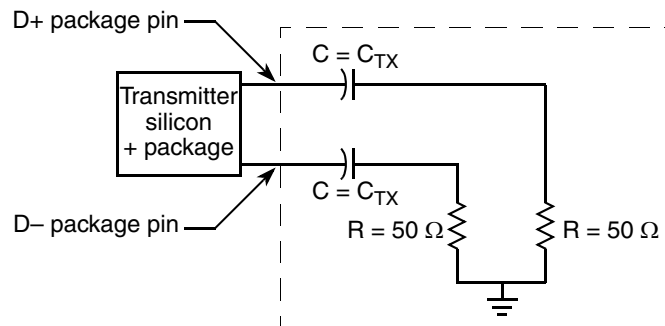


Figure 40. Test/Measurement Load

2.20.5 Serial RapidIO (sRIO)

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates: 2.50, 3.125, and 5 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter must be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ± 100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

2.20.5.1 Signal Definitions

This section defines the terms used in the description and specification of the differential signals used by the LP-Serial links. This figure shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where $A > B$. Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals—TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ —each have a peak-to-peak swing of $A - B$ volts.
- The differential output signal of the transmitter, V_{OD} , is defined as $V_{\text{TD}} - V_{\overline{\text{TD}}}$
- The differential input signal of the receiver, V_{ID} , is defined as $V_{\text{RD}} - V_{\overline{\text{RD}}}$
- The differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ volts
- The peak value of the differential transmitter output signal and the differential receiver input signal is $A - B$ volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A - B)$ volts.

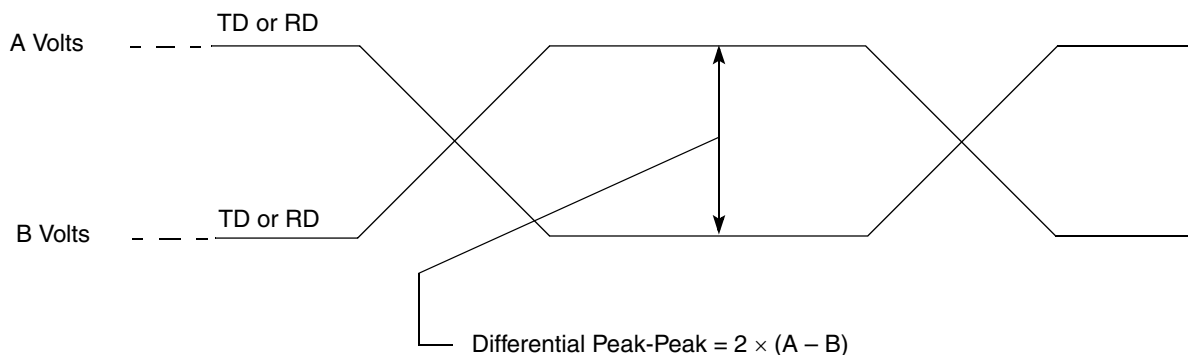


Figure 41. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V, and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.20.5.2 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- Pre-emphasis on the transmitter
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.

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- The use of active circuits in the receiver, often referred to as adaptive equalization.

2.20.5.3 Serial RapidIO Clocking Requirements for SD_REF_CLK_n and SD_REF_CLK_n

SerDes bank 1 (SD_REF_CLK1 and $\overline{\text{SD_REF_CLK1}}$) may be used for various SerDes Serial RapidIO configurations based on the RCW configuration field SRDS_PRTCL. Serial RapidIO is not supported on SerDes banks 2.

For more information on these specifications, see [Section 2.20.2, “SerDes Reference Clocks.”](#)

2.20.5.4 DC Requirements for Serial RapidIO

This section explains the DC requirements for the Serial RapidIO interface.

2.20.5.4.1 DC Serial RapidIO Timing Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case is better than the following:

- -10 dB for $(\text{Baud Frequency}) \div 10 < \text{Freq}(f) < 625 \text{ MHz}$
- $-10 \text{ dB} + 10\log(f \div 625 \text{ MHz}) \text{ dB}$ for $625 \text{ MHz} \leq \text{Freq}(f) \leq \text{Baud Frequency}$

The reference impedance for the differential return loss measurements is 100- Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 20 ps at 2.50 GBaud and 15 ps at 3.125 GBaud and XX ps at 5 GBaud.

This table defines the transmitter DC specifications for Serial RapidIO operating at $XV_{DD} = 1.5 \text{ V}$ or 1.8 V .

Table 70. Serial RapidIO Transmitter DC Timing Specifications—2.5 GBaud, 3.125 GBaud, 5 GBaud

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------------------|---------------------|-------|-----|------|--------|------|
| Output voltage | V_O | -0.40 | — | 2.30 | V | 1 |
| Long-run differential output voltage | V_{DIFFPP} | 800 | — | 1600 | mV p-p | — |
| Short-run differential output voltage | V_{DIFFPP} | 500 | — | 1000 | mV p-p | — |

Note:

1. Voltage relative to COMMON of either signal comprising a differential pair.

2.20.5.4.2 DC Serial RapidIO Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to $(0.8) \times (\text{Baud Frequency})$. This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100- Ω resistive for differential return loss and 25- Ω resistive for common mode.

This table defines the receiver DC specifications for Serial RapidIO operating at $XV_{DD} = 1.5\text{ V}$ or 1.8 V .

Table 71. Serial RapidIO Receiver DC Timing Specifications—2.5 GBaud, 3.125 GBaud, 5 GBaud

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|----------------------------|----------|-----|-----|------|--------|------|
| Differential input voltage | V_{IN} | 200 | — | 1600 | mV p-p | 1 |

Note:

1. Measured at the receiver.

2.20.5.5 AC Requirements for Serial RapidIO

This section explains the AC requirements for the Serial RapidIO interface.

2.20.5.5.1 AC Requirements for Serial RapidIO Transmitter

This table defines the transmitter AC specifications for the Serial RapidIO interface. The AC timing specifications do not include RefClk jitter.

Table 72. Serial RapidIO Transmitter AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit |
|----------------------------|--------|--------------|---------|--------------|--------|
| Deterministic jitter | J_D | — | — | 0.17 | UI p-p |
| Total jitter | J_T | — | — | 0.35 | UI p-p |
| Unit interval: 2.5 GBaud | UI | 400 – 100ppm | 400 | 400 + 100ppm | ps |
| Unit interval: 3.125 GBaud | UI | 320 – 100ppm | 320 | 320 + 100ppm | ps |

This table defines the receiver AC specifications for Serial RapidIO. The AC timing specifications do not include RefClk jitter.

Table 73. Serial RapidIO Receiver AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|--|----------|--------------|---------|--------------|--------|------|
| Deterministic jitter tolerance | J_D | 0.37 | — | — | UI p-p | 1 |
| Combined deterministic and random jitter tolerance | J_{DR} | 0.55 | — | — | UI p-p | 1 |
| Total jitter tolerance ² | J_T | 0.65 | — | — | UI p-p | 1 |
| Bit error rate | BER | — | — | 10^{-12} | — | — |
| Unit interval: 2.5 GBaud | UI | 400 – 100ppm | 400 | 400 + 100ppm | ps | — |
| Unit interval: 3.125 GBaud | UI | 320 – 100ppm | 320 | 320 + 100ppm | ps | — |

Note:

1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 42](#). The sinusoidal jitter component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.

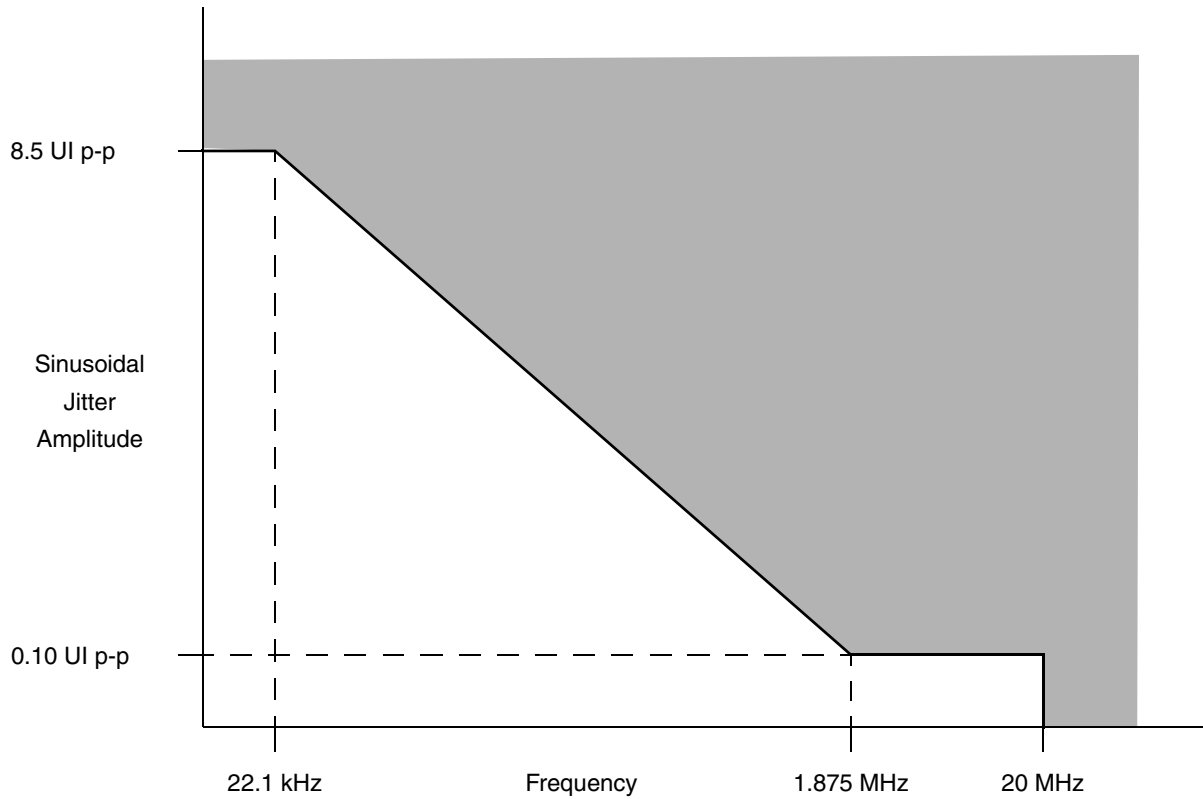


Figure 42. Single-Frequency Sinusoidal Jitter Limits

2.20.6 Aurora

This section describes the Aurora clocking requirements and AC and DC electrical characteristics.

2.20.6.1 Aurora DC Electrical Characteristics

This section describes the DC electrical characteristics for Aurora.

2.20.6.1.1 Aurora DC Clocking Requirements for $\overline{SD_REF_CLKn}$ and $\overline{SD_REF_CLKn}$

Only SerDes bank 2 ($\overline{SD_REF_CLK2}$ and $\overline{SD_REF_CLK2}$) may be used for SerDes Aurora configurations based on the RCW configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 1.

For more information on these specifications, see [Section 2.20.2, “SerDes Reference Clocks.”](#)

2.20.6.1.2 Aurora Transmitter DC Electrical Characteristics

This table provides the Aurora transmitter DC electrical characteristics ($XV_{DD} = 1.5\text{ V}$ or 1.8 V).

Table 74. Aurora Transmitter DC Electrical Characteristics ($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit |
|-----------------------------|--------------|-----|---------|------|--------|
| Differential output voltage | V_{DIFFPP} | 800 | — | 1600 | mV p-p |

2.20.6.1.3 Aurora Receiver DC Electrical Characteristics

This table provides the Aurora receiver DC electrical characteristics ($XV_{DD} = 1.5\text{ V}$ or 1.8 V).

Table 75. Aurora Receiver DC Electrical Characteristics ($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|----------------------------|----------|-----|---------|------|--------|------|
| Differential input voltage | V_{IN} | 120 | 900 | 1200 | mV p-p | 1 |

Note:

1. Measured at receiver

2.20.6.2 Aurora AC Timing Specifications

This section describes the AC timing specifications for Aurora.

2.20.6.2.1 Aurora AC Clocking Requirements for SD_REF_CLKn and $\overline{SD_REF_CLKn}$

Only SerDes bank 2 (SD_REF_CLK2 and $\overline{SD_REF_CLK2}$) may be used for SerDes Aurora configurations based on the RCW configuration field $SRDS_PRTCL$. Aurora is not supported on SerDes banks 1.

2.20.6.2.2 Aurora Transmitter AC Timing Specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 76. Aurora Transmitter AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit |
|----------------------------|--------|---------------|---------|---------------|--------|
| Deterministic jitter | J_D | — | — | 0.17 | UI p-p |
| Total jitter | J_T | — | — | 0.35 | UI p-p |
| Unit Interval: 2.5 GBaud | UI | 400 – 100 ppm | 400 | 400 + 100 ppm | ps |
| Unit Interval: 3.125 GBaud | UI | 320 – 100 ppm | 320 | 320 + 100 ppm | ps |
| Unit Interval: 5.0 GBaud | UI | 200 – 100 ppm | 200 | 200 + 100 ppm | ps |

2.20.6.2.3 Aurora Receiver AC Timing Specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 77. Aurora Receiver AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|--|----------|------|---------|------------|--------|------|
| Deterministic jitter tolerance | J_D | 0.37 | — | — | UI p-p | 1 |
| Combined deterministic and random jitter tolerance | J_{DR} | 0.55 | — | — | UI p-p | 1 |
| Total jitter tolerance | J_T | 0.65 | — | — | UI p-p | 1, 2 |
| Bit error rate | BER | — | — | 10^{-12} | — | — |

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Table 77. Aurora Receiver AC Timing Specifications (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|----------------------------|--------|---------------|---------|---------------|------|------|
| Unit Interval: 2.5 GBaud | UI | 400 – 100 ppm | 400 | 400 + 100 ppm | ps | — |
| Unit Interval: 3.125 GBaud | UI | 320 – 100 ppm | 320 | 320 + 100 ppm | ps | — |
| Unit Interval: 5.0 GBaud | UI | 200 – 100 ppm | 200 | 200 + 100 ppm | ps | — |

Note:

1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 42](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

2.20.7 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) interface.

2.20.7.1 SATA DC Electrical Characteristics

This section describes the DC electrical characteristics for SATA.

2.20.7.1.1 SATA DC Transmitter Output Characteristics

This table provides the DC differential transmitter output DC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 78. Gen1i/1.5G Transmitter (Tx) DC Specifications ($XV_{DD} = 1.5\text{ V or }1.8\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--------------------------------|----------------------|-----|-----|-----|----------|------|
| Tx differential output voltage | V_{SATA_TXDIFF} | 400 | — | 600 | mV p-p | 1 |
| Tx differential pair impedance | $Z_{SATA_TXDIFFIM}$ | 85 | 100 | 115 | Ω | 2 |

Note:

1. Terminated by 50 Ω load.
2. DC impedance

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 79. Gen 2i/3G Transmitter (Tx) DC Specifications ($XV_{DD} = 1.5\text{ V or }1.8\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--------------------------------|----------------------|-----|-----|-----|----------|------|
| Tx diff output voltage | V_{SATA_TXDIFF} | 400 | — | 700 | mV p-p | 1 |
| Tx differential pair impedance | $Z_{SATA_TXDIFFIM}$ | 85 | 100 | 115 | Ω | — |

Note:

1. Terminated by 50 Ω load.

2.20.7.1.2 SATA DC Receiver (Rx) Input Characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 80. Gen1i/1.5 G Receiver (Rx) Input DC Specifications ($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---------------------------------|--------------------|-----|---------|-----|----------|------|
| Differential input voltage | V_{SATA_RXDIFF} | 240 | — | 600 | mV p-p | 1 |
| Differential Rx input impedance | Z_{SATA_RXSEIM} | 85 | 100 | 115 | Ω | — |
| OOB signal detection threshold | V_{SATA_OOB} | 50 | 120 | 240 | mV p-p | — |

Note:

1. Voltage relative to common of either signal comprising a differential pair

This table provides the Gen2i or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 81. Gen2i/3 G Receiver (Rx) Input DC Specifications ($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---------------------------------|--------------------|-----|---------|-----|----------|------|
| Differential input voltage | V_{SATA_RXDIFF} | 275 | — | 750 | mV p-p | 1 |
| Differential Rx input impedance | Z_{SATA_RXSEIM} | 85 | 100 | 115 | Ω | 2 |
| OOB signal detection threshold | V_{SATA_OOB} | 75 | 120 | 240 | mV p-p | 2 |

Note:

1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

2.20.7.2 SATA AC Timing Specifications

This section discusses the SATA AC timing specifications.

2.20.7.2.1 AC Requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in this table to be guaranteed by the customer's application design.

Table 82. SATA Reference Clock Input Requirements

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|-----------------|------|---------|------|------|------|
| SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ frequency range | t_{CLK_REF} | — | 100/125 | — | MHz | 1 |
| SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ clock frequency tolerance | t_{CLK_TOL} | -350 | — | +350 | ppm | — |
| SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ reference clock duty cycle (measured at 1.6 V) | t_{CLK_DUTY} | 40 | 50 | 60 | % | — |

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Table 82. SATA Reference Clock Input Requirements (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|---------------|-----|-----|-----|------|---------|
| SD_REF_CLK/SD_REF_CLK cycle-to-cycle clock jitter (period jitter) | t_{CLK_CJ} | — | — | 100 | ps | 2 |
| SD_REF_CLK/SD_REF_CLK total reference clock jitter, phase jitter (peak-peak) | t_{CLK_PJ} | -50 | — | +50 | ps | 2, 3, 4 |

Note:

- Caution:** Only 100, 125 MHz have been tested. In-between values do not work correctly with the rest of the system.
- At RefClk input
- In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}
- Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.

This figure shows the reference clock timing waveform.

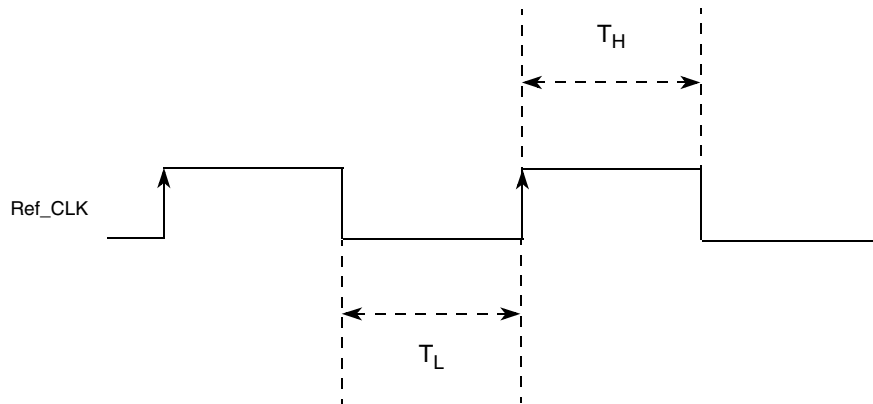


Figure 43. Reference Clock Timing Waveform

2.20.7.3 AC Transmitter Output Characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 83. Gen1i/1.5 G Transmitter (Tx) AC Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|-----------------------|----------|----------|----------|--------|------|
| Channel speed | t_{CH_SPEED} | — | 1.5 | — | Gbps | — |
| Unit Interval | T_{UI} | 666.4333 | 666.6667 | 670.2333 | ps | — |
| Total jitter data-data 5 UI | $U_{SATA_TXTJ5UI}$ | — | — | 0.355 | UI p-p | 1 |
| Total jitter, data-data 250 UI | $U_{SATA_TXTJ250UI}$ | — | — | 0.47 | UI p-p | 1 |
| Deterministic jitter, data-data 5 UI | $U_{SATA_TXDJ5UI}$ | — | — | 0.175 | UI p-p | 1 |
| Deterministic jitter, data-data 250 UI | $U_{SATA_TXDJ250UI}$ | — | — | 0.22 | UI p-p | 1 |

Table 83. Gen1i/1.5 G Transmitter (Tx) AC Specifications (continued)For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|-----------|--------|-----|-----|-----|------|------|
|-----------|--------|-----|-----|-----|------|------|

Note:

1. Measured at Tx output pins peak to peak phase variation, random data pattern

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 84. Gen 2i/3 G Transmitter (Tx) AC SpecificationsFor recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|-------------------------|----------|----------|----------|--------|------|
| Channel speed | t_{CH_SPEED} | — | 3.0 | — | Gbps | — |
| Unit Interval | T_{UI} | 333.2167 | 333.3333 | 335.1167 | ps | — |
| Total jitter $f_{C3dB} = f_{BAUD} \div 10$ | $U_{SATA_TXTJfB/10}$ | — | — | 0.3 | UI p-p | 1 |
| Total jitter $f_{C3dB} = f_{BAUD} \div 500$ | $U_{SATA_TXTJfB/500}$ | — | — | 0.37 | UI p-p | 1 |
| Total jitter $f_{C3dB} = f_{BAUD} \div 1667$ | $U_{SATA_TXTJfB/1667}$ | — | — | 0.55 | UI p-p | 1 |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$ | $U_{SATA_TXDJfB/10}$ | — | — | 0.17 | UI p-p | 1 |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$ | $U_{SATA_TXDJfB/500}$ | — | — | 0.19 | UI p-p | 1 |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$ | $U_{SATA_TXDJfB/1667}$ | — | — | 0.35 | UI p-p | 1 |

Note:

1. Measured at Tx output pins peak-to-peak phase variation, random data pattern

2.20.7.4 AC Differential Receiver Input Characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 85. Gen 1i/1.5G Receiver (Rx) AC SpecificationsFor recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|--|-----------------------|----------|----------|----------|--------|------|
| Unit Interval | T_{UI} | 666.4333 | 666.6667 | 670.2333 | ps | — |
| Total jitter data-data 5 UI | $U_{SATA_TXTJ5UI}$ | — | — | 0.43 | UI p-p | 1 |
| Total jitter, data-data 250 UI | $U_{SATA_TXTJ250UI}$ | — | — | 0.60 | UI p-p | 1 |
| Deterministic jitter, data-data 5 UI | $U_{SATA_TXDJ5UI}$ | — | — | 0.25 | UI p-p | 1 |
| Deterministic jitter, data-data 250 UI | $U_{SATA_TXDJ250UI}$ | — | — | 0.35 | UI p-p | 1 |

Note:

1. Measured at receiver.

Electrical Characteristics

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 2i/3G Receiver (Rx) AC Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|-------------------------|----------|----------|----------|--------|------|
| Unit Interval | T_{UI} | 333.2167 | 333.3333 | 335.1167 | ps | — |
| Total jitter $f_{C3dB} = f_{BAUD} \div 10$ | $U_{SATA_TXTJfB/10}$ | — | — | 0.46 | UI p-p | 1 |
| Total jitter $f_{C3dB} = f_{BAUD} \div 500$ | $U_{SATA_TXTJfB/500}$ | — | — | 0.60 | UI p-p | 1 |
| Total jitter $f_{C3dB} = f_{BAUD} \div 1667$ | $U_{SATA_TXTJfB/1667}$ | — | — | 0.65 | UI p-p | 1 |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$ | $U_{SATA_TXDJfB/10}$ | — | — | 0.35 | UI p-p | 1 |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$ | $U_{SATA_TXDJfB/500}$ | — | — | 0.42 | UI p-p | 1 |
| Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$ | $U_{SATA_TXDJfB/1667}$ | — | — | 0.35 | UI p-p | 1 |

Note:

1. Measured at receiver.

2.20.8 SGMII Interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the device, as shown in [Figure 44](#), where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50- Ω output impedance. Each input of the SerDes receiver differential pair features 50- Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in [Figure 39](#).

2.20.8.0.1 SGMII Clocking Requirements for $\overline{SD_REF_CLKn}$ and $\overline{SD_REF_CLKn}$

When operating in SGMII mode, the EC_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on $\overline{SD_REF_CLK[1:2]}$ and $\overline{SD_REF_CLK[1:2]}$ pins. SerDes banks 1–2 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see [Section 2.20.2, “SerDes Reference Clocks.”](#)

2.20.8.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.20.8.1.1 SGMII Transmit DC Timing Specifications

This table describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics for 1.25 GBaud. Transmitter DC characteristics are measured at the transmitter outputs ($\overline{SD_TXn}$ and $\overline{SD_TXn}$) as shown in [Figure 45](#).

Table 87. SGMII DC Transmitter Electrical Characteristics ($XV_{DD} = 1.5\text{ V or }1.8\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------|----------|--------------------|-----|-----------------------------|------|------|
| Output high voltage | V_{OH} | — | — | $1.5 \times V_{OD} _{max}$ | mV | 1 |
| Output low voltage | V_{OL} | $ V_{OD} _{min}/2$ | — | — | mV | 1 |

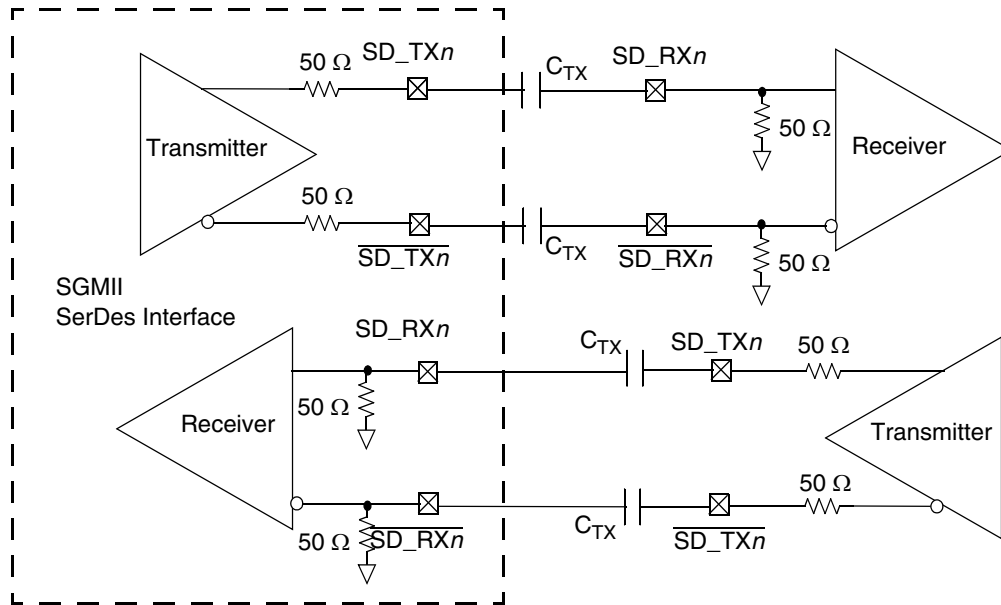
Table 87. SGMII DC Transmitter Electrical Characteristics ($XV_{DD} = 1.5\text{ V}$ or 1.8 V) (continued)

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|------------|------------------------------------|-------|-------|------|---|
| Output differential voltage ^{2, 3, 4} (XV_{DD-Typ} at 1.5 V and 1.8 V) | $ V_{OD} $ | 320 | 500.0 | 725.0 | mV | B(1-2)TECR(lane)0[AMP_RED] =0b000000 |
| | | 293.8 | 459.0 | 665.6 | | B(1-2)TECR(lane)0[AMP_RED] =0b000010 |
| | | 266.9 | 417.0 | 604.7 | | B(1-2)TECR(lane)0[AMP_RED] =0b000101 |
| | | 240.6 | 376.0 | 545.2 | | B(1-2)TECR(lane)0[AMP_RED] =0b001000 |
| | | 213.1 | 333.0 | 482.9 | | B(1-2)TECR(lane)0[AMP_RED] =0b001100 |
| | | 186.9 | 292.0 | 423.4 | | B(1-2)TECR(lane)0[AMP_RED] =0b001111 |
| | | 160.0 | 250.0 | 362.5 | | B(1-2)TECR(lane)0[AMP_RED] =0b010011 |
| | | Output impedance (single-ended) | R_O | 40 | | 50 |

Note:

- This does not align to DC-coupled SGMII.
- $V_{OD} = |V_{SD_TXn} - V_{SD_TXn}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 * |V_{OD}|$.
- Example amplitude reduction setting for SGMII on SerDes bank 1 lane E: B1TECRE0[AMP_RED] = 0b000010 for an output differential voltage of 459 mV typical.
- The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XV_{DD_SRDSn-Typ} = 1.5\text{ V}$ or 1.8 V , no common mode offset variation. SerDes transmitter is terminated with $100\text{-}\Omega$ differential load between SD_TXn and SD_TXn .

**Figure 44. 4-Wire AC-Coupled SGMII Serial Link Connection Example**

Electrical Characteristics

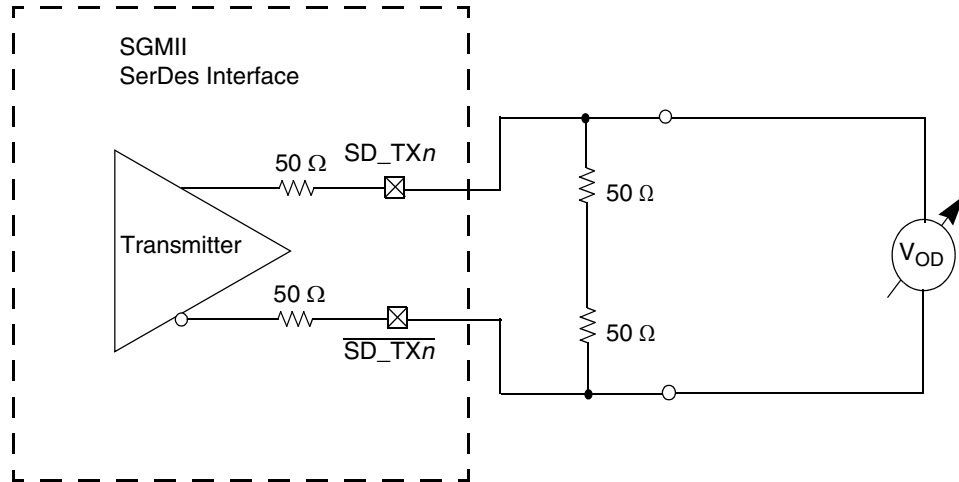


Figure 45. SGMII Transmitter DC Measurement Circuit

This table defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 GBaud.

Table 88. SGMII 2.5x Transmitter DC Electrical Characteristics ($XV_{DD} = 1.5\text{ V or }1.8\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|-----------------------------|--------------|-------|---------|------|--------|------|
| Output voltage | V_O | -0.40 | — | 2.30 | V | 1 |
| Differential output voltage | V_{DIFFPP} | 800 | — | 1600 | mV p-p | — |

Note:

1. Absolute output voltage limit

2.20.8.1.2 SGMII DC Receiver Electrical Characteristics

This table lists the SGMII DC receiver electrical characteristics for 1.25 GBaud. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 89. SGMII DC Receiver Electrical Characteristics ($XV_{DD} = 1.5\text{ V or }1.8\text{ V}$)

For recommended operating conditions, see [Table 3](#).

| Parameter | | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------------------|-------------------|-------------------|-----|-----|------|----------|------|
| DC Input voltage range | | — | N/A | | | — | 1 |
| Input differential voltage | REIDL_CTL = 001xx | $V_{RX_DIFFp-p}$ | 100 | — | 1200 | mV | 2, 4 |
| | REIDL_CTL = 100xx | | 175 | — | | | |
| Loss of signal threshold | REIDL_CTL = 001xx | V_{LOS} | 30 | — | 100 | mV | 3, 4 |
| | REIDL_CTL = 100xx | | 65 | — | 175 | | |
| Receiver differential input impedance | | Z_{RX_DIFF} | 80 | — | 120 | Ω | — |

Table 89. SGMII DC Receiver Electrical Characteristics ($XV_{DD} = 1.5\text{ V}$ or 1.8 V) (continued)For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|-----------|--------|-----|-----|-----|------|------|
|-----------|--------|-----|-----|-----|------|------|

Note:

1. Input must be externally AC coupled.
2. $V_{RX_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to [Section 2.20.4.4, “PCI Express DC Physical Layer Receiver Specifications,”](#) and [Section 2.20.4.5.2, “PCI Express AC Physical Layer Receiver Specifications,”](#) for further explanation.
4. The REIDL_CTL shown in the table refers to the chip's SerDes control register B(1–3)GCR(lane)1[REIDL_CTL] bit field.

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

Table 90. SGMII 2.5x Receiver DC Timing Specifications ($XV_{DD} = 1.5\text{ V}$ or 1.8 V)For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|----------------------------|----------|-----|---------|------|--------|------|
| Differential input voltage | V_{IN} | 200 | 900 | 1600 | mV p-p | 1 |

Note:

1. Measured at the receiver.

2.20.8.2 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

2.20.8.2.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 91. SGMII Transmit AC Timing SpecificationsFor recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|----------------------------|----------|---------------|-----|---------------|--------|------|
| Deterministic jitter | JD | — | — | 0.17 | UI p-p | — |
| Total jitter | JT | — | — | 0.35 | UI p-p | 1 |
| Unit interval: 1.25 GBaud | UI | 800 – 100 ppm | 800 | 800 + 100 ppm | ps | — |
| Unit interval: 3.125 GBaud | UI | 320 – 100 ppm | 320 | 320 + 100 ppm | ps | — |
| AC coupling capacitor | C_{TX} | 10 | | 200 | nF | 2 |

Note:

1. See [Figure 42](#) for single frequency sinusoidal jitter measurements.
2. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.20.8.2.2 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TXn and $\overline{SD_TXn}$) or at the receiver inputs (SD_RXn and $\overline{SD_RXn}$) respectively, as depicted in this figure.

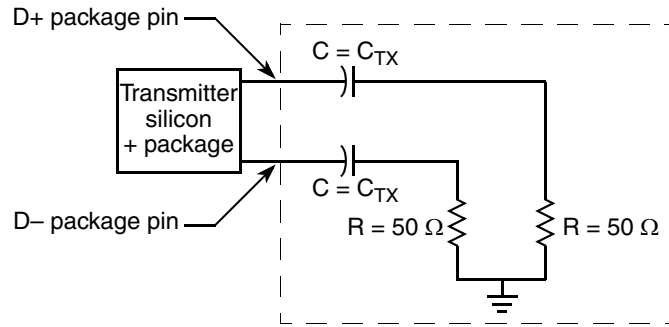


Figure 46. SGMII AC Test/Measurement Load

2.20.8.2.3 SGMII Receiver AC Timing Specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 92. SGMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|--------|---------------|-----|---------------|--------|---------|
| Deterministic jitter tolerance | JD | 0.37 | — | — | UI p-p | 1, 2 |
| Combined deterministic and random jitter tolerance | JDR | 0.55 | — | — | UI p-p | 1, 2 |
| Total jitter tolerance | JT | 0.65 | — | — | UI p-p | 1, 2, 3 |
| Bit error ratio | BER | — | — | 10^{-12} | — | — |
| Unit Interval: 1.25 GBaud | UI | 800 – 100 ppm | 800 | 800 + 100 ppm | ps | 1 |
| Unit Interval: 3.125 GBaud | UI | 320 – 100 ppm | 320 | 320 + 100 ppm | ps | 1 |

Note:

1. Measured at receiver
2. Refer to RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 42. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 42.

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 System Clocking

This section describes the PLL configuration of the device.

This device includes six PLLs, as follows:

- There are two selectable core cluster PLLs that generate a core clock from the externally supplied SYSCLK input. Core complex 0–1 and platform can select from CC1 PLL; core complex 2–3 can select from CC2 PLL. The frequency ratio between the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Section 3.1.3,

“e500mc Core Cluster to SYSCLK PLL Ratio.” The frequency for each core complex 0–3 is selected using the configuration bits as described in Table 96.

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, “Platform to SYSCLK PLL Ratio.”
- The DDR block PLL generates the DDR clock from the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode). The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in Section 3.1.5, “DDR Controller PLL Ratios.”
- Each of the three SerDes blocks has a PLL which generate a core clock from their respective externally supplied SD_REF_CLK_n/SD_REF_CLK_n inputs. The frequency ratio is selected using the SerDes PLL ratio configuration bits as described in Section 3.1.6, “Frequency Options.”

3.1.1 Clock Ranges

This table provides the clocking specifications for the processor core, platform, memory, and local bus.

Table 93. Processor Clocking Specifications

| Parameter | Maximum Processor Core Frequency | | | | | | | | Unit | Note |
|----------------------------|----------------------------------|-----|---------|-----|----------|------|----------|------|------|---------|
| | 667 MHz | | 800 MHz | | 1000 MHz | | 1200 MHz | | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | | |
| e500mc core PLL frequency | 667 | 667 | 667 | 800 | 667 | 1000 | 667 | 1200 | MHz | 1,4 |
| e500mc core frequency | 333 | 667 | 333 | 800 | 333 | 1000 | 333 | 1200 | MHz | 4, 8 |
| Platform clock frequency | 400 | 533 | 400 | 533 | 400 | 533 | 400 | 600 | MHz | 1 |
| Memory bus clock frequency | 400 | 533 | 400 | 533 | 400 | 533 | 400 | 600 | MHz | 1,2,5,6 |
| Local bus clock frequency | — | 67 | — | 67 | — | 67 | — | 75 | MHz | 3 |
| PME | — | 267 | — | 267 | — | 267 | — | 300 | MHz | 7 |
| FMan | — | 467 | — | 467 | — | 467 | — | 500 | MHz | — |

Note:

1. **Caution:** The platform clock to SYSCLK ratio and e500-mc core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, e500mc (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR3/DDR3L data rate. DDR3 memory bus clock frequency is limited to min = 400 MHz.
3. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. See the chip reference manual for more information.
4. The e500mc core can run at e500mc core complex PLL/1 or PLL/2. With a minimum core complex PLL frequency of 667 MHz, this results in a minimum allowable e500mc core frequency of 333 MHz for PLL/2.
5. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
6. In asynchronous mode, the memory bus clock speed is dictated by its own PLL.
7. The PME runs synchronously to the platform clock, running at a frequency of platform clock/2.
8. Core frequency must be at least as fast as the platform frequency (Rev 1.1 silicon).

3.1.2 Platform to SYSCLK PLL Ratio

This table shows the allowed platform clock-to-SYSCLK ratios.

The chip platform clock frequency is always below 666 MHz frequencies; set the RCW configuration field `SYS_PLL_CFG = 0b01`.

Table 94. Platform to SYSCLK PLL Ratios

| Binary Value of <code>SYS_PLL_RAT</code> | Platform:SYSCLK Ratio |
|--|-----------------------|
| 0_0100 | 4:1 |
| 0_0101 | 5:1 |
| 0_0110 | 6:1 |
| 0_0111 | 7:1 |
| 0_1000 | 8:1 |
| 0_1001 | 9:1 |
| All Others | Reserved |

3.1.3 e500mc Core Cluster to SYSCLK PLL Ratio

The clock ratio between SYSCLK and each of the two core cluster PLLs is determined at power up by the binary value of the RCW field `CCn_PLL_RAT`. This table describes the supported ratios. Note that a core cluster PLL frequency targeting 1 GHz and above must set RCW field `CCn_PLL_CFG = 0b00` for frequency targeting below 1 GHz set `CCn_PLL_CFG = 0b01`.

This table lists the supported Core Cluster to SYSCLK ratios.

Table 95. e500mc Core Cluster PLL to SYSCLK Ratios

| Binary Value of <code>CCn_PLL_RAT</code> | Core Cluster:SYSCLK Ratio |
|--|---------------------------|
| 0_1000 | 8:1 |
| 0_1001 | 9:1 |
| 0_1010 | 10:1 |
| 0_1011 | 11:1 |
| 0_1100 | 12:1 |
| 0_1101 | 13:1 |
| 0_1110 | 14:1 |
| 0_1111 | 15:1 |
| 1_0000 | 16:1 |
| 1_0001 | 17:1 |
| 1_0010 | 18:1 |
| All Others | Reserved |

3.1.4 e500mc Core Complex PLL Select

The clock frequency of each the e500mc core 0–3 complex is determined by the binary value of the RCW field $CC_n_PLL_SEL$. These tables describe the supported ratios for each core complex 0–3, where each individual core complex can select a frequency from the table.

Table 96. e500mc Core Complex [0,1] PLL Select

| Binary Value of $C_n_PLL_SEL$ for $n=[0,1]$ | e500mc:Core Cluster Ratio |
|---|---------------------------|
| 0000 | CC1 PLL /1 |
| 0001 | CC1 PLL /2 |
| 0100 | CC2 PLL /1 |
| All Others | Reserved |

Table 97. e500mc Core Complex [2,3] PLL Select

| Binary Value of $C_n_PLL_SEL$ for $n=[0,1]$ | e500mc:Core Cluster Ratio |
|---|---------------------------|
| 0000 | CC1 PLL /1 |
| 0100 | CC2 PLL /1 |
| 0101 | CC2 PLL /2 |
| All Others | Reserved |

3.1.5 DDR Controller PLL Ratios

The single DDR memory controller complexes can be asynchronous to the platform, depending on configuration.

[Table 98](#) describes the clock ratio between the DDR memory controller PLLs and the externally supplied SYSCLK input (asynchronous mode).

In asynchronous DDR mode, the DDR data rate to SYSCLK ratios supported are listed in this table. This ratio is determined by the binary value of the RCW configuration field $MEM_PLL_RAT[10:14]$.

The RCW configuration field $MEM_PLL_CFG[8:9]$ must be set to $MEM_PLL_CFG[8:9] = 0b01$ if the applied DDR PLL reference clock frequency is greater than the cutoff frequency listed in [Table 98](#) for asynchronous DDR clock ratios; otherwise, set $MEM_PLL_CFG[8:9] = 0b00$.

NOTE

The RCW Configuration field DDR_SYNC (bit 184) must be set to 0b0 for asynchronous mode.

The RCW Configuration field DDR_RATE (bit 232) must be set to b'0 for asynchronous mode

The RCW Configuration field DDR_RSV0 (bit 234) must be set to b'0 for all ratios.

Table 98. Asynchronous DDR Clock Ratio

| Binary Value of MEM_PLL_RAT[10:14] | DDR:SYSCLK Ratio | Set MEM_PLL_CFG = 01 for SYSCLK Freq ¹ |
|------------------------------------|------------------|---|
| 0_0101 | 5:1 | >96.7 MHz |
| 0_0110 | 6:1 | >80.6 MHz |
| 0_1000 | 8:1 | >120.9 MHz |
| 0_1001 | 9:1 | >107.4 MHz |
| 0_1010 | 10:1 | >96.7 MHz |
| 0_1100 | 12:1 | >80.6 MHz |
| 0_1101 | 13:1 | >74.4 MHz |
| 1_0000 | 16:1 | >60.4 MHz |
| 1_0010 | 18:1 | >53.7 MHz |
| All Others | Reserved | — |

Note:

1. Set RCW field MEM_PLL_CFG = 0b01 if the applied DDR PLL reference clock (SYSCLK) frequency is greater than the given cutoff; otherwise, set to 0b00 for a frequency that is less than or equal to the cutoff.

In synchronous mode, the DDR data rate to platform clock ratios supported are listed in this table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14].

Table 99. Synchronous DDR Clock Ratio

| Binary Value of MEM_PLL_RAT[10:14] | DDR:Platform CLK Ratio | Set MEM_PLL_CFG=01 for Platform CLK Freq ¹ |
|------------------------------------|------------------------|---|
| 0_0001 | 1:1 | >600 MHz |
| All Others | Reserved | — |

Note:

1. Set MEM_PLL_CFG=0b01 if the applied DDR PLL reference clock (Platform clock) frequency is greater than given cutoff, else set to 0b00 for frequency that is less than or equal to cutoff.

3.1.6 Frequency Options

This section discusses interface frequency options.

3.1.6.1 SYCLK and Platform Frequency Options

This table shows the expected frequency options for SYCLK and platform frequencies.

Table 100. SYCLK and Platform Frequency Options

| Platform: SYCLK Ratio | SYCLK (MHz) | | | | |
|-----------------------------|---------------------------------------|-------|--------|--------|--------|
| | 66.66 | 83.33 | 100.00 | 111.11 | 133.33 |
| | Platform Frequency (MHz) ¹ | | | | |
| 4:1 | | | | | 533 |
| 5:1 | | | | 555 | |
| 6:1 | | | 600 | | |
| 7:1 | | 583 | | | |
| 8:1 | 533 | | | | |

¹ Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.1.6.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to the values shown in these figures.

$$\frac{527 \text{ MHz} \times (\text{PCI Express link width})}{8}$$

Figure 47. Gen 1 PCI Express Minimum Platform Frequency

$$\frac{527 \text{ MHz} \times (\text{PCI Express link width})}{4}$$

Figure 48. Gen 2 PCI Express Minimum Platform Frequency

See Section 18.1.3.2, “Link Width,” in the chip reference manual for PCI Express interface width details. Note that “PCI Express link width” in the above equation refers to the negotiated link width of the single widest port used (not combined width of the number ports used) as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper Serial RapidIO operation, the platform clock frequency must be greater than or equal to:

$$\frac{2 \times 0.8512 \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

Figure 49. sRIO Minimum Platform Frequency

Hardware Design Considerations

See Section 19.4 “LP-Serial Signal Descriptions,” in the chip reference manual for Serial RapidIO interface width and frequency details.

3.1.7 SerDes PLL Ratio

The clock ratio between each of the three SerDes PLLs and their respective externally supplied $SD_REF_CLK_n/SD_REF_CLK_n$ inputs is determined by the binary value of the RCW Configuration field $SRDS_RATIO_B_n$ as shown in this table. Furthermore, each SerDes lane grouping can be run at a SerDes PLL frequency divider determined by the binary value of the RCW field $SRDS_DIV_B_n$ as shown in Table 103.

This table lists the supported SerDes PLL Bank n to $SD_REF_CLK_n$ ratios.

Table 101. SerDes PLL Bank n to $SD_REF_CLK_n$ Ratios

| Binary Value of $SRDS_RATIO_B1$ | $SRDS_PLL_n:SD_REF_CLK_n$ Ratio | |
|-----------------------------------|-------------------------------------|------------------|
| | $n = 1$ (Bank) | $n = 2$ (Bank 2) |
| 000 | Reserved | Reserved |
| 001 | Reserved | 20:1 |
| 010 | 25:1 | 25:1 |
| 011 | 40:1 | 40:1 |
| 100 | 50:1 | 50:1 |
| 101 | Reserved | 24:1 |
| 110 | Reserved | 30:1 |
| All Others | Reserved | Reserved |

These tables list the supported SerDes PLL dividers.

This table shows the PLL divider support for each pair of lanes on SerDes Bank 1.

Table 102. SerDes Bank 1 PLL Dividers

| Binary Value of $SRDS_DIV_B1[0:4]$ | SerDes Bank 1 PLL Divider |
|--------------------------------------|----------------------------|
| 0b0 | Divide by 1 off Bank 1 PLL |
| 0b1 | Divide by 2 off Bank 1 PLL |

Note: 1 bit (of 5 total $SRDS_DIV_B1$ bits) controls each pair of lanes.

This table shows the PLL dividers supported for each 4-lane for SerDes Banks 2.

Table 103. SerDes Banks 2 PLL Dividers

| Binary Value of $SRDS_DIV_B2$ | SerDes Bank 2 PLL Divider |
|---------------------------------|----------------------------|
| 0b0 | Divide by 1 off Bank 2 PLL |
| 0b1 | Divide by 2 off Bank 2 PLL |

Note: 1 bit controls all four lanes of bank 2.

3.1.8 Frame Manager (FMan) Clock Select

The Frame Managers (FM) can each be synchronous to the platform.

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW clocking configuration fields FM_CLK_SEL.

Table 104. Frame Manager Clock Select

| Binary Value of FM_CLK_SEL | FM Frequency |
|----------------------------|--|
| 0b0 | Platform Clock Frequency /2 |
| 0b1 | Core Cluster 2 Frequency /2 ¹ |

Notes:

¹ For asynchronous mode, max frequency, see [Table 93](#).

3.2 Supply Power Default Setting

The device is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in [Table 105](#), properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

Table 105. I/O Voltage Selection

| Signals | Value (Binary) | VDD Voltage Selection | | |
|----------------------------------|-------------------|-----------------------|-------|----------|
| | | BVDD | CVDD | LVDD |
| IO_VSEL[0:4] Default (0_0000) | 0_0000 | 3.3 V | 3.3 V | 3.3 V |
| | 0_0001 | | | 2.5 V |
| | 0_0010 | | | Reserved |
| | 0_0011 | 3.3 V | 2.5 V | 3.3 V |
| | 0_0100 | | | 2.5 V |
| | 0_0101 | | | Reserved |
| | 0_0110 | 3.3 V | 1.8 V | 3.3 V |
| | 0_0111 | | | 2.5 V |
| | 0_1000 | | | Reserved |
| | 0_1001 | 2.5 V | 3.3 V | 3.3 V |
| | 0_1010 | | | 2.5 V |
| | 0_1011 | | | Reserved |
| | 0_1100 | 2.5 V | 2.5 V | 3.3 V |
| | 0_1101 | | | 2.5 V |
| | 0_1110 | | | Reserved |
| | 0_1111 | 2.5 V | 1.8 V | 3.3 V |
| | 1_0000 | | | 2.5 V |
| | 1_0001 | | | Reserved |
| | 1_0010 | 1.8 V | 3.3 V | 3.3 V |
| | 1_0011 | | | 2.5 V |
| | 1_0100 | | | Reserved |
| | 1_0101 | 1.8 V | 2.5 V | 3.3 V |
| | 1_0110 | | | 2.5 V |
| | 1_0111 | | | Reserved |
| | 1_1000 | 1.8 V | 1.8 V | 3.3 V |
| | 1_1001 | | | 2.5 V |
| | 1_1010 | | | Reserved |
| | 1_1011 | 3.3 V | 3.3 V | 3.3 V |
| | 1_1100 | | | |
| | 1_1101 | | | |
| 1_1110 | | | | |
| 1_1111 | | | | |

3.3 Power Supply Design

This section discusses the power supply design.

3.3.1 PLL Power Supply Filtering

Each of the PLLs described in [Section 3.1, “System Clocking,”](#) is provided with power through independent power supply pins (AV_{DD_PLAT} , AV_{DD_CCn} , AV_{DD_DDR} , and AV_{DD_SRDSn}). AV_{DD_PLAT} , AV_{DD_CCn} and AV_{DD_DDR} voltages must be derived directly from the $V_{DD_CA_CB_PL}$ source through a low frequency filter scheme. AV_{DD_SRDSn} voltages must be derived directly from the SV_{DD} source through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in [Figure 50](#), one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL’s resonant frequency range from a 500-kHz to 10-MHz range.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

[Figure 50](#) shows the PLL power supply filter circuit.

Where:

$$R = 5 \Omega \pm 5\%$$

$$C1 = 10 \mu\text{F} \pm 10\%, \text{ 0603, X5R, with ESL} \leq 0.5 \text{ nH}$$

$$C2 = 1.0 \mu\text{F} \pm 10\%, \text{ 0402, X5R, with ESL} \leq 0.5 \text{ nH}$$

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL \leq 0.5 nH).

Voltage for AV_{DD} is defined at the PLL supply filter and not the pin of AV_{DD} .

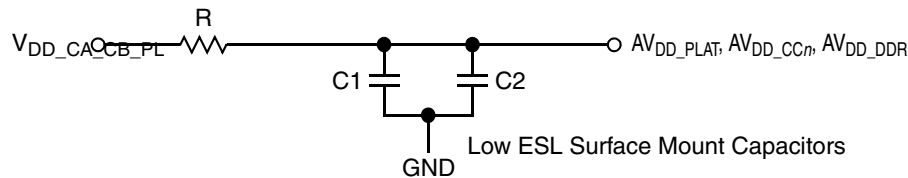


Figure 50. PLL Power Supply Filter Circuit

The AV_{DD_SRDSn} signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following [Figure 51](#). For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD_SRDSn} balls. The 0.003- μF capacitor is closest to the balls, followed by two 2.2- μF capacitors, and finally the 1- Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn}

Hardware Design Considerations

to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide, and direct.

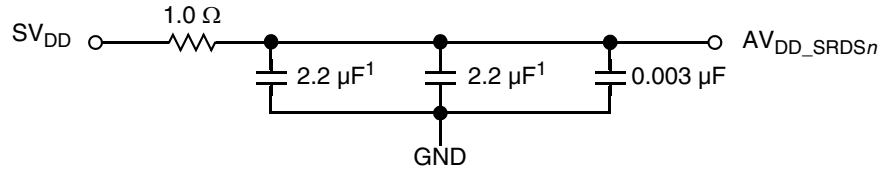


Figure 51. SerDes PLL Power Supply Filter Circuit

Note the following:

- AV_{DD_SRDSn} must be a filtered version of SV_{DD} .
- Signals on the SerDes interface are fed from the XV_{DD} power plane.
- Voltage for AV_{DD_SRDSn} is defined at the PLL supply filter and not the pin of AV_{DD_SRDSn} .
- A 0805 sized capacitor is recommended for system initial bring-up.

3.3.2 XV_{DD} Power Supply Filtering

XV_{DD} may be supplied by a linear regulator or sourced by a filtered GV_{DD} . Systems may design in both options to allow flexibility to address system noise dependencies.

An example solution for XV_{DD} filtering, where XV_{DD} is sourced from GV_{DD} , is illustrated in Figure 52. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

$C1 = 2.2 \mu\text{F} \pm 10\%$, X5R, with $\text{ESL} \leq 0.5 \text{ nH}$

$C2 = 2.2 \mu\text{F} \pm 10\%$, X5R, with $\text{ESL} \leq 0.5 \text{ nH}$

F1 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite

F2 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite

Bulk and decoupling capacitors are added, as needed, per power supply design.

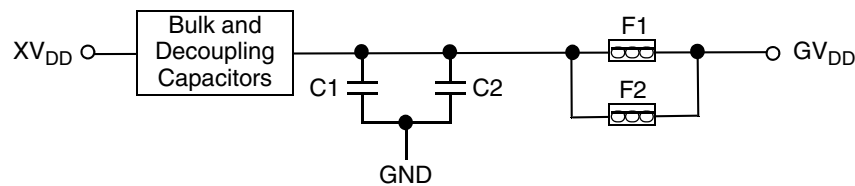


Figure 52. XV_{DD} Power Supply Filter Circuit

3.3.3 $USB_V_{DD_1P0}$ Power Supply Filtering

$USB_V_{DD_1P0}$ must be sourced by a filtered $V_{DD_CA_CB_PL}$ using a star connection. An example solution for $USB_V_{DD_1P0}$ filtering, where $USB_V_{DD_1P0}$ is sourced from $V_{DD_CA_CB_PL}$, is illustrated in Figure 53. The component values in this example filter is system dependent and are still under characterization; component values may need adjustment based on the system or environment noise.

Where:

$C1 = 2.2 \mu\text{F} \pm 20\%$, X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)

F1 = 120 Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)

Bulk and decoupling capacitors are added, as needed, per power supply design.

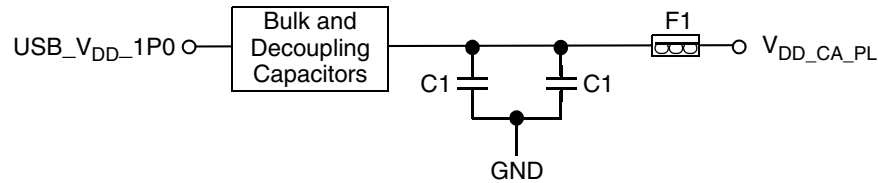


Figure 53. USB_VDD_1P0 Power Supply Filter Circuit

3.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip's system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , BV_{DD} , OV_{DD} , CV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , BV_{DD} , OV_{DD} , CV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , BV_{DD} , OV_{DD} , CV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON).

3.5 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

- First, the board should have at least 10×10 -nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a 1- μF ceramic chip capacitor on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10- μF , low ESR SMT tantalum chip capacitor and a 100- μF , low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

3.6 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD} , BV_{DD} , CV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD} , BV_{DD} , CV_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND pins of the device.

The Ethernet controllers 1 and/or 2 input pins may be disabled by setting their respective RCW configuration field EC1 (bits 360–361) and EC2 (bits 363–364) to 0b11 = No parallel mode Ethernet. When disabled, these inputs do not need to be externally pulled to an appropriate signal level.

Hardware Design Considerations

ECn_GTX_CLK125 is a 125-MHz input clock on the dTSEC ports. If the dTSEC ports are not used for RGMII, the ECn_GTX_CLK125 input can be tied off to GND.

If RCW field I2C = 0b0100 or 0b0101 (RCW bits 354–357), the SDHC_WP and $\overline{\text{SDHC_CD}}$ input signals are enabled for external use. If SDHC_WP and $\overline{\text{SDHC_CD}}$ are selected and not used, they must be externally pulled low such that SDHC_WP = 0 (write enabled) and $\overline{\text{SDHC_CD}} = 0$ (card detected). If RCW field I2C \neq 0b0100 or 0b0101, thereby selecting either I2C3 or GPIO functionality, SDHC_WP and $\overline{\text{SDHC_CD}}$ are internally driven such that SDHC_WP = write enabled and $\overline{\text{SDHC_CD}} =$ card detected and the selected I2C3 or GPIO external pin functionality may be used.

$\overline{\text{TMP_DETECT}}$ pin and $\overline{\text{LP_TMP_DETECT}}$ pin are active low input to the Security Monitor (refer to the “Secure Boot and Trust Architecture” chapter of the chip reference manual). If a tamper sensor is used, it must maintain the signal at the specified voltage until a tamper is detected. A 1K pull-down resistor strongly recommended. If Trust is used without tamper sensors, tie high.VDD_LP must be connected even if Low Power features aren’t used. Otherwise, the LP_Section will generate internal errors that will prevent the high power trust section from reaching Trusted/Secure state.

3.6.1 Legacy JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 55](#). Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{PORESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 55](#) allows the COP port to independently assert $\overline{\text{PORESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{PORESET}}$ as well.

The COP interface has a standard header, shown in [Figure 54](#), for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in [Figure 54](#) is common to all known emulators.

3.6.1.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ must be tied to $\overline{\text{PORESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 55](#). If this is not possible, the

isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, or TDO.

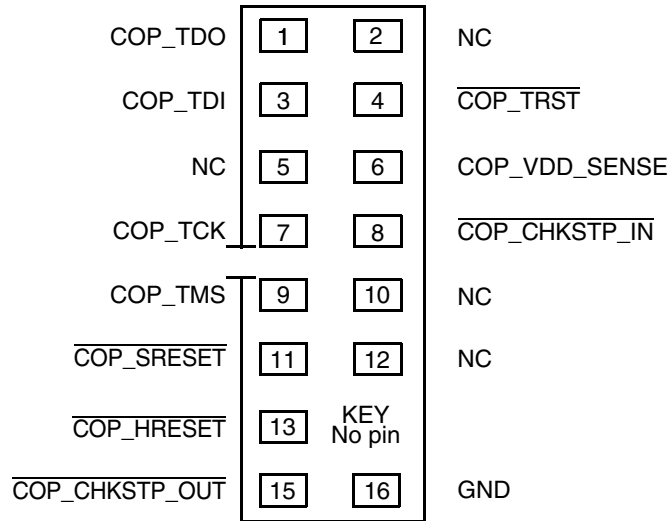
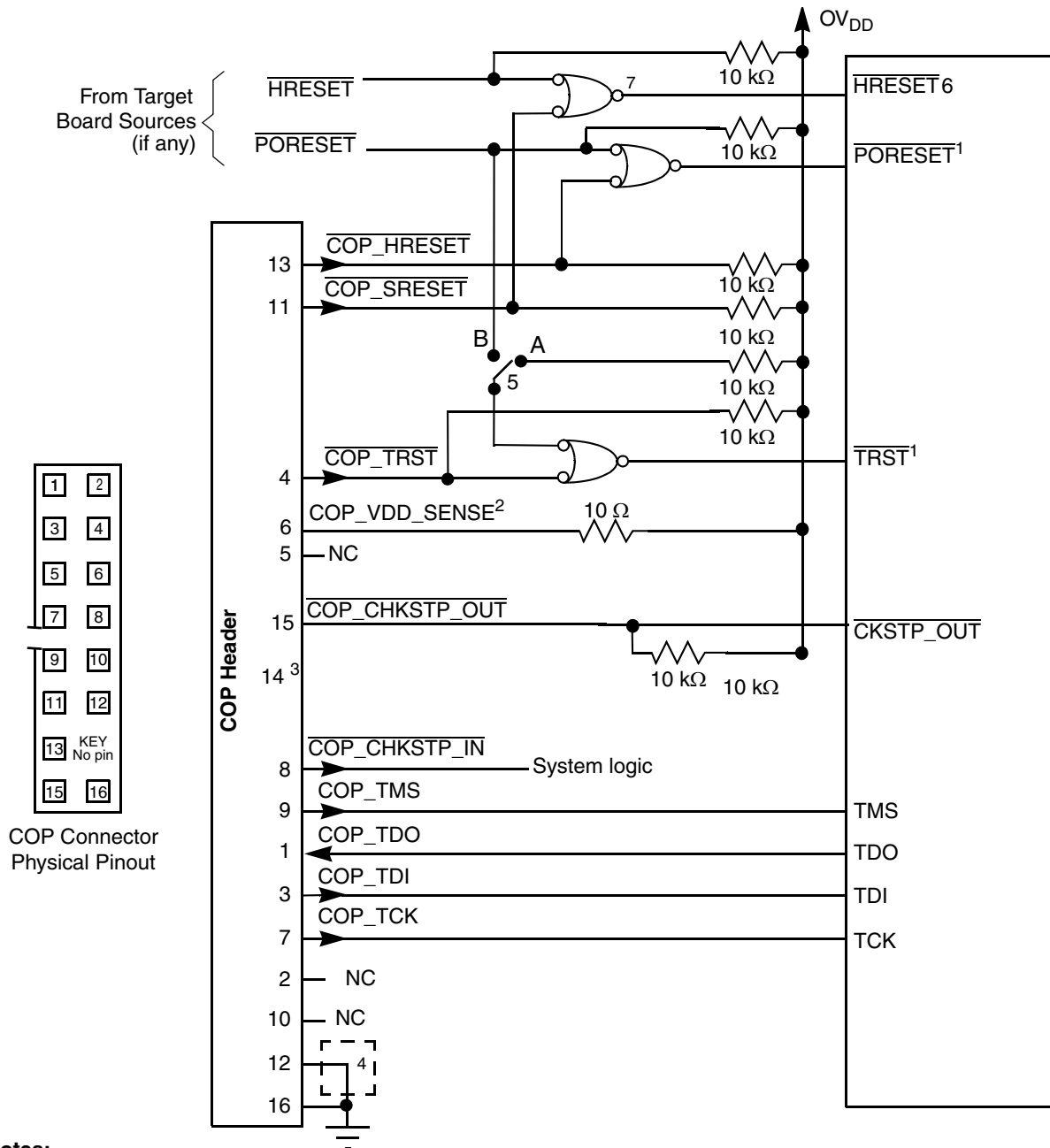


Figure 54. Legacy COP Connector Physical Pinout



Notes:

1. The COP port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch must be closed to position B.
6. Asserting HRESET causes a hard reset on the device.
7. This is an open-drain gate.

Figure 55. Legacy JTAG Interface Connection

3.6.2 Aurora Configuration Signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in [Figure 56](#) and [Figure 57](#). Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Freescale recommends that the Aurora 22 pin duplex connector be designed into the system as shown in [Figure 58](#) or the 70 pin duplex connector be designed into the system as shown in [Figure 59](#).

If the Aurora interface is not used, Freescale recommends the legacy COP header be designed into the system as described in [Section 3.6.1.1, “Termination of Unused Signals.”](#)

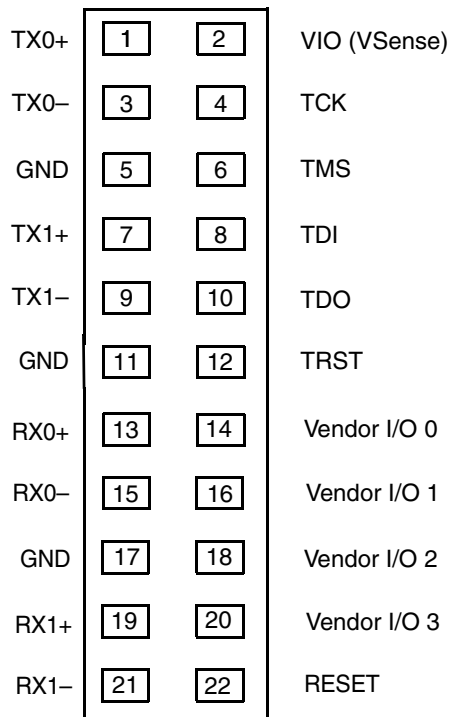


Figure 56. Aurora 22 Pin Connector Duplex Pinout

| | | | |
|------|----|----|--------------|
| TX0+ | 1 | 2 | VIO (VSense) |
| TX0- | 3 | 4 | TCK |
| GND | 5 | 6 | TMS |
| TX1+ | 7 | 8 | TDI |
| TX1- | 9 | 10 | TDO |
| GND | 11 | 12 | TRST |
| RX0+ | 13 | 14 | Vendor I/O 0 |
| RX0- | 15 | 16 | Vendor I/O 1 |
| GND | 17 | 18 | Vendor I/O 2 |
| RX1+ | 19 | 20 | Vendor I/O 3 |
| RX1- | 21 | 22 | RESET |
| GND | 23 | 24 | GND |
| TX2+ | 25 | 26 | CLK+ |
| TX2- | 27 | 28 | CLK- |
| GND | 29 | 30 | GND |
| TX3+ | 31 | 32 | Vendor I/O 4 |
| TX3- | 33 | 34 | Vendor I/O 5 |
| GND | 35 | 36 | GND |
| RX2+ | 37 | 38 | N/C |
| RX2- | 39 | 40 | N/C |
| GND | 41 | 42 | GND |
| RX3+ | 43 | 44 | N/C |
| RX3- | 45 | 46 | N/C |
| GND | 47 | 48 | GND |
| TX4+ | 49 | 50 | N/C |
| TX4- | 51 | 52 | N/C |
| GND | 53 | 54 | GND |
| TX5+ | 55 | 56 | N/C |
| TX5- | 57 | 58 | N/C |
| GND | 59 | 60 | GND |
| TX6+ | 61 | 62 | N/C |
| TX6- | 63 | 64 | N/C |
| GND | 65 | 66 | GND |
| TX7+ | 67 | 68 | N/C |
| TX7- | 69 | 70 | N/C |

Figure 57. Aurora 70 Pin Connector Duplex Pinout

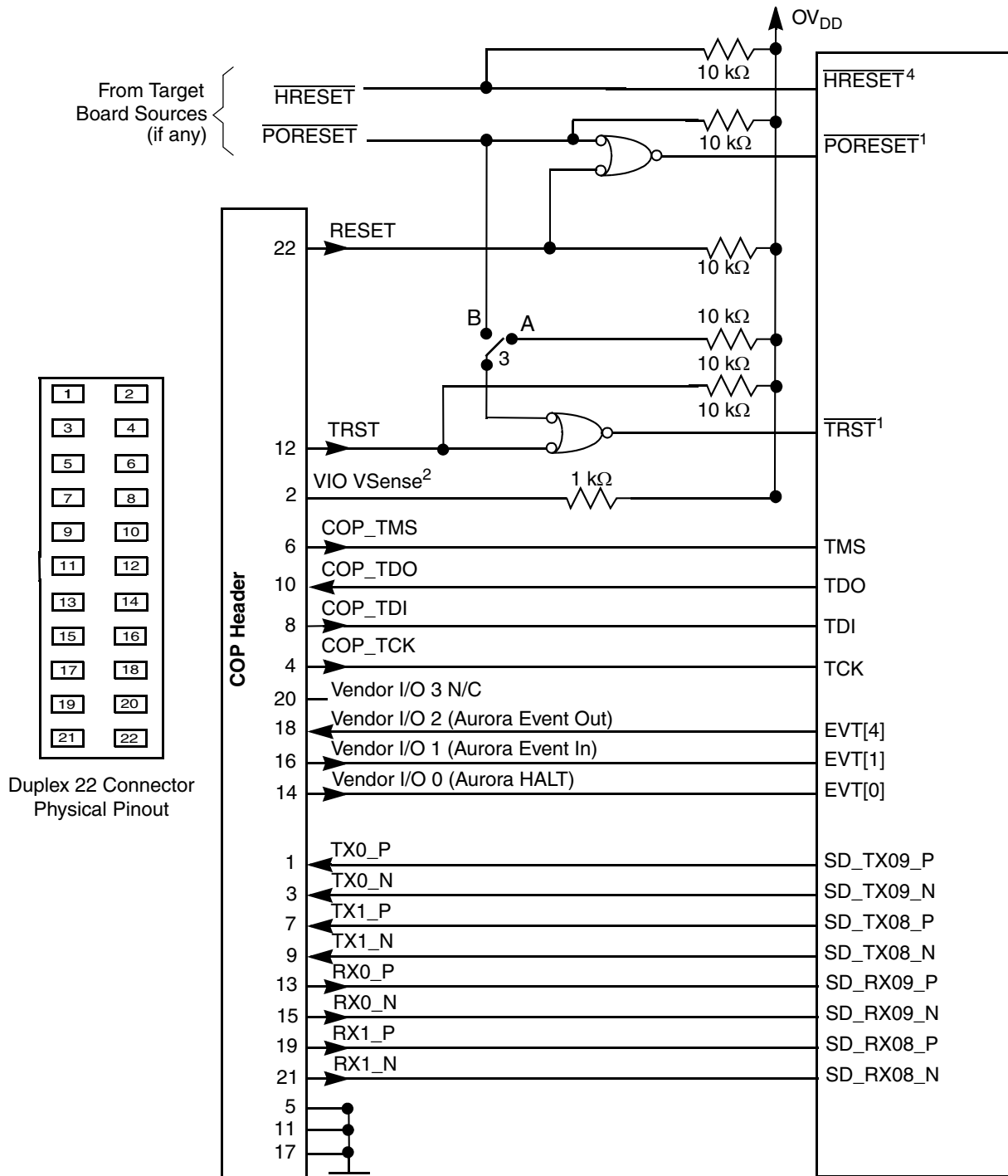


Figure 58. Aurora 22 Pin Connector Duplex Interface Connection

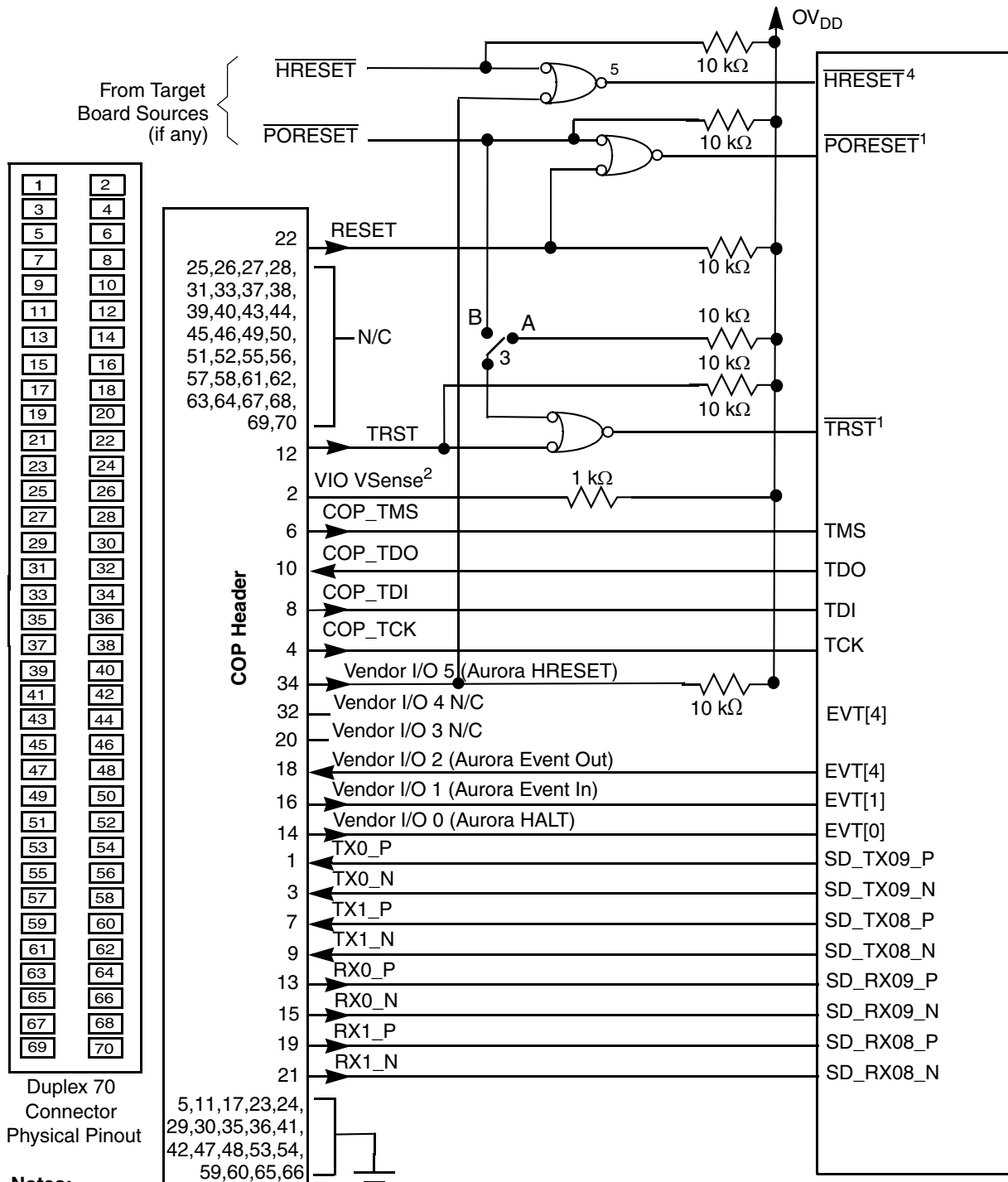


Figure 59. Aurora 70 Pin Connector Duplex Interface Connection

3.6.3 Guidelines for High-Speed Interface Termination

This section provides the guidelines for when the SerDes interface is either entirely unused or partly unused.

3.6.3.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[7:2], SD_TX[13:10]
- $\overline{\text{SD_TX}}[7:2]$, $\overline{\text{SD_TX}}[13:10]$
- SD_IMP_CAL_RX
- SD_IMP_CAL_TX

The following pins must be connected to SGND:

- SD_RX[7:2], SD_RX[13:10]
- $\overline{\text{SD_RX}}[13:10]$, $\overline{\text{SD_RX}}[13:10]$
- SD_REF_CLK1, SD_REF_CLK2
- $\overline{\text{SD_REF_CLK1}}$, $\overline{\text{SD_REF_CLK2}}$

In the RCW configuration fields SRDS_LPD_B1 and SRDS_LPD_B2, all bits must be set to power down all the lanes in each bank.

RCW configuration field SRDS_EN may be cleared to power down the SerDes block for power saving. Setting RCW[SRDS_EN] = 0 power-downs the PLLs of both banks.

Additionally, software may configure SRDSB n RSTCTL[SDRD] = 1 for the unused banks to power down the SerDes bank PLLs to save power.

Note that both SV_{DD} and XV_{DD} must remain powered.

3.6.3.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following unused pins must be left unconnected:

- SD_TX[n]
- $\overline{\text{SD_TX}}[n]$

The following unused pins must be connected to SGND:

- SD_RX[n]
- $\overline{\text{SD_RX}}[n]$
- SD_REF_CLK1, $\overline{\text{SD_REF_CLK1}}$ (If entire SerDes bank 1 unused)
- SD_REF_CLK2, $\overline{\text{SD_REF_CLK2}}$ (If entire SerDes bank 2 unused)

In the RCW configuration field for each bank SRDS_LPD_B n with unused lanes, the respective bit for each unused lane must be set to power down the lane.

3.6.4 USB Controller Connections

This section details the hardware connections required for the USB controllers.

3.6.4.1 USB Divider Network

This figure shows the required divider network for the VBUS interface for the device. Additional requirements for the external components are as follows:

- Both resistors require 0.1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.
- The zener diode must have a value of 5 V–5.25 V.
- The 0.6 V diode requires an $I_F = 10 \text{ mA}$, $I_R < 500 \text{ nA}$ and $V_{F(\text{Max})} = 0.8 \text{ V}$.

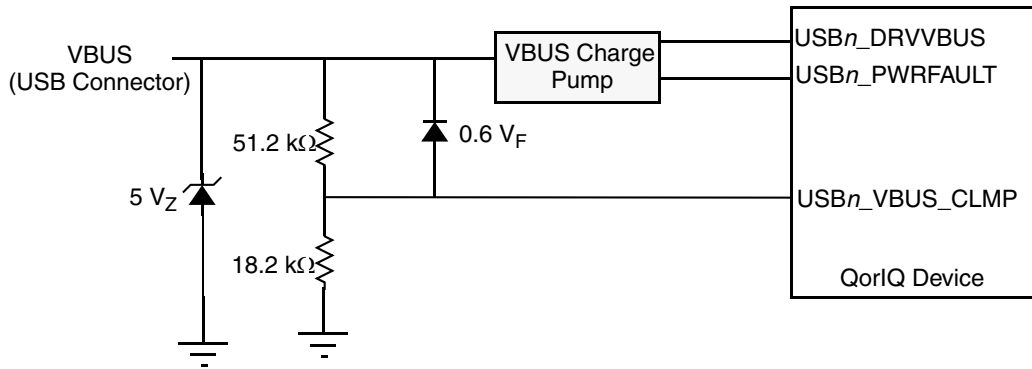


Figure 60. Divider Network at VBUS

USB1_DRVVBUS and USB1_PWRFAULT are muxed on GPIO[25] and GPIO[27] pins, respectively. USB2_DRVVBUS and USB2_PWRFAULT are muxed on GPIO[6:7] pins, respectively. Setting RCW[GPIO] selects USB functionality on the GPIO pins.

3.6.4.2 USB_n_V_{DD}_1P8_DECAP Capacitor Options

The USB_n_V_{DD}_1P8_DECAP pins require a capacitor connected to GND.

This table lists the recommended capacitors for the USB_n_V_{DD}_1P8_DECAP signal.

Table 106. Recommended Capacitor Parts for USB_n_V_{DD}_1P8_DECAP

| Manufacturer | Part Number | Value | ESR | Package |
|-----------------|----------------------|--------------|---------|---------|
| Kemet | T494B105(1)025A(2) | 1 uF, 25 V | 2 Ω | B(3528) |
| | T494B155(1)025A(2) | 1.5 uF, 25 V | 1.5 Ω | — |
| NIC | NMC0603X7R106KTRPF | 1 uF, 10 V | Low ESR | 0603 |
| TDK Corporation | CERB2CX5R0G105M | 1 uF, 4 V | 200 m-Ω | 0603 |
| Vishay | TR3B105(1)035(2)1500 | 1 uF, 35 V | 1.5 Ω | B(3528) |

3.7 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.8 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow,

and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 61. The heat sink must be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

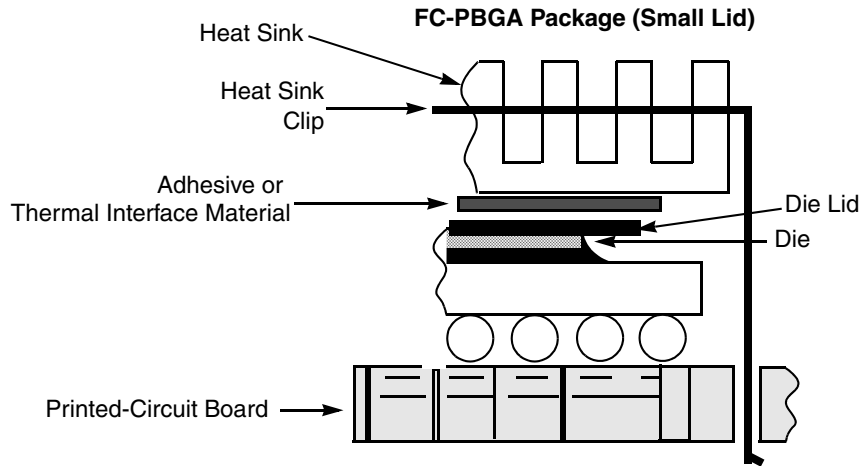


Figure 61. Package Exploded Cross-Sectional View—FC-PBGA (w/ Lid) Package

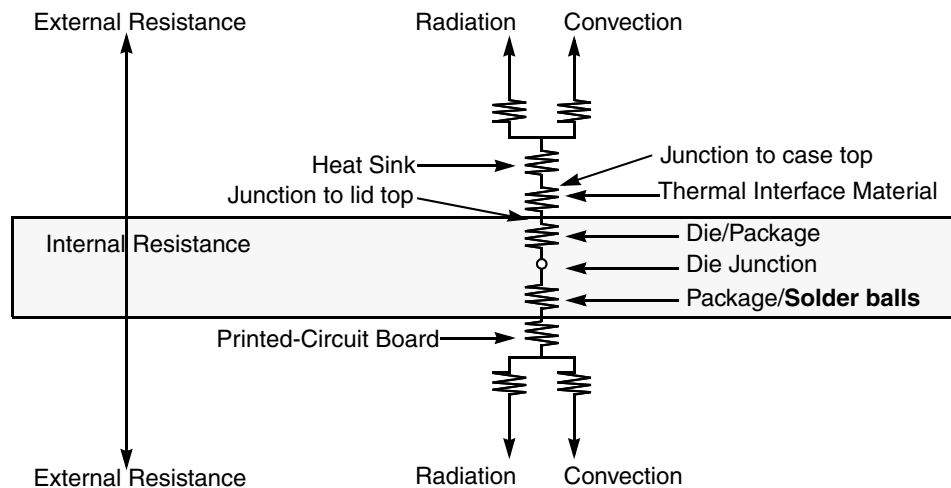
The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.8.1 Internal Package Conduction Resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

Figure 62 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 62. Package with Heat Sink Mounted to a Printed-Circuit Board

Package Information

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.8.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see [Figure 61](#)).

The system board designer can choose among several types of commercially-available thermal interface materials.

3.8.3 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

- Operating range: 10 – 230μA
- Ideality factor over 13.5 – 220 μA: $n = 1.00589 \pm 0.008$

4 Package Information

The following section describes the detailed content and mechanical description of the package.

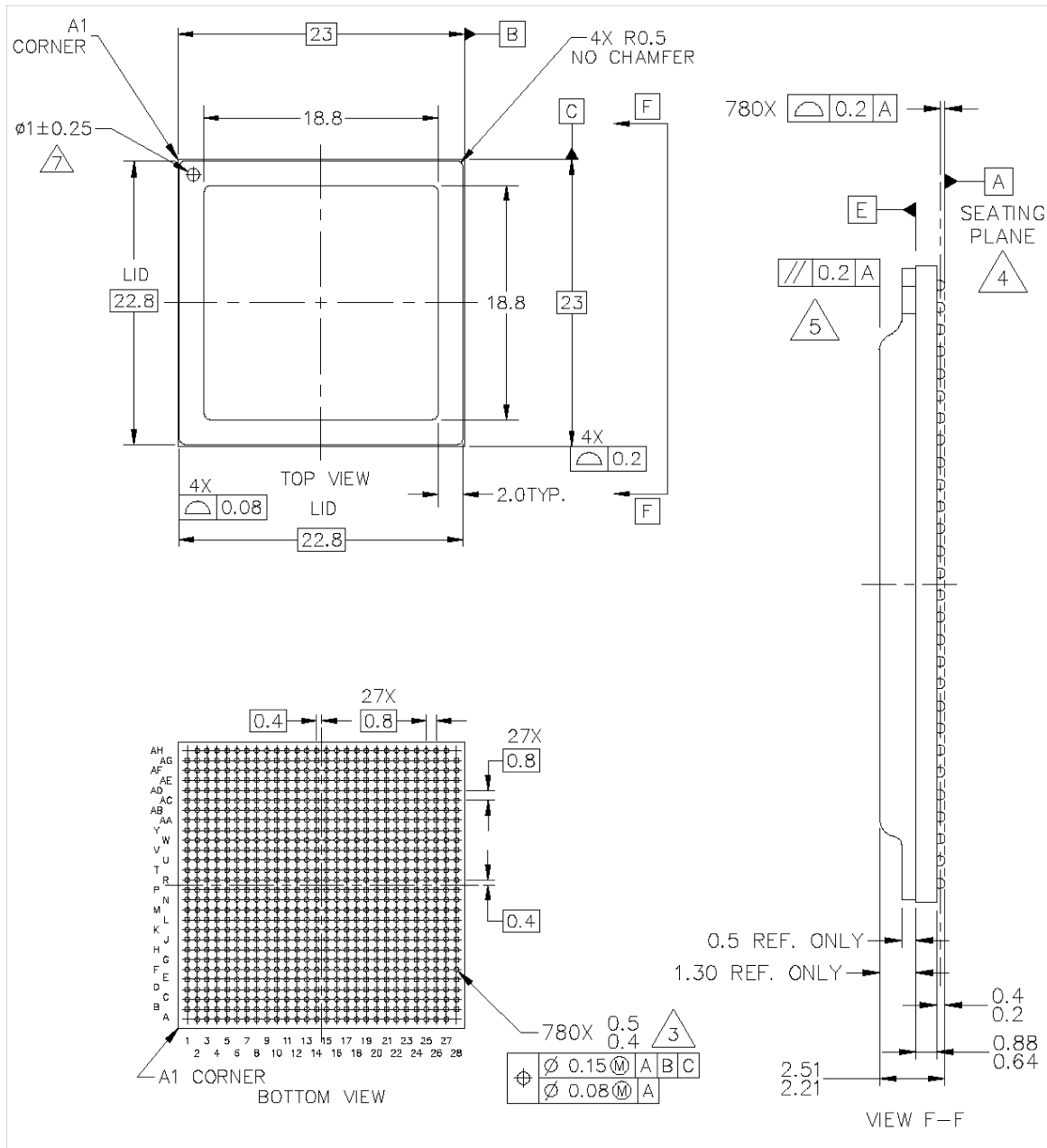
4.1 Package Parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 23 mm × 23 mm, 780 flip chip plastic ball grid array (FC-PBGA).

| | |
|-------------------------|------------------------------|
| Package outline | 23 mm × 23mm |
| Interconnects | 780 |
| Ball Pitch | 0.8 mm |
| Ball Diameter (typical) | 0.40 mm |
| Solder Balls | 96.5% Sn, 3% Ag, 0.5% Cu |
| Module height (typical) | 2.21 mm to 2.51 mm (Maximum) |

4.2 Mechanical Dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the device.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement excludes any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
7. Pin 1 thru hole is centered within foot area.

Figure 63. Mechanical Dimensions of the FC-PBGA with Full Lid

5 Security Fuse Processor

The device implements the QorIQ platform's Trust Architecture supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD} pin per [Section 2.2, "Power Up Sequencing."](#) POV_{DD} should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times POV_{DD} must be connected to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in [Figure 8](#). To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per [Table 3](#).

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD} to GND.

6 Ordering Information

Contact your local Freescale sales office or regional marketing team for ordering information.

6.1 Part Numbering Nomenclature

This table provides the Freescale QorIQ platform part numbering nomenclature. Not all possible combinations of part numbers implied by the part numbering scheme are supported. For a list of available part numbers, contact your Freescale Sales office. Each part number also contains a revision code which refers to the die mask revision number.

Table 107. Part Numbering Nomenclature

| <i>p</i> | <i>n</i> | <i>nn</i> | <i>n</i> | <i>x</i> | <i>t</i> | <i>e</i> | <i>n</i> | <i>c</i> | <i>d</i> | <i>r</i> |
|------------|----------|---|------------|---|---|--|--|--|--------------------------------|---|
| Generation | Platform | Number of Cores | Derivative | Qual Status | Temp. Range | Encryption | Package Type | CPU Freq | DDR Data Rate | Die Revision |
| P = 45 nm | 1–5 | 01 = 1 core 02 = 2 cores 04 = 4 cores | 0–9 | P = Prototype N = Industrial qualification | S = Std temp X = Extended temp (–40 to 105C) | E = SEC present N = SEC not present | 1 = FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free | F = 667 MHz H = 800 MHz K = 1000 MHz M = 1200 MHz | L = 1067 MT/s M = 1200 MT/s | A = Rev 1.0 B = Rev 1.1 C = Rev 2.0 |

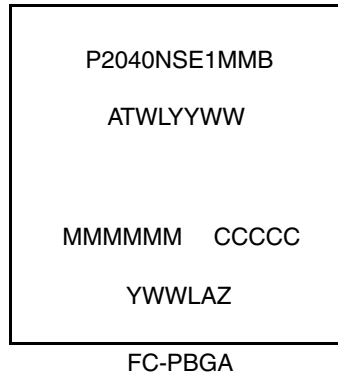
6.2 Orderable Part Numbers Addressed by this Document

This table provides the Freescale orderable part numbers addressed by this document for the chip.

| Part Number | <i>p</i> | <i>n</i> | <i>nn</i> | <i>n</i> | <i>x</i> | <i>t</i> | <i>e</i> | <i>n</i> | <i>c</i> | <i>d</i> | <i>r</i> | | |
|------------------------------|----------|----------|----------------|----------|------------------------------------|-------------------------|------------------------|---|------------------|------------------|----------|------------------|------------------|
| P2040NSE1FLB P2040NSE7FLC | P | 2 | 04 = 4 core | 1 | N = Industrial qualification | S = Std temp | E = SEC present | 1 = FC-PBGA Pb-free spheres 7 = FC-PBGA C4 and sphere Pb-free | F = 667 MHz | L = 1067 MT/s | B C | | |
| P2040NSN1FLB P2040NSN7FLC | | | | | | | N = SEC not present | | | | | | |
| P2040NSE1HLB P2040NSE7HLC | | | | | | | E = SEC present | | | | | H = 800 MHz | |
| P2040NSN1HLB P2040NSN7HLC | | | | | | | N = SEC not present | | | | | | |
| P2040NSE1KLB P2040NSE7KLC | | | | | | | E = SEC Present | | | | | K = 1000 MHz | |
| P2040NSN1KLB P2040NSN7KLC | | | | | | | N = SEC not present | | | | | | |
| P2040NSE1MMB P2040NSE7MMC | | | | | | | E = SEC Present | | | | | M = 1200 MHz | M = 1200 MT/s |
| P2040NSN1MMB P2040NSN7MMC | | | | | | | N = SEC not present | | | | | | |
| P2040NXE1FLB P2040NXE7FLC | | | | | | X = Extended temp | E = SEC Present | F = 667 MHz | L = 1067 MT/s | | | | |
| P2040NXN1FLB P2040NXN7FLC | | | | | | | N = SEC not present | | | | | | |
| P2040NXE1MMB P2040NXE7MMC | | | | | | | E = SEC Present | | | M = 1200 MHz | | M = 1200 MT/s | |
| P2040NXN1MMB P2040NXN7MMC | | | | | | | N = SEC not present | | | | | | |

6.2.1 Part Marking

Parts are marked as in the example shown in this figure.



Notes:

P2040NSE1MMB is the orderable part number. See [Table 107](#) for details.

ATWLYYWW is the test traceability code.

MMMMMM is the mask number.

CCCCC is the country code.

YWWLAZ is the assembly traceability code.

Figure 64. Part Marking for FC-PBGA Device

7 Revision History

This table provides a revision history for this document.

Table 108. Revision History

| Rev. Number | Date | Description |
|-------------|---------|--|
| 2 | 02/2013 | <ul style="list-style-type: none"> • In Table 7, “P2040 I/O Power Supply Estimated Values,” updated the USB power supply with USB_Vdd_3P3 and updated the typical value with “0.003” in the Others (Reset, System Clock, JTAG & Misc.) row. • In Table 8, “Device AVDD Power Dissipation,” removed V_{DD_LP} from table. • Added Table 10, “VDD_LP Power Dissipation.” • In Table 53, “MPIC Input AC Timing Specifications,” added Trust inputs AC timing and footnote 2. • In Table 93, “Processor Clocking Specifications,” updated footnote 8 with Rev 1.1 silicon. • In Table 107, “Part Numbering Nomenclature,” added “C” in the Die Revision column. • In Section 6.2, “Orderable Part Numbers Addressed by this Document,” added the device part numbers for Rev 2.0 silicon. |

Table 108. Revision History (continued)

| Rev. Number | Date | Description |
|-------------|---------|---|
| 1 | 09/2012 | <ul style="list-style-type: none"> • In Table 1, “Pin List by Bus”, added note for pin V_{DD_LP} • Updated Table 8, “Device AVDD Power Dissipation”. • In Table 12, “SYSCLK DC Electrical Characteristics ($OV_{DD} = 3.3\text{ V}$)”, updated the input current max value and added input capacitance max value. • In Table 51, “eSDHC AC Timing Specifications”, updated input setup times from 5 ns to 2.5 ns. • In Section 3.1.6.2, “Minimum Platform Frequency Requirements for High-Speed Interfaces”, updated the note that the “PCI Express link width” refers to “a single port”. • In Section 4.1, “Package Parameters for the FC-PBGA”, updated the solder ball composition and module height. • In Section 4.2, “Mechanical Dimensions of the FC-PBGA”, updated the figure for the mechanical dimensions. • In Section 3.6, “Connection Recommendations”, removed the sentence “If no aspect of Trust Architecture is to be used, all Trust Architecture pins can be tied to GND.” |
| 0 | 06/2012 | Initial public release |

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