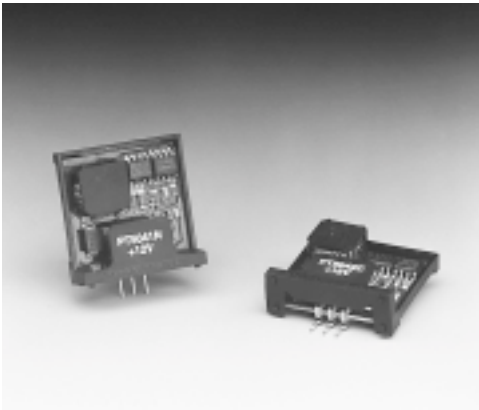




THE DATASHEET OF PT5042C





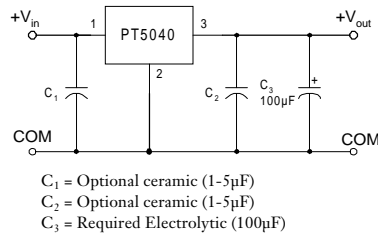
Features

- Wide Input Voltage Range
- 85% Efficiency
- Internal Over-Temperature Protection
- Laser-trimmed Output Voltage
- Soft Start
- 5-Pin Mount Option (Suffixes L & M)

Description

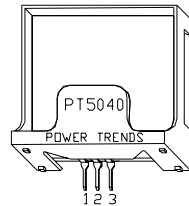
The PT5040 is a series of 3-pin boost-voltage Integrated Switching Regulators (ISRs). These ISRs are designed for use with +5V bus systems that require an additional regulated +8V to +20V with up to 1A of output current. These ISRs are packaged in the 3-pin, single in-line pin (SIP) package configuration.

Standard Application



Pin-Out Information

Pin	Function
1	V_{in}
2	GND
3	V_{out}



Ordering Information

- PT5041□ = +12 Volts
- PT5042□ = +15 Volts
- PT5044□ = +8 Volts
- PT5045□ = +9 Volts
- PT5046□ = +10 Volts
- PT5047□ = +18 Volts
- PT5048□ = +12.6 Volts
- PT5049□ = +20 Volts

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code*
Vertical	N	(EAD)
Horizontal	A	(EAA)
SMD	C	(EAC)
Horizontal, 2-pin Tab	M	(EAM)
SMD, 2-Pin Tab	L	(EAL)

* Previously known as package styles 100/110.
 (Reference the applicable package code drawing for the dimensions and PC board layout)

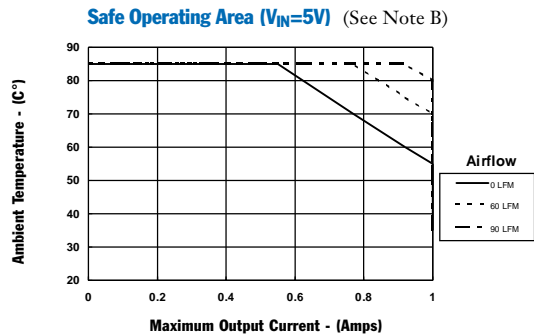
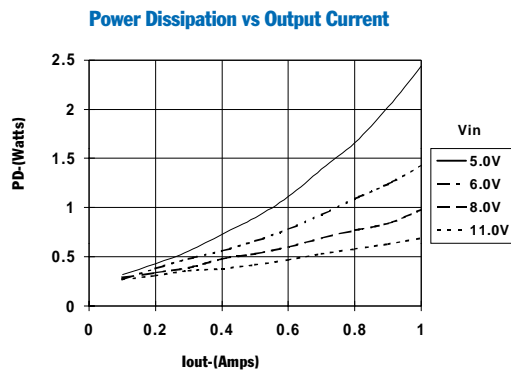
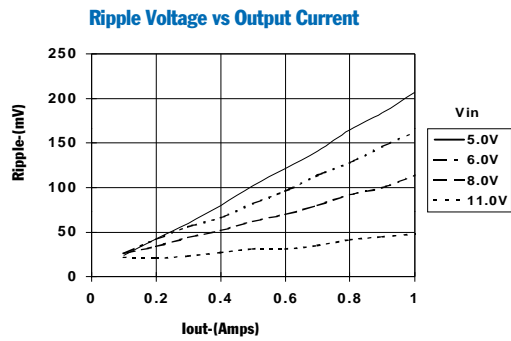
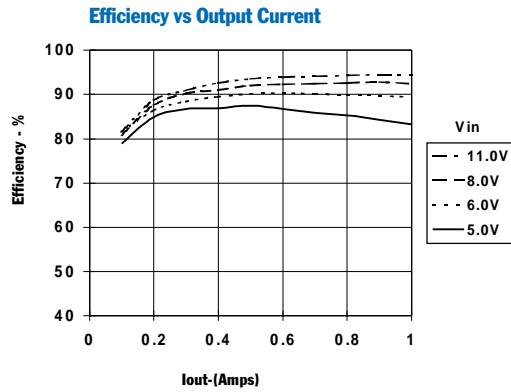
NOTE: Boost Topology ISRs are not Short-Circuit Protected.

Specifications (Unless otherwise stated, $T_a = 25^\circ\text{C}$, $V_{in} = 5\text{V}$, $I_o = I_{o,max}$, $C_3 = 100\mu\text{F}$)

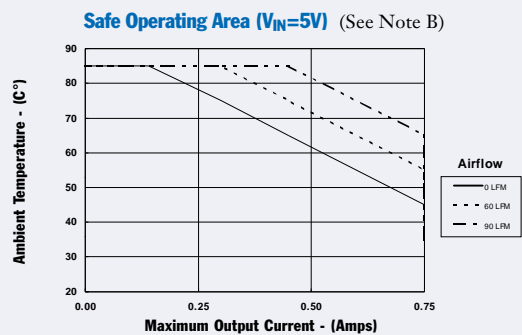
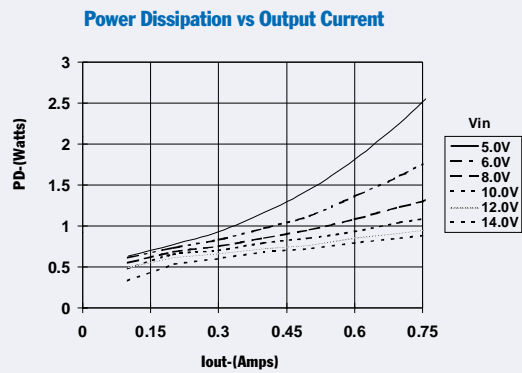
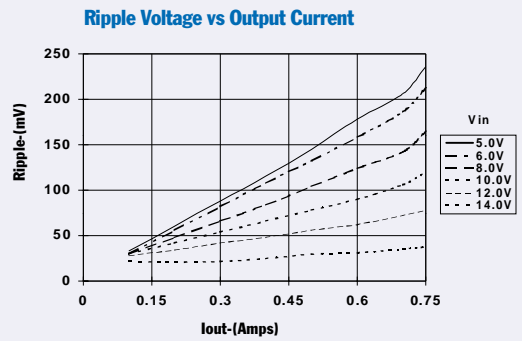
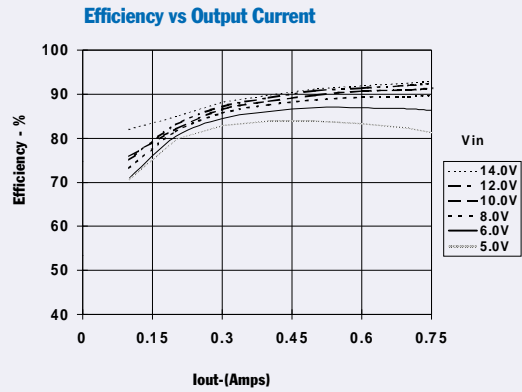
Characteristics	Symbol	Conditions	PT5040 SERIES			Units	
			Min	Typ	Max		
Output Current	I_o	Over V_{in} range	PT5049	0.1 (1)	—	0.5	A
			PT5047	0.1 (1)	—	0.6	
			PT5041/48	0.1 (1)	—	1.0	
			PT5042	0.1 (1)	—	0.75	
			PT5044	0.1 (1)	—	1.5	
			PT5045/46	0.1 (1)	—	1.2	
Input Voltage Range	V_{in}	Over I_o range	PT5047/5049	4.75	—	$(V_o - 1)$ 14	V
Output Voltage Tolerance	ΔV_o	Over V_{in} Range $T_a = -20^\circ\text{C}$ to SOA derating limit (3)	—	± 1.5	± 3.0	$\%V_o$	
Line Regulation	Reg_{line}	Over V_{in} range	—	± 0.5	± 1.0	$\%V_o$	
Load Regulation	Reg_{load}	$I_{o,min} \leq I_o \leq I_{o,max}$	—	± 0.5	± 1.0	$\%V_o$	
Efficiency	η	$I_o = 0.5\text{A}$	—	85	—	%	
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	—	± 2	± 5	$\%V_o$	
Transient Response	t_{tr}	25% load change V_o over/undershoot	—	500	—	μSec	
	V_{os}		—	3.0	5.0	$\%V_o$	
Current Limit	I_{lim}	—	—	150 (2)	—	$\%I_{o,max}$	
Inrush Current	I_{ir}	On start up	—	5.5 (3)	—	A	
	t_{ir}		—	1	—	mSec	
Switching Frequency	f_s	Over V_{in} and I_o ranges	$V_o < 15\text{V}$	500	650	800	kHz
			$V_o \geq 15\text{V}$	650	800	950	
Operating Temperature Range	T_a	—	-20	—	+85 (4)	$^\circ\text{C}$	
Thermal Resistance	θ_{pa}	Free Air Convection (40-60LFM)	—	40	—	$^\circ\text{C}/\text{W}$	
Storage Temperature	T_s	—	-40	—	+125	$^\circ\text{C}$	
Mechanical Shock	—	Per Mil-STD-883D, Method 2002.3 1 msec, Half Sine, mounted to a fixture	—	500	—	G's	
Mechanical Vibration Per Mil-STD-883D, 20-2000 Hz	—	Suffixes N, A, & C Suffixes L & M	—	5	—	G's	
			—	20 (5)	—		
Weight	—	Suffixes N, A, & C Suffixes L & M	—	4.5	—	grams	
			—	6.5	—		

- Notes:**
- (1) The ISR will operate at no load with reduced specifications.
 - (2) Boost topology ISRs are not short circuit protected.
 - (3) The inrush current stated is above the normal input current for the associated output load.
 - (4) See Safe Operating Area curves or consult the factory for the appropriate derating
 - (5) The tab pins on the 5-pin mount package types (suffixes L & M) must be soldered. For more information see the applicable package outline drawing.

PT5041, +12.0 VDC (See Note A)



PT5042, +15.0 VDC (See Note A)



Note A: Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.
Note B: Thermal derating graphs are developed in free-air convection cooling, which corresponds to approximately 40–60LFM of airflow.

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