



# THE DATASHEET OF RT5047AGSP



## **Single Output LNB Supply and Control Voltage Regulator**

### **General Description**

The RT5047A is a highly integrated voltage regulator and interface IC, specifically design for supplying power and control signals from advanced satellite set-top box (STB) modules to the LNB down-converter in the antenna dish or to the multi-switch box.

The device is consists of the independent current-mode boost controller and low dropout linear regulator along with the circuitry required for 22KHz tone shaping to support DiSEqC<sup>TM</sup>1.x communications.

The RT5047A has fault protection (over-current, over-temperature and under-voltage lockout).

The RT5047A are available in a SOP-8 (Exposed Pad) package to achieve optimized solution for thermal dissipation.

### **Ordering Information**

|         |                                      |
|---------|--------------------------------------|
| RT5047A | □□                                   |
|         | Package Type                         |
|         | SP : SOP-8 (Exposed Pad-Option 2)    |
|         | Lead Plating System                  |
|         | G : Green (Halogen Free and Pb Free) |

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

### **Features**

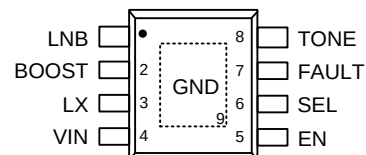
- Wide Input Supply Voltage Range : 8V to 16V
- Output Current Limit of 550mA with 45ms timer
- Low Noise LNB Output Voltage (13.3V and 18.3V by SEL Pin)
- $\pm 3\%$  High Accuracy for 0mA to 500mA Current Output
- Push-Pull Output Stage minimizes 13.3V to 18.3V and 18.3V to 13.3V Output Transition Time
- External 22kHz Tone Input
- Meet DiSEqC<sup>TM</sup>1.x Protocol
- Output Short Circuit Protection
- Over-Temperature Protection

### **Applications**

- LNB Power Supply and Control for Satellite Set-Top Box
- Analog and Digital Satellite Receivers/Satellite TV, Satellite PC cards

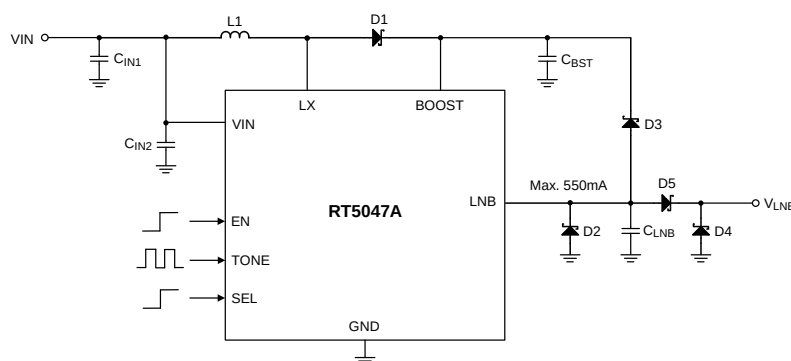
### **Pin Configurations**

(TOP VIEW)



SOP-8 (Exposed Pad)

### **Simplified Application Circuit**



## Marking Informaton

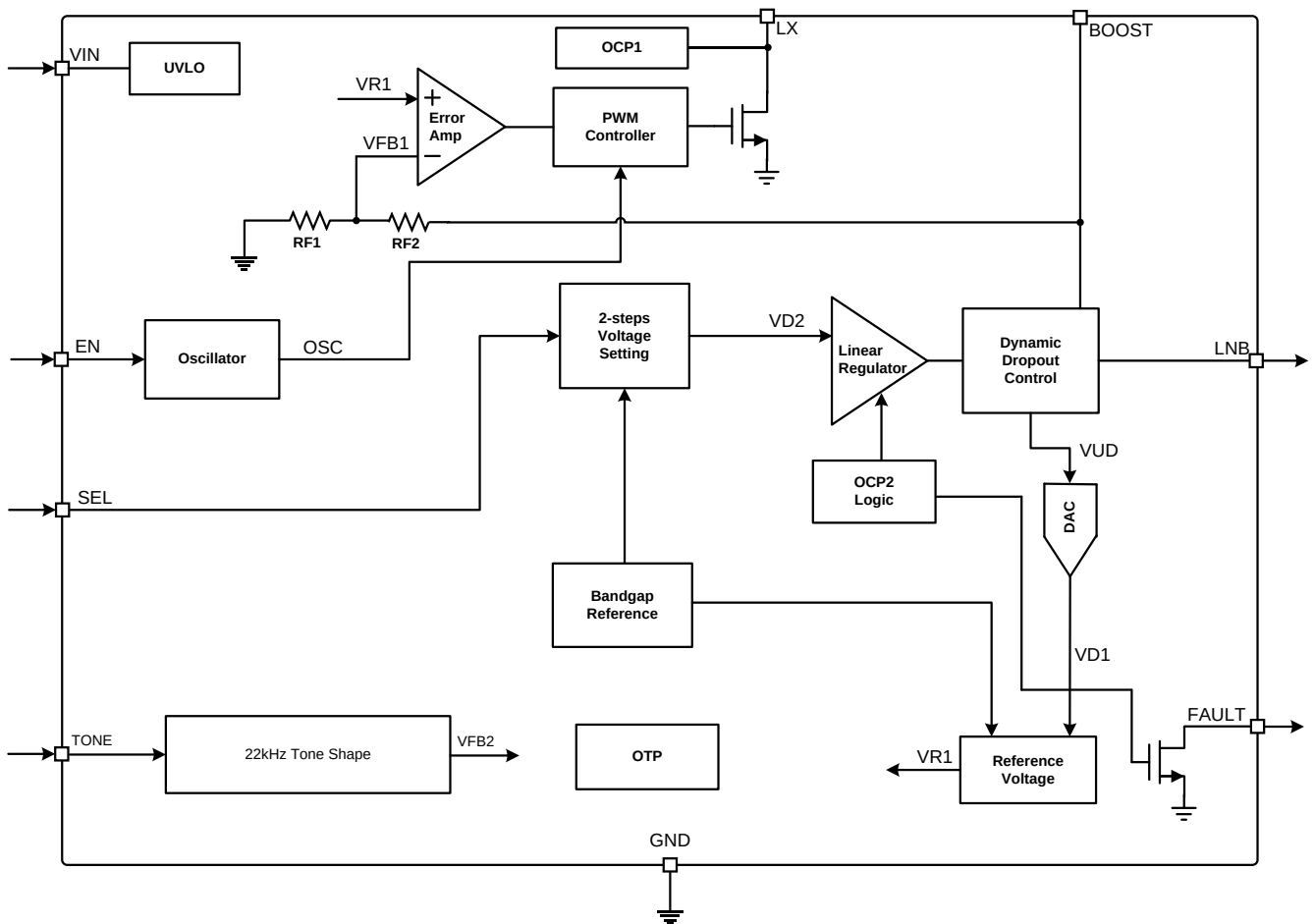
RT5047A  
GSPYMDNN

RT5047AGSP : Product Number  
YMDNN : Date Code

## Functional Pin Description

| Pin No.         | Pin Name | Pin Function                                                                                                |
|-----------------|----------|-------------------------------------------------------------------------------------------------------------|
| 1               | LNB      | Output voltage for LNB.                                                                                     |
| 2               | BOOST    | Boost output and tracking supply voltage to LNB.                                                            |
| 3               | LX       | Switching node of DC-DC boost converter.                                                                    |
| 4               | VIN      | Power supply input.                                                                                         |
| 5               | EN       | LNB output enable.                                                                                          |
| 6               | SEL      | LNB output voltage selection pin (Low is for 13.3V, high is for 18.3V).                                     |
| 7               | FAULT    | Fault detection pin. Pull to 3.3V by 4.7kΩ resistor.                                                        |
| 8               | TONE     | 22kHz TONE input.                                                                                           |
| 9 (Exposed Pad) | GND      | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |

## Function Block Diagram



## Operation

The RT5047A integrates a current mode boost converter and linear regulator. Use the SEL pin to control the LNB voltage and the boost converter track is at least greater 850mV than LNB voltage. The boost converter is the high efficiency PWM architecture with 700kHz operation frequency. The linear regulator has the capability to source current up to 550mA during continuous operation. All the loop compensation, current sensing, and slope compensation functions are provided internally.

### OCP

Both the boost converter and the linear regulator have independent current limit. In the boost converter (OCP1), this is achieved through cycle-by-cycle internal current limit (typ. 3A). In the linear regulator (OCP2), when the linear regulator exceeds OCP more than 48ms, the LNB output will be disabled and re-start after 1.8s.

### Tone Circuit

This circuit is used for tone generation. Use the TONE pin to control output amplitude of LNB.

### OTP

When the junction temperature reaches the critical temperature (typically 150°C), the boost converter and the linear regulator are immediately disabled.

### UVLO

The UVLO circuit compares the VIN with the UVLO threshold (7.7V rising typically) to ensure that the input voltage is high enough for reliable operation. The 350mV (typ.) hysteresis prevents supply transients from causing a shutdown.

### PWM Controller

The loop compensation, current sensing, and slope compensation functions are provided internally.

**Absolute Maximum Ratings** (Note 1)

- Supply Input Voltage,  $V_{IN}$ ----- -0.3V to 28V
- Output Voltage LNB, LX and BOOST Pins ----- -0.3V to 30V
- Others Pin to GND ----- -0.3V to 6V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ\text{C}$   
     SOP-8 (Exposed pad)----- 3.44W
- Package Thermal Resistance (Note 2)  
     SOP-8 (Exposed pad),  $\theta_{JA}$ -----  $29^\circ\text{C/W}$   
     SOP-8 (Exposed pad),  $\theta_{JC}$ -----  $2^\circ\text{C/W}$
- Lead Temperature (Soldering, 10 sec.)-----  $260^\circ\text{C}$
- Junction Temperature-----  $150^\circ\text{C}$
- Storage Temperature Range-----  $-65^\circ\text{C}$  to  $150^\circ\text{C}$
- ESD Susceptibility (Note 3)  
     HBM (Human Body Model)----- 2kV

**Recommended Operating Conditions** (Note 4)

- Supply Input Voltage ----- 8V to 16V
- Ambient Temperature Range-----  $-40^\circ\text{C}$  to  $85^\circ\text{C}$
- Junction Temperature Range -----  $-40^\circ\text{C}$  to  $125^\circ\text{C}$

**Electrical Characteristics**

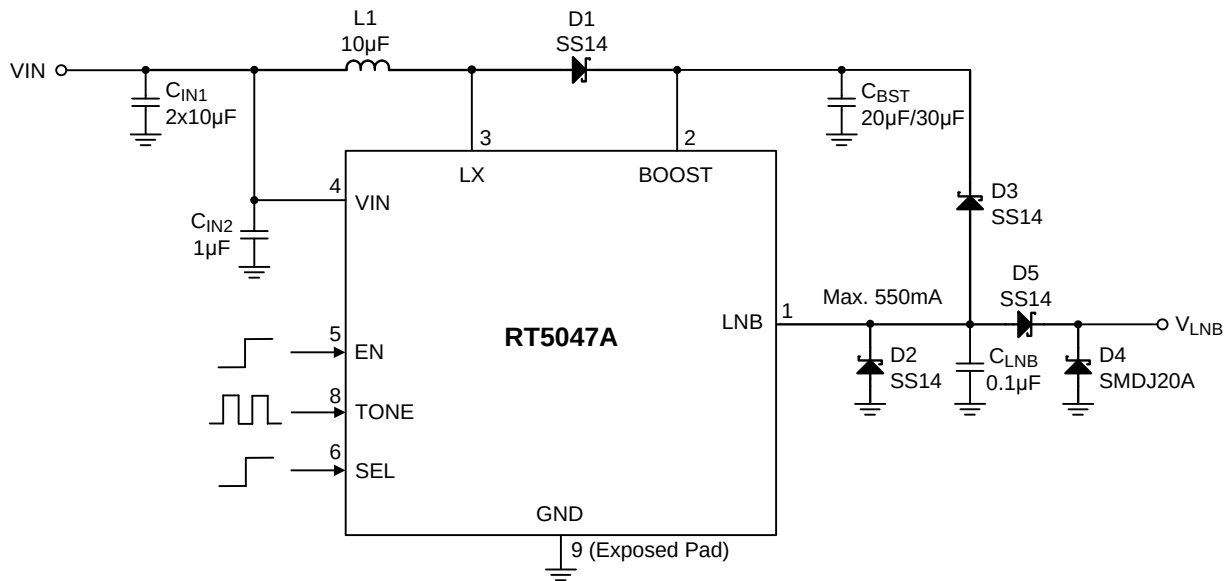
( $V_{IN(\text{typ.})} = 12\text{V}$ ,  $V_{IN} = 8\text{V}$  to  $16\text{V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified)

| Parameter                                     | Symbol        | Test Conditions                                                                                             | Min | Typ  | Max | Unit       |
|-----------------------------------------------|---------------|-------------------------------------------------------------------------------------------------------------|-----|------|-----|------------|
| <b>General</b>                                |               |                                                                                                             |     |      |     |            |
| LNB Output Accuracy, Load and Line Regulation | $E_{RR}$      | Relative to selected $V_{LNB}$ target level, $I_{LNB} = 0$ to $450\text{mA}$                                | -3  | --   | 3   | %          |
| Supply Current                                | $I_{IN\_OFF}$ | EN = 0, LNB output disabled                                                                                 | --  | 0.3  | 0.5 | mA         |
|                                               | $I_{IN\_ON}$  | EN = 1, $V_{LNB} = 18.3\text{V}$ , Tone = 0V                                                                | --  | 10   | 18  | mA         |
|                                               | $I_{IN\_ON}$  | EN = 1, $V_{LNB} = 18.3\text{V}$ , 22kHz TONE Input                                                         | --  | 16   | 28  | mA         |
| Boost Switch On Resistance                    | $R_{DS(ON)}$  | $I_{LNB} = 450\text{mA}$                                                                                    | --  | 150  | 300 | m $\Omega$ |
| Switching Frequency                           | $f_{SW}$      |                                                                                                             | 600 | 700  | 800 | kHz        |
| Switch Current Limit                          | $I_{LIMSW}$   | $V_{IN} = 10\text{V}$ , $V_{LNB} = 20.5\text{V}$                                                            | --  | 3    | --  | A          |
| Linear Regulator Voltage Drop                 | $V_{DROP}$    | $V_{BOOST} - V_{LNB}$ , $I_{LNB} = 450\text{mA}$                                                            | --  | 0.85 | --  | V          |
| Output Voltage Rise Time                      | $T_{R\_LNB}$  | For $V_{LNB} = 13.3\text{V} \rightarrow 18.3\text{V}$ , $C_{LNB} = 100\text{nF}$ , $I_{LNB} = 450\text{mA}$ | --  | 3    | 10  | ms         |
| Output Voltage Pull-Down Time                 | $T_{F\_LNB}$  | For $V_{LNB} = 18.3\text{V} \rightarrow 13.3\text{V}$ , $C_{LNB} = 100\text{nF}$ , $I_{LNB} = 0\text{mA}$   | --  | 3    | 10  | ms         |

| Parameter                                        | Symbol                           | Test Conditions                                                               | Min | Typ  | Max | Unit             |
|--------------------------------------------------|----------------------------------|-------------------------------------------------------------------------------|-----|------|-----|------------------|
| Ripple and Noise on LNB Output                   | V <sub>RIP_PP</sub>              | 20MHz bandwidth limit (GBD)                                                   | --  | 20   | --  | mV <sub>PP</sub> |
| Load Regulation                                  | V <sub>OUT_LOAD</sub>            | V <sub>LNB</sub> = 13.3V, I <sub>LNB</sub> = 50mA to 450mA                    | --  | 38   | 76  | mV               |
|                                                  |                                  | V <sub>LNB</sub> = 18.3V, I <sub>LNB</sub> = 50mA to 450mA                    | --  | 45   | 90  |                  |
| Line Regulation                                  | V <sub>OUT_LINE</sub>            | V <sub>IN</sub> = 9 to 14V, V <sub>LNB</sub> = 13.3V, I <sub>LNB</sub> = 50mA | −10 | --   | 10  | mV               |
|                                                  |                                  | V <sub>IN</sub> = 9 to 14V, V <sub>LNB</sub> = 18.3V, I <sub>LNB</sub> = 50mA | −10 | --   | 10  |                  |
| Protection                                       |                                  |                                                                               |     |      |     |                  |
| Output Over-Current Limit                        | I <sub>LIM_LNB1</sub>            | V <sub>LNB</sub> = 13.3V/18.3V                                                | 500 | 550  | 650 | mA               |
| Output Over-Current Disable Time                 | T <sub>DIS_ON</sub>              | V <sub>LNB</sub> short to GND                                                 | --  | 45   | --  | ms               |
| Output Over-Current Disable Time                 | T <sub>DIS_OFF</sub>             | V <sub>LNB</sub> short to GND (GBD)                                           | --  | 1800 | --  | ms               |
| V <sub>IN</sub> Under-Voltage Lockout Threshold  | V <sub>UVLO</sub>                | V <sub>IN</sub> Fflling                                                       | --  | 7.35 | --  | V                |
| V <sub>IN</sub> Turn On Threshold                | V <sub>IN_TH</sub>               | V <sub>IN</sub> rising                                                        | --  | 7.7  | 8   | V                |
| V <sub>IN</sub> Under-Voltage Lockout Hysteresis | V <sub>UVLOHYS</sub>             |                                                                               | --  | 350  | --  | mV               |
| OTP Threshold                                    | T <sub>OTP</sub>                 |                                                                               | --  | 140  | --  | °C               |
| OTP Hysteresis                                   | T <sub>OTPHYS</sub>              |                                                                               | --  | 15   | --  | °C               |
| TONE                                             |                                  |                                                                               |     |      |     |                  |
| TONE Frequency                                   | F <sub>TONE</sub>                |                                                                               | 20  | 22   | 24  | kHz              |
| TONE Amplitude, Peak to Peak                     | V <sub>TONE_PP</sub>             | I <sub>LNB</sub> = 50 to 450mA, C <sub>LNB</sub> = 200nF                      | 550 | 700  | 900 | mV <sub>PP</sub> |
| TONE Duty Cycle                                  | D <sub>C</sub> <sub>TONE</sub>   | I <sub>LNB</sub> = 0 to 450mA, C <sub>LNB</sub> = 570nF                       | 40  | 50   | 60  | %                |
| TONE Rise Time                                   | T <sub>RTONE</sub>               | I <sub>LNB</sub> = 0 to 450mA, C <sub>LNB</sub> = 570nF                       | 5   | 10   | 15  | μs               |
| TONE Fall Time                                   | T <sub>FTONE</sub>               | I <sub>LNB</sub> = 0 to 450mA, C <sub>LNB</sub> = 570nF                       | 5   | 10   | 15  | μs               |
| TONE Logic Input                                 | V <sub>TONE_H</sub>              |                                                                               | 1.2 | --   | --  | V                |
|                                                  | V <sub>TONE_L</sub>              |                                                                               | --  | --   | 0.4 | V                |
| TONE Input Leakage                               | I <sub>TONE</sub> <sub>LKG</sub> |                                                                               | --  | 5    | 10  | μA               |
| ENABLE, SEL Pins                                 |                                  |                                                                               |     |      |     |                  |
| EN Logic Input                                   | V <sub>EN_H</sub>                |                                                                               | 1.2 | --   | --  | V                |
|                                                  | V <sub>EN_L</sub>                |                                                                               | --  | --   | 0.4 | V                |
| EN Input Leakage                                 | I <sub>EN</sub> <sub>LKG</sub>   |                                                                               | --  | 5    | 10  | μA               |
| SEL Logic Input                                  | V <sub>SEL_H</sub>               |                                                                               | 1.2 | --   | --  | V                |
|                                                  | V <sub>SEL_L</sub>               |                                                                               | --  | --   | 0.4 | V                |
| SEL Input Leakage                                | I <sub>SEL</sub> <sub>LKG</sub>  |                                                                               | --  | 5    | 10  | μA               |

- Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
- Note 2.**  $\theta_{JA}$  is measured at  $T_A = 25^{\circ}\text{C}$  on a high effective thermal conductivity four-layer test board per JEDEC 51-7.  $\theta_{JC}$  is measured at the exposed pad of the package.
- Note 3.** Devices are ESD sensitive. Handling precaution is recommended.
- Note 4.** The device is not guaranteed to function outside its operating conditions.
- Note 5.** Operation at  $V_{IN} = 16\text{V}$  may be limited by power loss in the linear regulator.

## Typical Application Circuit



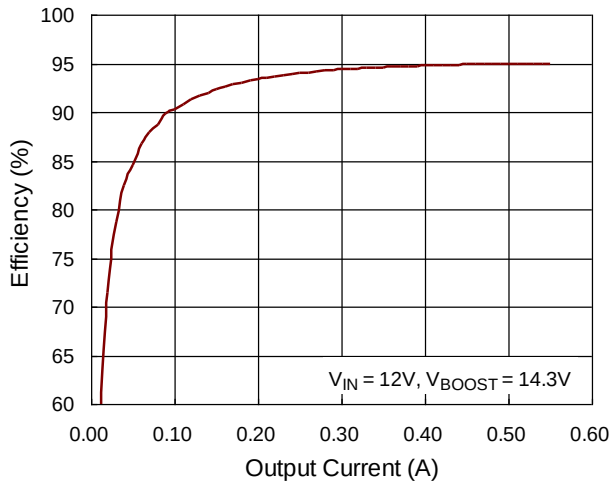
Note :

1. D2, D3, D4, D5 are used for surge protection.
2. The capacitor C3 should not be less than 1 $\mu$ F for the power stability.
3. EN, TONE and SEL are connected to microcontroller directly.

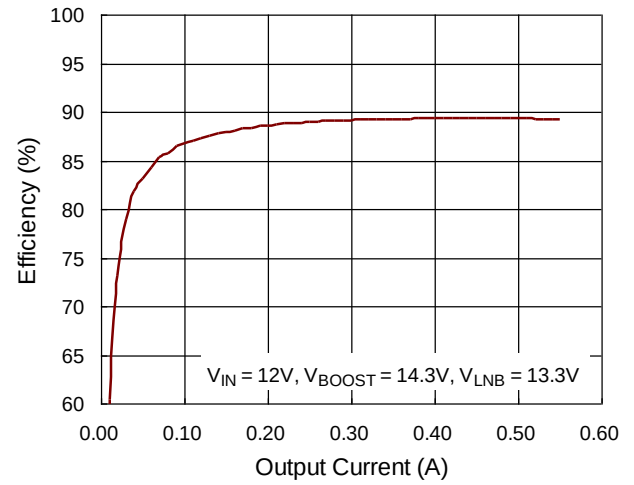


## Typical Operating Characteristics

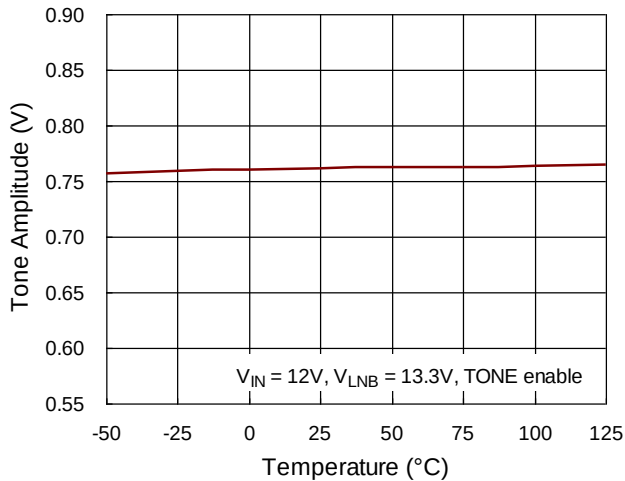
### Boost Efficiency vs. Output Current



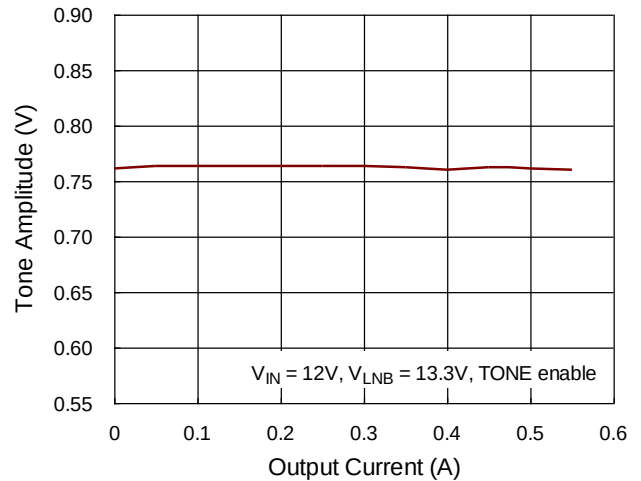
### System Efficiency vs. Output Current



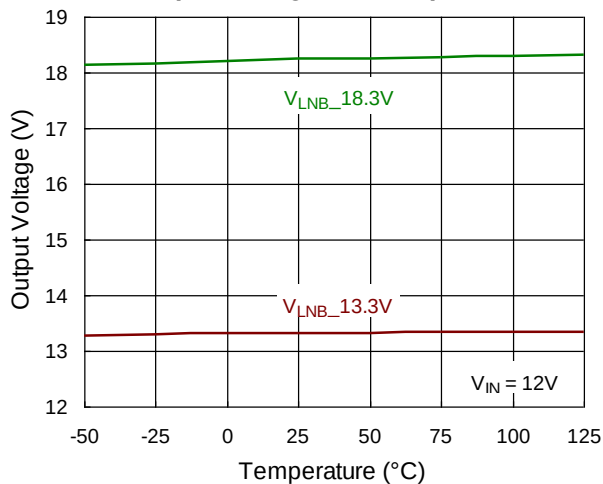
### Tone Amplitude vs. Temperature



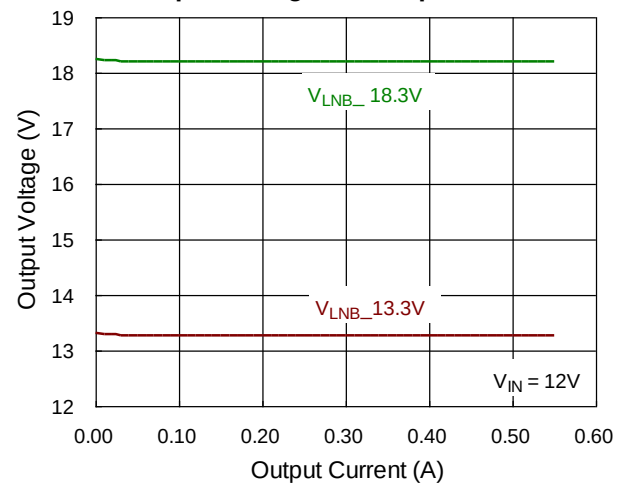
### Tone Amplitude vs. Output Current



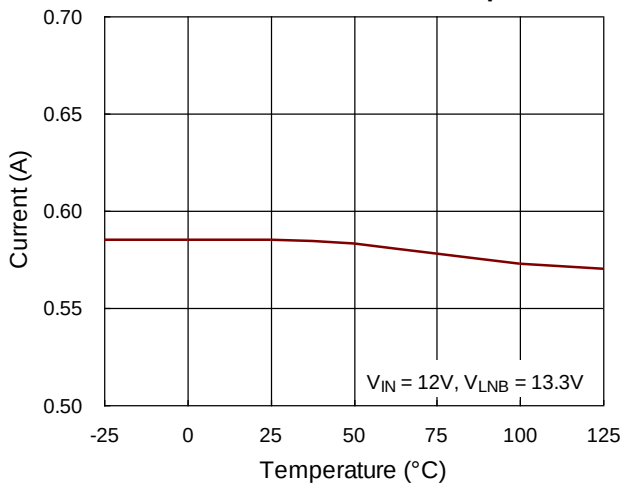
### Output Voltage vs. Temperature



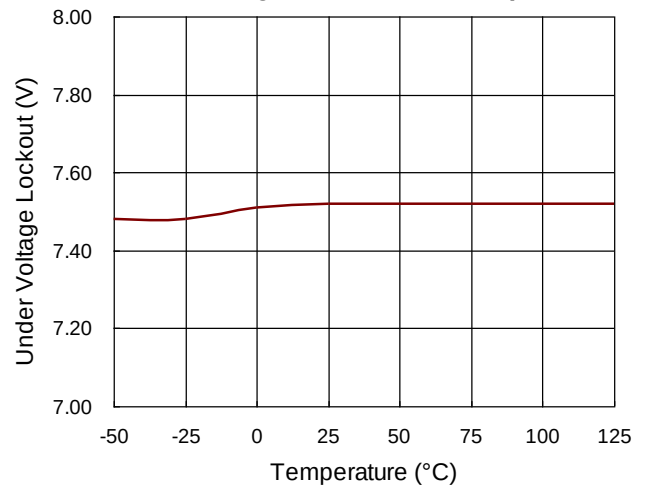
### Output Voltage vs. Output Current



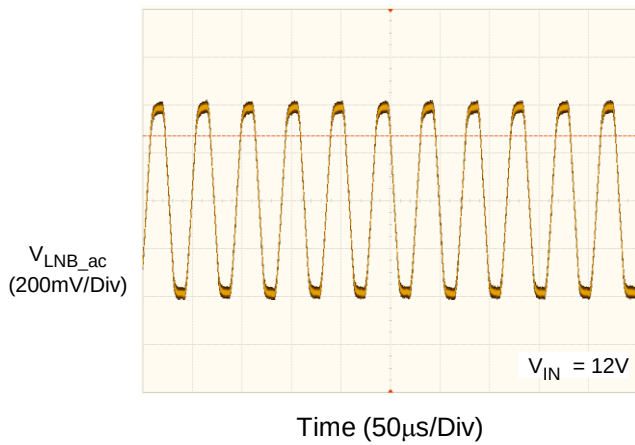
Over Current Protect vs. Temperature



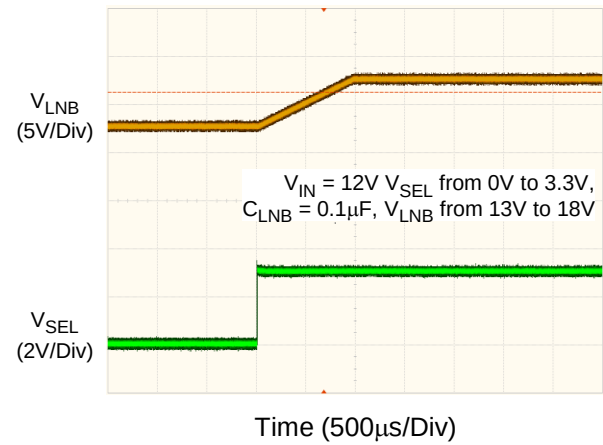
Under Voltage Lockout vs. Temperature



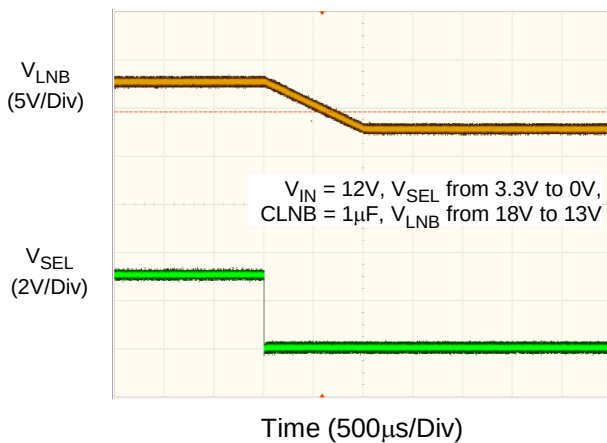
Tone Output



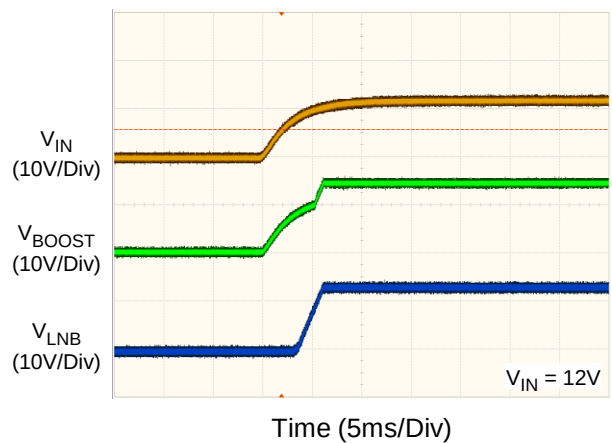
Output Voltage Transition Rising

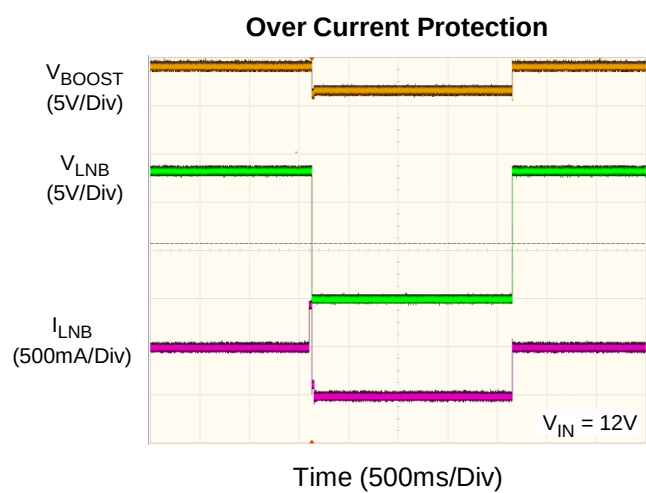


Output Voltage Transition Falling



Power On Sequence





## Application Information

### Boost Converter/Linear Regulator

The 5047A integrates a current-mode boost converter and linear regulator. Use the SEL pin to control the LNB voltage and the boost converter track is at least greater 800mV than the LNB voltage. The boost converter is high efficiency PWM architecture with 700kHz operation frequency. The linear regulator has the capability to source current up to 550mA during continuous operation. All the loop compensation, current sensing, and slope compensation functions are provided internally.

The RT5047A has current limiting on the boost converter and the LNB output to protect the IC against short circuits. The internal MOSFET will turn off when the LX current is higher than 3A cycle-by-cycle. The LNB output will turn off when the output current higher than the 550mA and 45ms and turn-on after 1800ms automatically.

### Input Capacitor Selection

The input capacitor reduces voltage spikes from the input supply and minimizes noise injection to the converter. A 30μF capacitance is sufficient for most applications. Nevertheless, a higher or lower value may be used depending on the noise level from the input supply and the input current to the converter. Note that the voltage rating of the input capacitor must be greater than the maximum input voltage.

### Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

where  $\eta$  is the efficiency of the converter,  $I_{IN(MAX)}$  is the maximum input current, and  $I_{RIPPLE}$  is the inductor ripple current. The input peak current can then be obtained by adding the maximum input current

with half of the inductor ripple current as shown in the following equation :

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

note that the saturated current of the inductor must be greater than  $I_{PEAK}$ . The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where  $f_{OSC}$  is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

### Boost Output Capacitor Selection

The RT5047A boost regulator is internally compensated and relies on the inductor and output capacitor value for overall loop stability. The output capacitor is in the 30μF to 50μF range with a low ESR, as strongly recommended. The voltage rating on this capacitor should be in the 25V to 35V range since it is connected to the boost  $V_{OUT}$  rail.

The output ripple voltage is an important index for estimating chip performance. This portion consists of two parts. One is the product of the inductor current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. As shown in Figure 1,  $\Delta V_{OUT1}$  can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$Q = \frac{1}{2} \times \left[ \left( I_{IN} + \frac{1}{2} \Delta I_L - I_{OUT} \right) + \left( I_{IN} - \frac{1}{2} \Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

where  $f_{OSC}$  is the switching frequency and  $\Delta I_L$  is the inductor ripple current. Bring  $C_{OUT}$  to the left side to estimate the value of  $\Delta V_{OUT1}$  according to the following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

where  $D$  is the duty cycle and  $\eta$  is the boost converter efficiency. Finally, take ESR into consideration, the overall output ripple voltage can be determined by the following equation :

$$\Delta V_{OUT} = I_{IN} \times ESR + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

The output capacitor,  $C_{OUT}$ , should be selected accordingly.

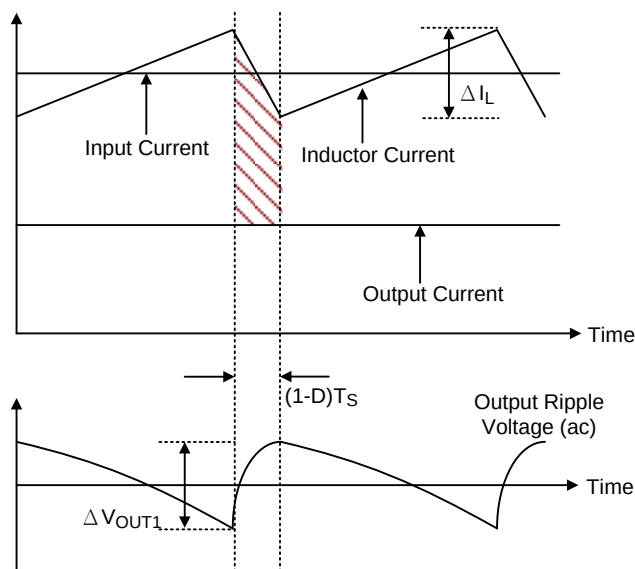


Figure 1. The Output Ripple Voltage without the Contribution of ESR

### Schottky Diode Selection

Schottky diodes are chosen for their low forward-voltage drop and fast switching speed. However, when making a selection, important parameters such as power dissipation, reverse voltage rating, and pulsating peak current should all be taken into consideration. A suitable Schottky diode's reverse voltage rating must be greater than the maximum output voltage and its average current rating must exceed the average output current. The chosen diode should also have a sufficiently low leakage current level, since it increases with temperature.

### Under-Voltage Lockout (UVLO)

The UVLO circuit compares the input voltage at  $V_{IN}$  with the UVLO threshold (7.7V rising typically) to ensure that the input voltage is high enough for reliable

operation. The 350mV (typ.) hysteresis prevents supply transients from causing a shutdown. Once the input voltage exceeds the UVLO rising threshold, start-up begins. When the input voltage falls below the UVLO falling threshold, all IC internal functions will be turned off by the controller.

### Over-Current Protection

The RT5047A features an over-current protection function to prevent chip damage from high peak currents. Both the boost converter and the linear regulator have independent current limit. In the boost converter, this is achieved through cycle-by-cycle internal current limit. During the ON-period, the chip senses the inductor current that is flowing into the LX pin. The internal NMOS will be turned off if the peak inductor current reaches the current-limit value of 3A (typ.). When the linear regulator exceeds 550mA (typ.) more than 45ms, the LNB output will be disabled. During this period of time, if the current limit condition disappears, the OCP will be cleared and the part restarts. If the part is still in current limit after this time period, the linear regulator and boost converter will automatically disable to prevent the part from overheating.

### Short Circuit Protection

If the LNB output is shorted to ground, and more than 45ms, the RT5047A will be disabled 1.8s then enable automatically.

### Over-Temperature Protection

When the junction temperature reaches the critical temperature (typically 140 °C), the boost converter and the linear regulator are immediately disabled. When the junction temperature cools down to a lower temperature threshold specified, the RT5047A will be allowed to restart by normal start operation.

### LNB Output Voltage

The RT5047A has voltage control function on the LNB output. This function provides 4 levels for the common standards and compensation if the cable line has voltage drop. These voltage levels are defined in table 1. The rise time and fall time of the VLNB is 3mS (typ.).

Table 1

| SEL Pin Status | LNB Output Voltage |
|----------------|--------------------|
| 0              | 13.3V              |
| 1              | 18.3V              |

### Tone Generation

The RT5047A provides the tone generation function, please refer to the Figure 2. Set the TONE pin with 22kHz logic signal, the LNB linear regulator output will carry a 22kHz, 700mV peak to peak signal for DiSEqC 1.x communication. It can meet base-band timings of 500 $\mu$ s ( $\pm$ 100 $\mu$ s) for a one-third bit PWK coded signal period on a nominal 22kHz ( $\pm$ 20 %).

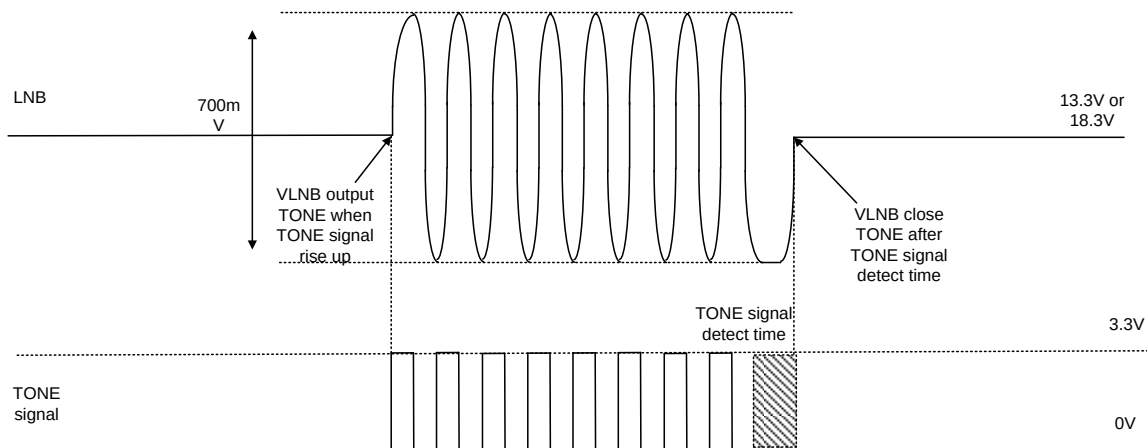


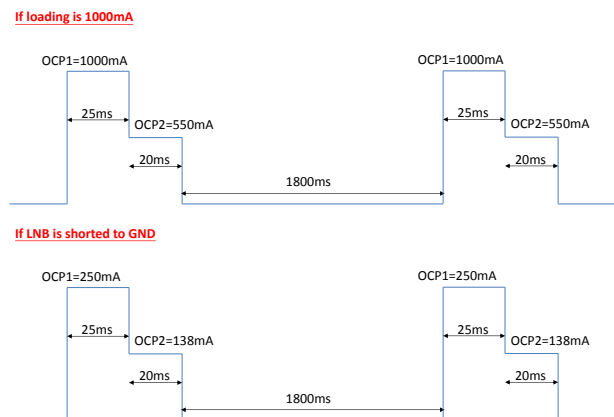
Figure 2. Tone Generation Options

### Pull-Down Rate Control

The output linear stage provides approximately 40mA of pull-down capability. This ensures that the output volts are ramped from 18.3V to 13.3V in a reasonable amount of time.

### Over-Current Disable Time

If the LNB output current exceeds 550mA, typical, for more than 45ms, then the LNB output will be disabled and device enters a TON = 45ms/TOFF = 1800ms routine. It will be returned to normal operation after a successful soft-start process.



### Inrush Current

At start-up or during a LNB reconfiguration event, a transient surge current above the normal DC operating level can be provided by the IC. This current increase can be as high as 550mA, typical, for as long as required, up to a maximum of 45ms.

## DC Current

The RT5047A can handle up to 500mA during continuous operation.

## Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance,  $\theta_{JA}$ , is 29°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (29^\circ\text{C/W}) = 3.44\text{W for SOP-8 (Exposed Pad) package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

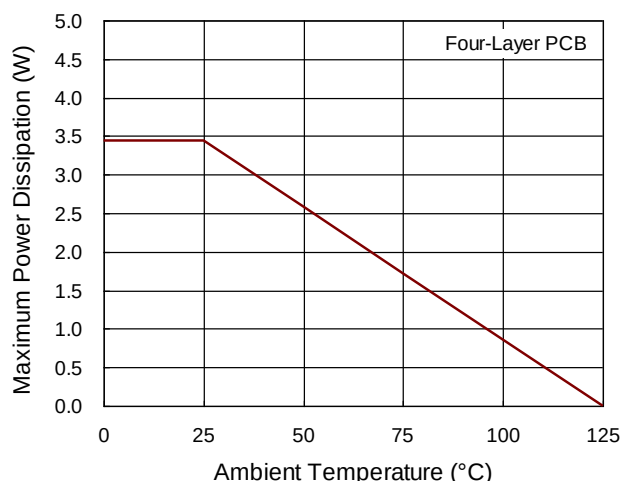


Figure 3. Derating Curve of Maximum Power Dissipation

## Layout Consideration

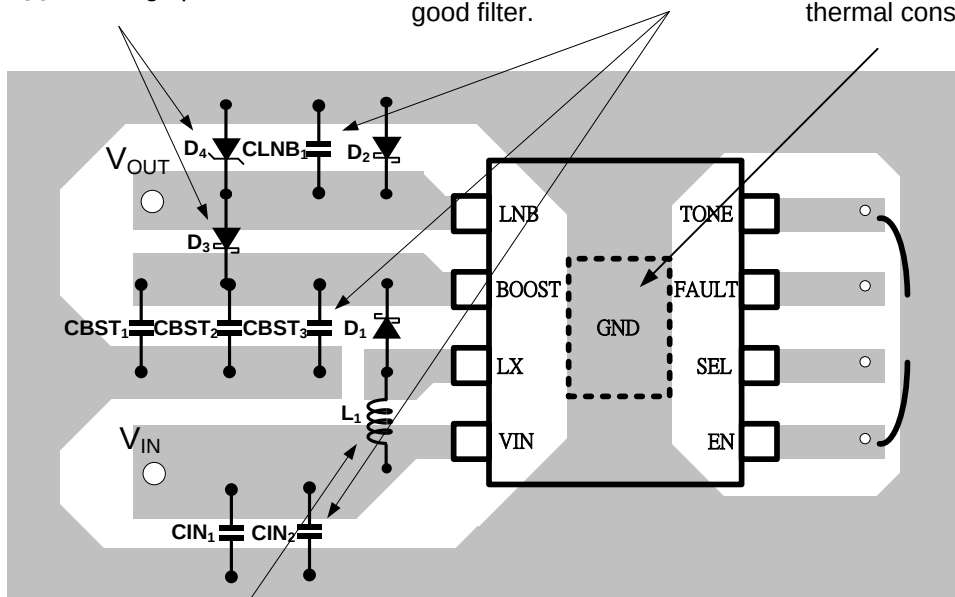
For high frequency switching power supplies, the PCB layout is important to get good regulation, high efficiency and stability. The following descriptions are the guidelines for better PCB layout.

- For good regulation, place the power components as close as possible. The traces should be wide and short enough especially for the high-current loop.
- Minimize the size of the LX node and keep it wide and shorter.
- The exposed pad of the chip should be connected to a strong ground plane for maximum thermal consideration.

D<sub>3</sub> and D<sub>4</sub> should be placed as closed as possible to V<sub>OUT</sub> for surge protection.

The CIN, CBST and CLNB should be placed as closed as possible to RT5047 for good filter.

The exposed pad of the chip should be connected to analog ground plane for thermal consideration.



The TONE, SEL and EN pin should be connected to MCU or GND. Do not floating these pins.

The inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.

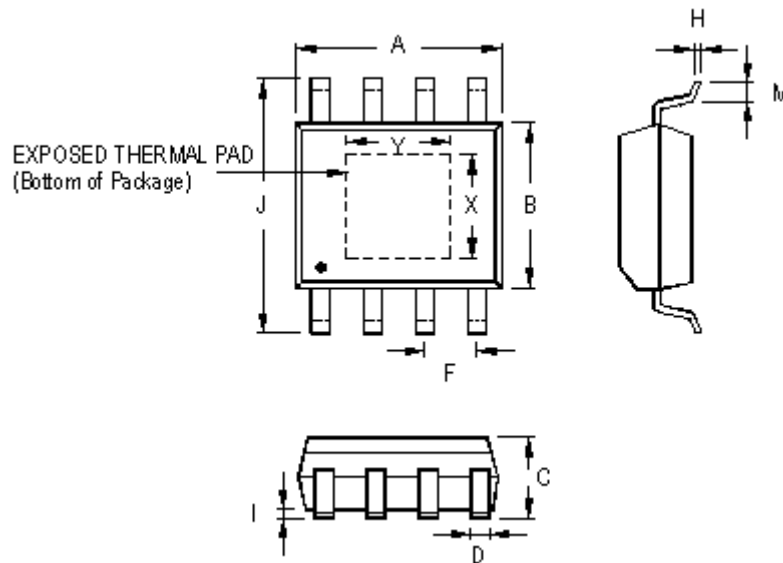
LX node copper area should be minimized for reducing EMI

Place the power components as close as possible. The traces should be wide and short especially for the high-current loop.

Figure 4. PCB Layout Guide



## Outline Dimension



| Symbol   |   | Dimensions In Millimeters |       | Dimensions In Inches |       |
|----------|---|---------------------------|-------|----------------------|-------|
|          |   | Min                       | Max   | Min                  | Max   |
| A        |   | 4.801                     | 5.004 | 0.189                | 0.197 |
| B        |   | 3.810                     | 4.000 | 0.150                | 0.157 |
| C        |   | 1.346                     | 1.753 | 0.053                | 0.069 |
| D        |   | 0.330                     | 0.510 | 0.013                | 0.020 |
| F        |   | 1.194                     | 1.346 | 0.047                | 0.053 |
| H        |   | 0.170                     | 0.254 | 0.007                | 0.010 |
| I        |   | 0.000                     | 0.152 | 0.000                | 0.006 |
| J        |   | 5.791                     | 6.200 | 0.228                | 0.244 |
| M        |   | 0.406                     | 1.270 | 0.016                | 0.050 |
| Option 1 | X | 2.000                     | 2.300 | 0.079                | 0.091 |
|          | Y | 2.000                     | 2.300 | 0.079                | 0.091 |
| Option 2 | X | 2.100                     | 2.500 | 0.083                | 0.098 |
|          | Y | 3.000                     | 3.500 | 0.118                | 0.138 |

8-Lead SOP (Exposed Pad) Plastic Package

## Richtek Technology Corporation

14F, No. 8, Tai Yuen 1<sup>st</sup> Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

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