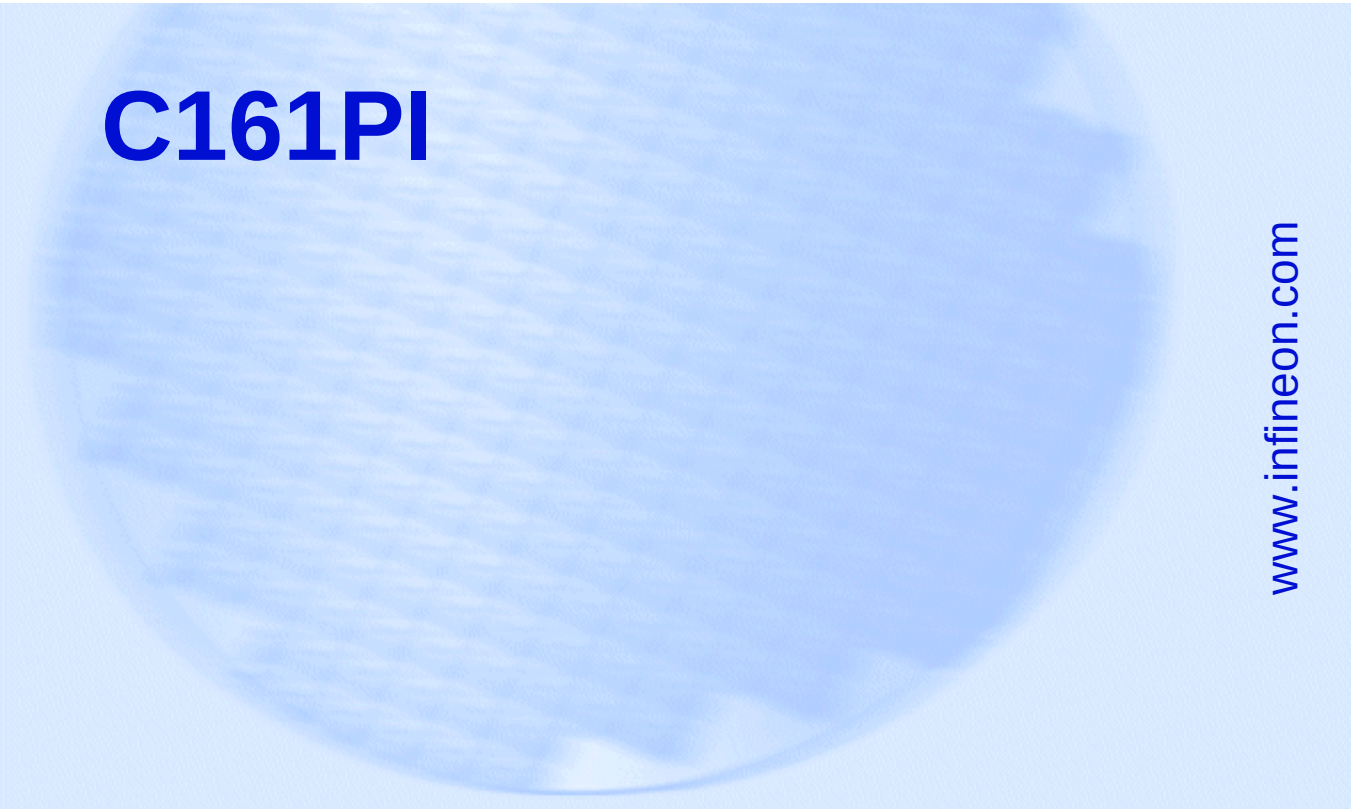
THE DATASHEET OF

C161PILF3VCAFXUMA1



Microcontrollers

C166 Family

16-Bit Single-Chip Microcontroller

C161PI

Data Sheet 1999-07

Preliminary

C161PI Revision History:	1999-07 Preliminary	
Previous Versions:	1998-05 1998-01 1997-12	(C161RI / Preliminary) (C161RI / Advance Information) (C161RI / Advance Information)

Page	Subjects
---	3 V specification introduced
4, 5, 7	Signal FOUT added
14	XRAM description added
15	Unlatched $\overline{CS}$ description added
23	Block Diagram corrected
24	Description of divider chain improved
25, 51, 52	ADC description updated to 10-bit
36, 37	Revised description of Absolute Max. Ratings and Operating Conditions
39, 44	Power supply values improved
45 - 50	Revised description for clock generation including PLL
54 ff.	Standard 25-MHz timing

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com

The C161PI is the successor of the C161RI. Therefore this data sheet also replaces the C161RI data sheet (see also revision history).

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C166 Family of C161PI
High-Performance CMOS 16-Bit Microcontrollers

Preliminary
C161PI 16-Bit Microcontroller

- High Performance 16-bit CPU with 4-Stage Pipeline
  - 80 ns Instruction Cycle Time at 25 MHz CPU Clock
  - 400 ns Multiplication (16 × 16 bit), 800 ns Division (32 / 16 bit)
  - Enhanced Boolean Bit Manipulation Facilities
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Single-Cycle Context Switching Support
  - 16 MBytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 27 Sources, Sample-Rate down to 40 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clk. Generation via on-chip PLL (1:1.5/2/2.5/3/4/5), via prescaler or via direct clk. inp.
- On-Chip Memory Modules
  - 1 KByte On-Chip Internal RAM (IRAM)
  - 2 KBytes On-Chip Extension RAM (XRAM)
- On-Chip Peripheral Modules
  - 4-Channel 10-bit A/D Converter with Programm. Conversion Time down to 7.8 µs
  - Two Multi-Functional General Purpose Timer Units with 5 Timers
  - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
  - I^2C Bus Interface (10-bit Addressing, 400 KHz) with 2 Channels (multiplexed)
- Up to 8 MBytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
- Idle and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- On-Chip Real Time Clock
- Up to 76 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 100-Pin MQFP / TQFP Package

This document describes the **SAB-C161PI-LM**, the **SAB-C161PI-LF**, the **SAF-C161PI-LM** and the **SAF-C161PI-LF**.
For simplicity all versions are referred to by the term **C161PI** throughout this document.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set
- the specified temperature range
- the package
- the type of delivery.

For the available ordering codes for the **C161PI** please refer to the „**Product Catalog Microcontrollers**“, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

Introduction

The C161PI is a derivative of the Infineon C166 Family of 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 8 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. The C161PI derivative is especially suited for cost sensitive applications.

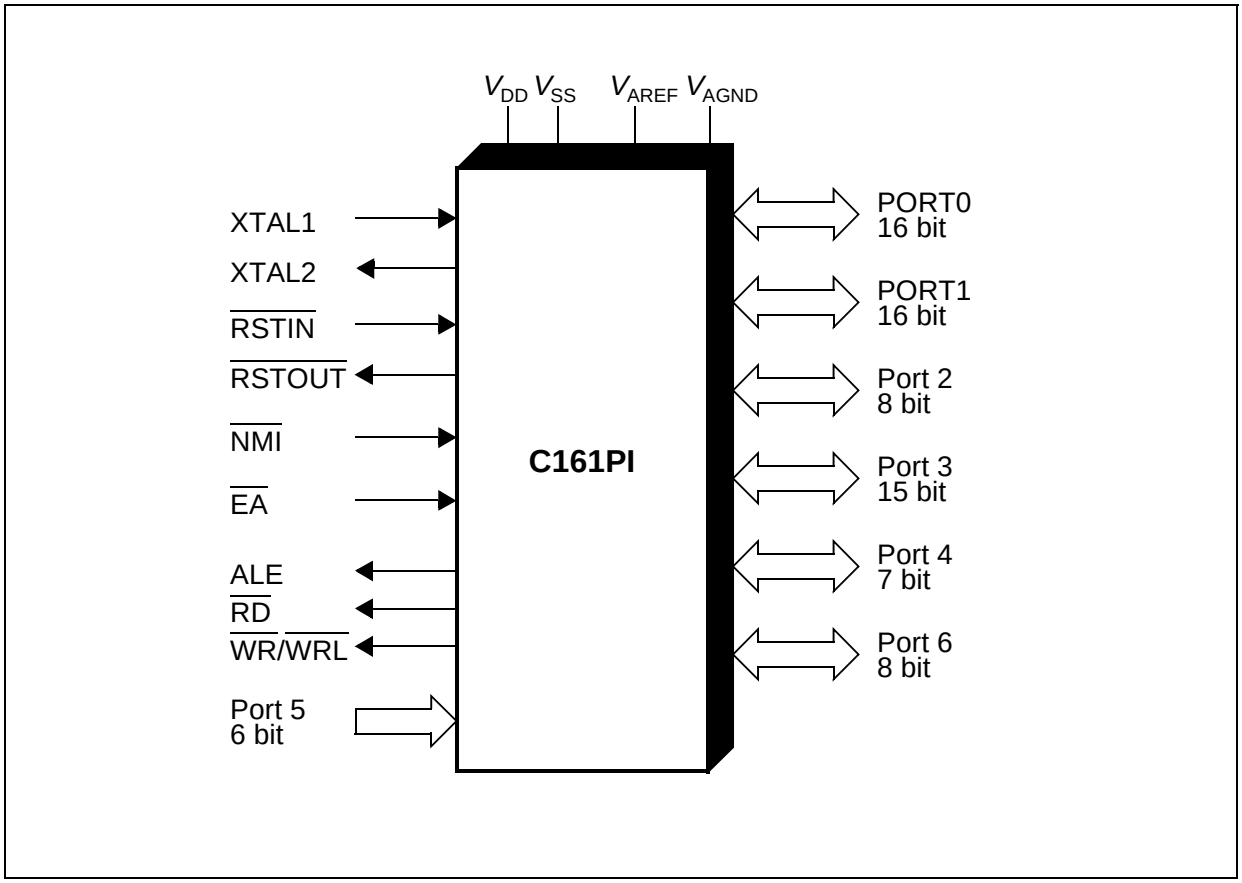


Figure 1 Logic Symbol

Pin Configuration MQFP Package

(top view)

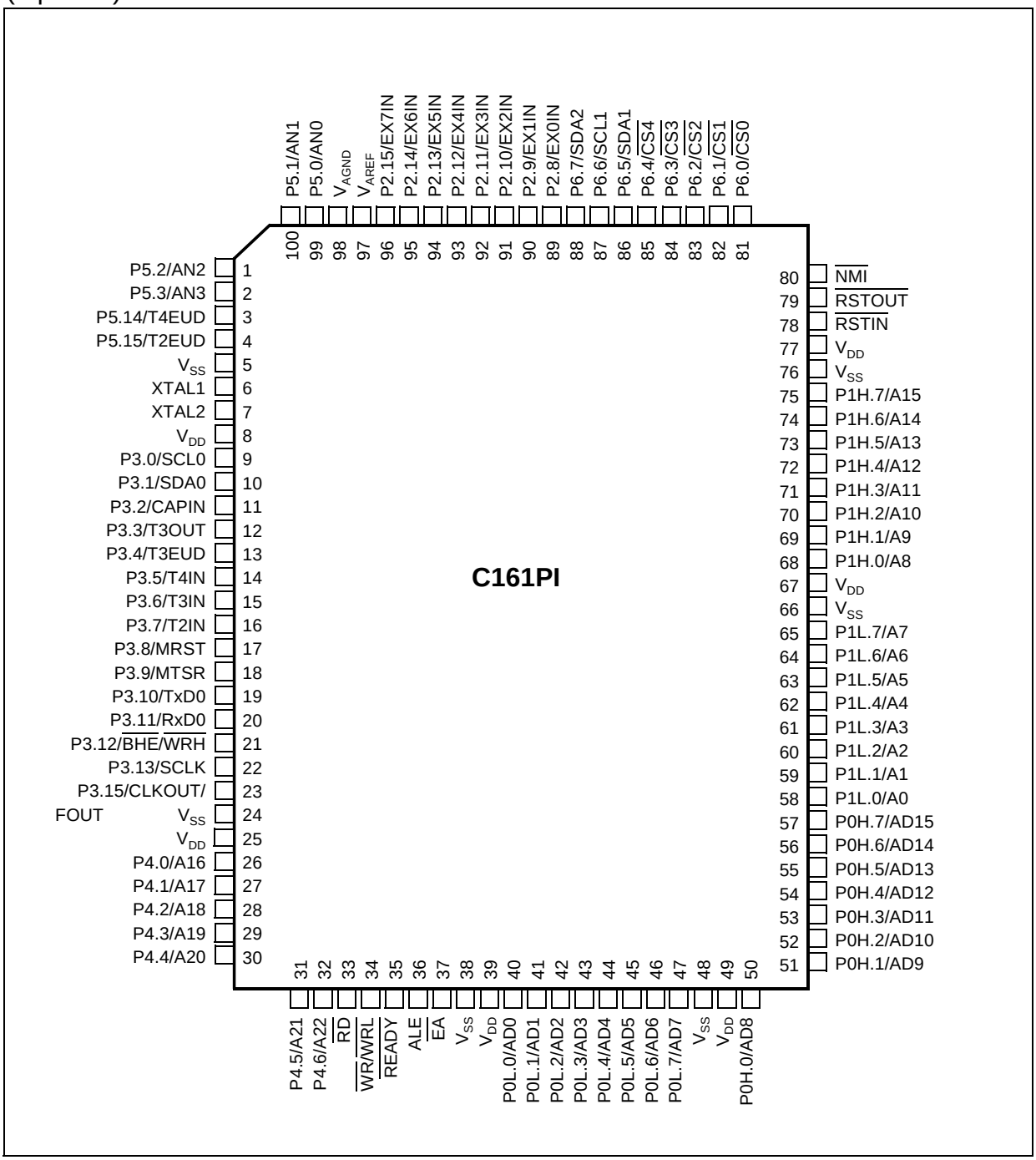


Figure 2

Pin Configuration TQFP Package

(top view)

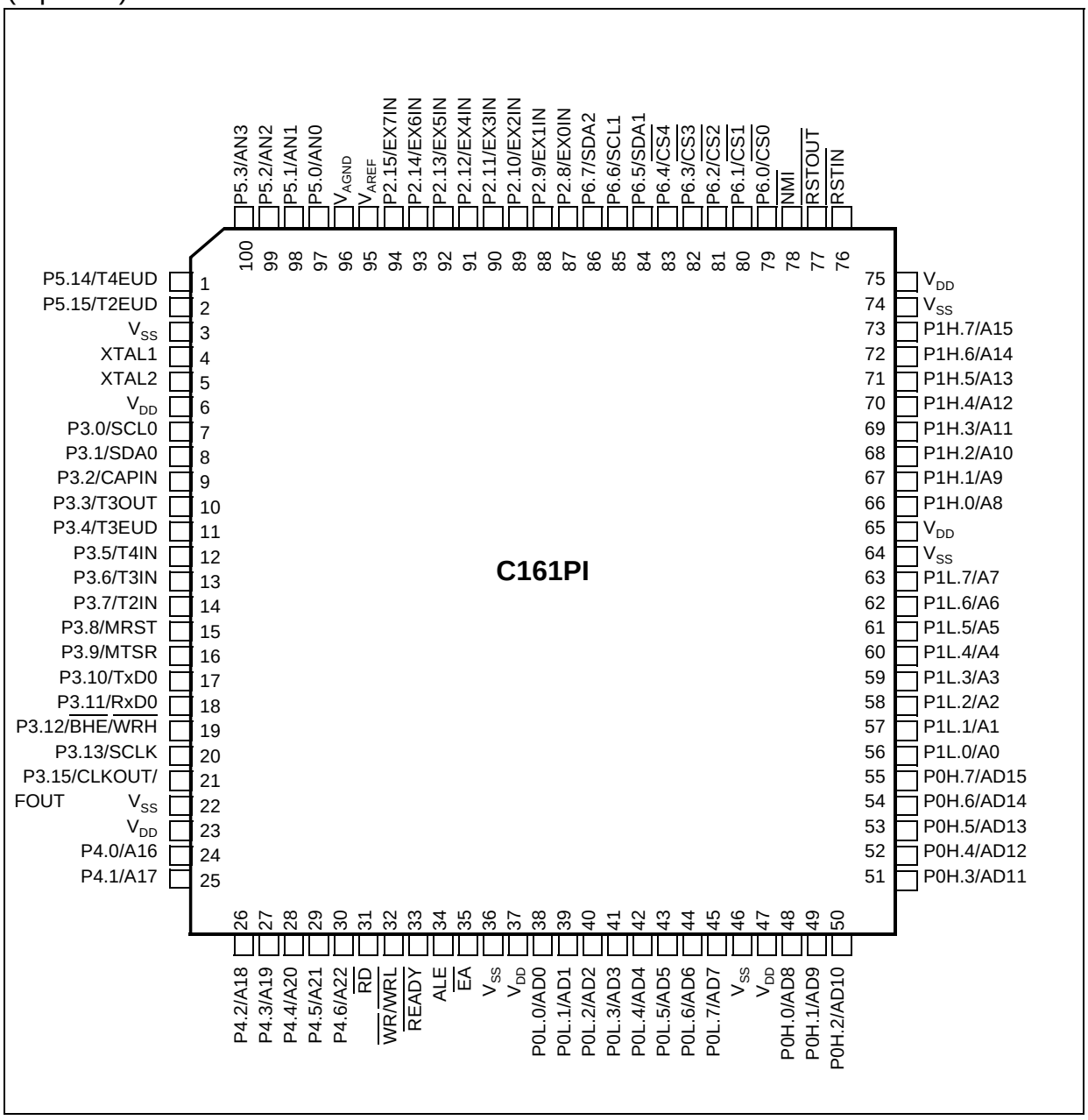


Figure 3

Table 1 Pin Definitions and Functions

Symbol	Pin Num. TQFP	Pin Num. MQFP	Input Outp.	Function
P5			I	Port 5 is a 6-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as (up to 4) analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	97	99	I	AN0
P5.1	98	100	I	AN1
P5.2	99	1	I	AN2
P5.3	100	2	I	AN3
P5.14	1	3	I	T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Input
P5.15	2	4	I	T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Input
XTAL1	4	6	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator
XTAL2	5	7	O	XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.

Table 1 Pin Definitions and Functions (continued)

Symbol	Pin Num. TQFP	Pin Num. MQFP	Input Outp.	Function	
P3			IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	7	9	I/O	SCL0	I2C Bus Clock Line 0
P3.1	8	10	I/O	SDA0	I2C Bus Data Line 0
P3.2	9	11	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	10	12	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	11	13	I	T3EUD	GPT1 Timer T3 External Up/Down Ctrl.Inp
P3.5	12	14	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/ Capture Input
P3.6	13	15	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	14	16	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/ Capture Input
P3.8	15	17	I/O	MRST	SSC Master-Rec. / Slave-Trans. Inp/Outp.
P3.9	16	18	I/O	MTSR	SSC Master-Trans. / Slave-Rec. Outp/Inp.
P3.10	17	19	O	T×D0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	18	20	I/O	R×D0	ASC0 Data Input (Async.) or I/O (Sync.)
P3.12	19	21	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
			O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe
P3.13	20	22	I/O	SCLK	SSC Master Clock Outp. / Slave Clock Inp.
P3.15	21	23	O	CLKOUT	System Clock Output (=CPU Clock)
			O	FOUT	Programmable Frequency Output
				Note: Pins P3.0 and P3.1 are open drain outputs only.	

Table 1 Pin Definitions and Functions (continued)

Symbol	Pin Num. TQFP	Pin Num. MQFP	Input Outp.	Function
P4			IO	Port 4 is a 7-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 4 is selectable (TTL or special). Port 4 can be used to output the segment address lines:
P4.0	24	26	O	A16 Least Significant Segment Address Line
P4.1	25	27	O	A17 Segment Address Line
P4.2	26	28	O	A18 Segment Address Line
P4.3	27	29	O	A19 Segment Address Line
P4.4	28	30	O	A20 Segment Address Line
P4.5	29	31	O	A21 Segment Address Line
P4.6	30	32	O	A22 Most Significant Segment Address Line
$\overline{RD}$	31	33	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/ WRL	32	34	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In WRL-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	33	35	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pullup device will hold this pin high when nothing is driving it.
ALE	34	36	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.

Table 1 Pin Definitions and Functions (continued)

Symbol	Pin Num. TQFP	Pin Num. MQFP	Input Outp.	Function
$\overline{EA}$	35	37	I	External Access Enable pin. A low level at this pin during and after Reset forces the C161PI to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to ‘0’.
PORT0 P0L.0-7 P0H.0-7	 38-45 48-55	 40-47 50-57	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of external bus configurations, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 - D7 P0H.0 – P0H.7: I/O D8 - D15 **Multiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7 P0H.0 – P0H.7: A8 - A15 AD8 - AD15
PORT1 P1L.0-7 P1H.0-7	 56-63 66-73	 58-65 68-75	IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.

Table 1 Pin Definitions and Functions (continued)

Symbol	Pin Num. TQFP	Pin Num. MQFP	Input Outp.	Function
$\overline{\text{RSTIN}}$	76	78	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C161PI. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table. *Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.*
$\overline{\text{RSTOUT}}$	77	79	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	78	80	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C161PI to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.

Table 1 Pin Definitions and Functions (continued)

Symbol	Pin Num. TQFP	Pin Num. MQFP	Input Outp.	Function
P6			IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The Port 6 pins also serve for alternate functions:
P6.0	79	81	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	80	82	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	81	83	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	82	84	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	83	85	O	CS4 Chip Select 4 Output
P6.5	84	86	I/O	SDA1 I^2C Bus Data Line 1
P6.6	85	87	I/O	SCL1 I^2C Bus Clock Line 1
P6.7	86	88	I/O	SDA2 I^2C Bus Data Line 2
				Note: Pins P6.7-5 are open drain outputs only.
P2			IO	Port 2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The Port 2 pins also serve for alternate functions:
P2.8	87	89	I	EX0IN Fast External Interrupt 0 Input
P2.9	88	90	I	EX1IN Fast External Interrupt 1 Input
P2.10	89	91	I	EX2IN Fast External Interrupt 2 Input
P2.11	90	92	I	EX3IN Fast External Interrupt 3 Input
P2.12	91	93	I	EX4IN Fast External Interrupt 4 Input
P2.13	92	94	I	EX5IN Fast External Interrupt 5 Input
P2.14	93	95	I	EX6IN Fast External Interrupt 6 Input
P2.15	94	96	I	EX7IN Fast External Interrupt 7 Input
V_{AREF}	95	97	-	Reference voltage for the A/D converter.
V_{AGND}	96	98	-	Reference ground for the A/D converter.

Table 1 Pin Definitions and Functions (continued)

Symbol	Pin Num. TQFP	Pin Num. MQFP	Input Outp.	Function
V_{DD}	6, 23, 37, 47, 65, 75	8, 25, 39, 49, 67, 77	-	Digital Supply Voltage: + 5 V or + 3 V during normal operation and idle mode. ≥ 2.5 V during power down mode
V_{SS}	3, 22, 36, 46, 64, 74	5, 24, 38, 48, 66, 76	-	Digital Ground.

Note: The following behaviour differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Functional Description

The architecture of the C161PI combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C161PI.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).

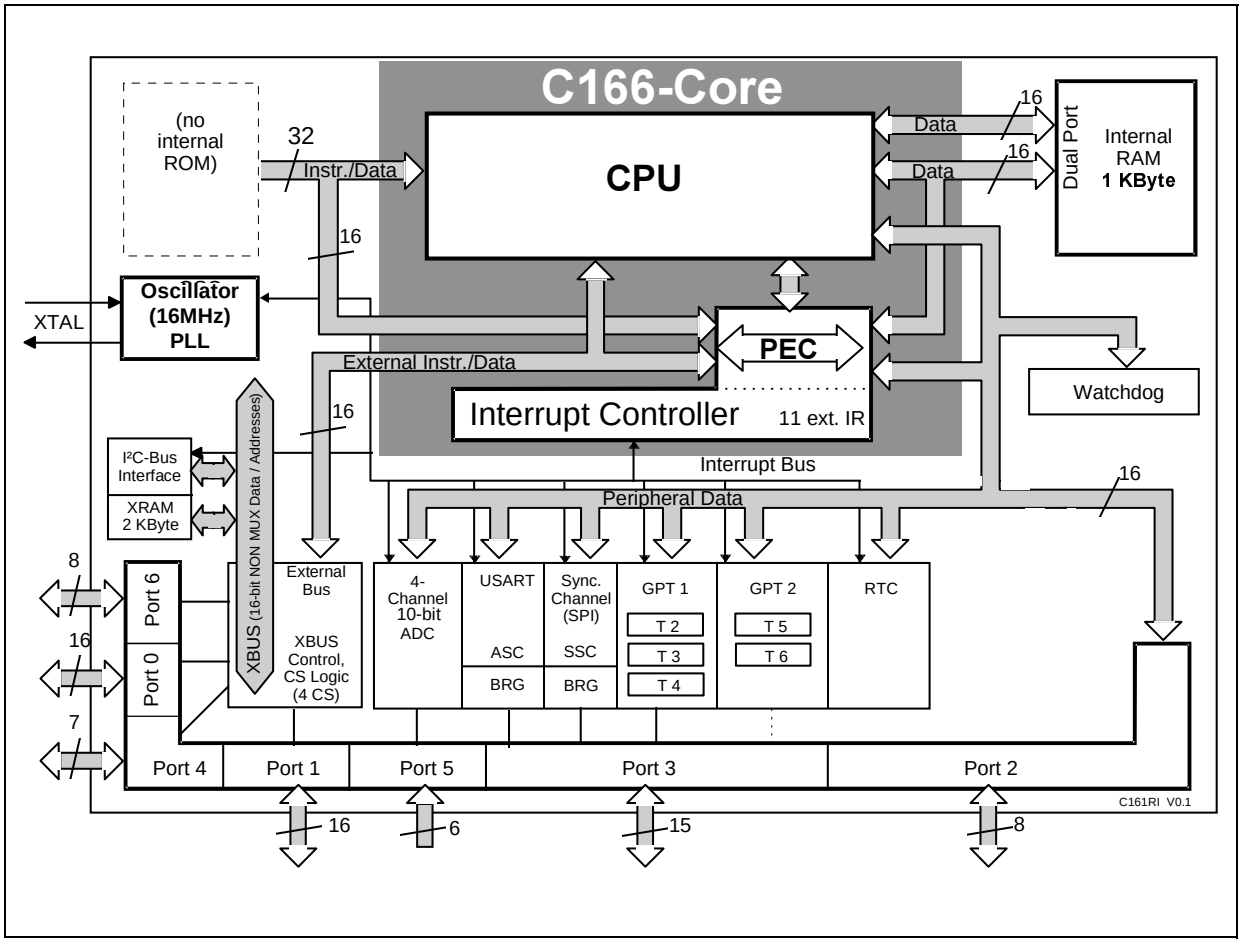


Figure 4 Block Diagram

Memory Organization

The memory space of the C161PI is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

1 KByte of on-chip Internal RAM (IRAM) is provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2 * 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

2 KBytes of on-chip Extension RAM (XRAM) are provided to store user data, user stacks, or code. The XRAM is accessed like external memory and therefore cannot be used for the system stack or for register banks and is not bitaddressable. The XRAM permits 16-bit accesses with maximum speed.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 8 MBytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

– 16-/18-/20-/23-bit Addresses, 16-bit Data, Demultiplexed
– 16-/18-/20-/23-bit Addresses, 16-bit Data, Multiplexed
– 16-/18-/20-/23-bit Addresses, 8-bit Data, Multiplexed
– 16-/18-/20-/23-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/ output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which allow to access different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.
Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C161PI offers the possibility to switch the $\overline{CS}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{CS}$ signals are directly generated from the address. The unlatched $\overline{CS}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories is supported via a particular ‘Ready’ function.

For applications which require less than 8 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte or to 64 KByte. In this case Port 4 outputs four, two or no address lines at all. It outputs all 7 address lines, if an address space of 8 MBytes is used.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C161PI's instructions can be executed in just one machine cycle which requires 2 CPU clocks (4 TCL). For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', reduces the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

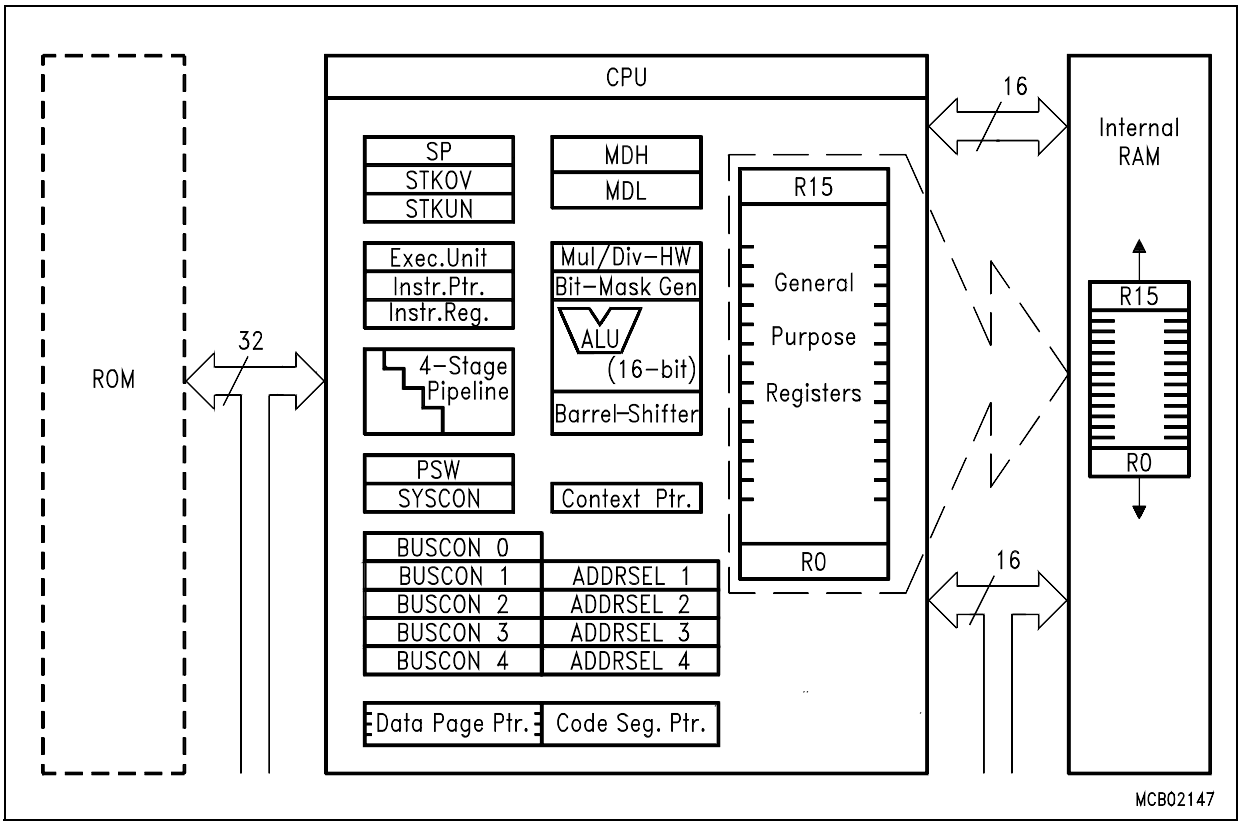


Figure 5 CPU Block Diagram

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C161PI instruction set which includes the following instruction classes:

– Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C161PI is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C161PI supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C161PI has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

The following table shows all of the possible C161PI interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 2 C161PI Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
External Interrupt 0	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
External Interrupt 1	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
External Interrupt 2	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
External Interrupt 3	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
External Interrupt 4	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
External Interrupt 5	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
External Interrupt 6	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
External Interrupt 7	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
GPT1 Timer 2	T2IR	T2IE	T2INT	$00'0088_H$	22_H
GPT1 Timer 3	T3IR	T3IE	T3INT	$00'008C_H$	23_H
GPT1 Timer 4	T4IR	T4IE	T4INT	$00'0090_H$	24_H
GPT2 Timer 5	T5IR	T5IE	T5INT	$00'0094_H$	25_H
GPT2 Timer 6	T6IR	T6IE	T6INT	$00'0098_H$	26_H
GPT2 CAPREL Register	CRIR	CRIE	CRINT	$00'009C_H$	27_H
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	$00'00A0_H$	28_H
A/D Overrun Error	ADEIR	ADEIE	ADEINT	$00'00A4_H$	29_H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	$00'00A8_H$	$2A_H$
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	$00'011C_H$	47_H
ASC0 Receive	S0RIR	S0RIE	S0RINT	$00'00AC_H$	$2B_H$
ASC0 Error	S0EIR	S0EIE	S0EINT	$00'00B0_H$	$2C_H$
SSC Transmit	SCTIR	SCTIE	SCTINT	$00'00B4_H$	$2D_H$
SSC Receive	SCRIR	SCRIE	SCRINT	$00'00B8_H$	$2E_H$
SSC Error	SCEIR	SCEIE	SCEINT	$00'00BC_H$	$2F_H$
I^2C Data Transfer Event	XP0IR	XP0IE	XP0INT	$00'0100_H$	40_H
I^2C Protocol Event	XP1IR	XP1IE	XP1INT	$00'0104_H$	41_H
X-Peripheral Node 2	XP2IR	XP2IE	XP2INT	$00'0108_H$	42_H
PLL Unlock / RTC	XP3IR	XP3IE	XP3INT	$00'010C_H$	43_H

The C161PI also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

Table 3 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Prio
Reset Functions:					
Hardware Reset		RESET	$00'0000_H$	00_H	III
Software Reset		RESET	$00'0000_H$	00_H	III
Watchdog Timer Overflow		RESET	$00'0000_H$	00_H	III
Class A Hardware Traps:					
Non-Maskable Interrupt	NMI	NMITRAP	$00'0008_H$	02_H	II
Stack Overflow	STKOF	STOTRAP	$00'0010_H$	04_H	II
Stack Underflow	STKUF	STUTRAP	$00'0018_H$	06_H	II
Class B Hardware Traps:					
Undefined Opcode	UNDOPC	BTRAP	$00'0028_H$	$0A_H$	I
Protected Instruction Fault	PRTFLT	BTRAP	$00'0028_H$	$0A_H$	I
Illegal Word Operand Access	ILLOPA	BTRAP	$00'0028_H$	$0A_H$	I
Illegal Instruction Access	ILLINA	BTRAP	$00'0028_H$	$0A_H$	I
Illegal External Bus Access	ILLBUS	BTRAP	$00'0028_H$	$0A_H$	I
Reserved			$[2C_H – 3C_H]$	$[0B_H – 0F_H]$	
Software Traps: TRAP Instruction			Any $[00'0000_H – 00'01FC_H]$ in steps of 4_H	Any $[00_H – 7F_H]$	Current CPU Priority

General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate eg. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer over-flow/underflow. The state of this latch may be output on a port pin (T3OUT) eg. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 are captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

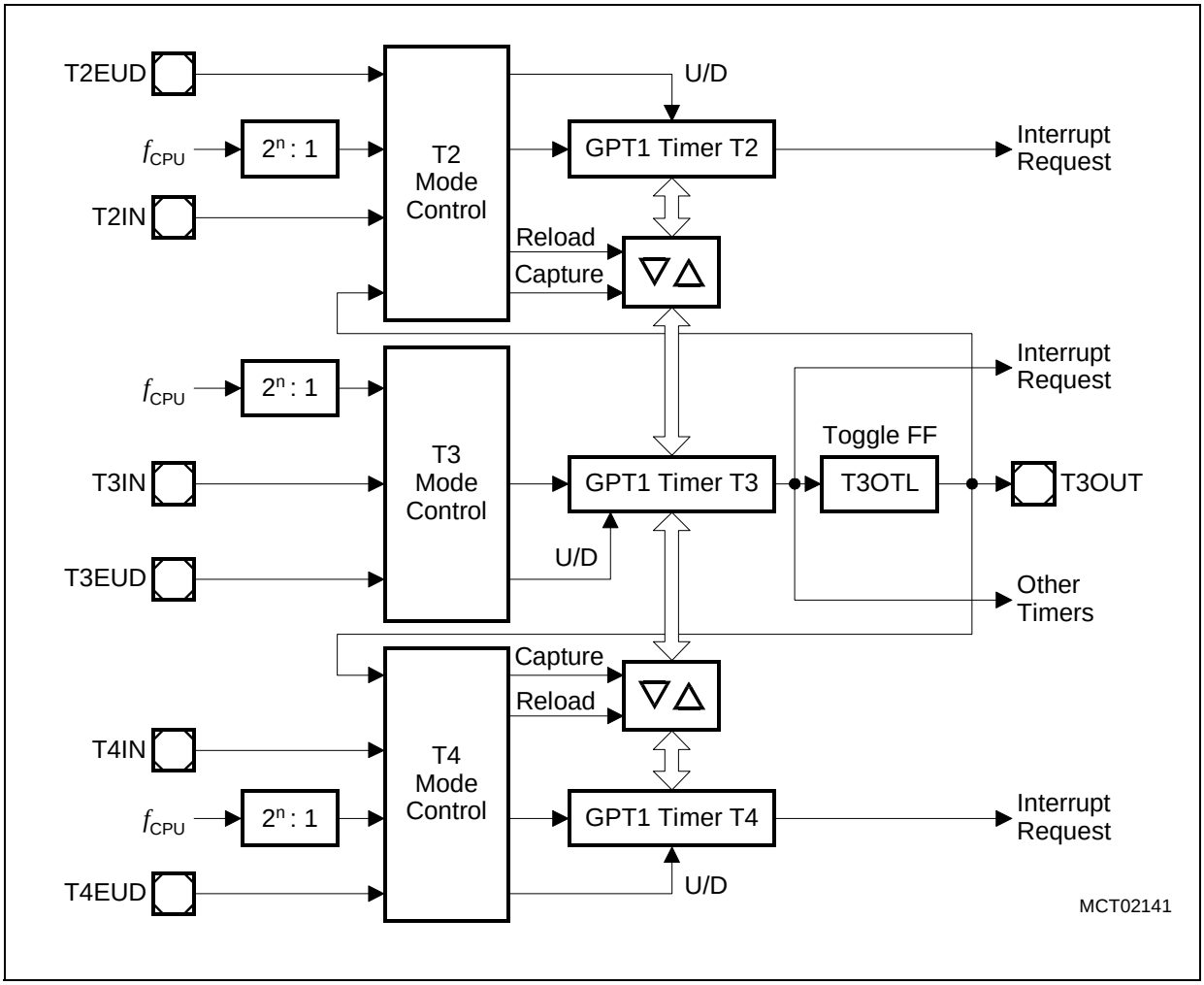


Figure 6 Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler. The count direction (up/down) for each timer is programmable by software. Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/ underflow.

The state of this latch may be used to clock timer T5. The overflows/underflows of timer T6 can additionally be used to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

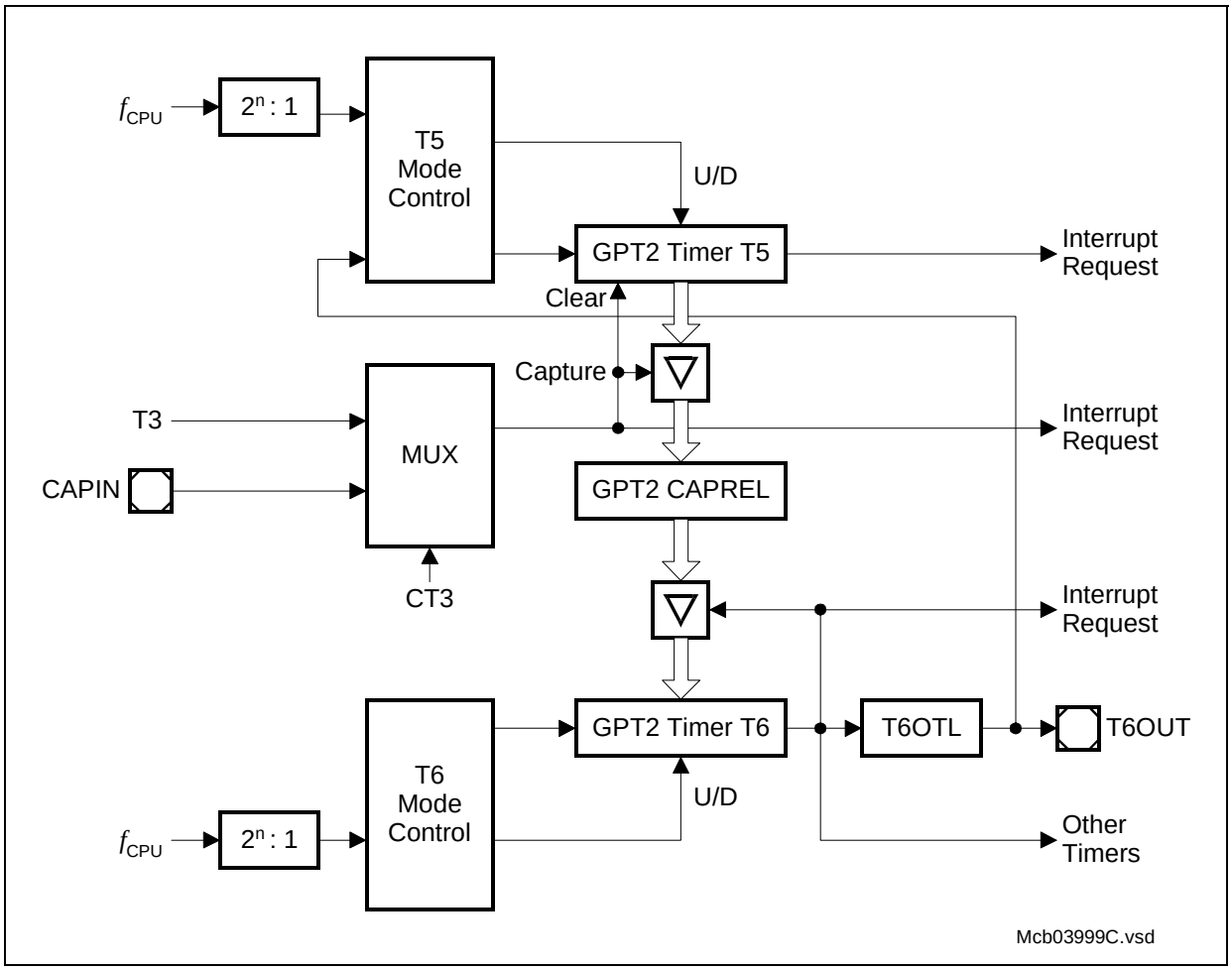


Figure 7 Block Diagram of GPT2

Real Time Clock

The Real Time Clock (RTC) module of the C161PI consists of a chain of 3 divider blocks, a fixed 8:1 divider, the reloadable 16-bit timer T14, and the 32-bit RTC timer (accessible via registers RTCH and RTCL). The RTC module is directly clocked with the on-chip oscillator frequency divided by 32 via a separate clock driver ($f_{RTC} = f_{OSC} / 32$) and is therefore independent from the selected clock generation mode of the C161PI. All timers count up.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time based interrupt
- 48-bit timer for long term measurements

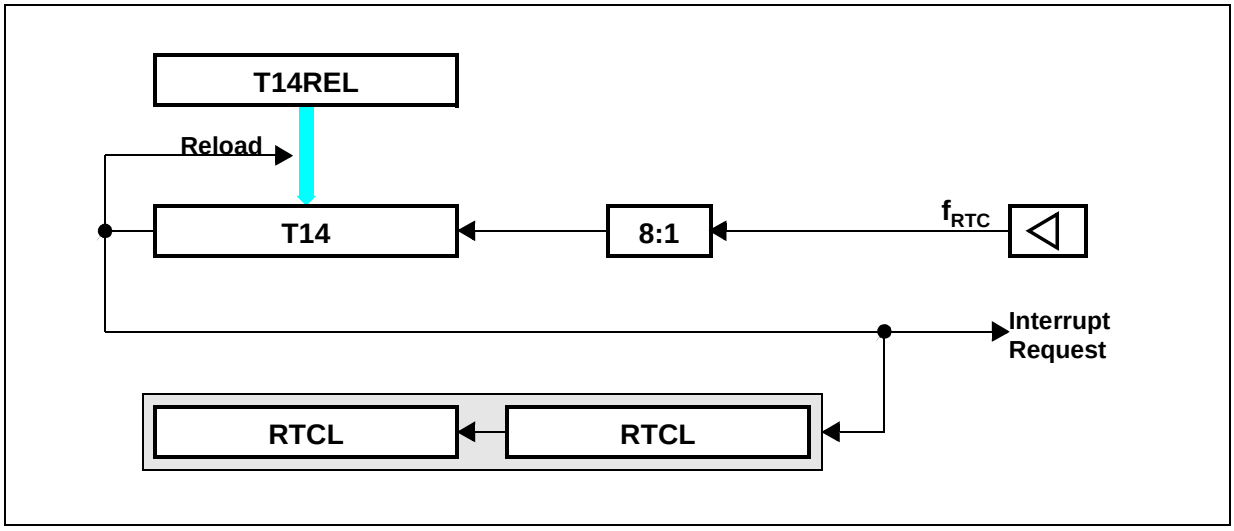


Figure 8 RTC Block Diagram

Note: The registers associated with the RTC are not effected by a reset in order to maintain the correct system time even when intermediate resets are executed.

A/D Converter

For analog signal measurement, a 10-bit A/D converter with 4 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 4 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C161PI supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via registers P5DIDIS (Port 5 Digital Input Disable).

Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (**ASC0**) and a High-Speed Synchronous Serial Channel (**SSC**).

The ASC0 is upward compatible with the serial ports of the Infineon 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 780 KBaud and half-duplex synchronous communication at up to 3.1 MBaud @ 25 MHz CPU clock.
A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake up bit mode).
In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The SSC supports full-duplex synchronous communication at up to 6.25 Mbaud @ 25 MHz CPU clock. It may be configured so it interfaces with serially linked peripheral components. A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 3 separate interrupt vectors are provided.
The SSC transmits or receives characters of 2...16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit and receive error supervise the correct handling of the data buffer. Phase and baudrate error detect incorrect serial data.

I²C Module

The integrated I²C Bus Module handles the transmission and reception of frames over the two-line I²C bus in accordance with the I²C Bus specification. The on-chip I²C Module can receive and transmit data using 7-bit or 10-bit addressing and it can operate in slave mode, in master mode or in multi-master mode.

Several physical interfaces (port pins) can be established under software control. Data can be transferred at speeds up to 400 Kbit/sec.

Two interrupt nodes dedicated to the I²C module allow efficient interrupt service and also support operation via PEC transfers.

Note: The port pins associated with the I²C interfaces feature open drain drivers only, as required by the I²C specification.

Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 20 µs and 336 ms can be monitored (@ 25 MHz).
The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

Parallel Ports

The C161PI provides up to 76 IO lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three IO ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. The other IO ports operate in push/pull mode, except for the I²C interface pins which are open drain pins only. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A22/19/17...A16 in systems where segmentation is enabled to access more than 64 KBytes of memory.

Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$ and the system clock output CLKOUT (or the programmable frequency output FOUT).
Port 5 is used for the analog input channels to the A/D converter or timer control signals.

Port 6 provides the optional chip select signals and interface lines for the I²C module.

The edge characteristics (transition time) of the C161PI's port drivers can be selected via the Port Driver Control Register (PDCR).

Instruction Set Summary

The table below lists the instructions of the C161PI in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“C166 Family Instruction Set Manual”**.

This document also provides a detailled description of each instruction.

Table 4 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

Table 4 Instruction Set Summary (continued)

Mnemonic	Description	Bytes
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand. with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack und update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on RSTOUT-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

Special Function Registers Overview

The following table lists all SFRs which are implemented in the C161PI in alphabetical order.
Bit-addressable SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers within on-chip X-Peripherals (I²C) are marked with the letter "**X**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Table 5 C161PI Registers, Ordered by Name

Name	Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC b	$FF98_H$	CC_H	A/D Converter End of Conversion Interrupt Control Register	0000_H
ADCON b	$FFA0_H$	$D0_H$	A/D Converter Control Register	0000_H
ADDAT	$FEA0_H$	50_H	A/D Converter Result Register	0000_H
ADDAT2	$F0A0_H$ **E**	50_H	A/D Converter 2 Result Register	0000_H
ADDRSEL1	$FE18_H$	$0C_H$	Address Select Register 1	0000_H
ADDRSEL2	$FE1A_H$	$0D_H$	Address Select Register 2	0000_H
ADDRSEL3	$FE1C_H$	$0E_H$	Address Select Register 3	0000_H
ADDRSEL4	$FE1E_H$	$0F_H$	Address Select Register 4	0000_H
ADEIC b	$FF9A_H$	CD_H	A/D Converter Overrun Error Interrupt Control Register	0000_H
BUSCON0 b	$FF0C_H$	86_H	Bus Configuration Register 0	0000_H
BUSCON1 b	$FF14_H$	$8A_H$	Bus Configuration Register 1	0000_H
BUSCON2 b	$FF16_H$	$8B_H$	Bus Configuration Register 2	0000_H
BUSCON3 b	$FF18_H$	$8C_H$	Bus Configuration Register 3	0000_H
BUSCON4 b	$FF1A_H$	$8D_H$	Bus Configuration Register 4	0000_H
CAPREL	$FE4A_H$	25_H	GPT2 Capture/Reload Register	0000_H
CC8IC b	$FF88_H$	$C4_H$	External Interrupt 0 Control Register	0000_H
CC9IC b	$FF8A_H$	$C5_H$	External Interrupt 1 Control Register	0000_H
CC10IC b	$FF8C_H$	$C6_H$	External Interrupt 2 Control Register	0000_H
CC11IC b	$FF8E_H$	$C7_H$	External Interrupt 3 Control Register	0000_H

Table 5 C161PI Registers, Ordered by Name (continued)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
CC12IC	**b**	$FF90_H$		$C8_H$	External Interrupt 4 Control Register	0000_H
CC13IC	**b**	$FF92_H$		$C9_H$	External Interrupt 5 Control Register	0000_H
CC14IC	**b**	$FF94_H$		CA_H	External Interrupt 6 Control Register	0000_H
CC15IC	**b**	$FF96_H$		CB_H	External Interrupt 7 Control Register	0000_H
CP		$FE10_H$		08_H	CPU Context Pointer Register	$FC00_H$
CRIC	**b**	$FF6A_H$		$B5_H$	GPT2 CAPREL Interrupt Ctrl. Register	0000_H
CSP		$FE08_H$		04_H	CPU Code Segment Pointer Register (8 bits, not directly writeable)	0000_H
DP0L	**b**	$F100_H$	**E**	80_H	P0L Direction Control Register	00_H
DP0H	**b**	$F102_H$	**E**	81_H	P0H Direction Control Register	00_H
DP1L	**b**	$F104_H$	**E**	82_H	P1L Direction Control Register	00_H
DP1H	**b**	$F106_H$	**E**	83_H	P1H Direction Control Register	00_H
DP2	**b**	$FFC2_H$		$E1_H$	Port 2 Direction Control Register	0000_H
DP3	**b**	$FFC6_H$		$E3_H$	Port 3 Direction Control Register	0000_H
DP4	**b**	$FFCA_H$		$E5_H$	Port 4 Direction Control Register	00_H
DP6	**b**	$FFCE_H$		$E7_H$	Port 6 Direction Control Register	00_H
DPP0		$FE00_H$		00_H	CPU Data Page Pointer 0 Register (10 bits)	0000_H
DPP1		$FE02_H$		01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2		$FE04_H$		02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3		$FE06_H$		03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON	**b**	$F1C0_H$	**E**	$E0_H$	External Interrupt Control Register	0000_H
ICADR		$ED06_H$	**X**	---	I²C Address Register	$0XXX_H$
ICCFG		$ED00_H$	**X**	---	I²C Configuration Register	$XX00_H$
ICCON		$ED02_H$	**X**	---	I²C Control Register	0000_H
ICRTB		$ED08_H$	**X**	---	I²C Receive/Transmit Buffer	XX_H
ICST		$ED04_H$	**X**	---	I²C Status Register	0000_H
IDCHIP		$F07C_H$	**E**	$3E_H$	Identifier	$09XX_H$
IDMANUF		$F07E_H$	**E**	$3F_H$	Identifier	1820_H
IDMEM		$F07A_H$	**E**	$3D_H$	Identifier	0000_H

Table 5 C161PI Registers, Ordered by Name (continued)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
IDPROG		$F078_H$	**E**	$3C_H$	Identifier	0000_H
ISNC	**b**	$F1DE_H$	**E**	EF_H	Interrupt Subnode Control Register	0000_H
MDC	**b**	$FF0E_H$		87_H	CPU Multiply Divide Control Register	0000_H
MDH		$FE0C_H$		06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL		$FE0E_H$		07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2	**b**	$F1C2_H$	**E**	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3	**b**	$F1C6_H$	**E**	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP6	**b**	$F1CE_H$	**E**	$E7_H$	Port 6 Open Drain Control Register	00_H
ONES	**b**	$FF1E_H$		$8F_H$	Constant Value 1’s Register (read only)	$FFFF_H$
P0L	**b**	$FF00_H$		80_H	Port 0 Low Reg. (Lower half of PORT0)	00_H
P0H	**b**	$FF02_H$		81_H	Port 0 High Reg. (Upper half of PORT0)	00_H
P1L	**b**	$FF04_H$		82_H	Port 1 Low Reg. (Lower half of PORT1)	00_H
P1H	**b**	$FF06_H$		83_H	Port 1 High Reg. (Upper half of PORT1)	00_H
P2	**b**	$FFC0_H$		$E0_H$	Port 2 Register	0000_H
P3	**b**	$FFC4_H$		$E2_H$	Port 3 Register	0000_H
P4	**b**	$FFC8_H$		$E4_H$	Port 4 Register (7 bits)	00_H
P5	**b**	$FFA2_H$		$D1_H$	Port 5 Register (read only)	$XXXX_H$
P5DIDIS	**b**	$FFA4_H$		$D2_H$	Port 5 Digital Input Disable Register	0000_H
P6	**b**	$FFCC_H$		$E6_H$	Port 6 Register (8 bits)	00_H
PECC0		$FEC0_H$		60_H	PEC Channel 0 Control Register	0000_H
PECC1		$FEC2_H$		61_H	PEC Channel 1 Control Register	0000_H
PECC2		$FEC4_H$		62_H	PEC Channel 2 Control Register	0000_H
PECC3		$FEC6_H$		63_H	PEC Channel 3 Control Register	0000_H
PECC4		$FEC8_H$		64_H	PEC Channel 4 Control Register	0000_H
PECC5		$FECA_H$		65_H	PEC Channel 5 Control Register	0000_H
PECC6		$FECC_H$		66_H	PEC Channel 6 Control Register	0000_H
PECC7		$FECE_H$		67_H	PEC Channel 7 Control Register	0000_H
PSW	**b**	$FF10_H$		88_H	CPU Program Status Word	0000_H
PDCR		$F0AA_H$	**E**	55_H	Pin Driver Control Register	0000_H
RP0H	**b**	$F108_H$	**E**	84_H	System Startup Config. Reg. (Rd. only)	XX_H

Table 5 C161PI Registers, Ordered by Name (continued)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
RTCH	F0D6$_H$ **E**	6B$_H$	RTC High Register	no
RTCL	F0D4$_H$ **E**	6A$_H$	RTC Low Register	no
S0BG	FEB4$_H$	5A$_H$	Serial Channel 0 Baud Rate Generator Reload Register	0000$_H$
S0CON b	FFB0$_H$	D8$_H$	Serial Channel 0 Control Register	0000$_H$
S0EIC b	FF70$_H$	B8$_H$	Serial Channel 0 Error Interrupt Control Register	0000$_H$
S0RBUF	FEB2$_H$	59$_H$	Serial Channel 0 Receive Buffer Reg. (read only)	XXXX$_H$
S0RIC b	FF6E$_H$	B7$_H$	Serial Channel 0 Receive Interrupt Control Register	0000$_H$
S0TBIC b	F19C$_H$ **E**	CE$_H$	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000$_H$
S0TBUF	FEB0$_H$	58$_H$	Serial Channel 0 Transmit Buffer Reg. (write only)	0000$_H$
S0TIC b	FF6C$_H$	B6$_H$	Serial Channel 0 Transmit Interrupt Control Register	0000$_H$
SP	FE12$_H$	09$_H$	CPU System Stack Pointer Register	FC00$_H$
SSCBR	F0B4$_H$ **E**	5A$_H$	SSC Baudrate Register	0000$_H$
SSCCON b	FFB2$_H$	D9$_H$	SSC Control Register	0000$_H$
SSCEIC b	FF76$_H$	BB$_H$	SSC Error Interrupt Control Register	0000$_H$
SSCRB	F0B2$_H$ **E**	59$_H$	SSC Receive Buffer	XXXX$_H$
SSCRIC b	FF74$_H$	BA$_H$	SSC Receive Interrupt Control Register	0000$_H$
SSCTB	F0B0$_H$ **E**	58$_H$	SSC Transmit Buffer	0000$_H$
SSCTIC b	FF72$_H$	B9$_H$	SSC Transmit Interrupt Control Register	0000$_H$
STKOV	FE14$_H$	0A$_H$	CPU Stack Overflow Pointer Register	FA00$_H$
STKUN	FE16$_H$	0B$_H$	CPU Stack Underflow Pointer Register	FC00$_H$
SYSCON b	FF12$_H$	89$_H$	CPU System Configuration Register	[1] 0xx0$_H$
SYSCON2 b	F1D0$_H$ **E**	E8$_H$	CPU System Configuration Register 2	0000$_H$
SYSCON3 b	F1D4$_H$ **E**	EA$_H$	CPU System Configuration Register 3	0000$_H$
T14	F0D2$_H$ **E**	69$_H$	RTC Timer 14 Register	no

Table 5 C161PI Registers, Ordered by Name (continued)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
T14REL	F0D0$_H$ **E**	68$_H$	RTC Timer 14 Reload Register	no
T2	FE40$_H$	20$_H$	GPT1 Timer 2 Register	0000$_H$
T2CON b	FF40$_H$	A0$_H$	GPT1 Timer 2 Control Register	0000$_H$
T2IC b	FF60$_H$	B0$_H$	GPT1 Timer 2 Interrupt Control Register	0000$_H$
T3	FE42$_H$	21$_H$	GPT1 Timer 3 Register	0000$_H$
T3CON b	FF42$_H$	A1$_H$	GPT1 Timer 3 Control Register	0000$_H$
T3IC b	FF62$_H$	B1$_H$	GPT1 Timer 3 Interrupt Control Register	0000$_H$
T4	FE44$_H$	22$_H$	GPT1 Timer 4 Register	0000$_H$
T4CON b	FF44$_H$	A2$_H$	GPT1 Timer 4 Control Register	0000$_H$
T4IC b	FF64$_H$	B2$_H$	GPT1 Timer 4 Interrupt Control Register	0000$_H$
T5	FE46$_H$	23$_H$	GPT2 Timer 5 Register	0000$_H$
T5CON b	FF46$_H$	A3$_H$	GPT2 Timer 5 Control Register	0000$_H$
T5IC b	FF66$_H$	B3$_H$	GPT2 Timer 5 Interrupt Control Register	0000$_H$
T6	FE48$_H$	24$_H$	GPT2 Timer 6 Register	0000$_H$
T6CON b	FF48$_H$	A4$_H$	GPT2 Timer 6 Control Register	0000$_H$
T6IC b	FF68$_H$	B4$_H$	GPT2 Timer 6 Interrupt Control Register	0000$_H$
TFR b	FFAC$_H$	D6$_H$	Trap Flag Register	0000$_H$
WDT	FEAE$_H$	57$_H$	Watchdog Timer Register (read only)	0000$_H$
WDTCON	FFAE$_H$	D7$_H$	Watchdog Timer Control Register	[2] 00xx$_H$
XP0IC b	F186$_H$ **E**	C3$_H$	I²C Data Interrupt Control Register	0000$_H$
XP1IC b	F18E$_H$ **E**	C7$_H$	I²C Protocol Interrupt Control Register	0000$_H$
XP2IC b	F196$_H$ **E**	CB$_H$	X-Peripheral 2 Interrupt Control Register	0000$_H$
XP3IC b	F19E$_H$ **E**	CF$_H$	RTC Interrupt Control Register	0000$_H$
ZEROS b	FF1C$_H$	8E$_H$	Constant Value 0's Register (read only)	0000$_H$

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

Absolute Maximum Ratings

Table 6 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD}+0.5	V	
Input current on any pin during overload condition		-10	10	mA	
Absolute sum of all input currents during overload condition		-	|100|	mA	
Power dissipation	P_{DISS}	-	1.5	W	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions (V_{IN}>V_{DD} or V_{IN}<V_{SS}) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C161PI. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 7 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Standard digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, f_{CPUmax} = 25 MHz
		2.5 [1]	5.5	V	PowerDown mode
Reduced digital supply voltage	V_{DD}	3.0	3.6	V	Active mode, f_{CPUmax} = 20 MHz
		2.5 [1]	3.6	V	PowerDown mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-	±5	mA	Per pin [2] [3]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	-	50	mA	[3]
External Load Capacitance	C_L	-	100	pF	Pin drivers in **fast edge** mode (PDCR.BIPEC = '0')
		-	50	pF	Pin drivers in **reduced edge** mode (PDCR.BIPEC = '1') [3]
Ambient temperature	T_A	0	70	°C	SAB-C161PI...
		-40	85	°C	SAF-C161PI...
		-40	125	°C	SAK-C161PI...

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operatings conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$+0.5V or $V_{OV} < V_{SS}$-0.5V). The absolute sum of input overload currents on all port pins may not exceed **50 mA**. The supply voltage must remain within the specified limits.

3) Not 100% tested, guaranteed by design characterization.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C161PI and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C161PI will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C161PI.

DC Characteristics (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage XTAL1, P3.0, P3.1, P6.5, P6.6, P6.7	V_{IL1} SR	– 0.5	0.3 V_{DD}	V	–
Input low voltage (TTL)	V_{IL} SR	– 0.5	0.2 V_{DD} – 0.1	V	–
Input low voltage (Special Threshold)	V_{ILS} SR	– 0.5	2.0	V	–
Input high voltage $\overline{\text{RSTIN}}$	V_{IH1} SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1, P3.0, P3.1, P6.5, P6.6, P6.7	V_{IH2} SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage (TTL)	V_{IH} SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS} SR	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V	–
Input Hysteresis (Special Threshold)	HYS	400	–	mV	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT, $\overline{\text{RSTOUT}}$)	V_{OL} CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (P3.0, P3.1, P6.5, P6.6, P6.7)	V_{OL2} CC	–	0.4	V	I_{OL2} = 3 mA

DC Characteristics (Standard Supply Voltage Range) (continued)
(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Output low voltage (all other outputs)	V_{OL1} CC	–	0.45	V	I_{OL} = 1.6 mA
Output high voltage [1] (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH} CC	2.4	–	V	I_{OH} = -2.4 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Output high voltage [1] (all other outputs)	V_{OH1} CC	2.4	–	V	I_{OH} = -1.6 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Input leakage current (Port 5)	I_{OZ1} CC	–	±200	nA	0.45V < V_{IN} < V_{DD}
Input leakage current (all other)	I_{OZ2} CC	–	±500	nA	0.45V < V_{IN} < V_{DD}
$\overline{RSTIN}$ inactive current [2]	I_{RSTH} [3]	–	-10	µA	V_{IN} = V_{IH1}
$\overline{RSTIN}$ active current [2]	I_{RSTL} [4]	-100	–	µA	V_{IN} = V_{IL}
Read/Write inactive current [5]	I_{RWH} [3]	–	-40	µA	V_{OUT} = 2.4 V
Read/Write active current [5]	I_{RWL} [4]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current [5]	I_{ALEL} [3]	–	40	µA	V_{OUT} = V_{OLmax}
ALE active current [5]	I_{ALEH} [4]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current [5]	I_{P6H} [3]	–	-40	µA	V_{OUT} = 2.4 V
Port 6 active current [5]	I_{P6L} [4]	-500	–	µA	V_{OUT} = V_{OL1max}
PORT0 configuration current [5]	I_{P0H} [3]	–	-10	µA	V_{IN} = V_{IHmin}
	I_{P0L} [4]	-100	–	µA	V_{IN} = V_{ILmax}
XTAL1 input current	I_{IL} CC	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance [6] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current (5V active) with all peripherals active	I_{DD5}	–	1 + 2*f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL2} f_{CPU} in [MHz] [7]
Idle mode supply current (5V) with all peripherals active	I_{IDX5}	–	1 + 0.8*f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [7]
Idle mode supply current (5V) with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO5} [8]	–	500 + 50*f_{OSC}	µA	$\overline{RSTIN}$ = V_{IH1} f_{OSC} in [MHz] [7]

DC Characteristics (Standard Supply Voltage Range) (continued)
(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power-down mode supply current (5V) with RTC running	I_{PDR5} 8)	–	200 + 25*f_{OSC}	µA	$V_{DD} = V_{DDmax}$ f_{OSC} in [MHz] 9)
Power-down mode supply current (5V) with RTC disabled	I_{PDO5}	–	50	µA	$V_{DD} = V_{DDmax}$ 9)

1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

2) These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 KΩ.

3) The maximum current may be drawn while the respective signal line remains inactive.

4) The minimum current must be drawn in order to drive the respective signal line active.

5) This specification is only valid during Reset, or during Hold- or Adapt-mode. During Hold mode Port 6 pins are only affected, if they are used (configured) for $\overline{\text{CS}}$ output and the open drain function is not enabled.

6) Not 100% tested, guaranteed by design characterization.

7) The supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.
The oscillator also contributes to the total supply current. The given values refer to the worst case, ie. I_{PDRmax}. For lower oscillator frequencies the respective supply current can be reduced accordingly.

8) This parameter is determined mainly by the current consumed by the oscillator. This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

9) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

DC Characteristics (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage XTAL1, P3.0, P3.1, P6.5, P6.6, P6.7	V_{IL1} SR	– 0.5	0.3 V_{DD}	V	–
Input low voltage (TTL)	V_{IL} SR	– 0.5	0.8	V	–
Input low voltage (Special Threshold)	V_{ILS} SR	– 0.5	1.3	V	–
Input high voltage $\overline{\text{RSTIN}}$	V_{IH1} SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1, P3.0, P3.1, P6.5, P6.6, P6.7	V_{IH2} SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage (TTL)	V_{IH} SR	1.8	V_{DD} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS} SR	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V	–
Input Hysteresis (Special Threshold)	HYS	250	–	mV	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, BHE, CLKOUT, $\overline{\text{RSTOUT}}$)	V_{OL} CC	–	0.45	V	I_{OL} = 1.6 mA
Output low voltage P3.0, P3.1, P6.5, P6.6, P6.7	V_{OL2} CC	–	0.4	V	I_{OL2} = 1.6 mA
Output low voltage (all other outputs)	V_{OL1} CC	–	0.45	V	I_{OL} = 1.0 mA
Output high voltage [1] (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, BHE, CLKOUT, $\overline{\text{RSTOUT}}$)	V_{OH} CC	0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Output high voltage [1] (all other outputs)	V_{OH1} CC	0.9 V_{DD}	–	V	I_{OH} = -0.25 mA
Input leakage current (Port 5)	I_{OZ1} CC	–	±200	nA	0.45V < V_{IN} < V_{DD}
Input leakage current (all other)	I_{OZ2} CC	–	±500	nA	0.45V < V_{IN} < V_{DD}
$\overline{\text{RSTIN}}$ inactive current [2]	I_{RSTH} [3]	–	-10	µA	V_{IN} = V_{IH1}

DC Characteristics (continued) **(Reduced Supply Voltage Range)**
(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
$\overline{\text{RSTIN}}$ active current [2]	I_{RSTL} [4]	-100	–	µA	$V_{IN} = V_{IL}$
Read/Write inactive current [5]	I_{RWH} [3]	–	-10	µA	V_{OUT} = 2.4 V
Read/Write active current [5]	I_{RWL} [4]	-500	–	µA	$V_{OUT} = V_{OLmax}$
ALE inactive current [5]	I_{ALEL} [3]	–	20	µA	$V_{OUT} = V_{OLmax}$
ALE active current [5]	I_{ALEH} [4]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current [5]	I_{P6H} [3]	–	-10	µA	V_{OUT} = 2.4 V
Port 6 active current [5]	I_{P6L} [4]	-500	–	µA	$V_{OUT} = V_{OL1max}$
PORT0 configuration current [5]	I_{P0H} [3]	–	-5	µA	$V_{IN} = V_{IHmin}$
	I_{P0L} [4]	-100	–	µA	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance [6] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current (3V active) with all peripherals active	I_{DD3}	–	1 + 1.1*f_{CPU}	mA	$\overline{\text{RSTIN}} = V_{IL2}$ f_{CPU} in [MHz] [7]
Idle mode supply current (3V) with all peripherals active	I_{IDX3}	–	1 + 0.5*f_{CPU}	mA	$\overline{\text{RSTIN}} = V_{IH1}$ f_{CPU} in [MHz] [7]
Idle mode supply current (3V) with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO3} [8]	–	300 + 30*f_{OSC}	µA	$\overline{\text{RSTIN}} = V_{IH1}$ f_{OSC} in [MHz] [7]
Power-down mode supply current (3V) with RTC running	I_{PDR3} [8]	–	100 + 10*f_{OSC}	µA	$V_{DD} = V_{DDmax}$ f_{OSC} in [MHz] [9]
Power-down mode supply current (3V) with RTC disabled	I_{PDO3}	–	30	µA	$V_{DD} = V_{DDmax}$ [9]

1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

2) These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 KΩ.

3) The maximum current may be drawn while the respective signal line remains inactive.

4) The minimum current must be drawn in order to drive the respective signal line active.

5) This specification is only valid during Reset, or during Hold- or Adapt-mode. During Hold mode Port 6 pins are only affected, if they are used (configured) for $\overline{\text{CS}}$ output and the open drain function is not enabled.

6) Not 100% tested, guaranteed by design characterization.

7) The supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.
The oscillator also contributes to the total supply current. The given values refer to the worst case, ie. I_{PDRmax}. For lower oscillator frequencies the respective supply current can be reduced accordingly.

8) This parameter is determined mainly by the current consumed by the oscillator. This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

9) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

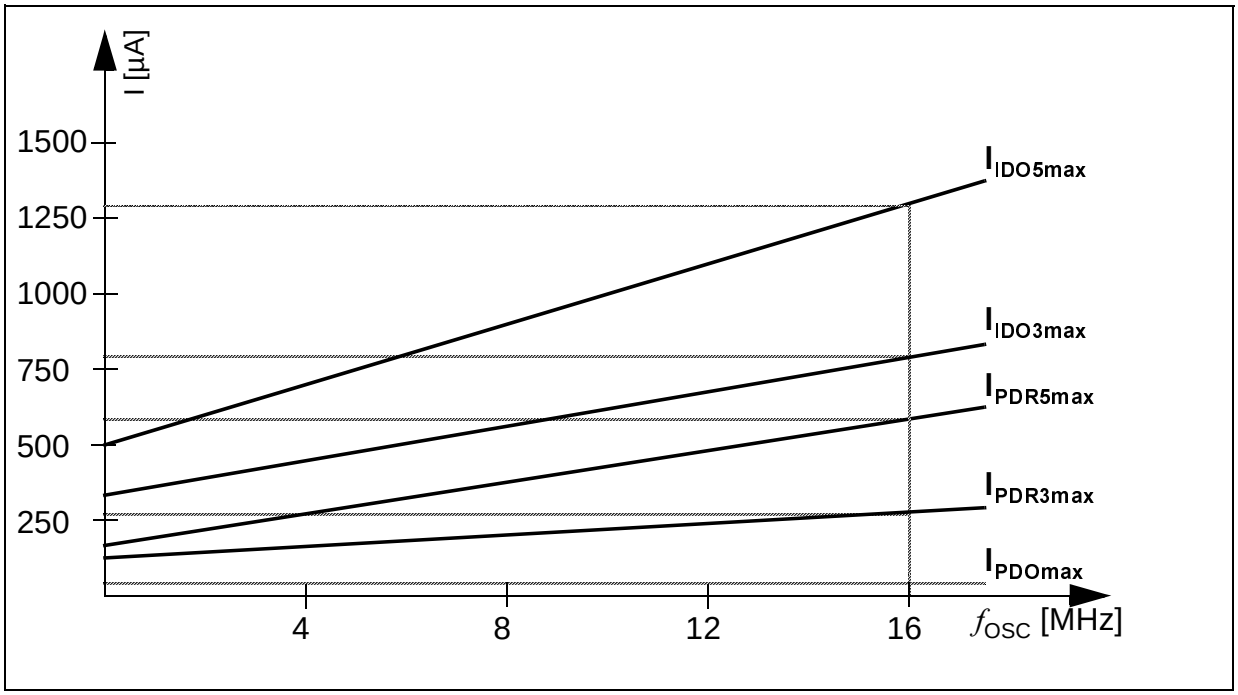


Figure 9 Idle and Power Down Supply Current as a Function of Oscillator Frequency

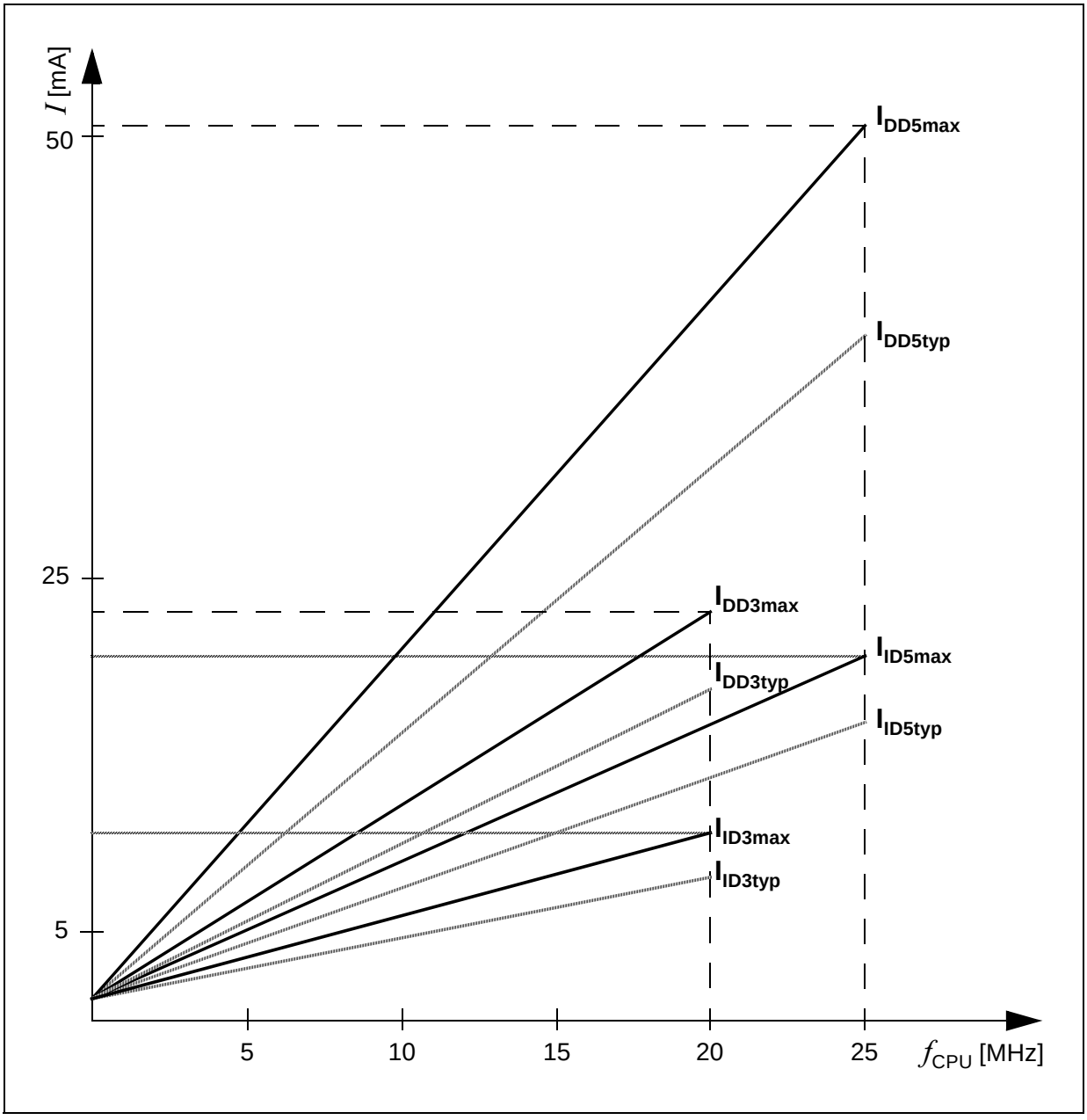


Figure 10 Supply/Idle Current as a Function of Operating Frequency

AC Characteristics
Definition of Internal Timing

The internal operation of the C161PI is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see figure below).

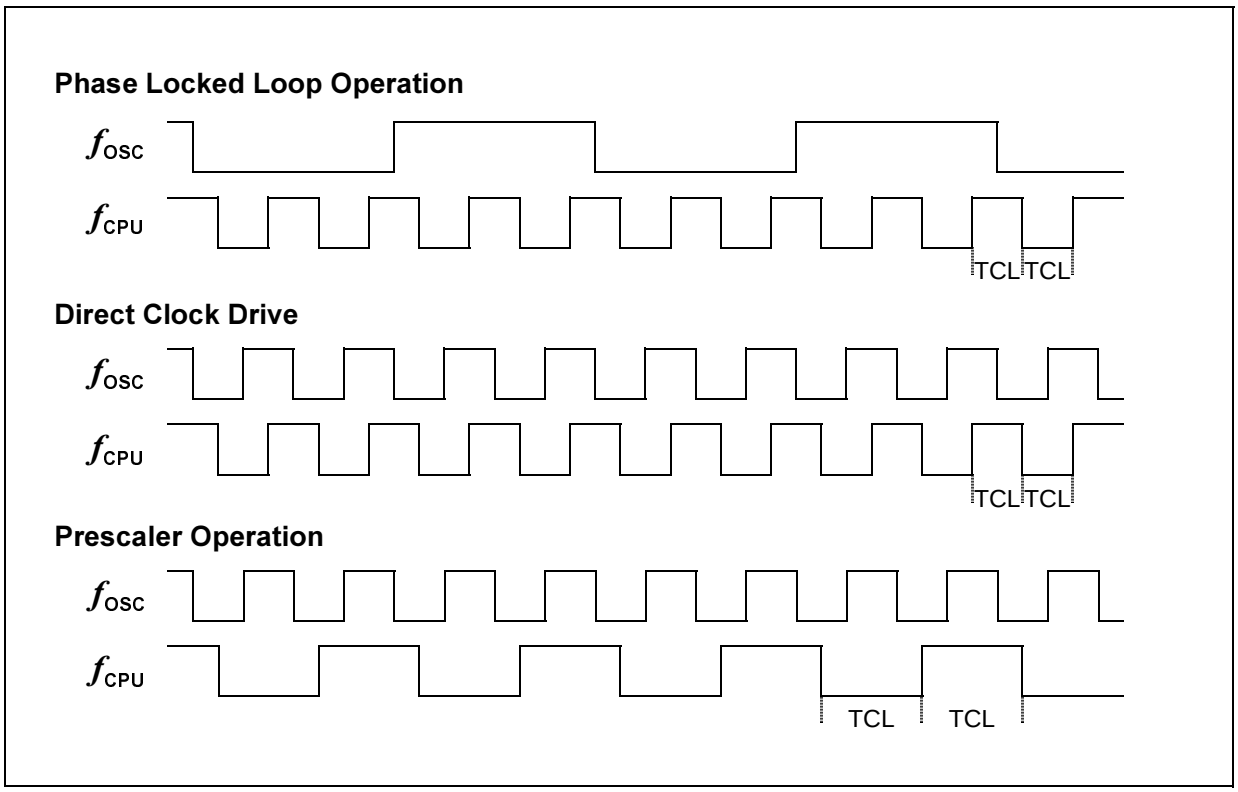


Figure 11 Generation Mechanisms for the CPU Clock

The CPU clock signal f_{CPU} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU}. This influence must be regarded when calculating the timings for the C161PI.

Note: The example for PLL operation shown in the fig. above refers to a PLL factor of 4.

The used mechanism to generate the CPU clock is selected during reset via the logic levels on pins P0.15-13 (P0H.7-5).

The table below associates the combinations of these three bits with the respective clock generation mode.

Table 8 C161PI Clock Generation Modes

P0.15-13 (P0H.7-5)	CPU Frequency $f_{CPU} = f_{OSC} * F$	External Clock Input Range [1]	Notes
1 1 1	$f_{OSC} * 4$	2.5 to 6.25 MHz	Default configuration
1 1 0	$f_{OSC} * 3$	3.33 to 8.33 MHz	
1 0 1	$f_{OSC} * 2$	5 to 12.5 MHz	
1 0 0	$f_{OSC} * 5$	2 to 5 MHz	
0 1 1	$f_{OSC} * 1$	1 to 25 MHz	Direct drive [2]
0 1 0	$f_{OSC} * 1.5$	6.66 to 16.6 MHz	
0 0 1	$f_{OSC} / 2$	2 to 50 MHz	CPU clock via prescaler
0 0 0	$f_{OSC} * 2.5$	4 to 10 MHz	

1) The external clock input range refers to a CPU clock range of 10...25 MHz.

2) The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When pins P0.15-13 (P0H.7-5) equal 001_B during reset the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

For all combinations of pins P0.15-13 (P0H.7-5) except for 001_B and 011_B the on-chip phase locked loop is enabled and provides the CPU clock (see table above). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{OSC} * \mathbf{F}$). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and figure below).
For a period of ***N*** * TCL the minimum value is computed using the corresponding deviation D_N:

$(N * TCL)_{min} = N * TCL_{NOM} - D_N$ $\quad D_N\,[ns] = \pm(13.3 + N*6.3) / f_{CPU}\,[MHz]$,
where ***N*** = number of consecutive TCLs $\quad$ and $1 \le N \le 40$.

So for a period of 3 TCLs @ 25 MHz (i.e. ***N*** = 3): $D_3 = (13.3 + 3 * 6.3) / 25 = 1.288$ ns, and $(3TCL)_{min} = 3TCL_{NOM} - 1.288$ ns = 58.7 ns (@ f_{CPU} = 25 MHz).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is neglectible.

Note: For all periods longer than 40 TCL the N=40 value can be used (see figure below).

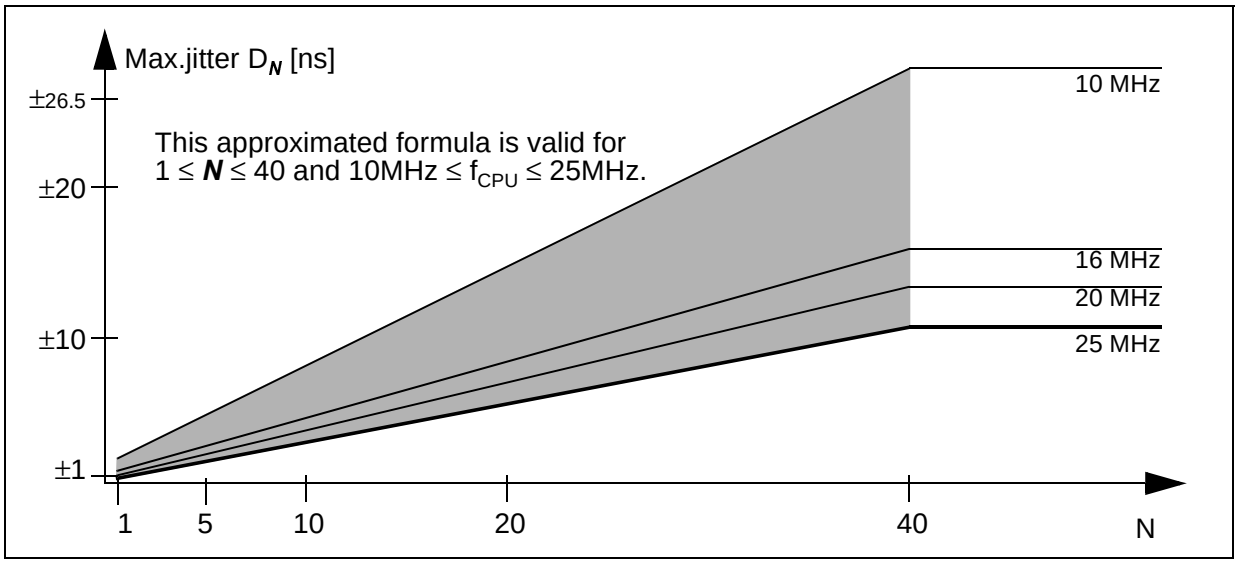


Figure 12 Approximated Maximum Accumulated PLL Jitter

Direct Drive

When pins P0.15-13 (P0H.7-5) equal 011_B during reset the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC}.
The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$TCL_{min} = 1/f_{OSC} * DC_{min}$ (DC = duty cycle)

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{OSC}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula $2TCL = 1/f_{OSC}$.

Note: The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{OSC} * DC_{max}$) instead of TCL_{min}.

AC Characteristics

External Clock Drive XTAL1 (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	40	–	20	–	60 [1]	500 [1]	ns
High time [2]	t_1	SR	20 [3]	–	6	–	10	–	ns
Low time [2]	t_2	SR	20 [3]	–	6	–	10	–	ns
Rise time [2]	t_3	SR	–	10	–	6	–	10	ns
Fall time [2]	t_4	SR	–	10	–	6	–	10	ns

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

2) The clock input signal must reach the defined levels V_{IL} and V_{IH2}.

3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

AC Characteristics

External Clock Drive XTAL1 (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	50	–	25	–	60 [1]	500 [1]	ns
High time [2]	t_1	SR	25 [3]	–	8	–	10	–	ns
Low time [2]	t_2	SR	25 [3]	–	8	–	10	–	ns
Rise time [2]	t_3	SR	–	10	–	6	–	10	ns
Fall time [2]	t_4	SR	–	10	–	6	–	10	ns

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

2) The clock input signal must reach the defined levels V_{IL} and V_{IH2}.

3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

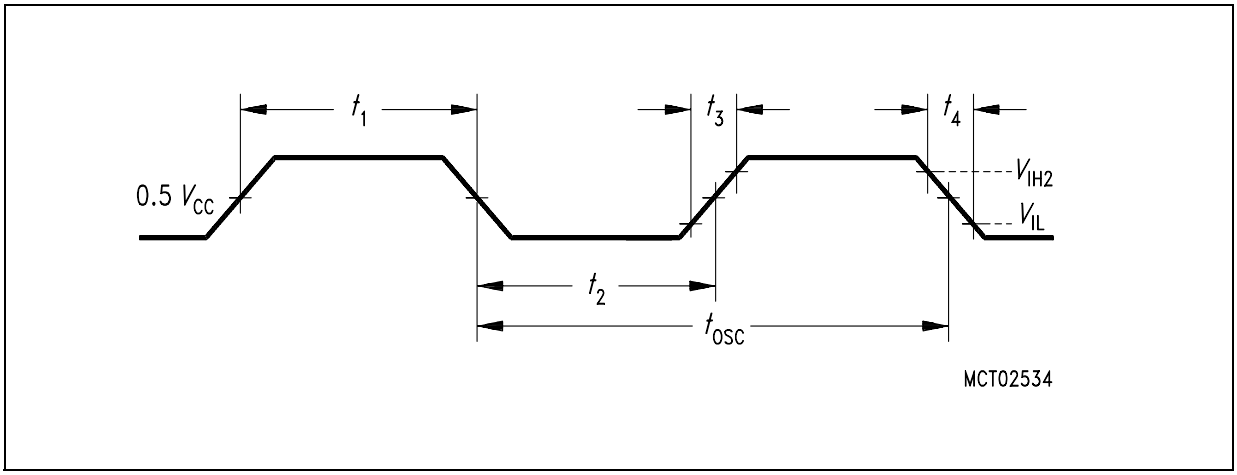


Figure 13 External Clock Drive XTAL1

Note: The main oscillator is optimized for oscillation with a crystal within a frequency range of 4...16 MHz. When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).
It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation.

A/D Converter Characteristics

(Operating Conditions apply)

4.0V (2.6V) ≤ V_{AREF} ≤ V_{DD} + 0.1V (Note the influence on TUE.)

V_{SS} - 0.1V ≤ V_{AGND} ≤ V_{SS} + 0.2V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage range	V_{AIN} SR	V_{AGND}	V_{AREF}	V	1)
Basic clock frequency	f_{BC}	0.5	6.25	MHz	2)
Conversion time	t_C CC	–	40 t_{BC} + t_S+2t_{CPU}		3) t_{CPU} = 1 / f_{CPU}
Total unadjusted error	TUE CC 4)	–	± 2	LSB	V_{AREF} ≥ 4.0 V 5)
		–	± 4	LSB	V_{AREF} ≥ 2.6 V
Internal resistance of reference voltage source	R_{AREF} SR	–	t_{BC} / 60 - 0.25	kΩ	t_{BC} in [ns] 6) 7)
Internal resistance of analog source	R_{ASRC} SR	–	t_S / 450 - 0.25	kΩ	t_S in [ns] 7) 8)
ADC input capacitance	C_{AIN} CC	–	33	pF	7)

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on the conversion time programming.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

4) TUE is tested at V_{AREF}=5.0V (3.3V), V_{AGND}=0V, V_{DD}=4.9V (3.2V). It is guaranteed by design for all other voltages within the defined voltage range.
The specified TUE is guaranteed only if an overload condition (see I_{OV} specification) occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB (±8 LSB @ 3V).

5) This case is not applicable for the reduced supply voltage range.

6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.

7) Not 100% tested, guaranteed by design.

8) During the sample time the input capacitance C_I can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample time t_S depend on programming and can be taken from the table below.

Sample time and conversion time of the C161PI's A/D Converter are programmable. The table below should be used to calculate the above timings.
The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 9 A/D Converter Computation Table

ADCON.15|14 (ADCTC)	A/D Converter Basic clock f_{BC}	ADCON.13|12 (ADSTC)	Sample time t_S
00	f_{CPU} / 4	00	t_{BC} * 8
01	f_{CPU} / 2	01	t_{BC} * 16
10	f_{CPU} / 16	10	t_{BC} * 32
11	f_{CPU} / 8	11	t_{BC} * 64

Converter Timing Example:

Assumptions:	f_{CPU}	= 25 MHz (i.e. t_{CPU} = 40 ns), ADCTC = '00', ADSTC = '00'.
Basic clock	f_{BC}	= f_{CPU} / 4 = 6.25 MHz, i.e. t_{BC} = 160 ns.
Sample time	t_S	= t_{BC} * 8 = 1280 ns.
Conversion time	t_C	= t_S + 40 t_{BC} + 2 t_{CPU} = (1280 + 6400 + 80) ns = 7.8 µs.

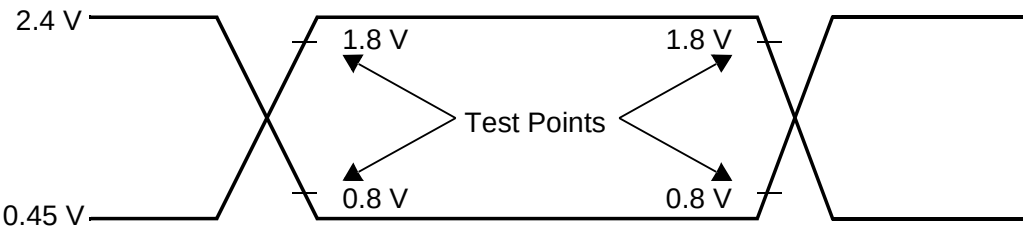
Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 10 Memory Cycle Variables

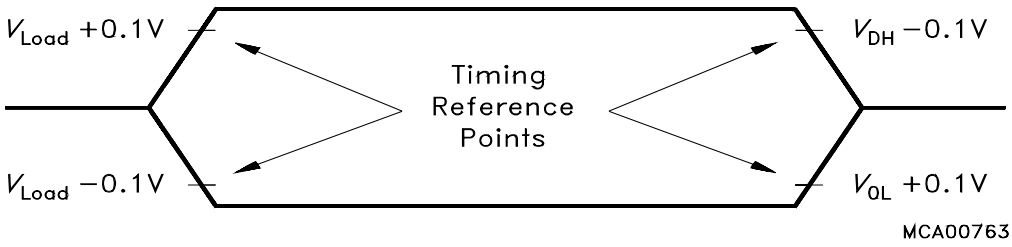
Description	Symbol	Values
ALE Extension	t_A	TCL * <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL * (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL * (1 - <MTTC>)

Testing Waveforms



AC inputs during testing are driven at 2.4 V for a logic ‘1’ and 0.45 V for a logic ‘0’.
Timing measurements are made at V_{IH} min for a logic ’1’ and V_{IL} max for a logic ’0’.

Figure 14 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

Figure 15 Float Waveforms

AC Characteristics

Multiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
Address hold after ALE	t_7	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	26	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL-10+t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	26 + t_F	–	2TCL - 14 + t_F	ns

Multiplexed Bus (Standard Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$ [1]	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In [1]	t_{39}	SR	–	40 + t_C + $2t_A$	–	3TCL - 20 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [1]	t_{40}	CC	46 + t_F	–	3TCL - 14 +t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	-4 + t_A	–	-4 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45}	CC	–	20	–	TCL	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns

Multiplexed Bus (Standard Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 6 TCL + 2t_A + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{\text{WrCS}}$	t_{50}	CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$	t_{52}	SR	–	20 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{54}	CC	20 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{56}	CC	20 + t_F	–	2TCL - 20 + t_F	–	ns

1) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

AC Characteristics

Multiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 6 TCL + 2t_A + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	11 + t_A	–	TCL - 14 + t_A	–	ns
Address setup to ALE	t_6	CC	5 + t_A	–	TCL - 20 + t_A	–	ns
Address hold after ALE	t_7	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	31	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	34 + t_C	–	2TCL - 16 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	59 + t_C	–	3TCL - 16 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	22 + t_C	–	2TCL - 28 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	47 + t_C	–	3TCL - 28 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	49 + t_A + t_C	–	3TCL - 30 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	57 + 2t_A + t_C	–	4TCL - 43 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	36 + t_F	–	2TCL - 14 + t_F	ns

Multiplexed Bus (Reduced Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{WR}$	t_{22}	CC	24 + t_C	–	2TCL - 26 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$ [1]	t_{38}	CC	-8 - t_A	10 - t_A	-8 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In [1]	t_{39}	SR	–	47 + t_C + $2t_A$	–	3TCL - 28 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [1]	t_{40}	CC	57 + t_F	–	3TCL - 18 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	19 + t_A	–	TCL - 6 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	-6 + t_A	–	-6 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45}	CC	–	25	–	TCL	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t_{46}	SR	–	20 + t_C	–	2TCL - 30 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t_{47}	SR	–	45 + t_C	–	3TCL - 30 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	t_{48}	CC	38 + t_C	–	2TCL - 12 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	t_{49}	CC	63 + t_C	–	3TCL - 12 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	28 + t_C	–	2TCL - 22 + t_C	–	ns

Multiplexed Bus (Reduced Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 6 TCL + 2t_A + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$	t_{52}	SR	–	30 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{54}	CC	30 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{56}	CC	30 + t_F	–	2TCL - 20 + t_F	–	ns

1) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

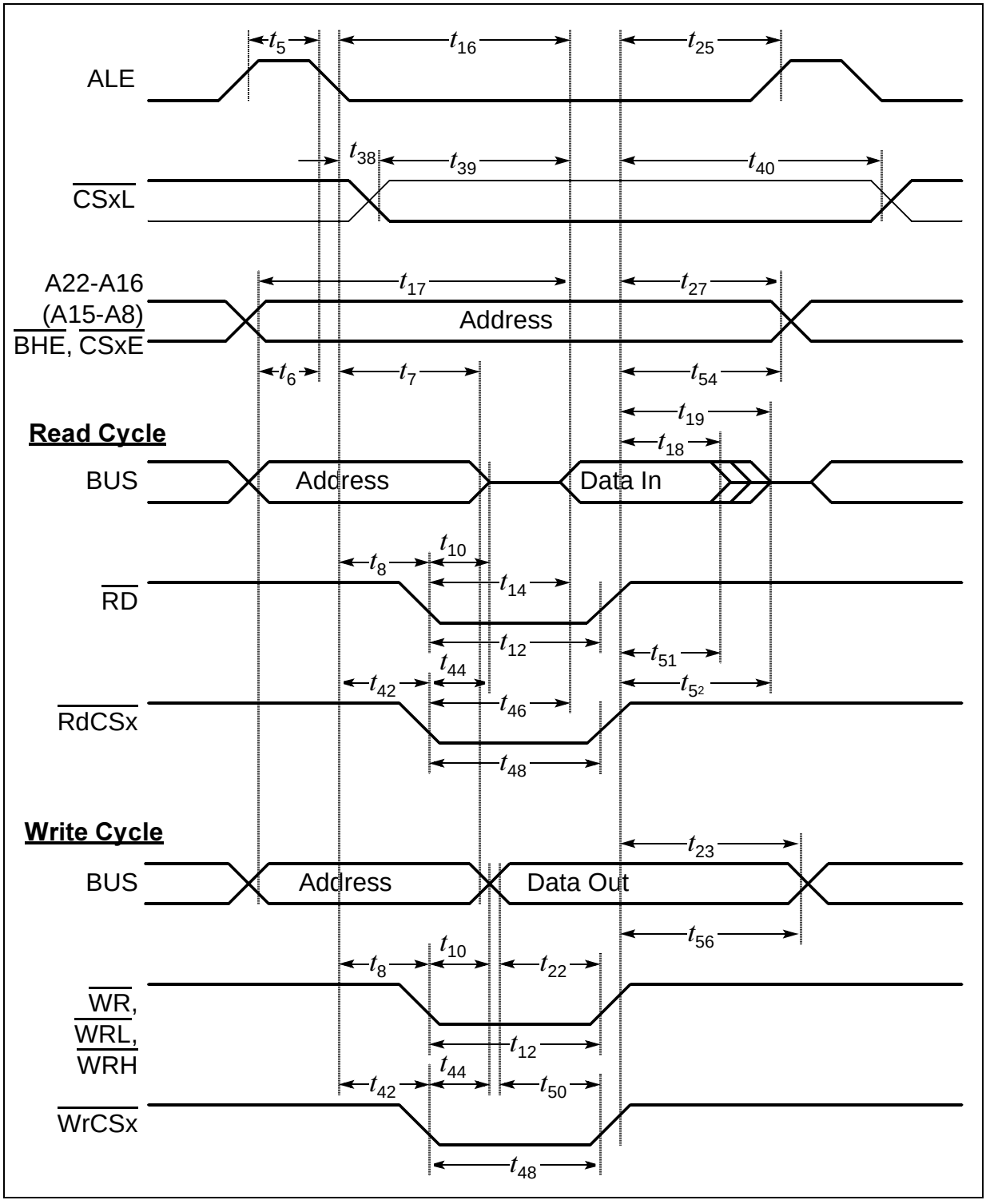


Figure 16 External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE

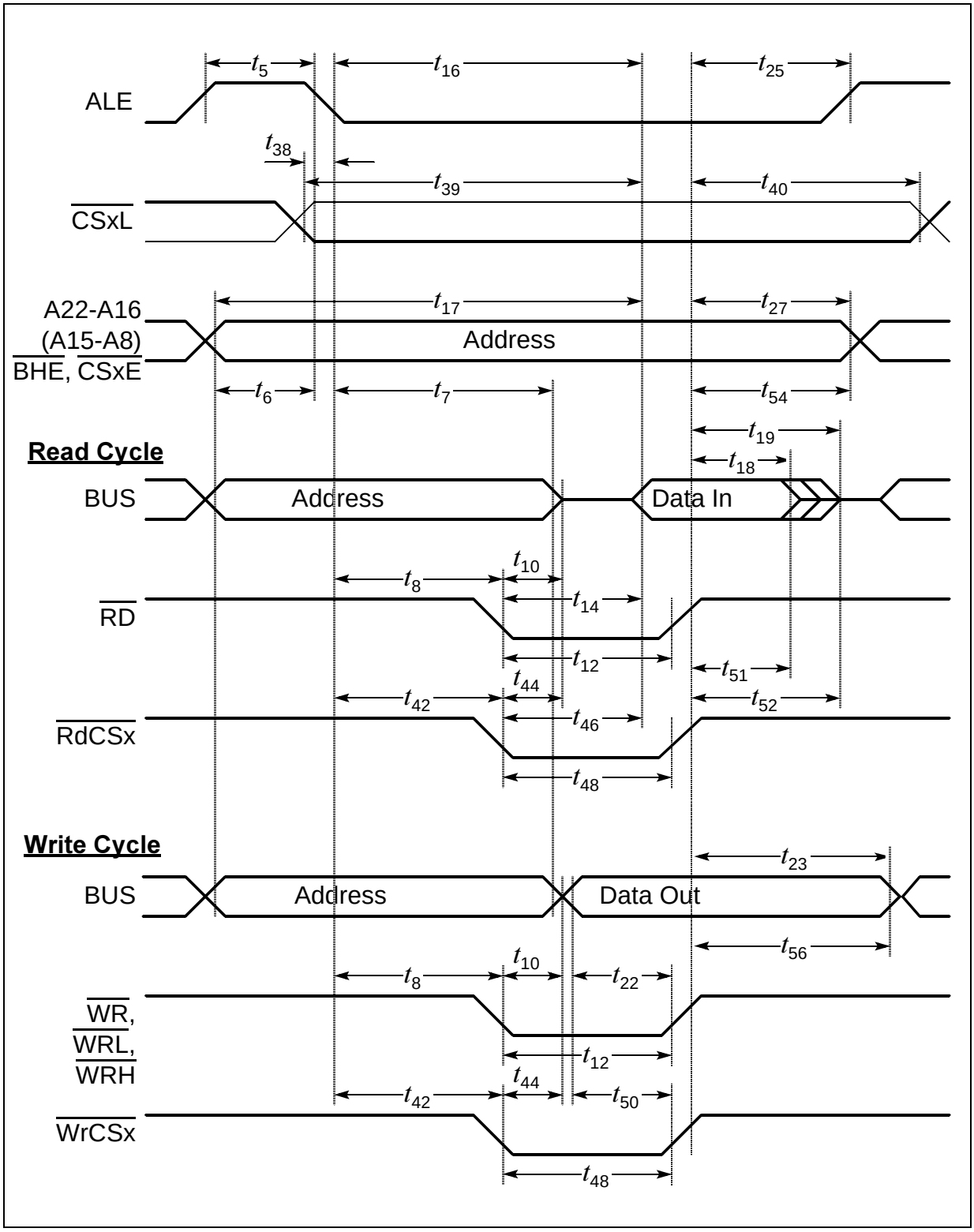


Figure 17 External Memory Cycle:
Multiplexed Bus, With Read/Write Delay, Extended ALE

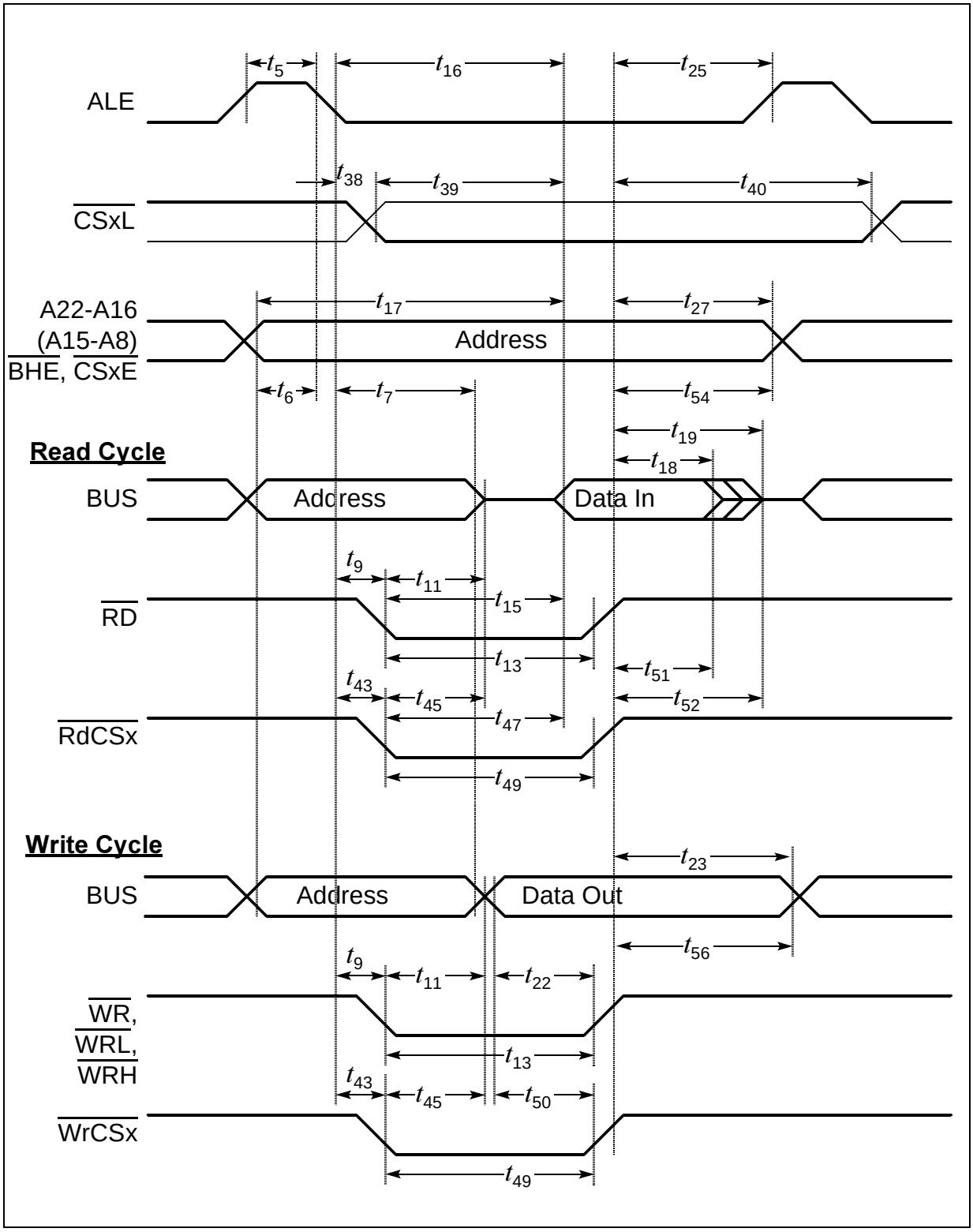


Figure 18 External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Normal ALE

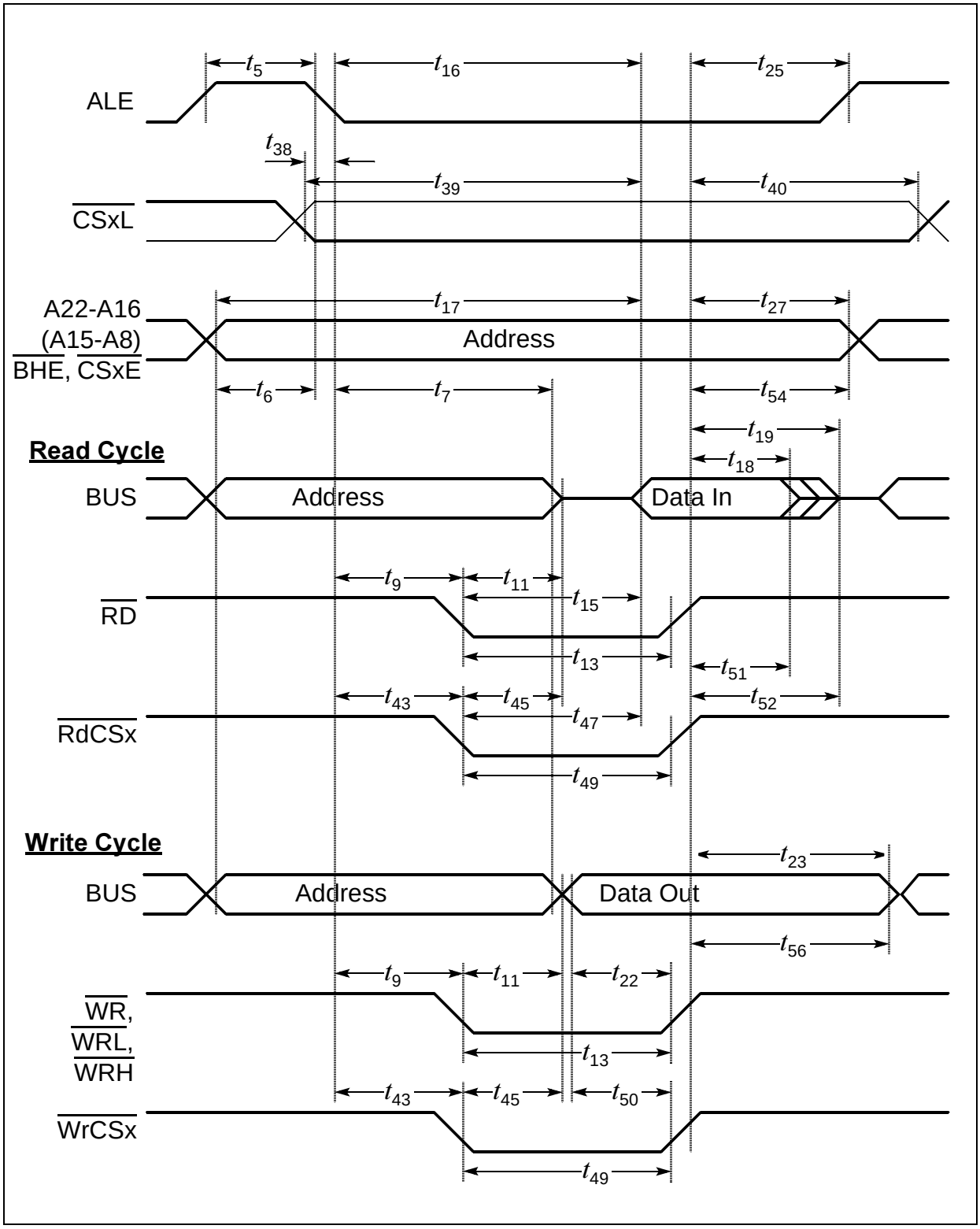


Figure 19 External Memory Cycle:
Multiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics

Demultiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A + t_C + t_F$ (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay [1])	t_{20}	SR	–	26 + $2t_A$ + t_F [1]	–	2TCL - 14 + $22t_A$ + t_F [1]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay [1])	t_{21}	SR	–	10 + $2t_A$ + t_F [1]	–	TCL - 10 + $22t_A$ + t_F [1]	ns
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns

Demultiplexed Bus (Standard Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data hold after $\overline{WR}$	t_{24}	CC	10 + t_F	–	TCL - 10 + t_F	–	ns
$\overline{ALE}$ rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-10 + t_F	–	-10 + t_F	–	ns
Address hold after $\overline{WR}$ [2]	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
$\overline{ALE}$ falling edge to $\overline{CS}$ [3]	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In [3]	t_{39}	SR	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [3]	t_{41}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns
$\overline{ALE}$ falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns
$\overline{ALE}$ falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	-4 + t_A	–	-4 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay) [1]	t_{53}	SR	–	20 + t_F	–	2TCL - 20 + 2t_A + t_F [1]	ns
Data float after $\overline{RdCS}$ (no RW-delay) [1]	t_{68}	SR	–	0 + t_F	–	TCL - 20 + 2t_A + t_F [1]	ns

Demultiplexed Bus (Standard Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol	Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
		min.	max.	min.	max.	
Address hold after RdCS, WrCS	t_{55} CC	-6 + t_F	–	-6 + t_F	–	ns
Data hold after WrCS	t_{57} CC	6 + t_F	–	TCL - 14 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising RD edge. Therefore address changes before the end of RD have no impact on read cycles.

3) These parameters refer to the latched chip select signals (CSxL). The early chip select signals (CSxE) are specified together with the address and signal BHE (see figures below).

AC Characteristics

Demultiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	11 + t_A	–	TCL - 14 + t_A	–	ns
Address setup to ALE	t_6	CC	5 + t_A	–	TCL - 20 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	34 + t_C	–	2TCL - 16 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	59 + t_C	–	3TCL - 16 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	22 + t_C	–	2TCL - 28 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	47 + t_C	–	3TCL - 28 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	49 + t_A + t_C	–	3TCL - 30 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	57 + $2t_A$ + t_C	–	4TCL - 43 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay [1])	t_{20}	SR	–	36 + $2t_A$ + t_F [1]	–	2TCL - 14 + $2t_A$ + t_F [1]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay [1])	t_{21}	SR	–	15 + $2t_A$ + t_F [1]	–	TCL - 10 + $2t_A$ + t_F [1]	ns
Data valid to $\overline{WR}$	t_{22}	CC	24 + t_C	–	2TCL - 26 + t_C	–	ns

Demultiplexed Bus (Reduced Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data hold after $\overline{WR}$	t_{24}	CC	15 + t_F	–	TCL - 10 + t_F	–	ns
$\overline{ALE}$ rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-12 + t_F	–	-12 + t_F	–	ns
Address hold after $\overline{WR}$ [2]	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
$\overline{ALE}$ falling edge to $\overline{CS}$ [3]	t_{38}	CC	-8 - t_A	10 - t_A	-8 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In [3]	t_{39}	SR	–	47 + t_C + 2t_A	–	3TCL - 28 + t_C + 2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [3]	t_{41}	CC	9 + t_F	–	TCL - 16 + t_F	–	ns
$\overline{ALE}$ falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	19 + t_A	–	TCL - 6 + t_A	–	ns
$\overline{ALE}$ falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	-6 + t_A	–	-6 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	20 + t_C	–	2TCL - 30 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	45 + t_C	–	3TCL - 30 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	38 + t_C	–	2TCL - 12 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	63 + t_C	–	3TCL - 12 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	28 + t_C	–	2TCL - 22 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay) [1]	t_{53}	SR	–	30 + t_F	–	2TCL - 20 + 2t_A + t_F [1]	ns
Data float after $\overline{RdCS}$ (no RW-delay) [1]	t_{68}	SR	–	5 + t_F	–	TCL - 20 + 2t_A + t_F [1]	ns

Demultiplexed Bus (Reduced Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
Address hold after RdCS, WrCS	t_{55} CC	-16 + t_F	–	-16 + t_F	–	ns
Data hold after WrCS	t_{57} CC	9 + t_F	–	TCL - 16 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising RD edge. Therefore address changes before the end of RD have no impact on read cycles.

3) These parameters refer to the latched chip select signals (CSxL). The early chip select signals (CSxE) are specified together with the address and signal BHE (see figures below).

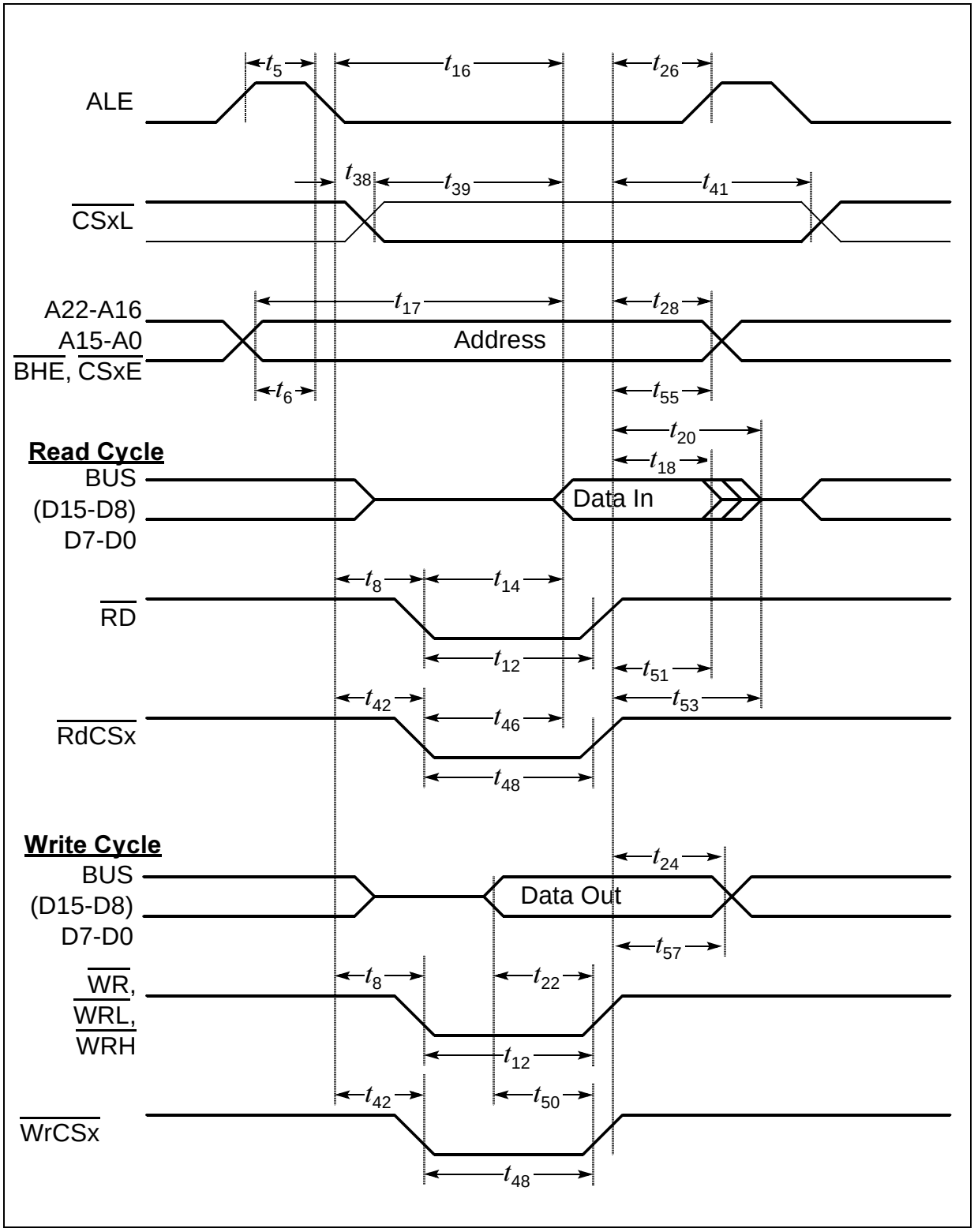


Figure 20 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Normal ALE

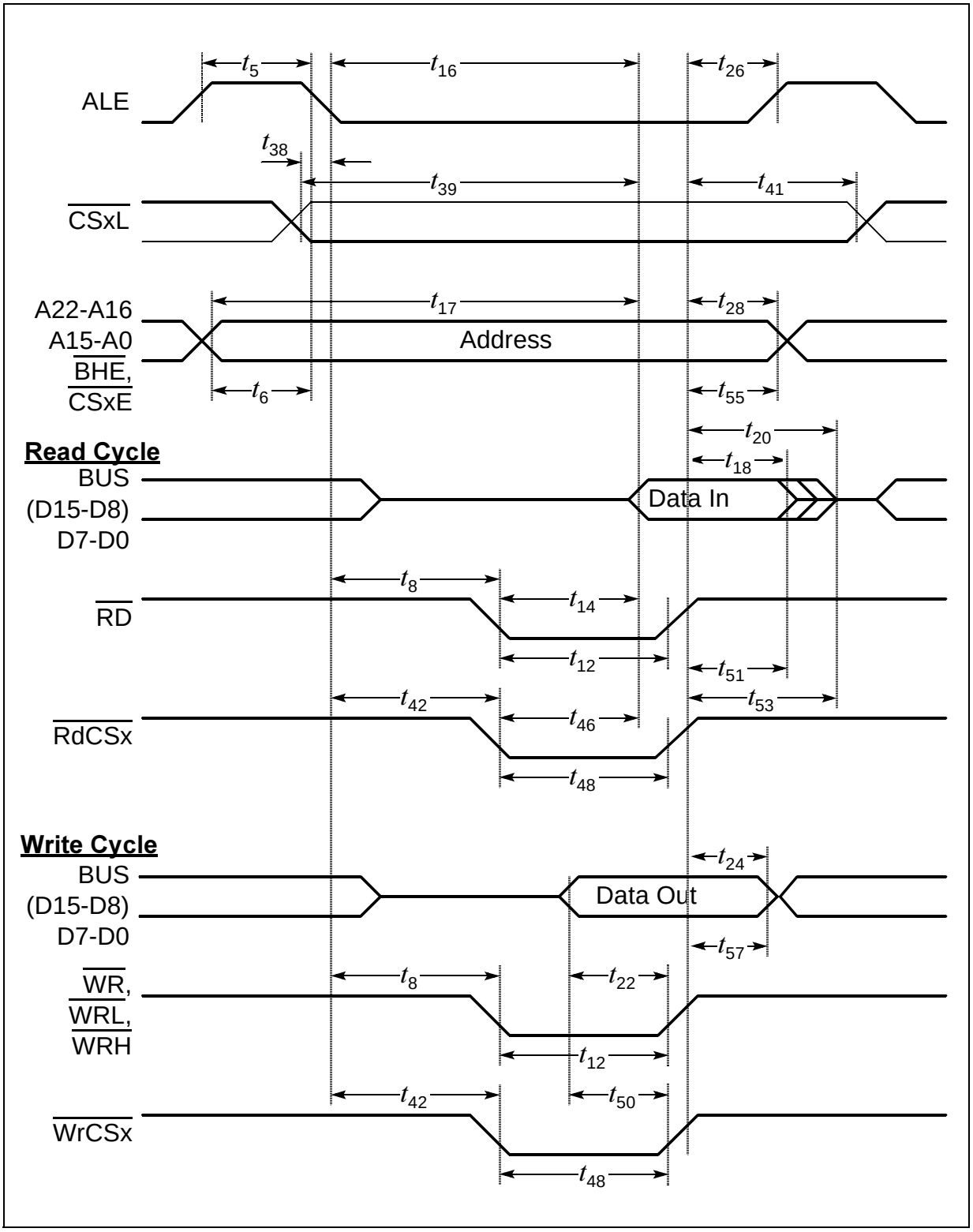


Figure 21 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE

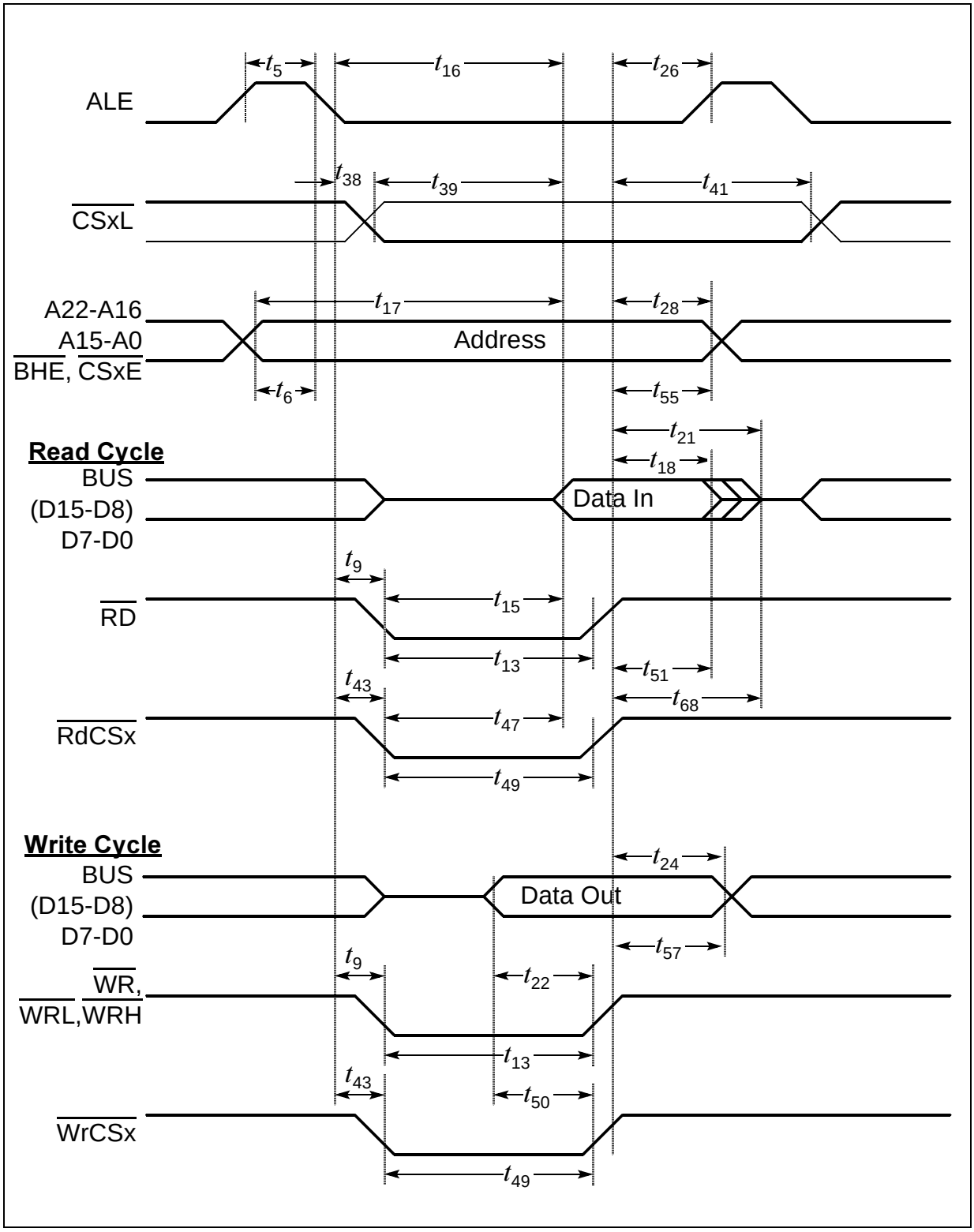


Figure 22 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE

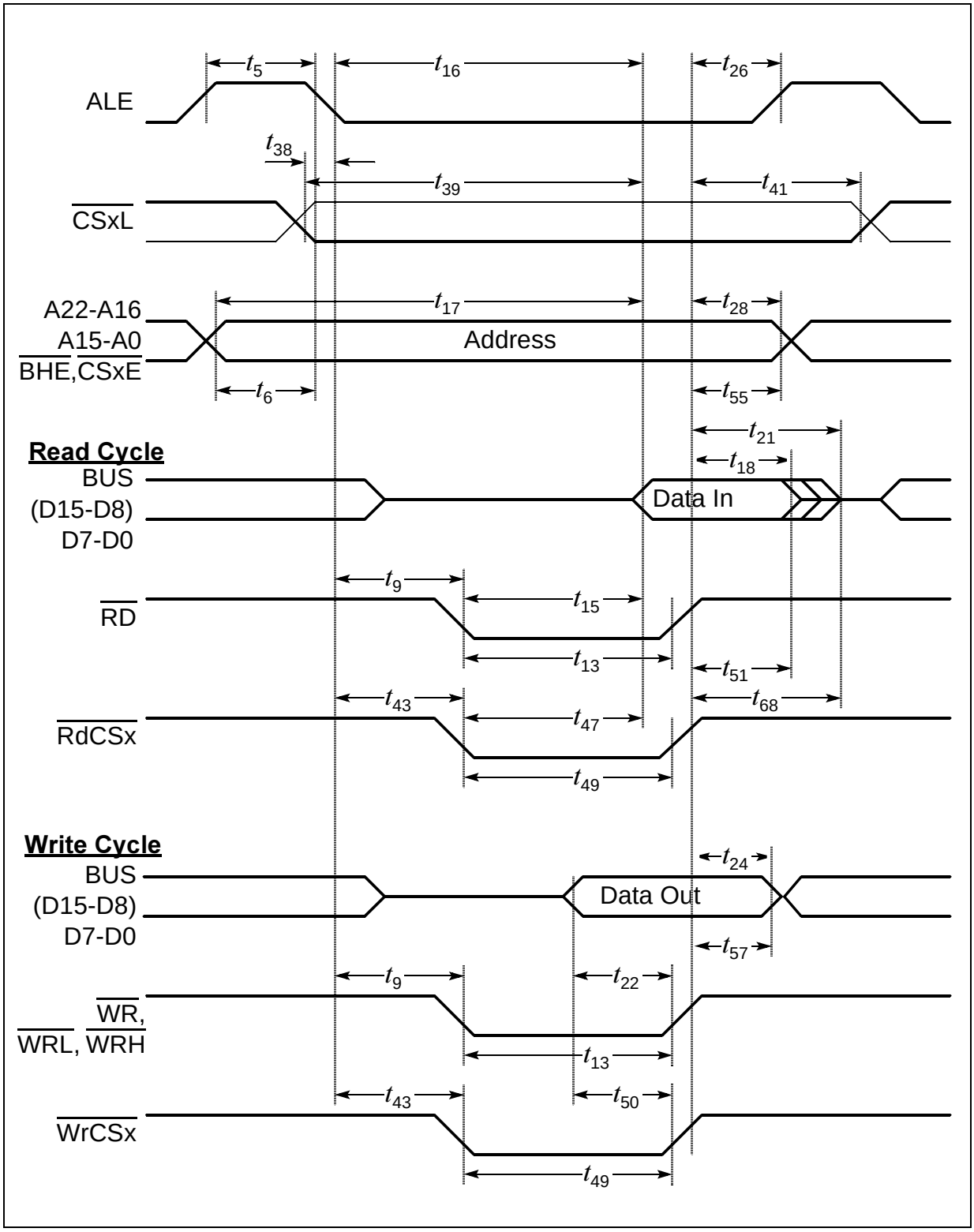


Figure 23 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics

CLKOUT and $\overline{\text{READY}}$ (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	14	–	TCL – 6	–	ns
CLKOUT low time	t_{31}	CC	10	–	TCL – 10	–	ns
CLKOUT rise time	t_{32}	CC	–	4	–	4	ns
CLKOUT fall time	t_{33}	CC	–	4	–	4	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	$0 + t_A$	$10 + t_A$	$0 + t_A$	$10 + t_A$	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35}	SR	14	–	14	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36}	SR	4	–	4	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37}	SR	54	–	$2TCL + t_{58}$	–	ns
Asynchronous $\overline{\text{READY}}$ setup time [1]	t_{58}	SR	14	–	14	–	ns
Asynchronous $\overline{\text{READY}}$ hold time [1]	t_{59}	SR	4	–	4	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	t_{60}	SR	0	$0 + 2t_A + t_C + t_F$ [2]	0	$TCL - 20 + 2t_A + t_C + t_F$ [2]	ns

1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.
The maximum limit for t_{60} must be fulfilled if the next following bus cycle is $\overline{\text{READY}}$ controlled.

AC Characteristics

CLKOUT and $\overline{\text{READY}}$ (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	15	–	TCL – 10	–	ns
CLKOUT low time	t_{31}	CC	13	–	TCL – 12	–	ns
CLKOUT rise time	t_{32}	CC	–	12	–	12	ns
CLKOUT fall time	t_{33}	CC	–	8	–	8	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	$0 + t_A$	$8 + t_A$	$0 + t_A$	$8 + t_A$	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35}	SR	18	–	18	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36}	SR	4	–	4	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37}	SR	68	–	$2TCL + t_{58}$	–	ns
Asynchronous $\overline{\text{READY}}$ setup time [1]	t_{58}	SR	18	–	18	–	ns
Asynchronous $\overline{\text{READY}}$ hold time [1]	t_{59}	SR	4	–	4	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	t_{60}	SR	0	$0 + 2t_A + t_C + t_F$ [2]	0	$TCL - 25 + 2t_A + t_C + t_F$ [2]	ns

1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.
The maximum limit for t_{60} must be fulfilled if the next following bus cycle is $\overline{\text{READY}}$ controlled.

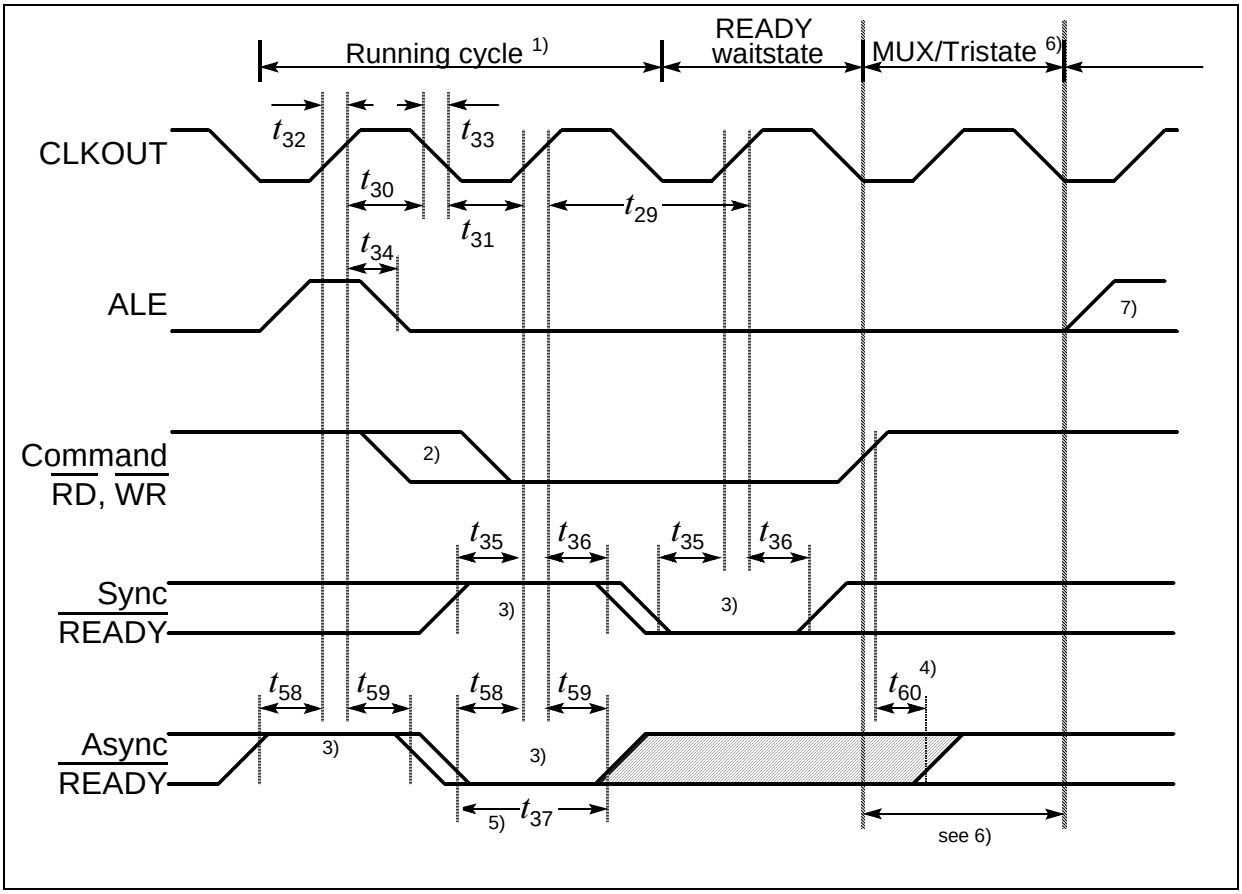


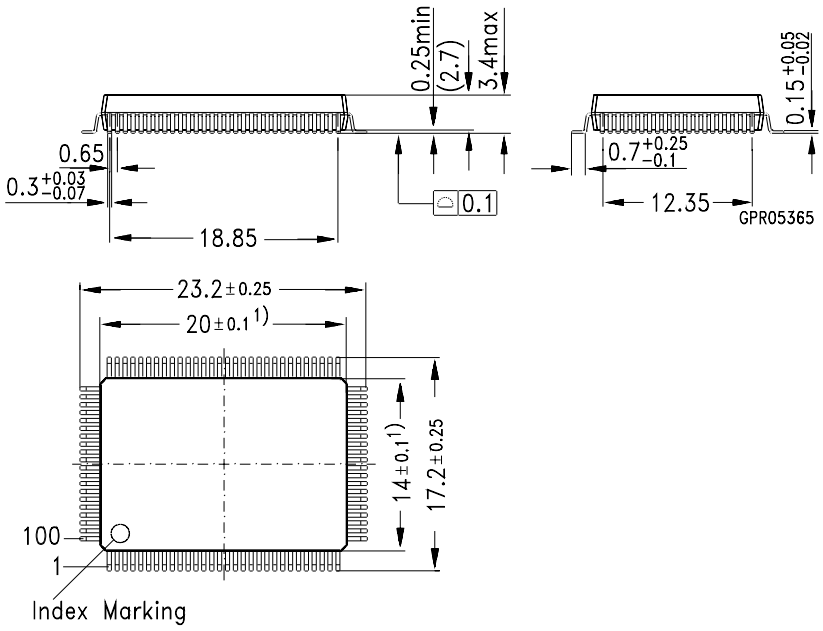
Figure 24 CLKOUT and READY

Notes

1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
2) The leading edge of the respective command depends on RW-delay.
3) READY sampled HIGH at this sampling point generates a READY controlled waitstate,
READY sampled LOW at this sampling point terminates the currently running bus cycle.
4) READY may be deactivated in response to the trailing (rising) edge of the corresponding command (RD or WR).
5) If the Asynchronous READY signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if READY is removed in reponse to the command (see Note 4)).
6) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.
7) The next external bus cycle may start here.

Package Outlines

Plastic Package, P-MQFP-100-2 (SMD)
(Plastic Metric Quad Flat Package)

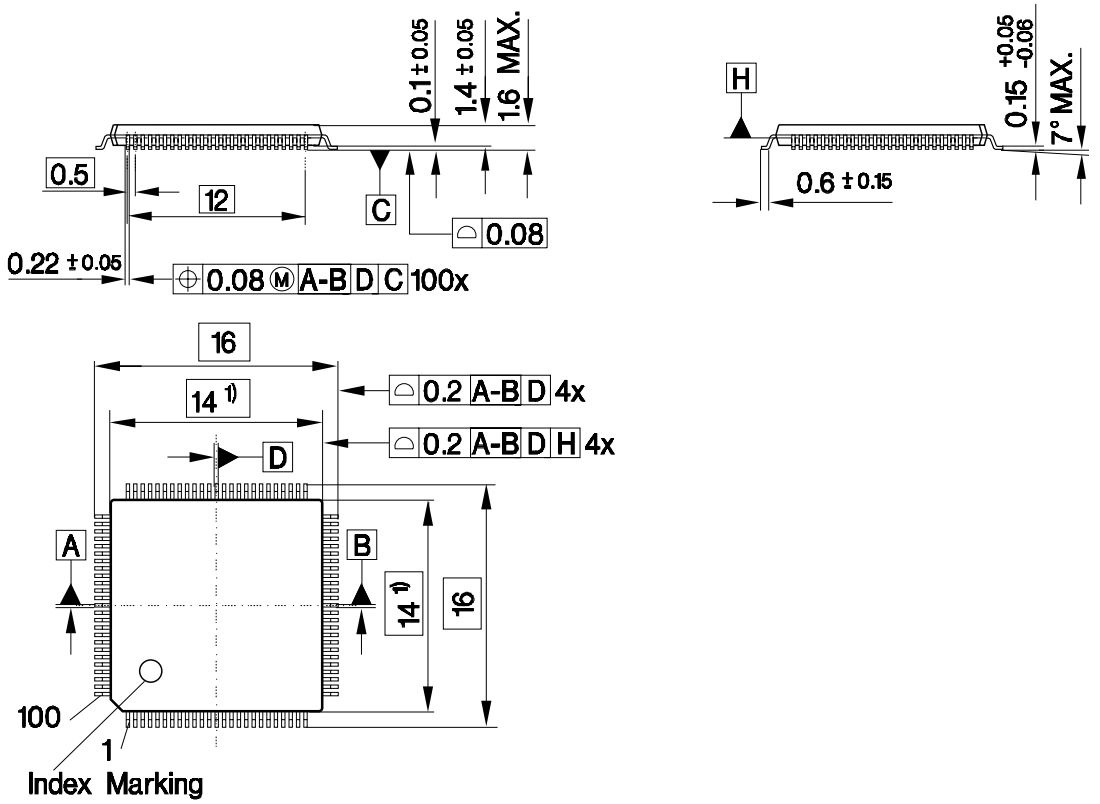


1) Does not include plastic or metal protrusions of 0.25max per side

Figure 25

Package Outlines (continued)

Plastic Package, P-TQFP-100-1 (SMD)
(Plastic Thin Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 26

Sorts of Packing

Package outlines for tubes, trays, etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

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