

DATA SHEET

BFG97

NPN 5 GHz wideband transistor

Product specification

September 1995



NPN 5 GHz wideband transistor

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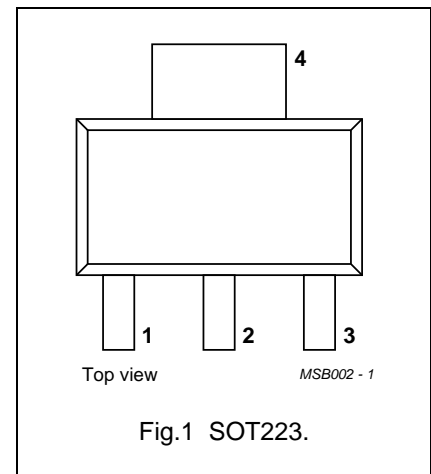
DESCRIPTION

NPN planar epitaxial transistor mounted in a plastic SOT223 envelope. It features excellent output voltage capabilities, and is primarily intended for use in MATV applications.

PNP complement is the BFG31.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	emitter
4	collector



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CB0}	collector-base voltage	open emitter	–	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	–	15	V
I_C	DC collector current		–	–	100	mA
P_{tot}	total power dissipation	up to $T_s = 125\text{ °C}$ (note 1)	–	–	1	W
h_{FE}	DC current gain	$I_C = 70\text{ mA}; V_{CE} = 10\text{ V}; T_j = 25\text{ °C}$	25	80	–	
f_T	transition frequency	$I_C = 70\text{ mA}; V_{CE} = 10\text{ V}; f = 500\text{ MHz}; T_{amb} = 25\text{ °C}$	–	5.5	–	GHz
G_{UM}	maximum unilateral power gain	$I_C = 70\text{ mA}; V_{CE} = 10\text{ V}; f = 500\text{ MHz}; T_{amb} = 25\text{ °C}$	–	16	–	dB
		$I_C = 70\text{ mA}; V_{CE} = 10\text{ V}; f = 800\text{ MHz}; T_{amb} = 25\text{ °C}$	–	12	–	dB
V_o	output voltage	$I_C = 70\text{ mA}; V_{CE} = 10\text{ V}; d_{im} = -60\text{ dB}; R_L = 75\text{ }\Omega; f_{(p+q-r)} = 793.25\text{ MHz}; T_{amb} = 25\text{ °C}$	–	700	–	mV

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CB0}	collector-base voltage	open emitter	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	15	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	DC collector current		–	100	mA
P_{tot}	total power dissipation	up to $T_s = 125\text{ °C}$ (note 1)	–	1	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	175	°C

Note

- T_s is the temperature at the soldering point of the collector tab.

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THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j-s}$	thermal resistance from junction to soldering point	up to $T_s = 125\text{ °C}$ (note 1)	50 K/W

Note

- T_s is the temperature at the soldering point of the collector tab.

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = 10\text{ V}$	–	–	100	nA
h_{FE}	DC current gain	$I_C = 70\text{ mA}; V_{CE} = 10\text{ V}$	25	80	–	
f_T	transition frequency	$I_C = 70\text{ mA}; V_{CE} = 10\text{ V};$ $f = 500\text{ MHz}; T_{amb} = 25\text{ °C}$	–	5.5	–	GHz
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$	–	1.5	–	pF
C_e	emitter capacitance	$I_C = i_c = 0; V_{EB} = 0.5\text{ V}; f = 1\text{ MHz}$	–	6.5	–	pF
C_{re}	feedback capacitance	$I_C = 0; V_{CE} = 10\text{ V}; f = 1\text{ MHz}$	–	1	–	pF
G_{UM}	maximum unilateral power gain (note 1)	$I_C = 70\text{ mA}; V_{CE} = 10\text{ V};$ $f = 500\text{ MHz}; T_{amb} = 25\text{ °C}$	–	16	–	dB
		$I_C = 70\text{ mA}; V_{CE} = 10\text{ V};$ $f = 800\text{ MHz}; T_{amb} = 25\text{ °C}$	–	12	–	dB
V_o	output voltage	note 2	–	750	–	mV
		note 3	–	700	–	mV
d_2	second order intermodulation distortion	note 4	–	–56	–	dB
		note 5	–	–53	–	dB

Notes

- G_{UM} is the maximum unilateral power gain, assuming S_{12} is zero and

$$G_{UM} = 10 \log \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} \text{ dB.}$$

- $d_{im} = -60\text{ dB}$ (DIN 45004B); $I_C = 70\text{ mA}; V_{CE} = 10\text{ V}; R_L = 75\text{ }\Omega; T_{amb} = 25\text{ °C}$
 $V_p = V_o$ at $d_{im} = -60\text{ dB}$;
 $V_q = V_o - 6\text{ dB}; f_p = 445.25\text{ MHz};$
 $V_r = V_o - 6\text{ dB}; f_q = 453.25\text{ MHz}; f_r = 455.25\text{ MHz};$
measured at $f_{(p+q-r)} = 443.25\text{ MHz}$.
- $d_{im} = -60\text{ dB}$ (DIN 45004B); $I_C = 70\text{ mA}; V_{CE} = 10\text{ V}; R_L = 75\text{ }\Omega; T_{amb} = 25\text{ °C}$
 $V_p = V_o$ at $d_{im} = -60\text{ dB}$;
 $V_q = V_o - 6\text{ dB}; f_p = 795.25\text{ MHz};$
 $V_r = V_o - 6\text{ dB}; f_q = 803.25\text{ MHz}; f_r = 805.25\text{ MHz};$
measured at $f_{(p+q-r)} = 793.25\text{ MHz}$.
- $I_C = 70\text{ mA}; V_{CE} = 10\text{ V}; R_L = 75\text{ }\Omega; T_{amb} = 25\text{ °C};$
 $V_p = V_q = V_o = 50\text{ dBmV}; f_{(p+q)} = 450\text{ MHz}; f_p = 50\text{ MHz}; f_q = 400\text{ MHz}.$
- $I_C = 70\text{ mA}; V_{CE} = 10\text{ V}; R_L = 75\text{ }\Omega; T_{amb} = 25\text{ °C};$
 $V_p = V_q = V_o = 50\text{ dBmV}; f_{(p+q)} = 810\text{ MHz}; f_p = 250\text{ MHz}; f_q = 560\text{ MHz}.$

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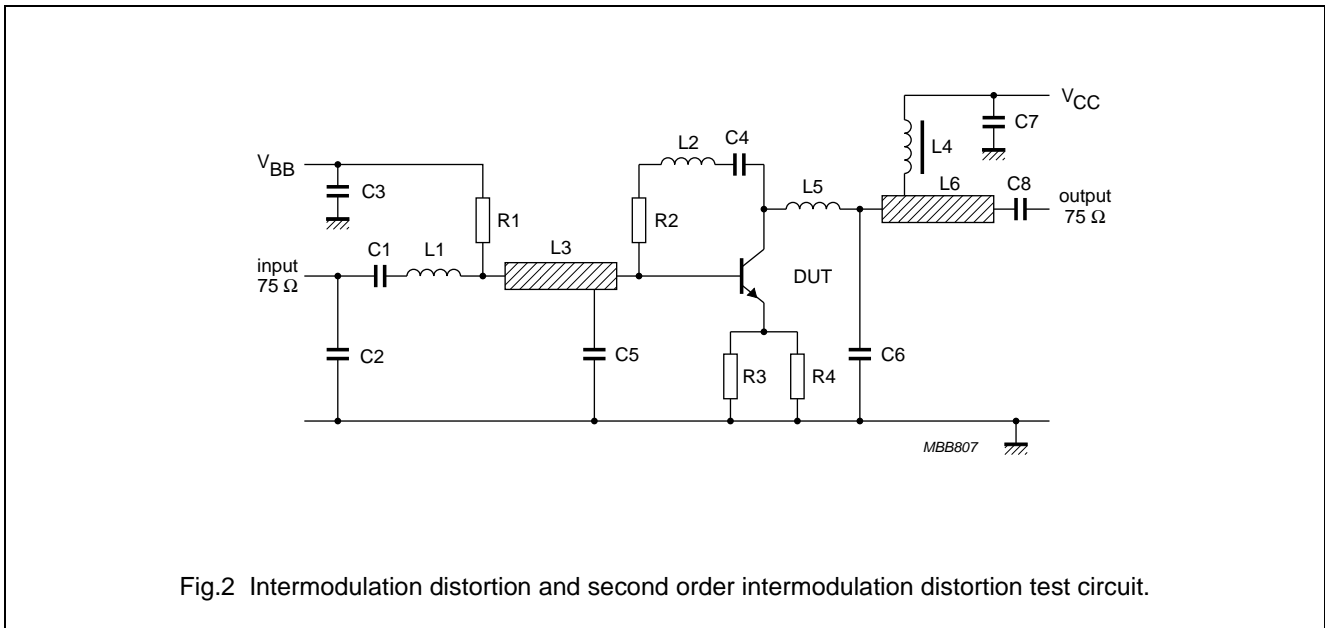


Fig.2 Intermodulation distortion and second order intermodulation distortion test circuit.

List of components (see test circuit)

DESIGNATION	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C2, C3, C7, C8	multilayer ceramic capacitor	10 nF		2222 590 08627
C1, C4, C6	multilayer ceramic capacitor	1.2 pF		2222 851 12128
C5 (note 1)	miniature ceramic plate capacitor	10 nF		2222 629 08103
L1 (note 1)	0.5 turns 0.4 mm copper wire		int. dia. 3 mm	
L2	microstripline	75 Ω	length 14 mm; width 2.5 mm	
L3	microstripline	75 Ω	length 8 mm; width 2.5 mm	
L4, L5 (note 1)	1.5 turns 0.4 mm copper wire		int. dia. 3 mm; winding pitch 1 mm	
L6	microstripline	75 Ω	length 19 mm; width 2.5 mm	
L7	Ferroxcube choke	5 μH		3122 108 20153
R1	metal film resistor	10 kΩ		2322 180 73103
R2 (note 1)	metal film resistor	220 Ω		2322 180 73221
R3, R4	metal film resistor	30 Ω		2322 180 73309

Notes

The circuit has been built on a double copper-clad printed circuit board with PTFE dielectric ($\epsilon_r = 2.2$); thickness $\frac{1}{16}$ inch; thickness of copper sheet $2 \times 35 \mu\text{m}$.

- Components C5, L1, L4, L5, and R2 are mounted on the underside of the PCB.

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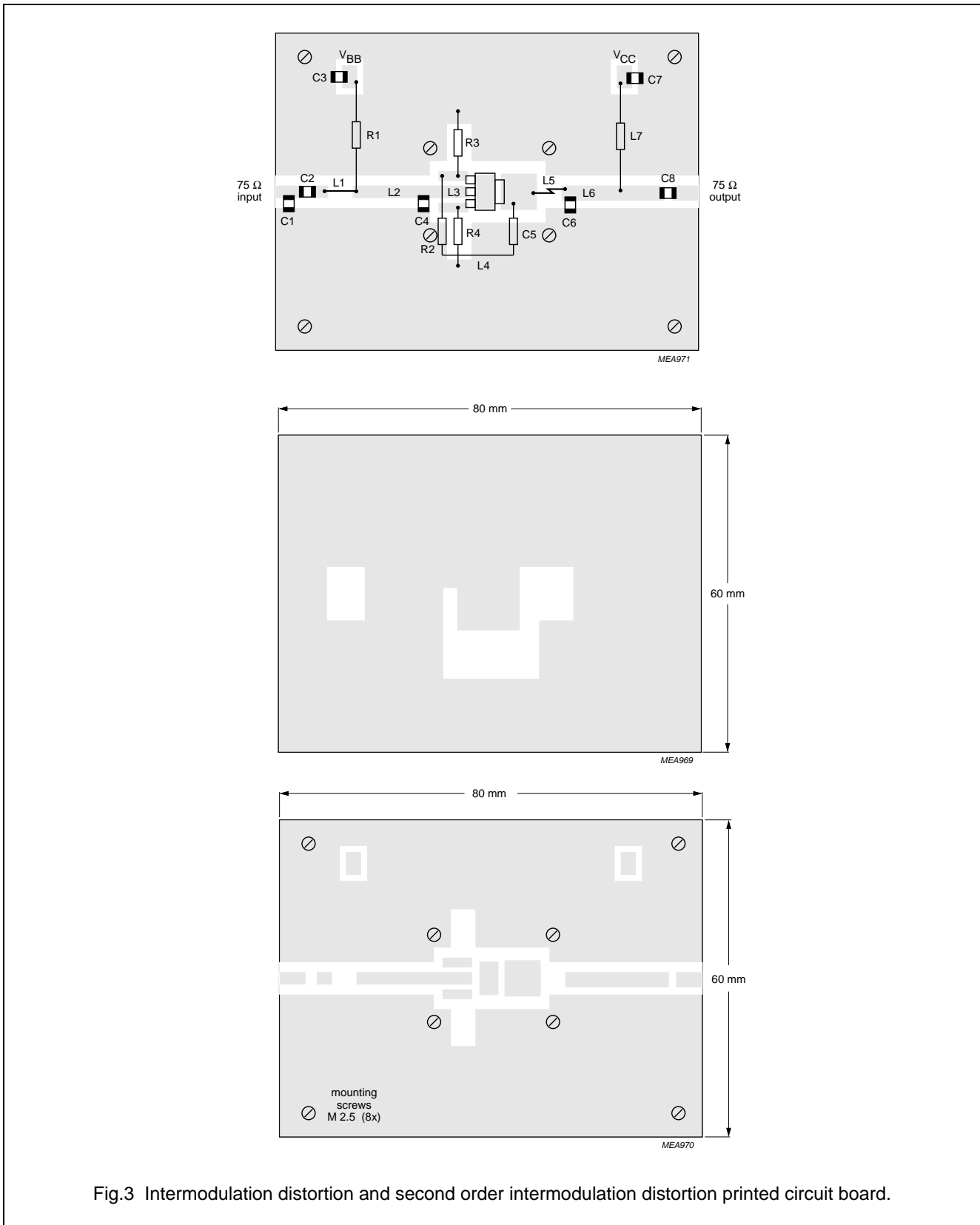
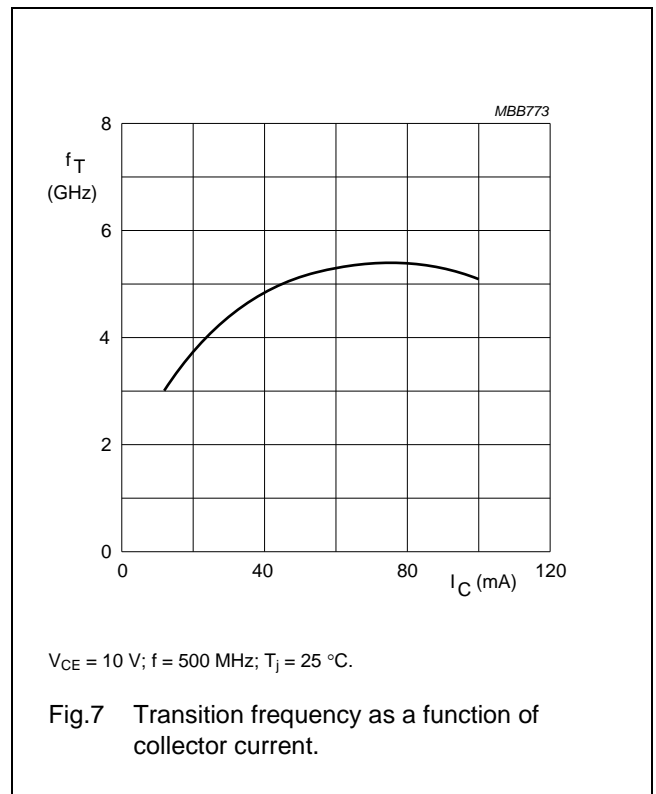
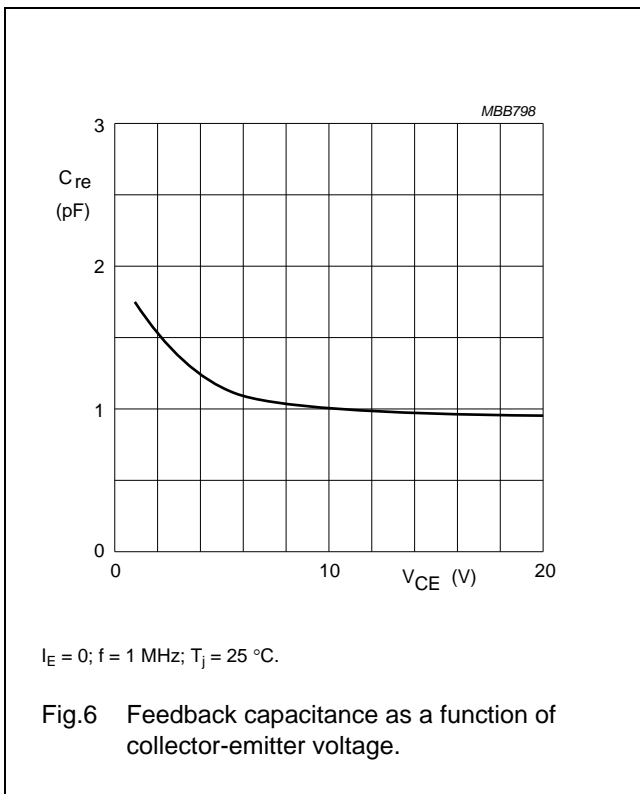
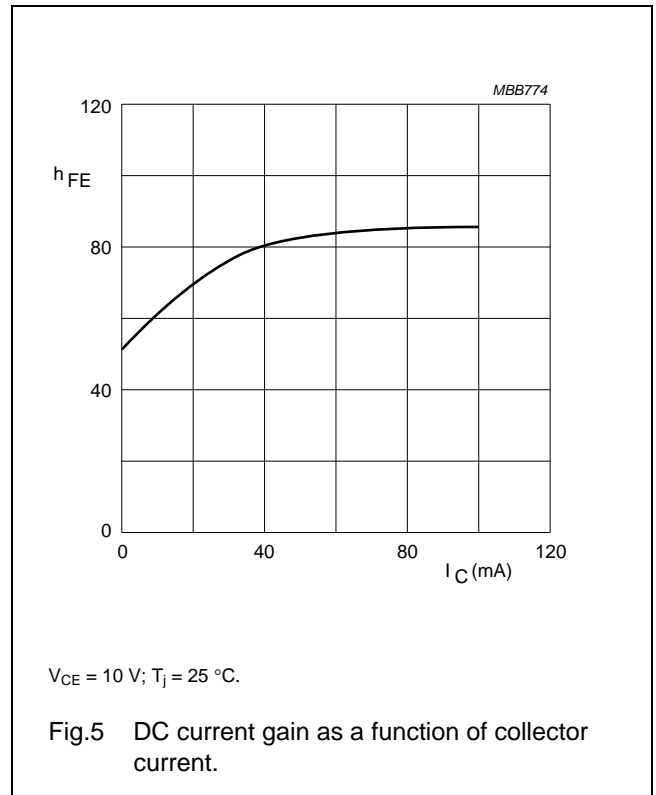
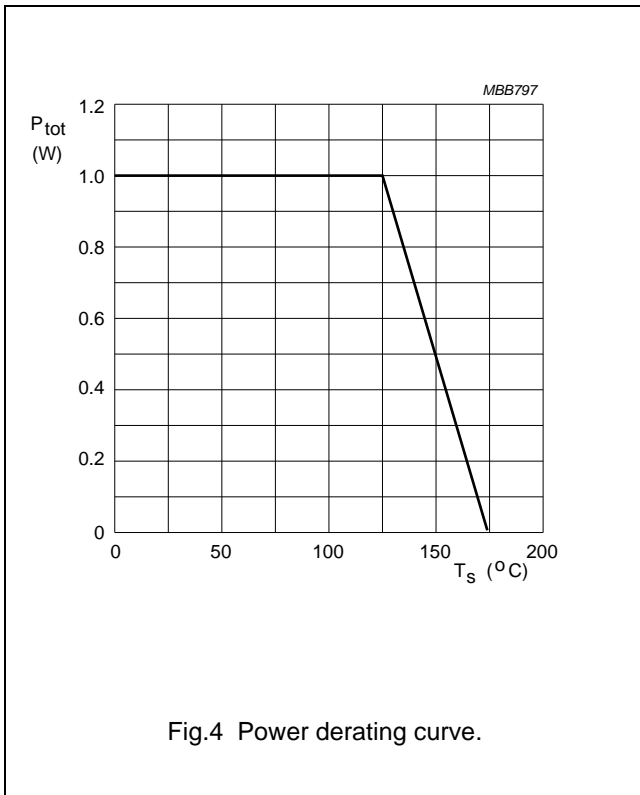


Fig.3 Intermodulation distortion and second order intermodulation distortion printed circuit board.

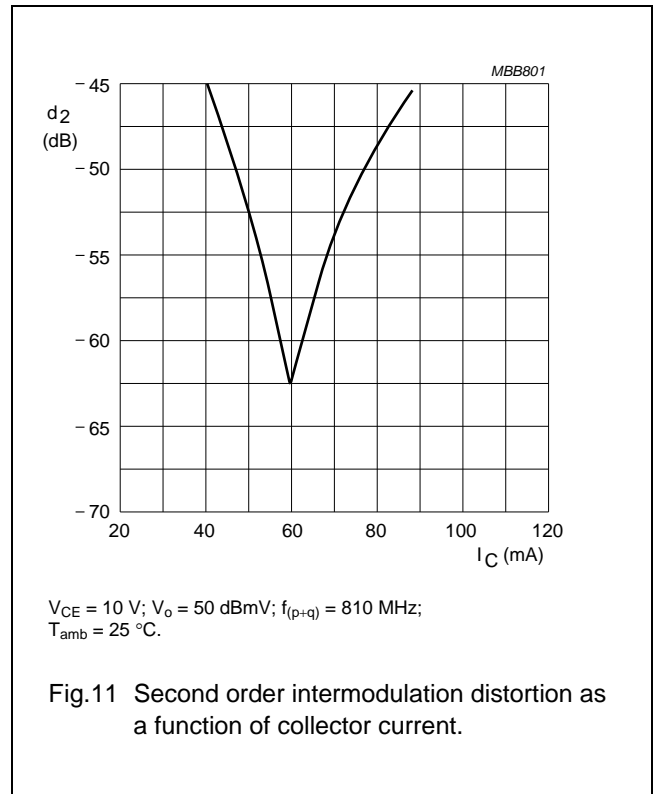
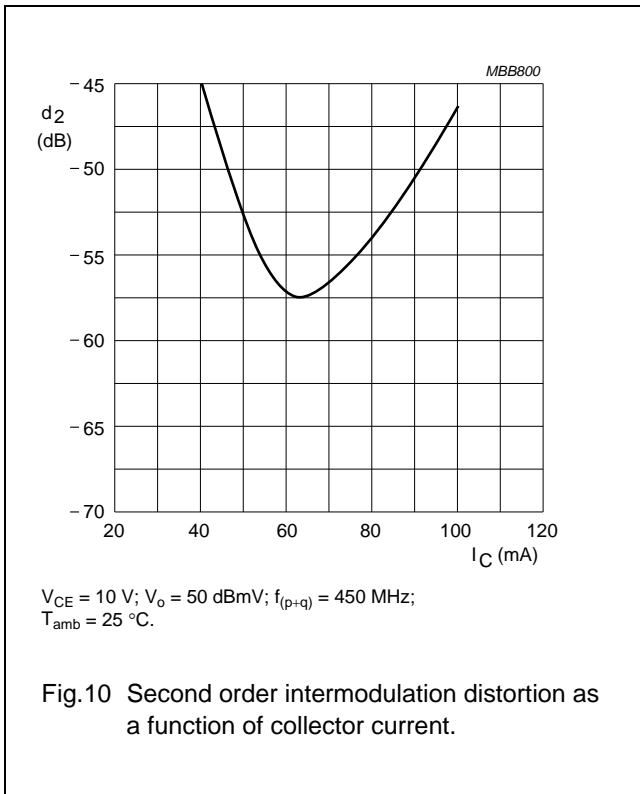
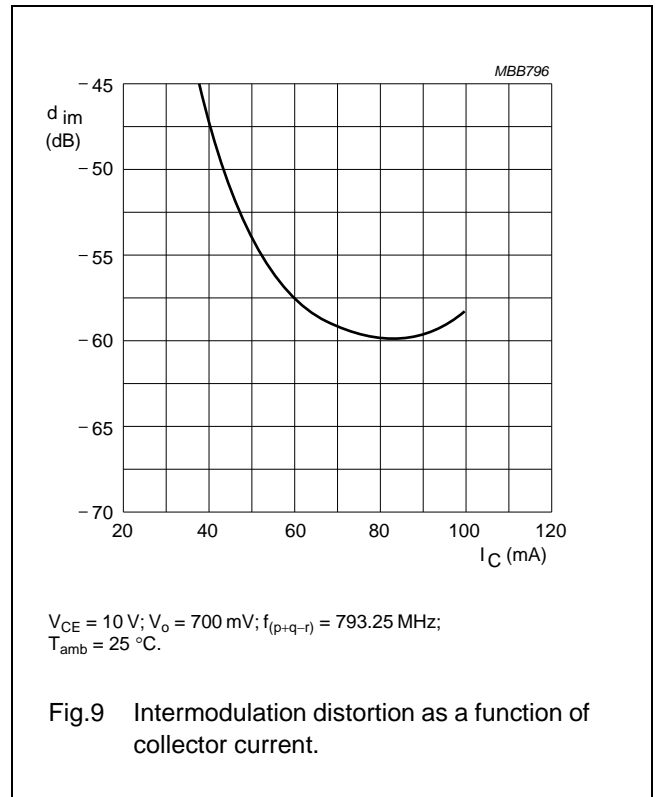
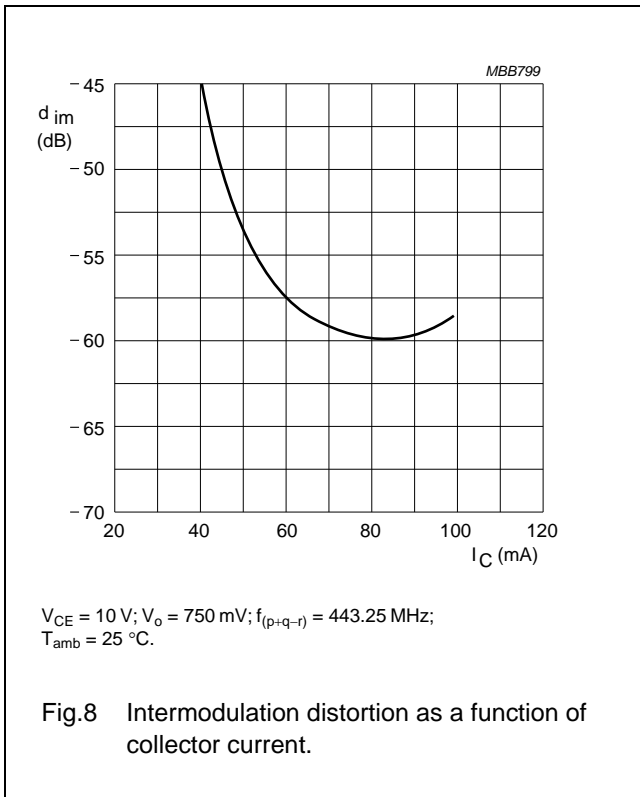
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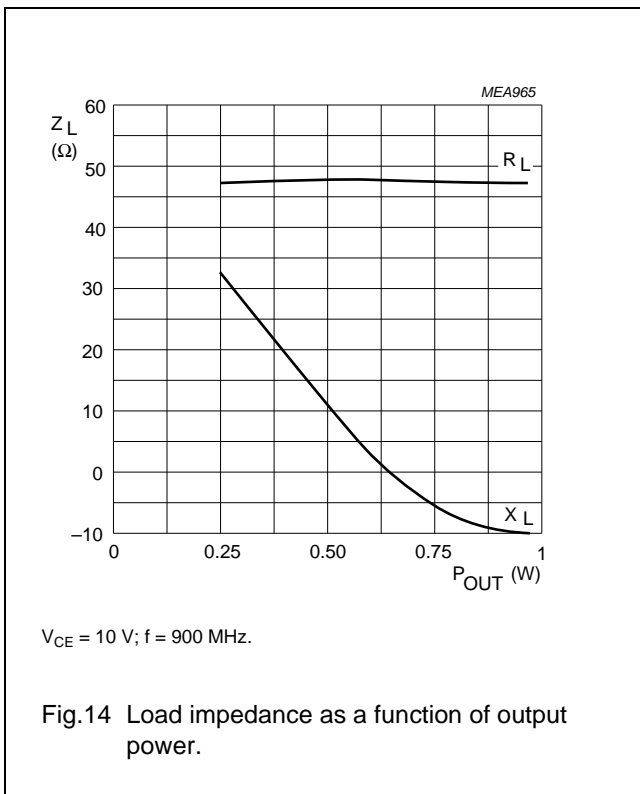
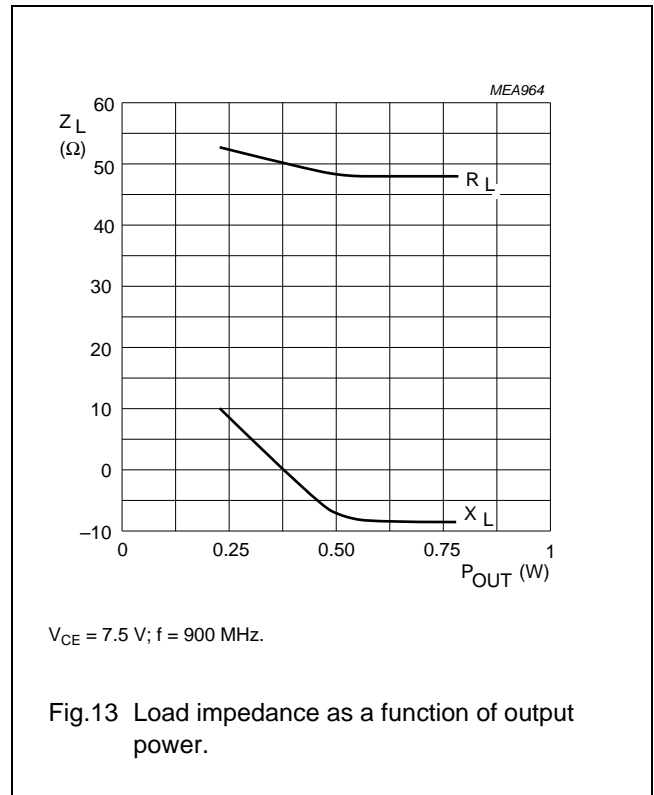
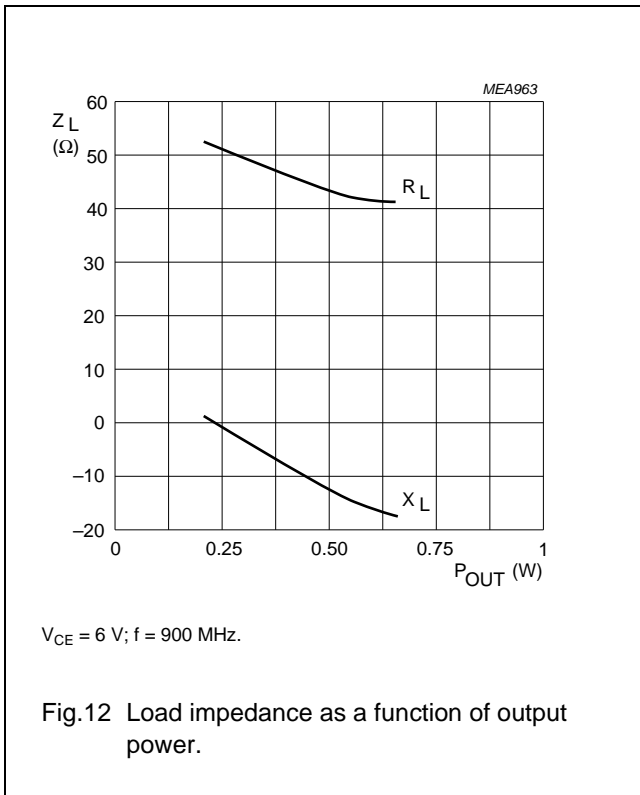
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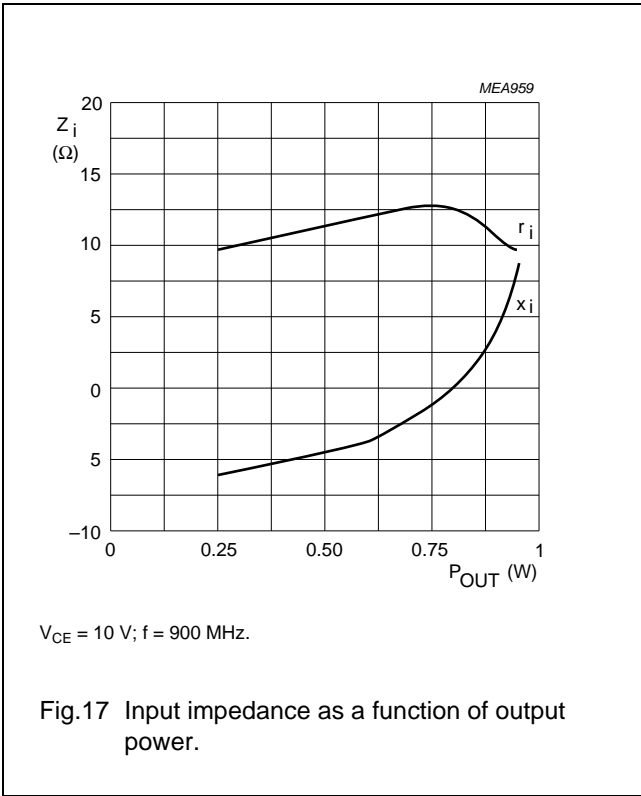
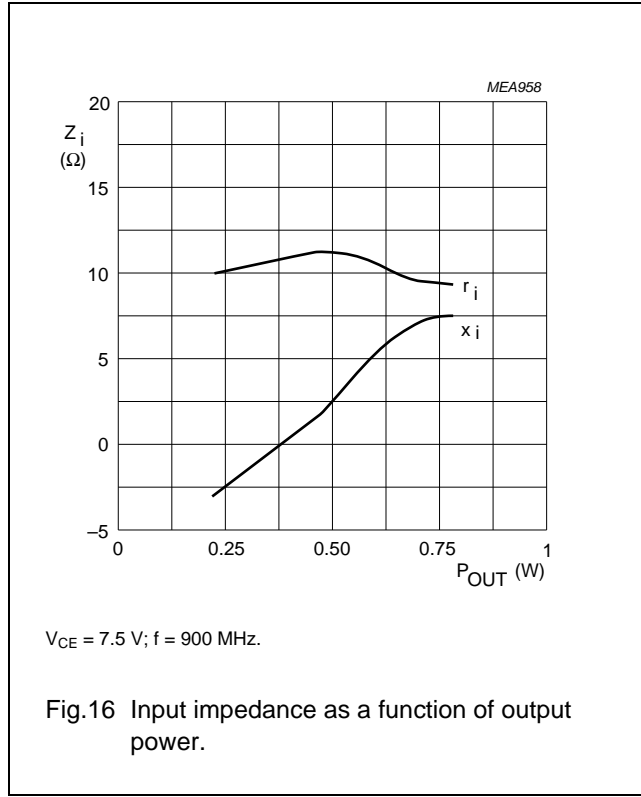
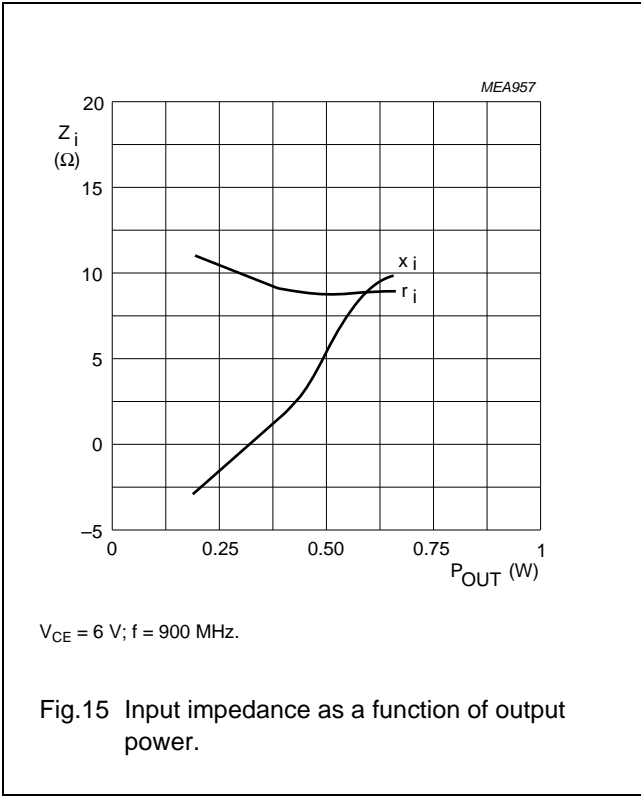
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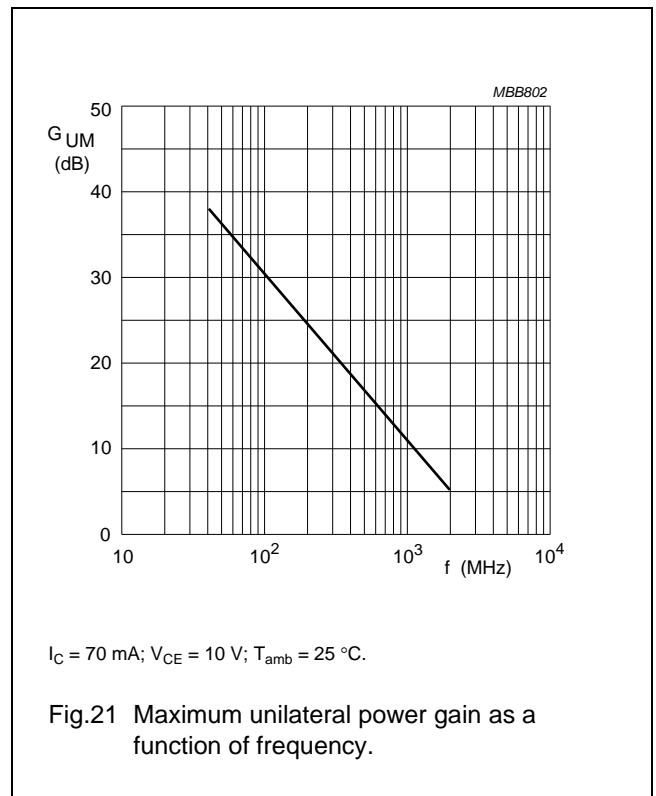
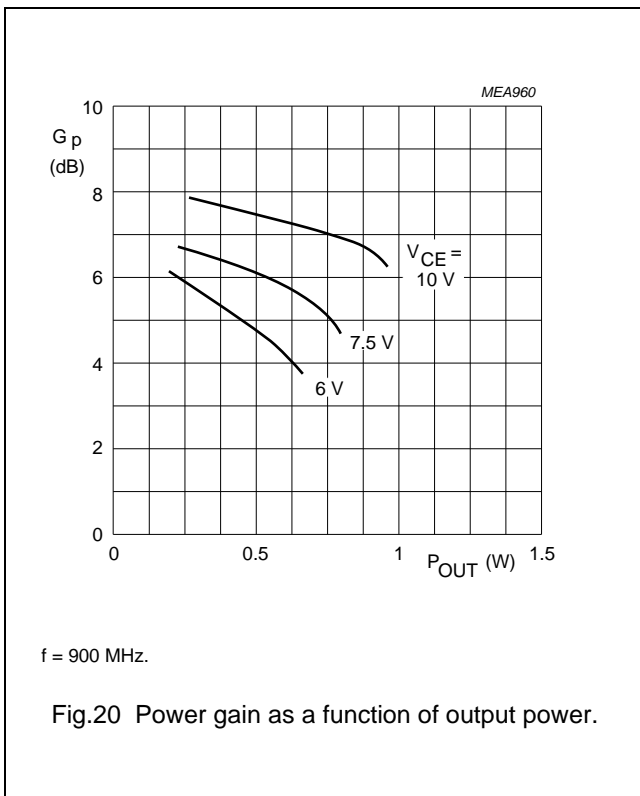
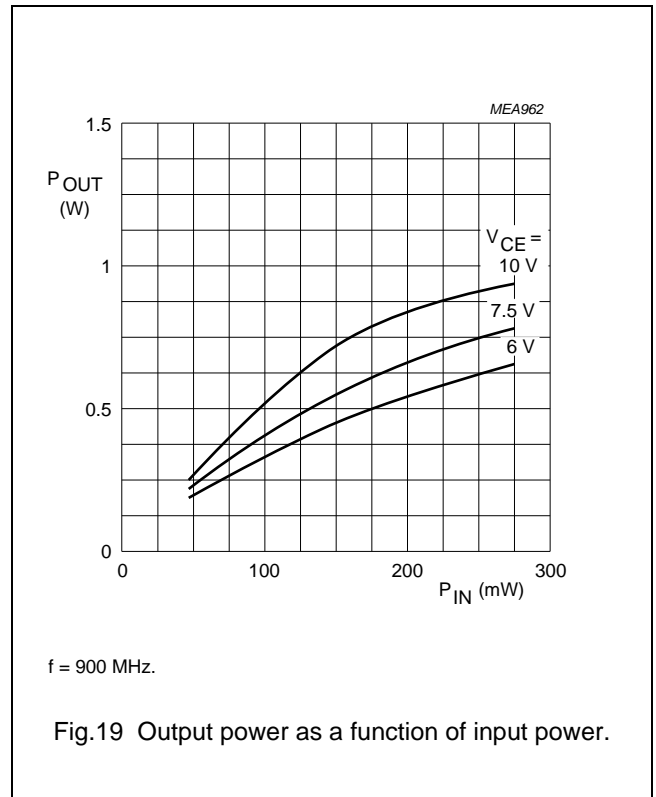
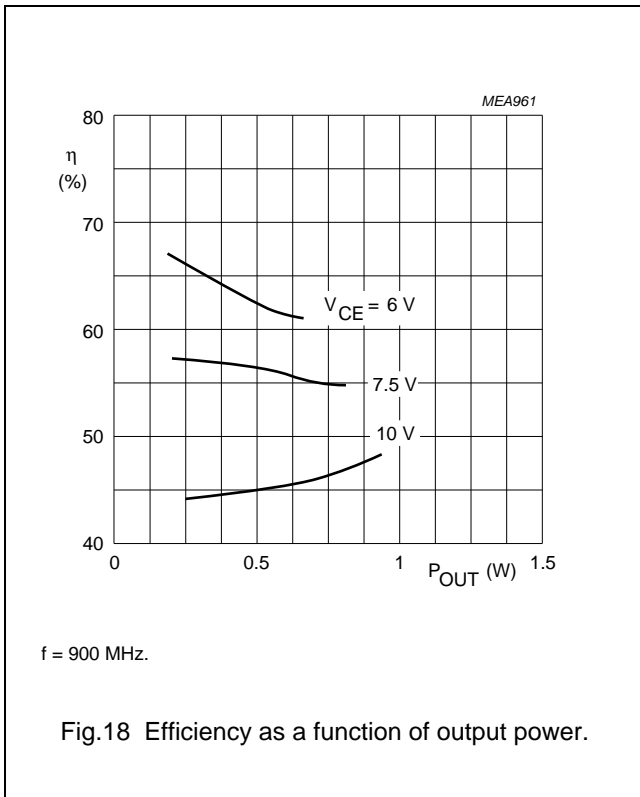
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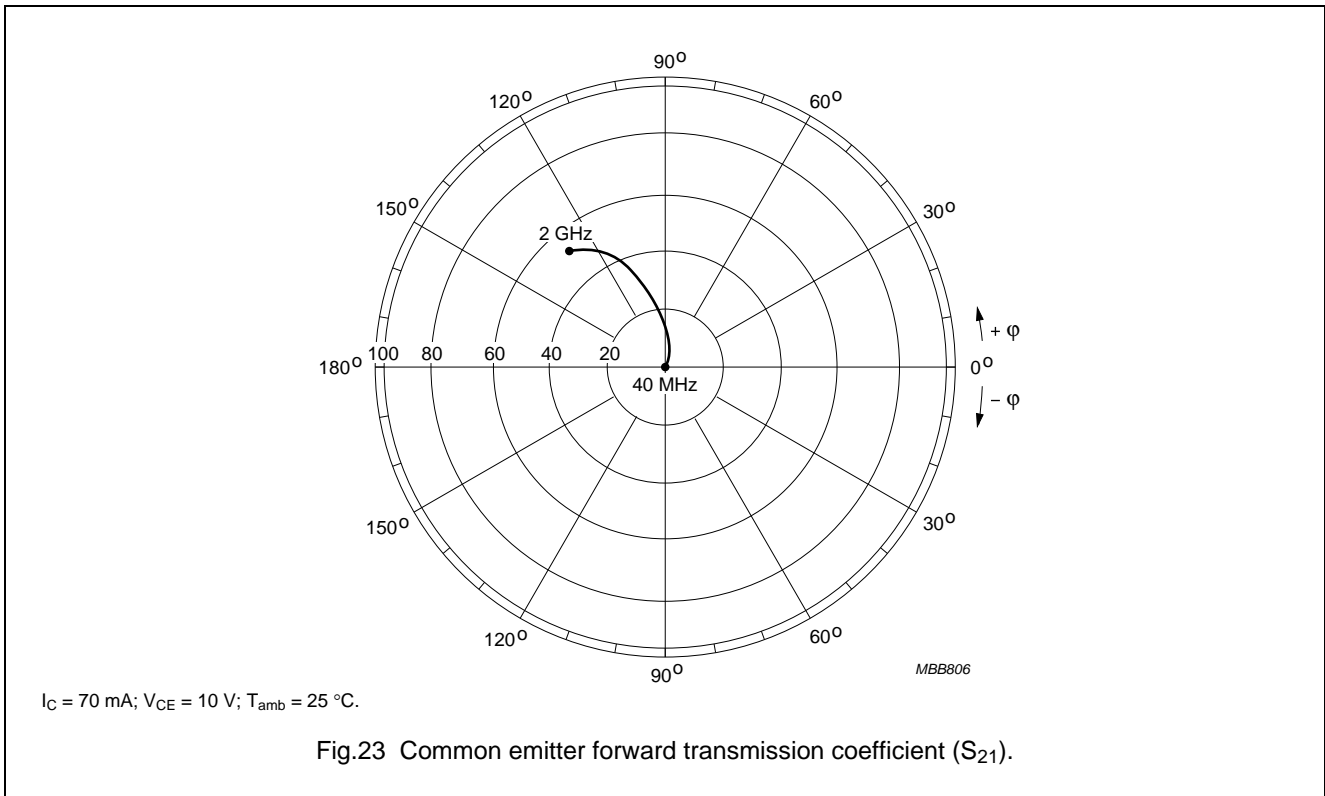
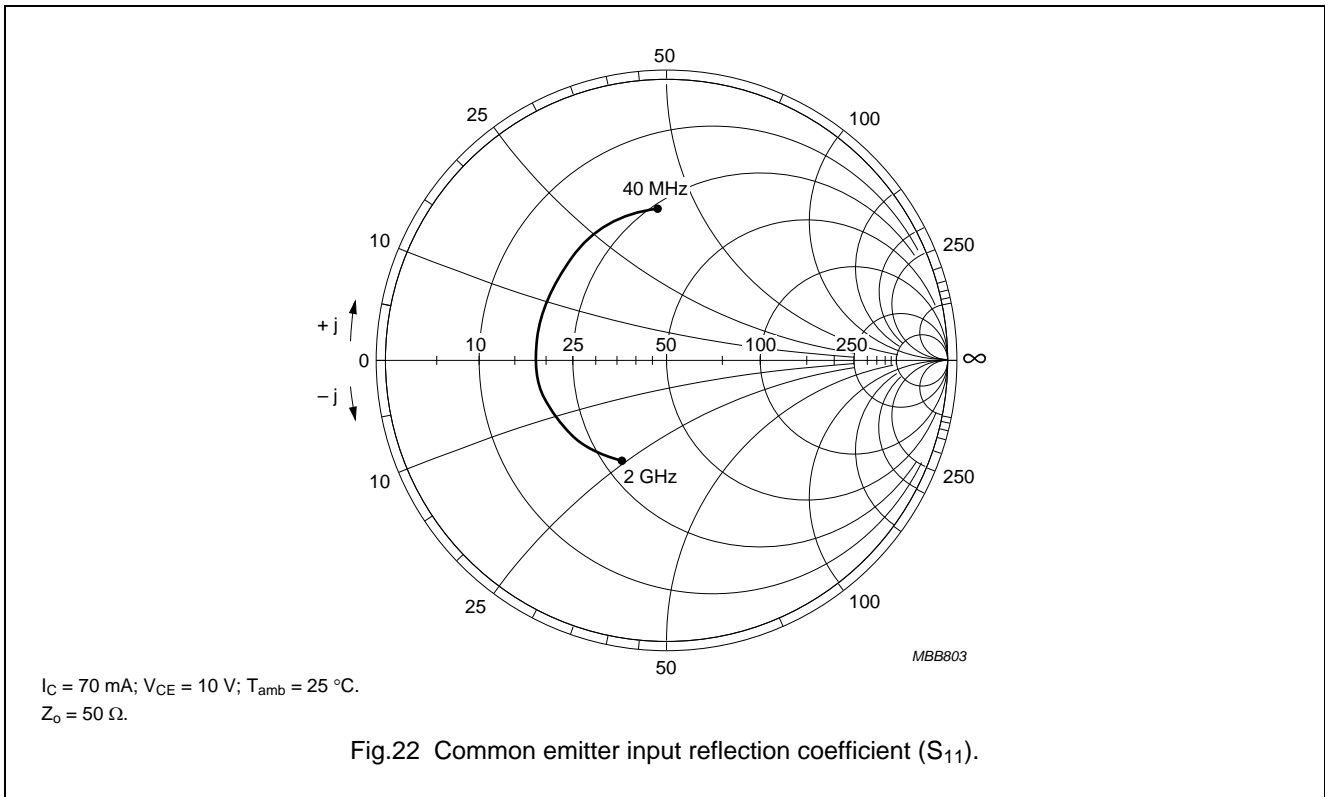
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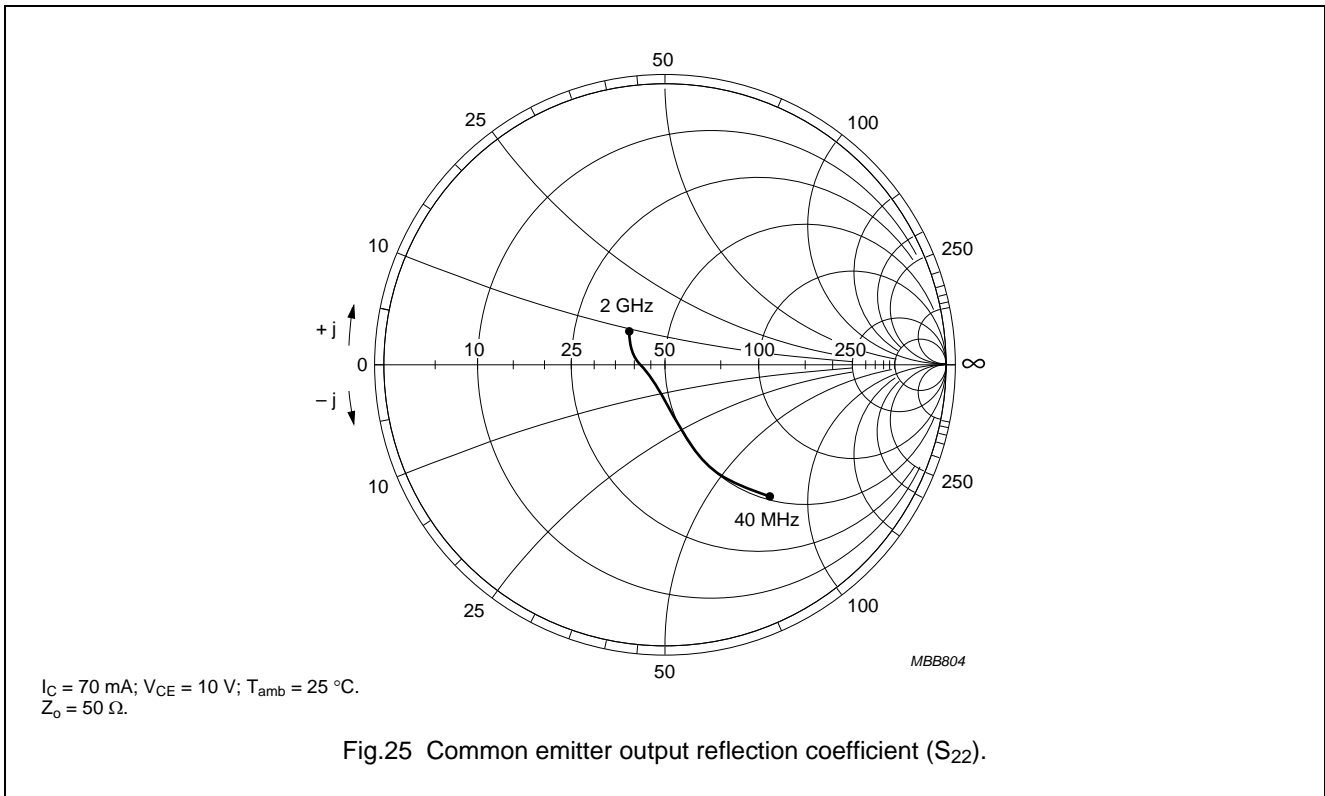
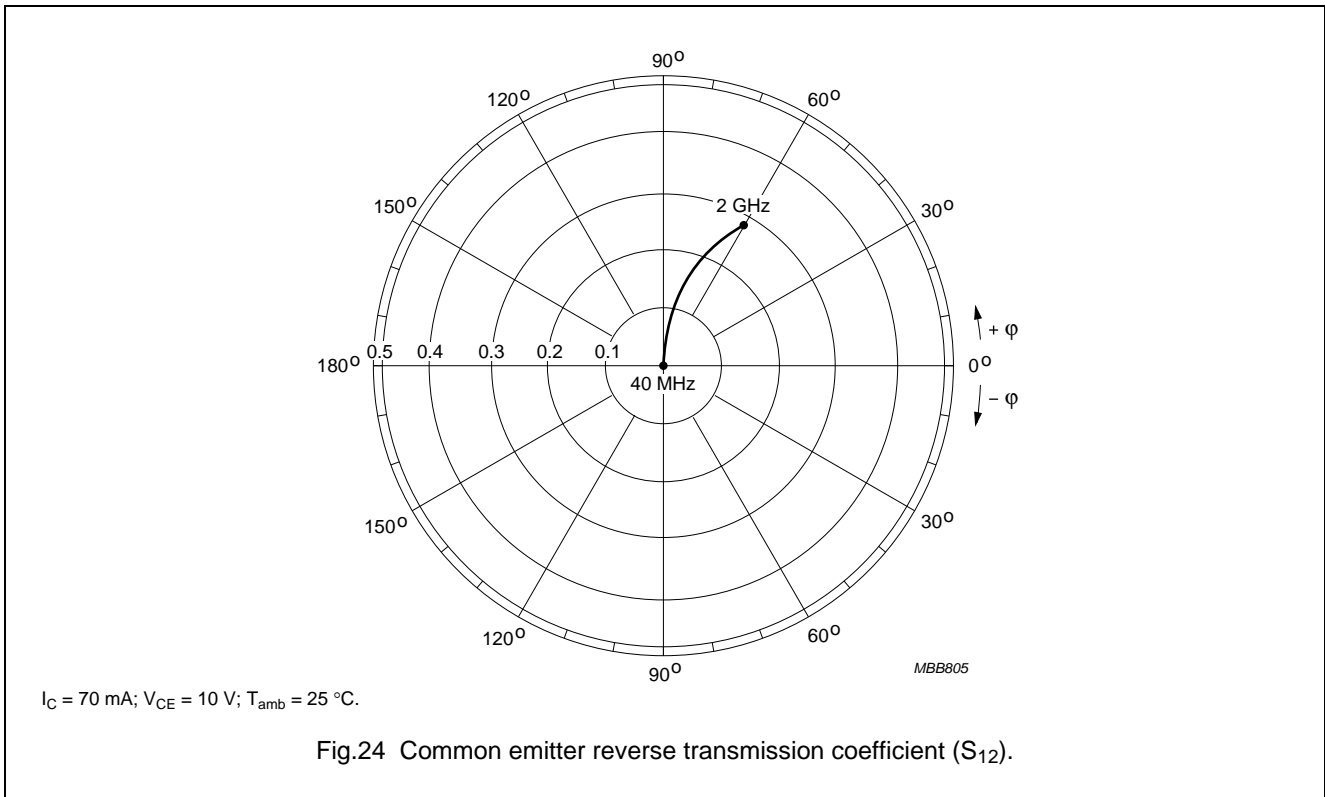
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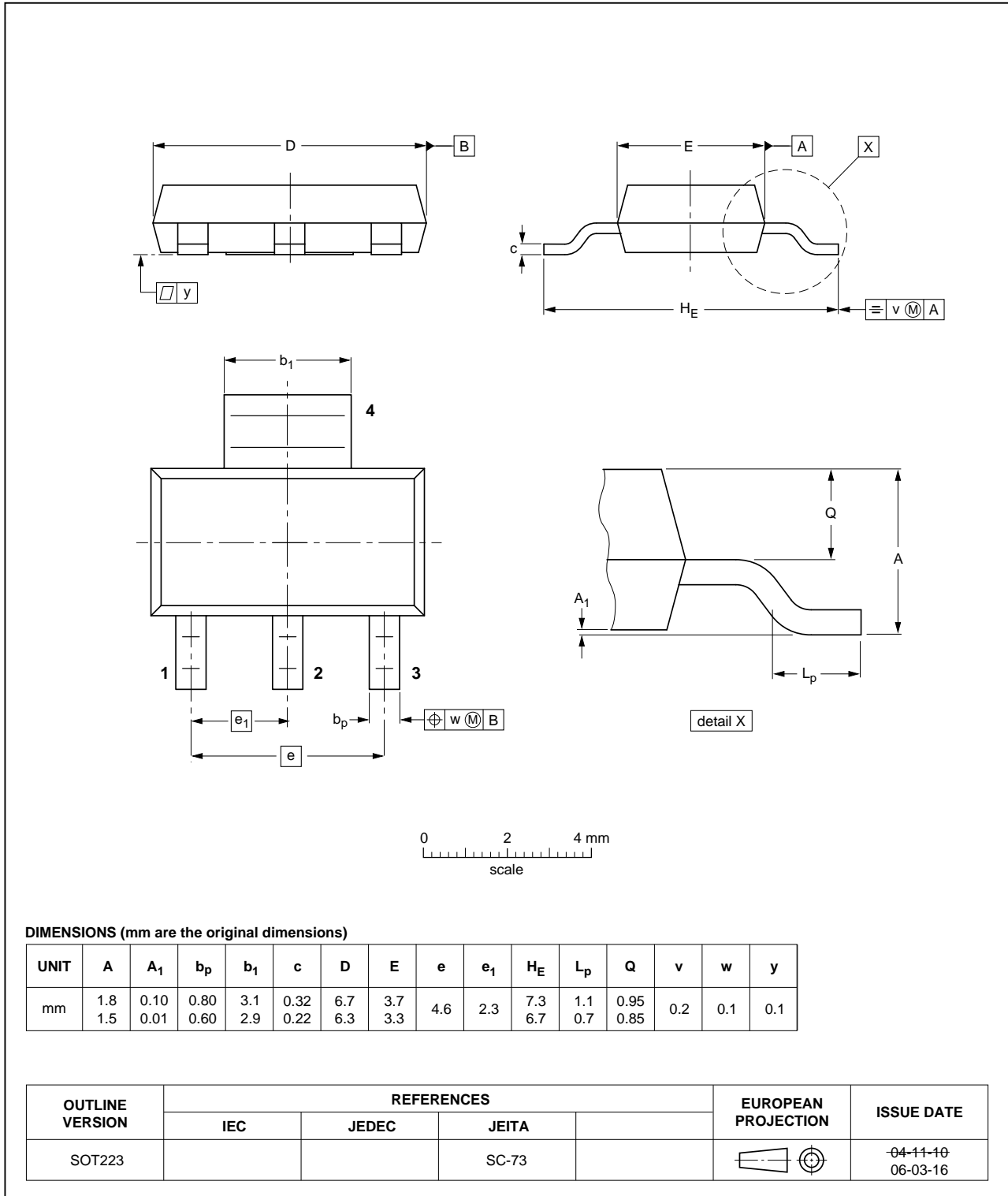
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PACKAGE OUTLINE

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223



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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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