

# DATA SHEET

**BFM520**

Dual NPN wideband transistor

Product specification  
Supersedes data of 1995 Sep 04

1996 Oct 08



# Dual NPN wideband transistor

# BFM520

## FEATURES

- Small size
- Temperature and  $h_{FE}$  matched
- Low noise and high gain
- High gain at low current and low capacitance at low voltage
- Gold metallization ensures excellent reliability.

## APPLICATIONS

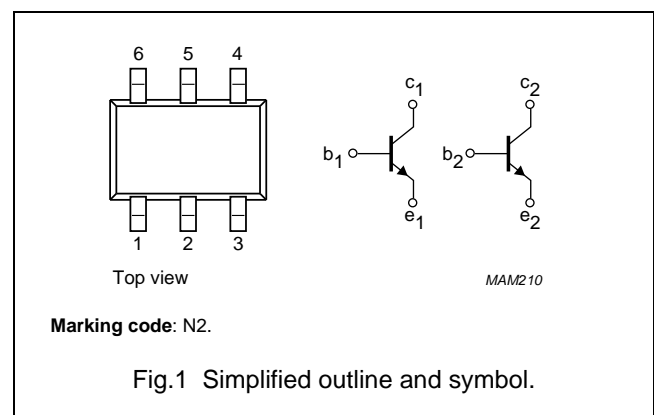
- Oscillator and buffer amplifiers
- Balanced amplifiers
- LNA/mixers.

## DESCRIPTION

Dual transistor with two silicon NPN RF dies in a surface mount 6-pin SOT363 (S-mini) package. The transistor is primarily intended for wideband applications in the GHz-range in the RF front end of analog and digital cellular phones, cordless phones, radar detectors, pagers and satellite TV-tuners.

## PINNING - SOT363A

PIN	SYMBOL	DESCRIPTION
1	b <sub>1</sub>	base 1
2	e <sub>1</sub>	emitter 1
3	c <sub>2</sub>	collector 2
4	b <sub>2</sub>	base 2
5	e <sub>2</sub>	emitter 2
6	c <sub>1</sub>	collector 1



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Any single transistor</b>						
C <sub>re</sub>	feedback capacitance	I <sub>e</sub> = 0; V <sub>CB</sub> = 3 V; f = 1 MHz	–	0.4	–	pF
f <sub>T</sub>	transition frequency	I <sub>C</sub> = 20 mA; V <sub>CE</sub> = 3 V; f = 900 MHz	–	9	–	GHz
S <sub>21</sub>   <sup>2</sup>	insertion power gain	I <sub>C</sub> = 20 mA; V <sub>CE</sub> = 3 V; f = 900 MHz; T <sub>amb</sub> = 25 °C	13	14.5	–	dB
G <sub>UM</sub>	maximum unilateral power gain	I <sub>C</sub> = 20 mA; V <sub>CE</sub> = 3 V; f = 900 MHz; T <sub>amb</sub> = 25 °C	–	15	–	dB
F	noise figure	I <sub>C</sub> = 5 mA; V <sub>CE</sub> = 3 V; f = 900 MHz; Γ <sub>S</sub> = Γ <sub>opt</sub>	–	1.2	1.6	dB
R <sub>th j-s</sub>	thermal resistance from junction to soldering point	single loaded	–	–	230	K/W
		double loaded	–	–	115	K/W

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**LIMITING VALUES**

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Any single transistor</b>					
V <sub>CBO</sub>	collector-base voltage	open emitter	–	20	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	8	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	2.5	V
I <sub>C</sub>	DC collector current		–	70	mA
P <sub>tot</sub>	total power dissipation	up to T <sub>s</sub> = 118 °C; note 1	–	1	W
T <sub>stg</sub>	storage temperature		–65	+175	°C
T <sub>j</sub>	junction temperature		–	175	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-s</sub>	thermal resistance from junction to soldering point; note 1	single loaded	230	K/W
		double loaded	115	K/W

**Note to the Limiting values and Thermal characteristics**

1. T<sub>s</sub> is the temperature at the soldering point of the collector pin.

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## CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>DC characteristics of any single transistor</b>						
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 2.5\ \mu\text{A}; I_E = 0$	20	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 10\ \mu\text{A}; I_B = 0$	8	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	$I_E = 2.5\ \mu\text{A}; I_C = 0$	2.5	–	–	V
$I_{CBO}$	collector-base leakage current	$V_{CB} = 6\ \text{V}; I_E = 0$	–	–	50	nA
$h_{FE}$	DC current gain	$I_C = 20\ \text{mA}; V_{CE} = 6\ \text{V}$	60	120	250	
<b>DC characteristics of the dual transistor</b>						
$\Delta h_{FE}$	ratio of highest and lowest DC current gain	$I_{C1} = I_{C2} = 20\ \text{mA}; V_{CE1} = V_{CE2} = 6\ \text{V}$	1	1.2	–	
$\Delta V_{BEO}$	difference between highest and lowest base-emitter voltage (offset voltage)	$I_{E1} = I_{E2} = 30\ \text{mA}; T_{amb} = 25\text{ °C}$	0	1	–	mV
<b>AC characteristics of any single transistor</b>						
$f_T$	transition frequency	$I_C = 20\ \text{mA}; V_{CE} = 3\ \text{V}; f = 1\ \text{GHz}$	–	9	–	GHz
$C_c$	collector capacitance	$I_E = i_e = 0; V_{CB} = 3\ \text{V}; f = 1\ \text{MHz}$	–	0.5	–	pF
$C_{re}$	feedback capacitance	$I_C = 0; V_{CB} = 3\ \text{V}; f = 1\ \text{MHz}$	–	0.4	–	pF
$G_{UM}$	maximum unilateral power gain; note 1	$I_C = 20\ \text{mA}; V_{CE} = 3\ \text{V}; T_{amb} = 25\text{ °C}; f = 900\ \text{MHz}$	–	15	–	dB
		$I_C = 20\ \text{mA}; V_{CE} = 3\ \text{V}; T_{amb} = 25\text{ °C}; f = 2\ \text{GHz}$	–	9	–	dB
$ S_{21} ^2$	insertion power gain	$I_C = 20\ \text{mA}; V_{CE} = 3\ \text{V}; f = 900\ \text{MHz}; T_{amb} = 25\text{ °C}$	13	14.5	–	dB
F	noise figure	$I_C = 5\ \text{mA}; V_{CE} = 3\ \text{V}; f = 900\ \text{MHz}; \Gamma_S = \Gamma_{opt}$	–	1.2	1.6	dB
		$I_C = 20\ \text{mA}; V_{CE} = 3\ \text{V}; f = 900\ \text{MHz}; \Gamma_S = \Gamma_{opt}$	–	1.7	2.1	dB
		$I_C = 5\ \text{mA}; V_{CE} = 3\ \text{V}; f = 2\ \text{GHz}; \Gamma_S = \Gamma_{opt}$	–	1.9	–	dB

## Note

1.  $G_{UM}$  is the maximum unilateral power gain, assuming  $s_{12}$  is zero.  $G_{UM} = 10 \log \frac{|s_{21}|^2}{(1 - |s_{11}|^2)(1 - |s_{22}|^2)}$  dB

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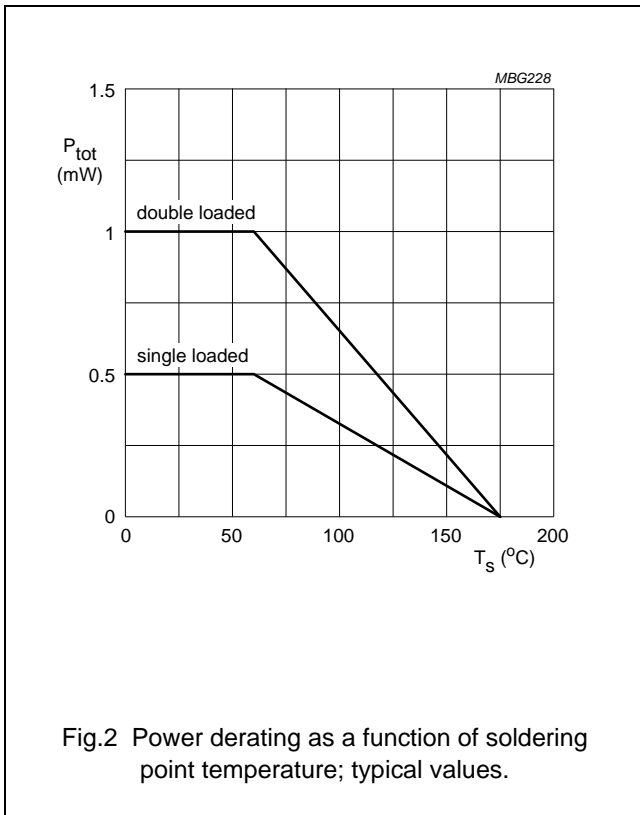
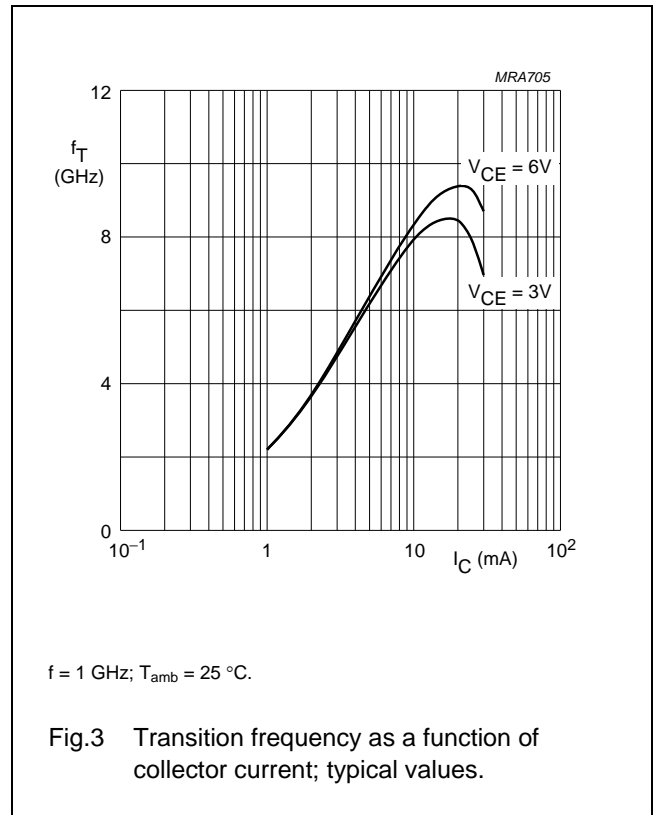
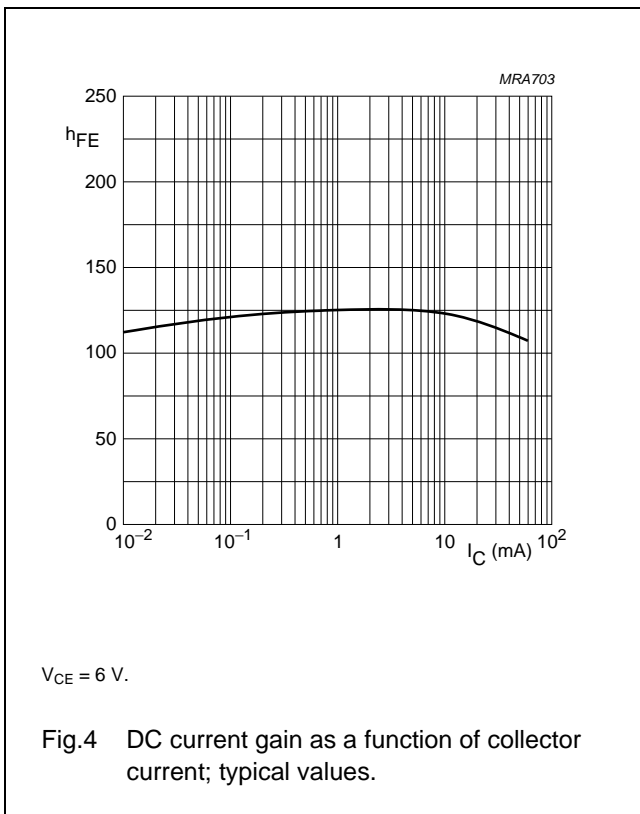


Fig.2 Power derating as a function of soldering point temperature; typical values.



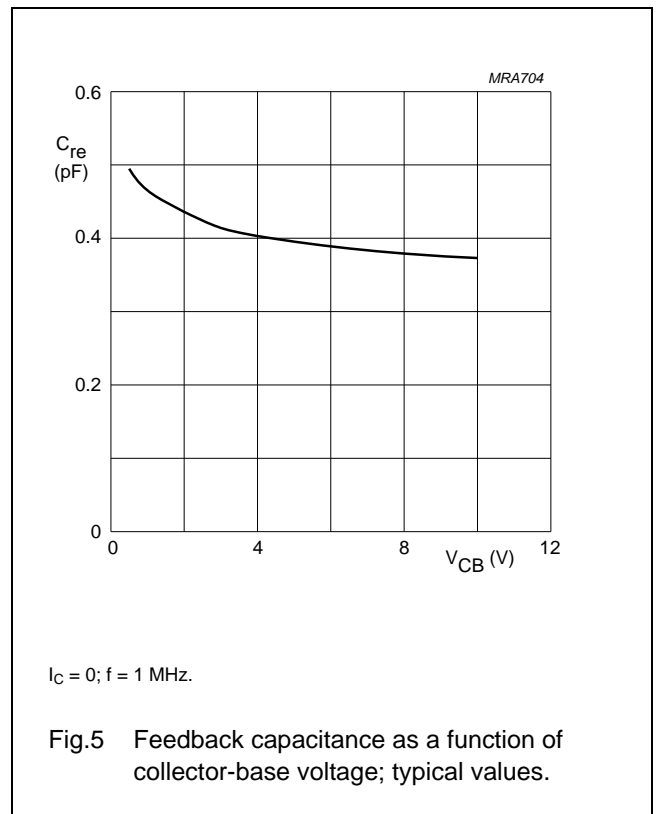
$f = 1 \text{ GHz}; T_{amb} = 25 \text{ }^\circ\text{C}.$

Fig.3 Transition frequency as a function of collector current; typical values.



$V_{CE} = 6 \text{ V}.$

Fig.4 DC current gain as a function of collector current; typical values.

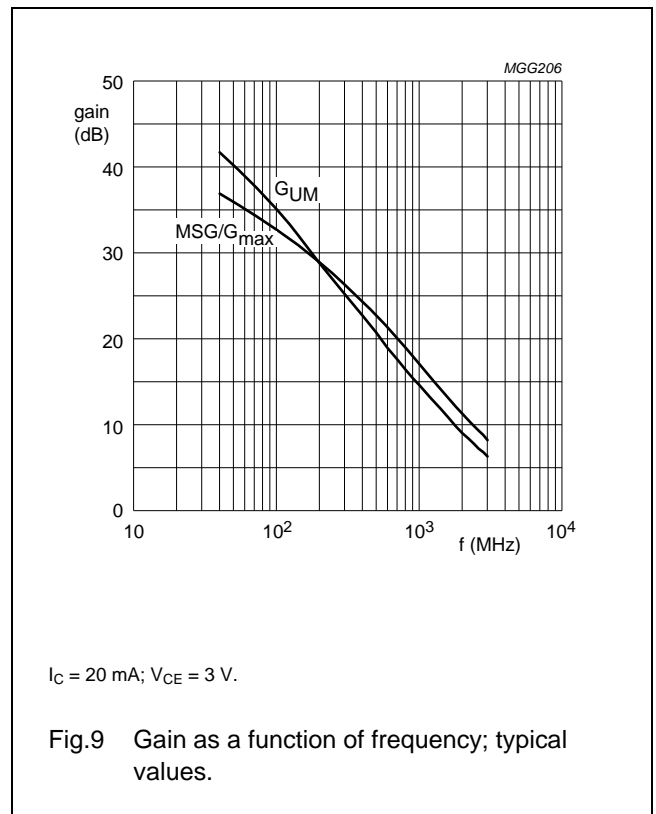
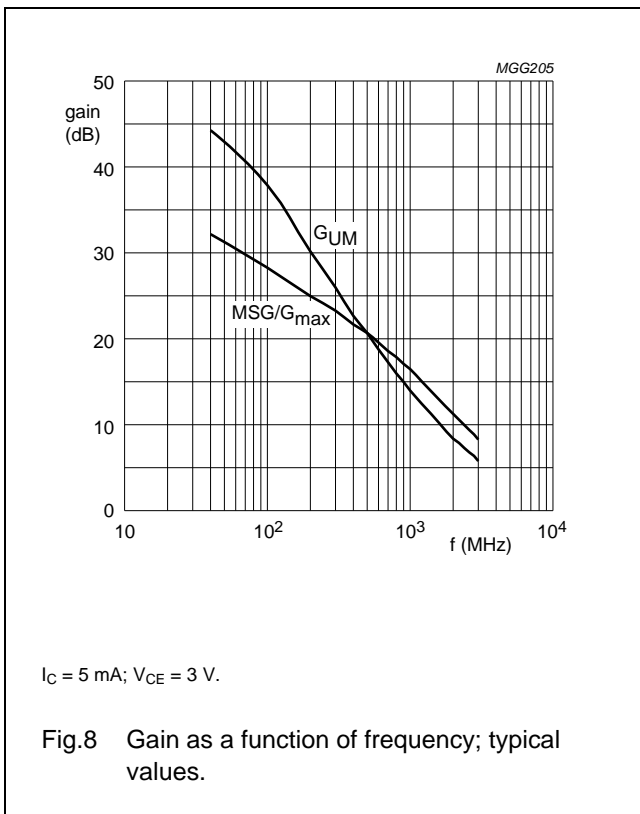
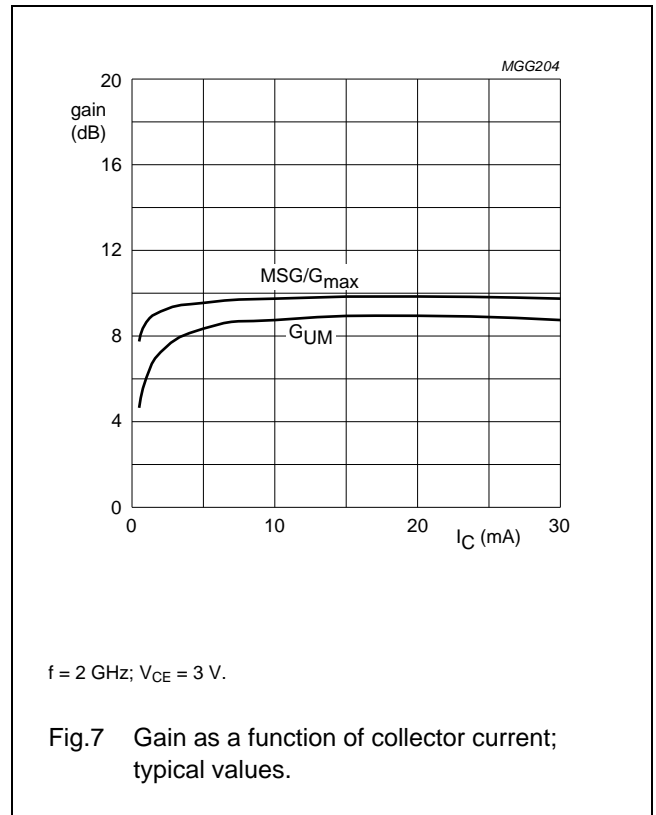
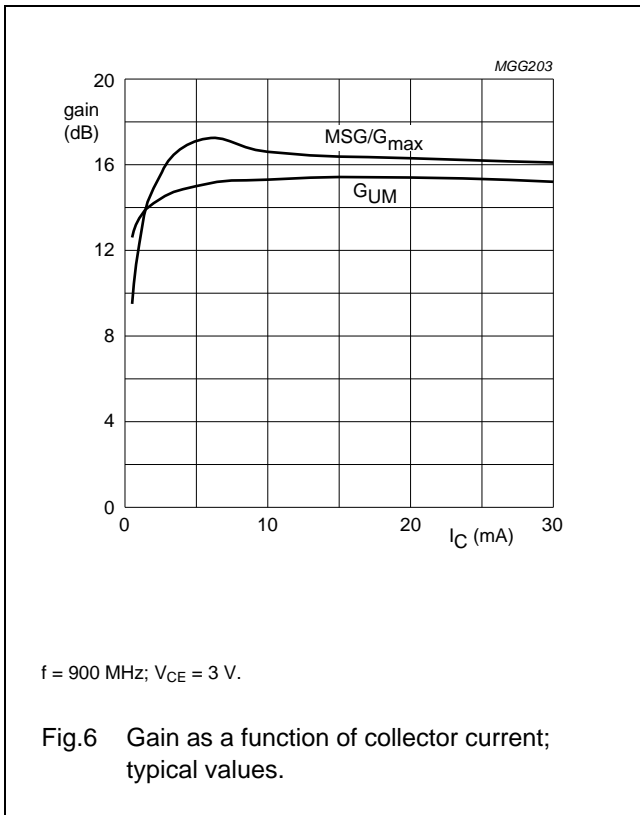


$I_C = 0; f = 1 \text{ MHz}.$

Fig.5 Feedback capacitance as a function of collector-base voltage; typical values.

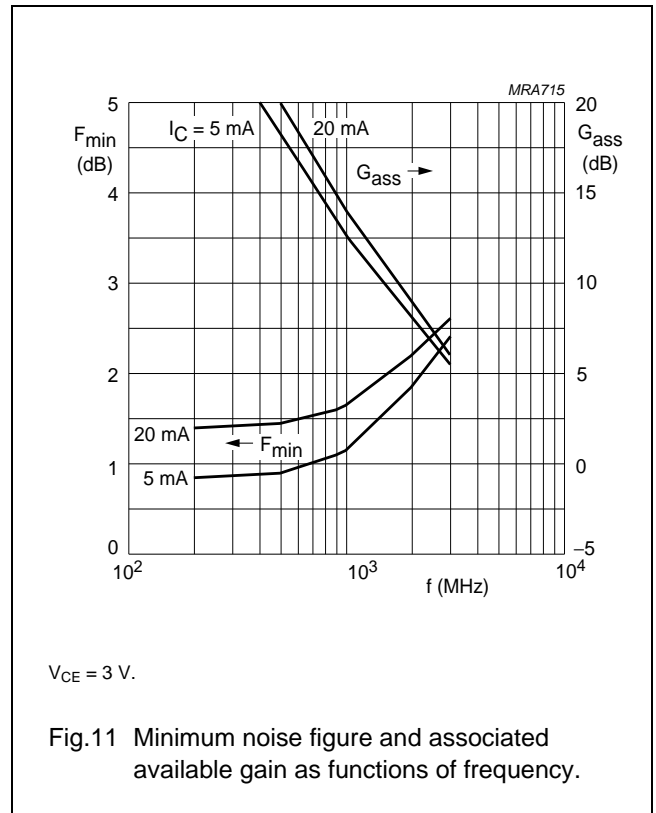
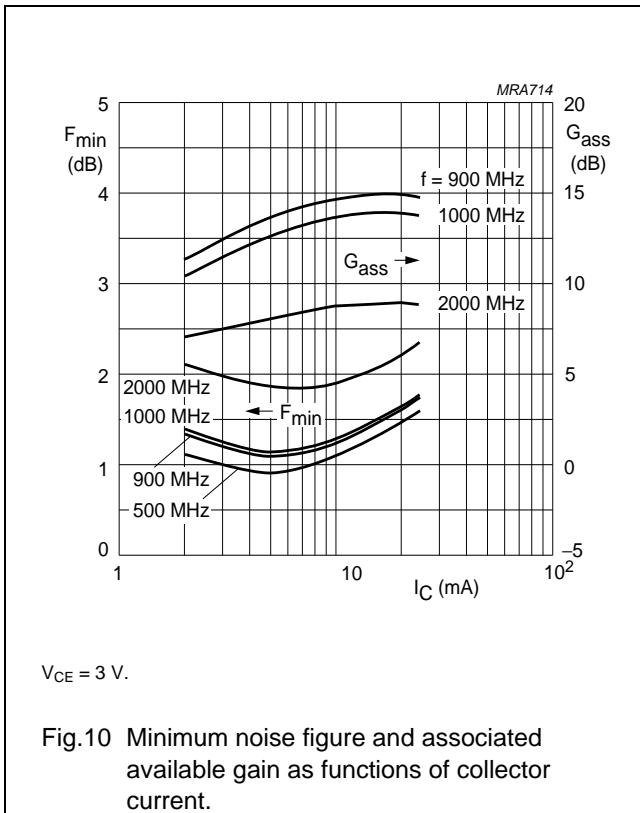
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## APPLICATION INFORMATION

### SPICE parameters for any single BFM520 die

SEQUENCE No.	PARAMETER	VALUE	UNIT
1	IS	1.016	fA
2	BF	220.1	–
3	NF	1.000	–
4	VAF	48.06	V
5	IKF	510.0	mA
6	ISE	283.0	fA
7	NE	2.035	–
8	BR	100.7	–
9	NR	0.988	–
10	VAR	1.692	V
11	IKR	2.352	mA
12	ISC	24.48	aA
13	NC	1.022	–
14	RB	10.00	Ω
15	IRB	1.000	μA
16	RBM	10.00	Ω
17	RE	0.775	Ω
18	RC	2.210	Ω
19 <sup>(1)</sup>	XTB	0.000	–
20 <sup>(1)</sup>	EG	1.110	eV
21 <sup>(1)</sup>	XTI	3.000	–
22	CJE	1.245	pF
23	VJE	600.0	mV
24	MJE	0.258	–
25	TF	8.616	ps
26	XTF	6.788	–
27	VTF	1.414	V
28	ITF	110.3	mA
29	PTF	45.01	deg
30	CJC	447.6	fF
31	VJC	189.2	mV
32	MJC	0.071	–
33	XCJC	0.130	–
34	TR	543.7	ps
35 <sup>(1)</sup>	CJS	0.000	F
36 <sup>(1)</sup>	VJS	750.0	mV
37 <sup>(1)</sup>	MJS	0.000	–
38	FC	0.780	–

**Note**

1. These parameters have not been extracted, the default values are shown.

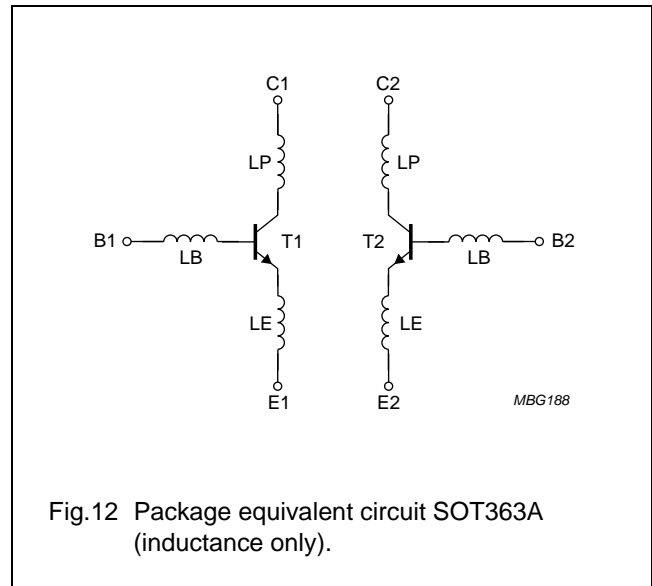


Fig.12 Package equivalent circuit SOT363A (inductance only).

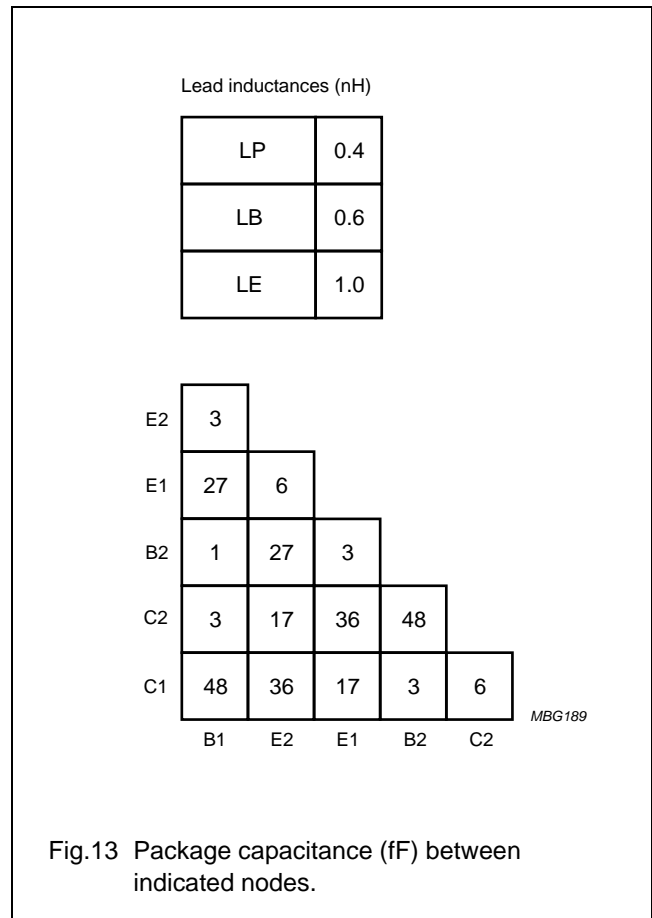


Fig.13 Package capacitance (fF) between indicated nodes.

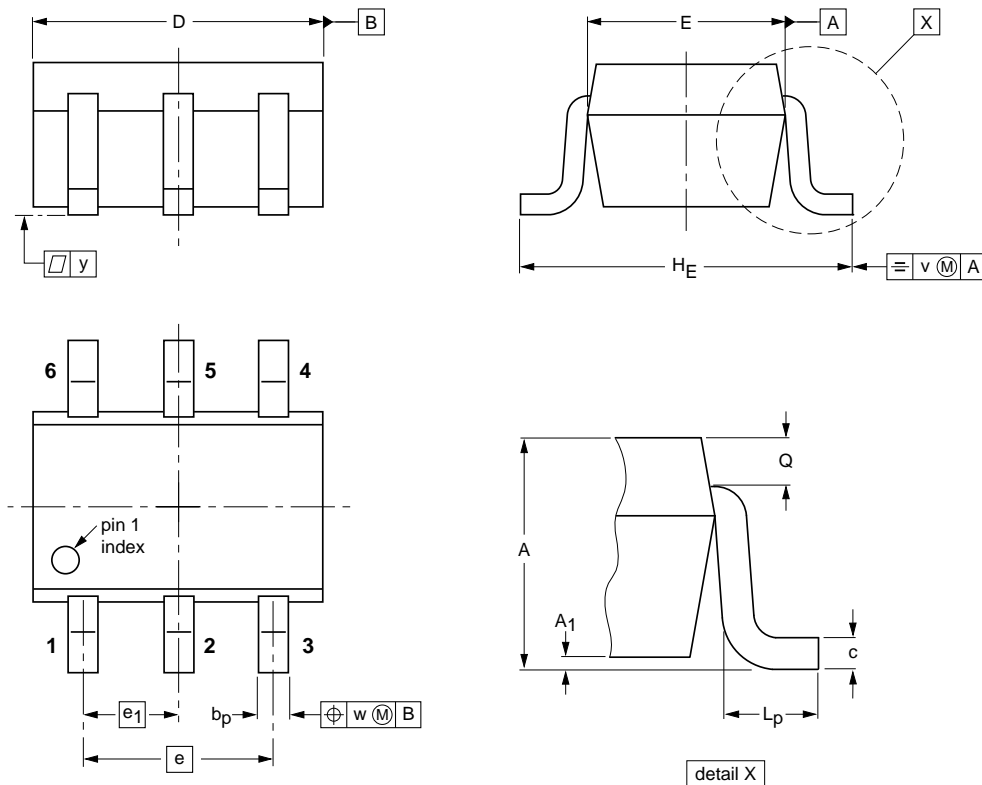
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PACKAGE OUTLINE

Plastic surface-mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			04-11-08 06-03-16

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## DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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