



**THE DATASHEET OF  
SG2843DM-TR**



# Current Mode PWM Controller

## Description

The SG1842/43 family of control IC's provides all the necessary features to implement off-line fixed frequency, current-mode switching power supplies with a minimum number of external components.

Current-mode architecture demonstrates improved line regulation, improved load regulation, pulse-by-pulse current limiting and inherent protection of the power supply output switch. The bandgap reference is trimmed to  $\pm 1\%$  over temperature.

Oscillator discharge current is trimmed to less than  $\pm 10\%$ . The SG1842/43 has under-voltage lockout, current limiting circuitry and start-up current of less than 1mA. The totem-pole output is optimized to drive the gate of a power MOSFET. The output is low in the off state to provide direct interface to an N-channel device. The SG1842/43 is specified for operation over the full military ambient temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SG2842/43 is specified for the industrial range of  $-25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , and the SG3842/43 is designed for the commercial range of  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

## Features

- Optimized For Off-Line Control
- Low Start-Up Current ( $<1\text{mA}$ )
- Automatic Feed Forward Compensation
- Trimmed Oscillator Discharge Current
- Pulse-By-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout with 6V Hysteresis (SG1842 only)
- Double-Pulse Suppression
- High-Current Totem-Pole Output (1A Peak)
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Undervoltage Lockout  
SG1842 - 16 volts  
SG1843 - 8.4 volts
- Low Shoot-Through Current  $<75\text{mA}$  Over Temperature

## Application

- Available To MIL-STD – 883, ¶ 1.2.1
- Available to DSCC  
- Standard Microcircuit Drawing (SMD)

## Product Highlight

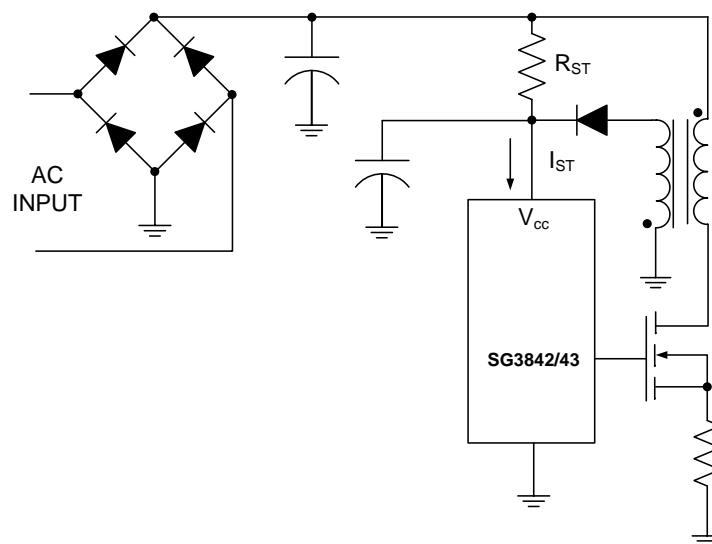
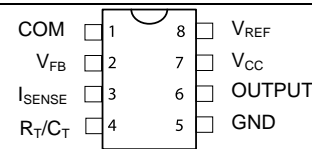
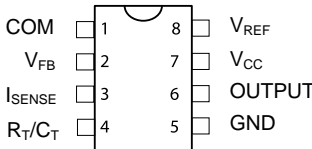
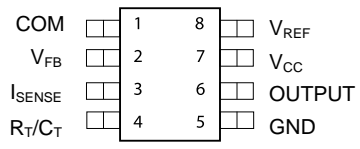
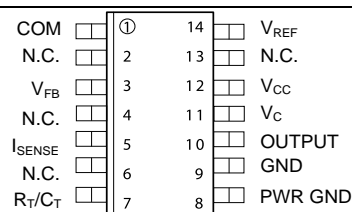
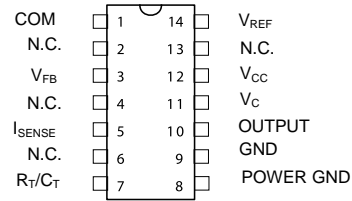


Figure 1 - Product Highlight

## Connection Diagrams and Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
0°C to 70°C	M	8-PIN PLASTIC DUAL INLINE PACKAGE	SG3842M	Plastic DIP	 <p><b>M PACKAGE</b> (Top View)</p> <p><b>M Package:</b> RoHS / Pb-free 100% Matte Tin Lead Finish</p>
-25°C to 85°C			SG3843M		
			SG2842M		
			SG2843M		
0°C to 70°C	Y	8-PIN CERAMIC DUAL INLINE PACKAGE	SG3842Y	CERDIP	 <p><b>Y PACKAGE</b> (Top View)</p> <p><b>PbSn Tin Lead Finish</b></p>
-25°C to 85°C			SG3843Y		
-55°C to 125°C			SG2842Y		
MIL-STD/883			SG2843Y		
DESC			SG1842Y		
			SG1843Y		
			SG1842Y-883B		
			SG1843Y-883B		
	SG1842Y-DESC				
	SG1843Y-DESC				
0°C to 70°C	DM	8-PIN SMALL OUTLINE INTEGRATED CIRCUIT	SG3842DM	SOIC	 <p><b>DM PACKAGE</b> (Top View)</p> <p><b>RoHS / Pb-free 100% Matte Tin Lead Finish</b></p>
-25°C to 85°C			SG3843DM		
			SG2842DM		
			SG2843DM		
0°C to 70°C	D	14-PIN SMALL OUTLINE INTEGRATED CIRCUIT	SG3842D	SOIC	 <p><b>D PACKAGE</b> (Top View)</p> <p><b>RoHS / Pb-free 100% Matte Tin Lead Finish</b></p>
-25°C to 85°C			SG3843D		
			SG2842D		
			SG2843D		
0°C to 70°C	N	14-PIN DUAL INLINE PLASTIC PACKAGE	SG3842N	PLASTIC DIP	 <p><b>N PACKAGE</b> (Top View)</p> <p><b>N Package:</b> RoHS / Pb-free 100% Matte Tin Lead Finish</p>
-25°C to 85°C			SG3843N		
			SG2842N		
			SG2843N		

## Connection Diagrams and Ordering Information (continued)

Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
-55°C to 125°C	J	14-PIN CERAMIC DUAL INLINE PACKAGE	SG1842J	CERDIP	<p><b>J PACKAGE</b> (Top View) PbSn Lead Finish</p>
			SG1843J		
MIL-STD/883			SG1842J-883B		
			SG1843J-883B		
DESC			SG1842J-DESC		
			SG1843J-DESC		
-55°C to 125°C	F	10-PIN CERAMIC FLAT PACK PACKAGE	SG1842F	FLAT PACK	<p><b>F PACKAGE</b> (Top View) PbSn Lead Finish</p>
			SG1843F		
MIL-STD/883			SG1842F-883B		
			SG1843F-883B		
DESC			SG1842F-DESC		
			SG1843F-DESC		
-55°C to 125°C	L	20-PIN CERAMIC	SG1842L	Ceramic Leadless Chip Carrier (LCC)	<p><b>L PACKAGE</b> (Top View) PbSn Lead Finish</p>
			SG1843L		
MIL-STD/883			SG1842L-883B		
			SG1843L-883B		
DESC			SG1842L-DESC		
			SG1843L-DESC		

**Notes:**

1. Contact factory for JAN and DESC part availability.
2. All parts are viewed from the top.
3. Available in Tape & Reel. Append the letters "TR" to the part number (SG3842N-TR).

## Absolute Maximum Ratings<sup>1 - 2</sup>

Parameter	Value	Units
Supply Voltage ( $I_{CC} < 30\text{mA}$ )	Self-limiting	V
Supply Voltage (Low Impedance Source)	30	V
Output Current (Peak)	$\pm 1$	A
Output Current (Continuous)	350	mA
Output Energy (Capacitive Load)	5	$\mu\text{J}$
Analog Inputs ( $V_{FB}$ , $I_{SENSE}$ )	-0.3 to +6.3	V
Error Amplifier Output Sink Current	10	mA
Power Dissipation at $T_A = 25^\circ\text{C}$ (DIL-8)	1	W
<b>Operating Junction Temperature</b>		
Hermetic (J, Y, F, L Packages)	150	$^\circ\text{C}$
Plastic (N, M, D, DM Packages)	150	$^\circ\text{C}$
Storage Temperature Range	-65 to +150	$^\circ\text{C}$
Lead Temperature (Soldering, 10 Seconds)	300	$^\circ\text{C}$
RoHS / Pb-free Peak Package Solder Reflow Temp. (40 second max. exposure)	260 (+0, -5)	$^\circ\text{C}$
<i>Notes:</i>		
1. Exceeding these ratings could cause damage to the device.		
2. All voltages are with respect to Pin 5. All currents are positive into the specified terminal.		

## Thermal Data

Parameter	Value	Units
<b>M Package:</b>		
Thermal Resistance-Junction to Ambient, $\theta_{JA}$	95	$^\circ\text{C/W}$
<b>N Package:</b>		
Thermal Resistance-Junction to Ambient, $\theta_{JA}$	65	$^\circ\text{C/W}$
<b>DM Package:</b>		
Thermal Resistance-Junction to Ambient, $\theta_{JA}$	165	$^\circ\text{C/W}$
<b>D Package:</b>		
Thermal Resistance-Junction to Ambient, $\theta_{JA}$	120	$^\circ\text{C/W}$
<b>Y Package:</b>		
Thermal Resistance-Junction to Ambient, $\theta_{JA}$	130	$^\circ\text{C/W}$
<b>J Package</b>		
Thermal Resistance-Junction to Ambient, $\theta_{JA}$	80	$^\circ\text{C/W}$
<b>F Package</b>		
Thermal Resistance-Junction to Case, $\theta_{JC}$	80	$^\circ\text{C/W}$
Thermal Resistance-Junction to Ambient, $\theta_{JA}$	145	$^\circ\text{C/W}$
<b>L Package</b>		
Thermal Resistance-Junction to Case, $\theta_{JC}$	35	$^\circ\text{C/W}$
Thermal Resistance-Junction to Ambient, $\theta_{JA}$	120	$^\circ\text{C/W}$
<i>Notes:</i>		
1. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$ .		
2. The $\theta_{JA}$ numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.		

## Recommended Operating Conditions

Symbol	Parameter	Recommended Operating Conditions			Units
		Min	Typ	Max	
V <sub>S</sub>	Supply Voltage Range		30		V
I <sub>PK</sub>	Output Current (Peak)		±1		A
I <sub>OUT</sub>	Output Current (Continuous)		200		mA
	Analog Inputs (V <sub>FB</sub> , I <sub>SENSE</sub> )	0		2.6	V
E <sub>ASINK</sub>	Error Amp Output Sink Current		5		mA
OSC <sub>FR</sub>	Oscillator Frequency Range	0.1		500	kHz
R <sub>T</sub>	Oscillator Timing Resistor	0.52		150	kΩ
C <sub>T</sub>	Oscillator Timing Capacitor	0.001		1.0	μF
<b>Operating Ambient Temperature Range</b>					
	SG1842/43	-55		125	°C
	SG2842/43	-25		85	°C
	SG3842/43	0		70	°C
<i>Note: Range over which the device is functional.</i>					

## Electrical Characteristics

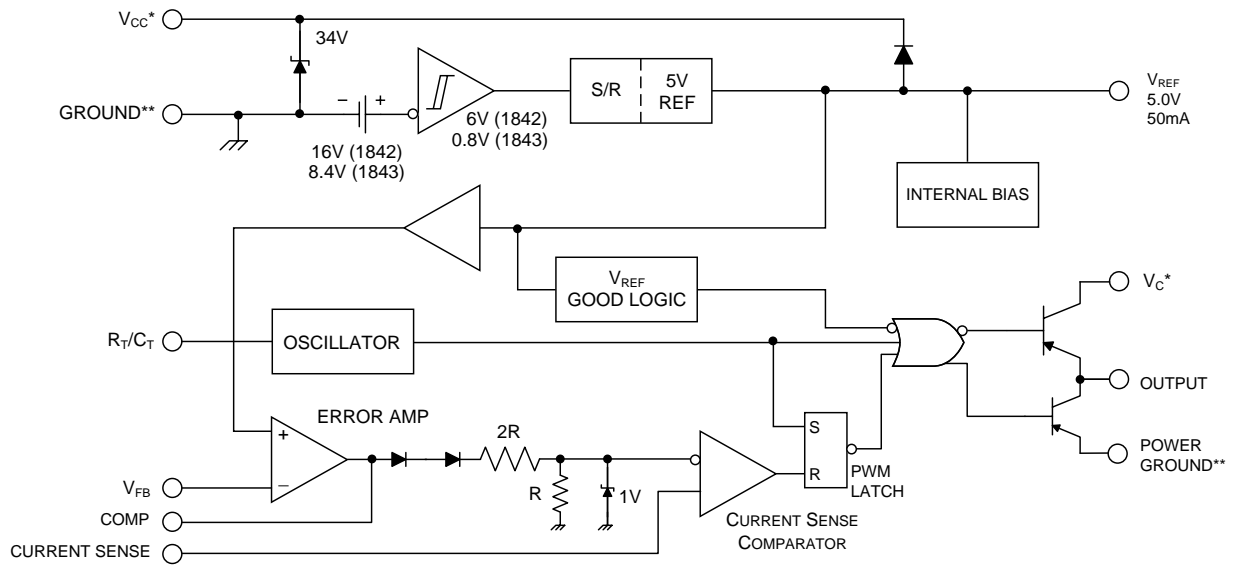
Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1842/SG1843 with  $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , SG2842/SG2843 with  $-25^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , SG3842/SG3843 with  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $V_{CC} = 15\text{V}$ ,  $R_T = 10\text{k}\Omega$ , and  $C_T = 3.3\text{nF}$ . Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Symbol	Parameter	Test Conditions	SG1842/43			SG2842/43			SG3842/43			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>Reference Section</b>												
$V_{REF}$	Output Voltage	$T_J = 25^{\circ}\text{C}$ , $I_O = 1\text{mA}$	4.95	5.00	5.05	4.95	5.00	5.05	4.90	5.00	5.10	V
$V_{REG}$	Line Regulation	$12\text{V} \leq V_{IN} \leq 25\text{V}$		6	20		6	20		6	20	mV
$I_{REG}$	Load Regulation	$1 \leq I_O \leq 20\text{mA}$		6	25		6	25		6	25	mV
	Temperature Stability <sup>1</sup>			0.2	0.4		0.2	0.4		0.2	0.4	mV/ $^{\circ}\text{C}$
	Total Output Variation <sup>1</sup>	Line, Load, Temperature	4.90		5.10	4.90		5.10	4.82		5.18	V
$V_N$	Output Noise Voltage <sup>1</sup>	$10\text{Hz} \leq f \leq 10\text{kHz}$ , $T_J = 25^{\circ}\text{C}$		50			50			50		$\mu\text{V}$
	Long Term Stability <sup>1</sup>	$T_A = 125^{\circ}\text{C}$ , 1000hrs		5	25		5	25		5	25	mV
$V_{REFOSC}$	Output Short Circuit		-30	-100	-180	-30	-100	-180	-30	-100	-180	mA
<b>Oscillator Section<sup>3</sup></b>												
f	Initial Accuracy <sup>5</sup>	$T_J = 25^{\circ}\text{C}$	47	52	57	47	52	57	47	52	57	kHz
$f_{REG}$	Voltage Stability	$12\text{V} \leq V_{CC} \leq 25\text{V}$		0.2	1		0.2	1		0.2	1	%
	Temperature Stability <sup>1</sup>	$T_{MIN} \leq T_A \leq T_{MAX}$		5			5			5		%
$OSC_{PP}$	Amplitude	$V_{RT/CT}$ (Peak to Peak)		1.7			1.7			1.7		V
$I_{DSG}$	Discharge Current	$T_J = 25^{\circ}\text{C}$	7.8	8.3	8.8	7.5	8.4	9.3	7.5	8.4	9.3	mA
		$T_{MIN} \leq T_A \leq T_{MAX}$	7.0		9.0	7.2		9.5	7.2		9.5	mA
<b>Error Amp Section</b>												
$EA_{IN}$	Input Voltage	$V_{COMP} = 2.5\text{V}$	2.45	2.50	2.55	2.45	2.50	2.55	2.42	2.50	2.58	V
$EA_{IB}$	Input Bias Current			-0.3	-1		-0.3	1		-0.3	-2	$\mu\text{A}$
$A_{VOL}$	Open Loop Gain	$2\text{V} \leq V_O \leq 4\text{V}$	65	90		65	90		65	90		dB
$EA_{BW}$	Unity Gain Bandwidth <sup>1</sup>	$T_J = 25^{\circ}\text{C}$	0.7	1		0.7	1		0.7	1		MHz
PSRR	Power Supply Rejection Ratio	$12\text{V} \leq V_{CC} \leq 25\text{V}$	60	70		60	70		60	70		dB
$EA_{SINK}$	Output Sink Current	$V_{VFB} = 2.7\text{V}$ , $V_{COMP} = 1.1\text{V}$	2	6		2	6		2	6		mA
$EA_{SRC}$	Output Source Current	$V_{VFB} = 2.3\text{V}$ , $V_{COMP} = 5\text{V}$	-0.5	-0.8		-0.5	-0.8		-0.5	-0.8		mA
$EA_{VOH}$	$V_{OUT}$ High	$V_{VFB} = 2.3\text{V}$ , $R_L = 15\text{k to GND}$	5	6		5	6		5	6		V
$EA_{VOL}$	$V_{OUT}$ Low	$V_{VFB} = 2.7\text{V}$ , $R_L = 15\text{k to } V_{REF}$		0.7	1.1		0.7	1.1		0.7	1.1	V

## Electrical Characteristics (continued)

Symbol	Parameter	Test Conditions	SG1842/43			SG2842/43			SG3842/43			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>Current Sense Section</b>												
CS <sub>AVOL</sub>	Gain <sup>2,3</sup>		2.85	3	3.15	2.85	3	3.15	2.85	3	3.15	V/V
	Maximum Input Signal <sup>2</sup>	V <sub>COMP</sub> = 5V	0.9	1	1.1	0.9	1	1.1	0.9	1	1.1	V
PSRR	Power Supply Rejection Ratio <sup>2</sup>	12V ≤ V <sub>CC</sub> ≤ 25V		70			70			70		dB
CS <sub>IB</sub>	Input Bias Current			-2	-10		-2	-10		-2	-10	μA
CS <sub>DELAY</sub>	Delay to Output <sup>1</sup>			150	300		150	300		150	300	ns
<b>Output Section</b>												
V <sub>OL</sub>	Output Low Level	I <sub>SINK</sub> = 20mA		0.1	0.4		0.1	0.4		0.1	0.4	V
		I <sub>SINK</sub> = 200mA		1.5	2.2		1.5	2.2		1.5	2.2	V
V <sub>OH</sub>	Output High Level	I <sub>SOURCE</sub> = 20mA	13	13.5		13	13.5		13	13.5		V
		I <sub>SOURCE</sub> = 200mA	12	13.5		12	13.5		12	13.5		V
R <sub>S</sub>	Rise Time	T <sub>J</sub> = 25°C, C <sub>L</sub> = 1nF		50	150		50	150		50	150	ns
F <sub>T</sub>	Fall Time	T <sub>J</sub> = 25°C, C <sub>L</sub> = 1nF		50	150		50	150		50	150	ns
<b>Under-Voltage Lockout Section</b>												
UVLO	Start Threshold	1842/2842/3842	15	16	17	15	16	17	14.5	16	17.5	V
		1843/2843/3843	7.8	8.4	9.0	7.8	8.4	9.0	7.8	8.4	9.0	V
V <sub>SMIN</sub>	Min. Operation Voltage After Turn-On	1842/2842/3842	9	10	11	9	10	11	8.5	10	11.5	V
		1843/2843/3843	7.0	7.6	8.3	7.0	7.6	8.2	7.0	7.6	8.2	V
<b>PWM Section</b>												
DC <sub>MAX</sub>	Maximum Duty Cycle		93	95	100	90	95	100	90	95	100	%
DC <sub>MIN</sub>	Minimum Duty Cycle				0			0			0	%
<b>Power Consumption Section</b>												
I <sub>S</sub>	Start-Up Current			0.5	1		0.5	1		0.5	1	mA
I	Operating Supply Current	V <sub>FB</sub> = V <sub>ISENSE</sub> = 0V		11	17		11	17		11	17	mA
Z	V <sub>CC</sub> Zener Voltage	I <sub>CC</sub> = 25mA		34			34			34		V
<b>Notes:</b> 1. These parameters, although guaranteed, are not 100% tested in production. 2. Parameter measured at trip point of latch with V <sub>VFB</sub> = 0. 3. Gain defined as: $A = \Delta V_{COMP} / \Delta V_{ISENSE}$ ; $0 \leq V_{ISENSE} \leq 0.8V$ 4. Adjust V <sub>CC</sub> above the start threshold before setting at 15V.												

## Block Diagram

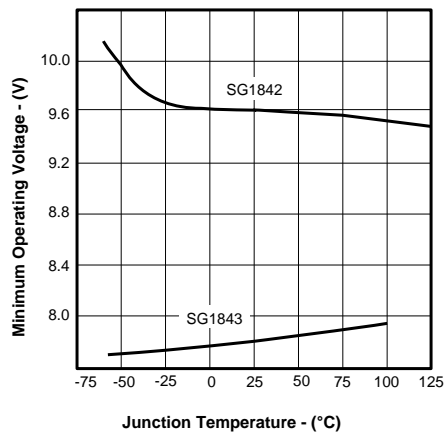


\* -  $V_{CC}$  and  $V_C$  are internally connected for 8-pin packages.

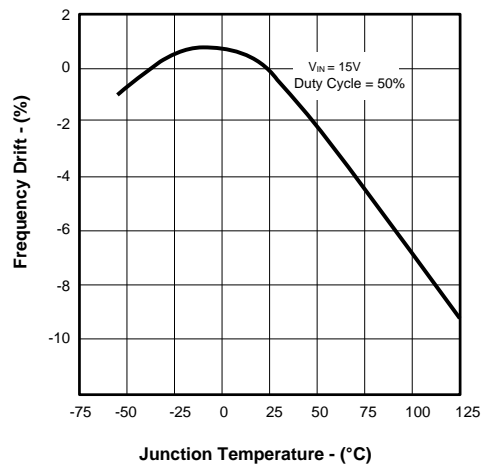
\*\* -  $POWER\ GROUND$  and  $GROUND$  are internally connected for 8-pin packages.

**Figure 2 - Block Diagram**

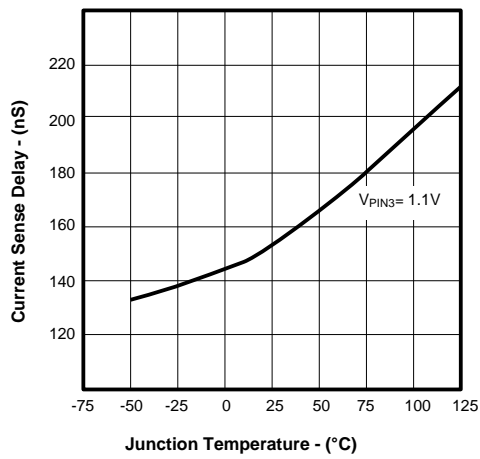
## Characteristic Curves



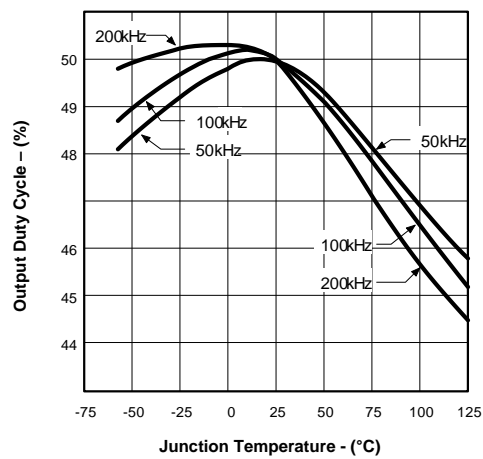
**Figure 3** - Dropout Voltage vs. Temperature



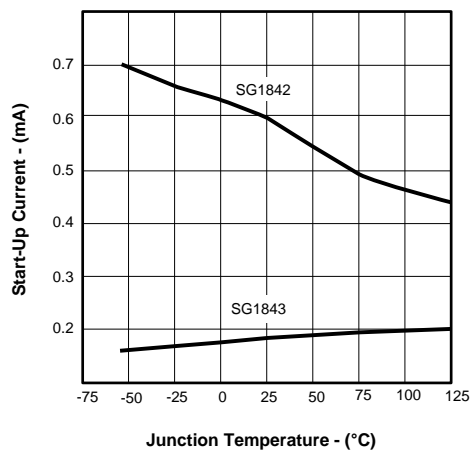
**Figure 4** - Oscillator Temperature Stability



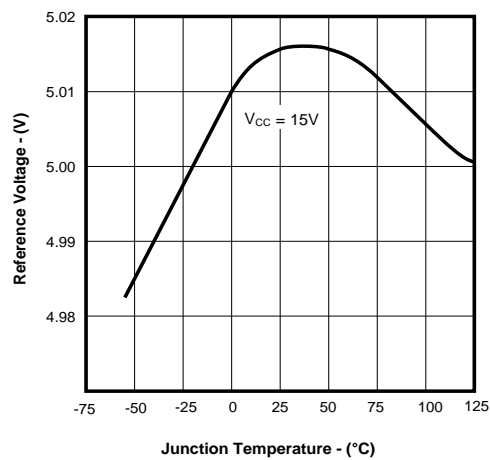
**Figure 5** - Current Sense to Output Delay vs. Temperature



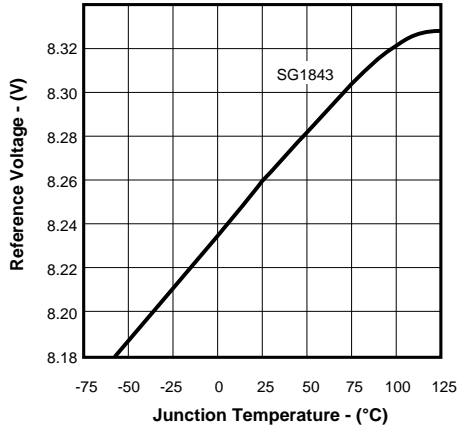
**Figure 6** - Output Duty Cycle vs. Temperature



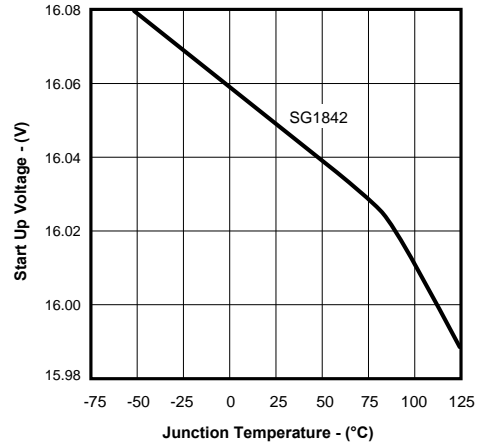
**Figure 7** - Start-Up Current vs. Temperature



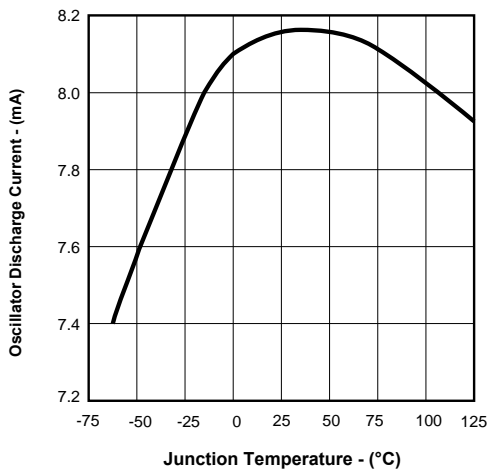
**Figure 8** - Reference Voltage vs. Temperature



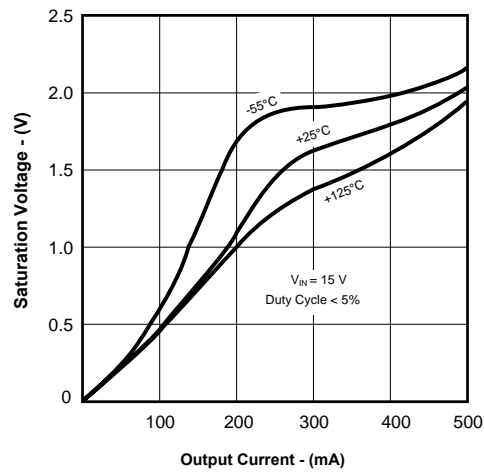
**Figure 9** - Start-Up Voltage Threshold vs. Temperature



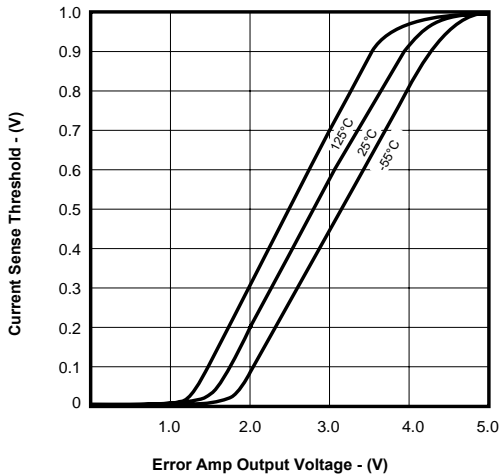
**Figure 10** - Start-Up Voltage Threshold vs. Temperature



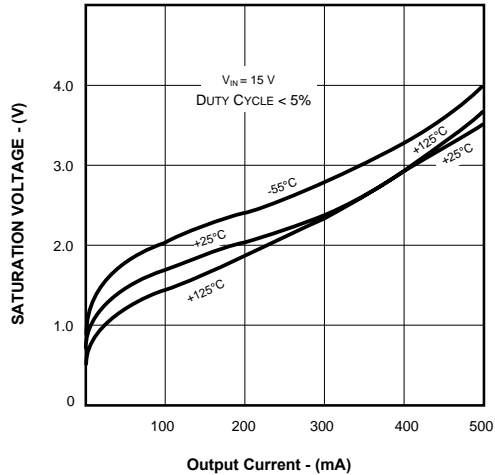
**Figure 11** - Oscillator Discharge Current vs. Temperature



**Figure 12** - Output Saturation Voltage vs. Output Current and Temperature (Sink Transistor)



**Figure 13** - Current Sense Threshold vs. Error Amplifier Output



**Figure 14** - Output Saturation Voltage vs. Output Current and Temperature

## Application Information

The oscillator of the 1842/43 family of PWM's is designed such that many values of  $R_T$  and  $C_T$  will give the same oscillator frequency, but only one combination will yield a specific duty cycle at a given frequency.

**Given:**

Frequency  $\equiv f$

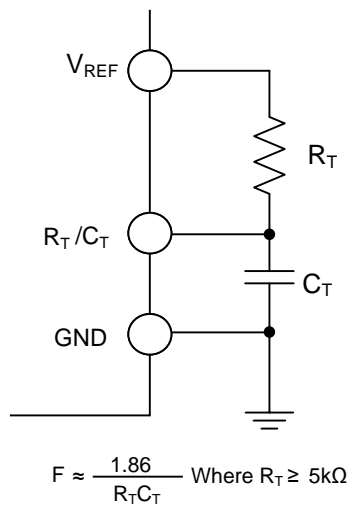
Maximum Duty Cycle  $\equiv D_m$

**Calculate:**  $R_T = 267 \left[ \frac{(1.76)^{1/D_m - 1}}{(1.76)^{(1 - D_m)/D_m - 1}} \right] (\Omega)$

where  $0.3 < D_m < 0.95$

$$C_T = \frac{1.86 * D_m}{f * R_T} (\mu F)$$

For Duty-Cycles above 95% use:



**Figure 15** - Oscillator Timing Circuit

A set of formulas are given to determine the values of  $R_T$  and  $C_T$  for a given frequency and maximum duty cycle. (Note: These formulas are less accurate for smaller duty cycles or higher frequencies. This will require trimming of  $R_T$  or  $C_T$  to correct for this error.)

**Example:**

A Flyback power supply requires a maximum of 45% duty cycle at a switching frequency of 50 kHz. What are the values of  $R_T$  and  $C_T$ ?

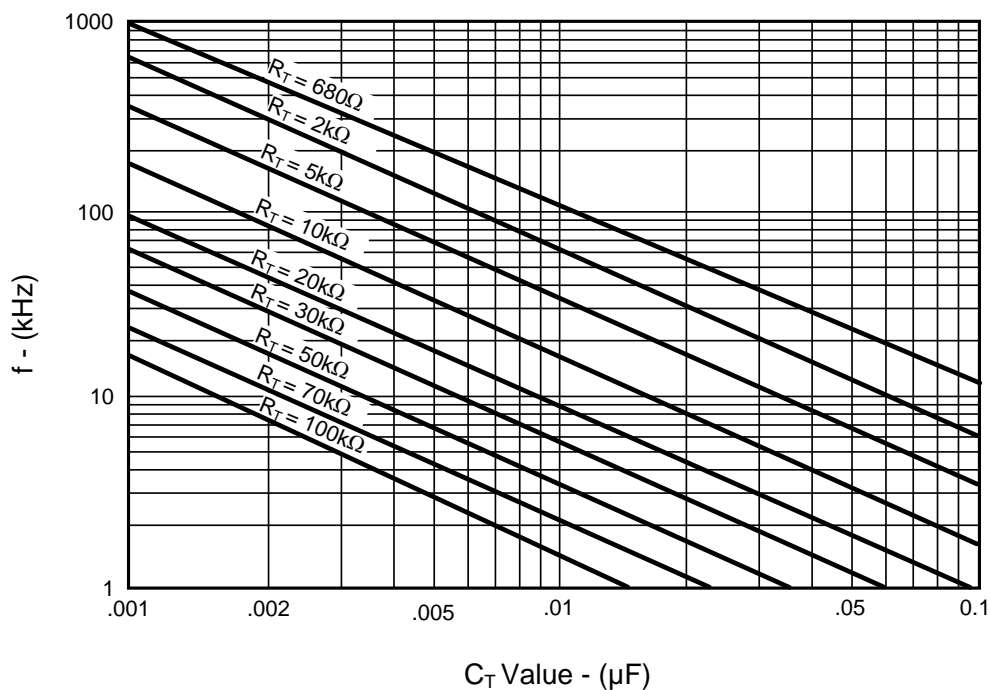
**Given:**

$f = 50\text{kHz}$

$D_m = 0.45$

**Calculate:**  $R_T = 267 \left[ \frac{(1.76)^{\frac{1}{.55}} - 1}{(1.76)^{.45} - 1} \right] = 674 \Omega$

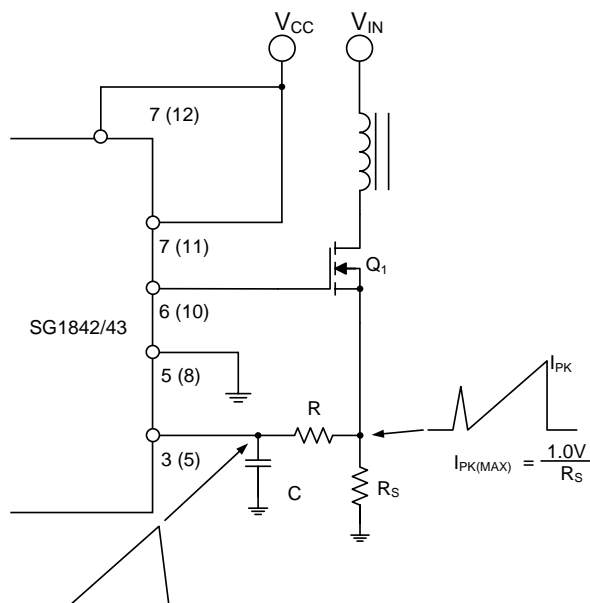
$C_T = \frac{1.86 * 0.45}{50000 * 674} = .025 (\mu\text{F})$



**Figure 16** - Oscillator Frequency Vs.  $R_T$  For Various  $C_T$

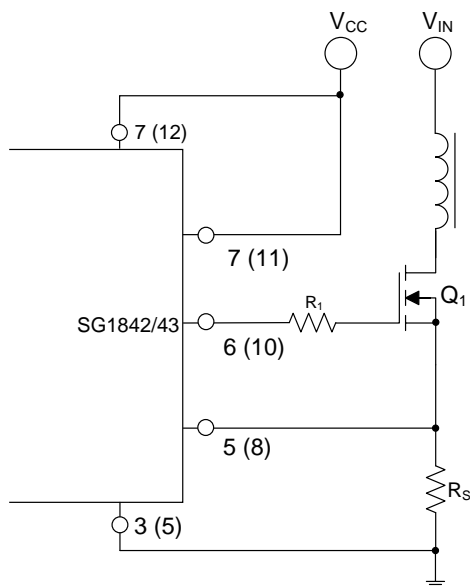
## Typical Application Circuits

Pin numbers referenced are for 8-pin package and pin numbers in parenthesis are for 14-pin package.



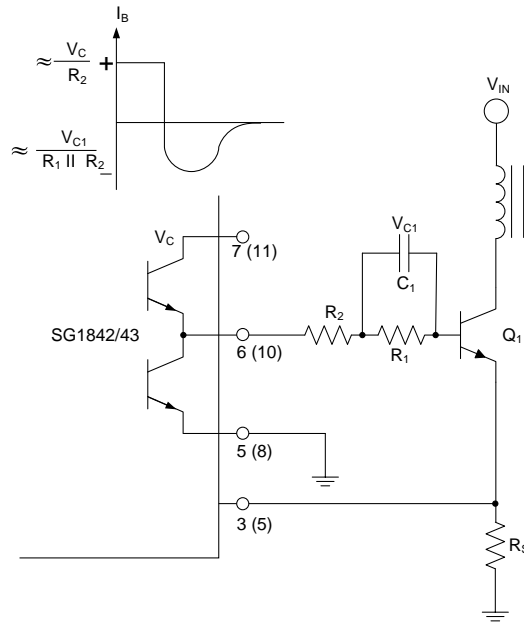
**Figure 17** • Current Sense Spike Suppression

The RC low-pass filter eliminates the leading edge current spike caused by parasitic of Power MOSFET.



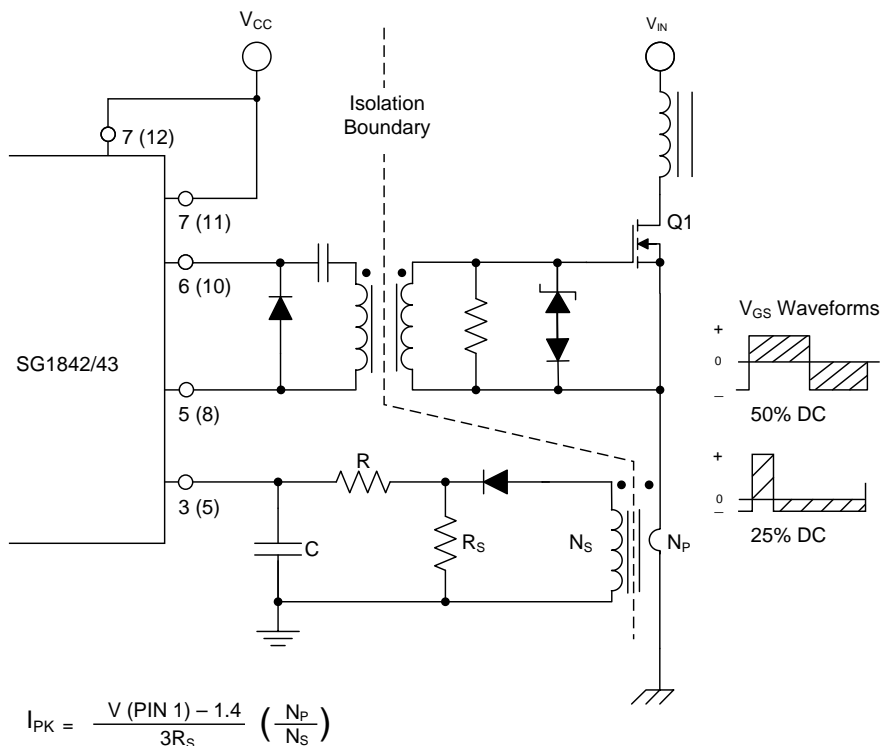
**Figure 18** • MOSFET Parasitic Oscillations

A resistor (R1) in series with the MOSFET gate reduce overshoot and ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)



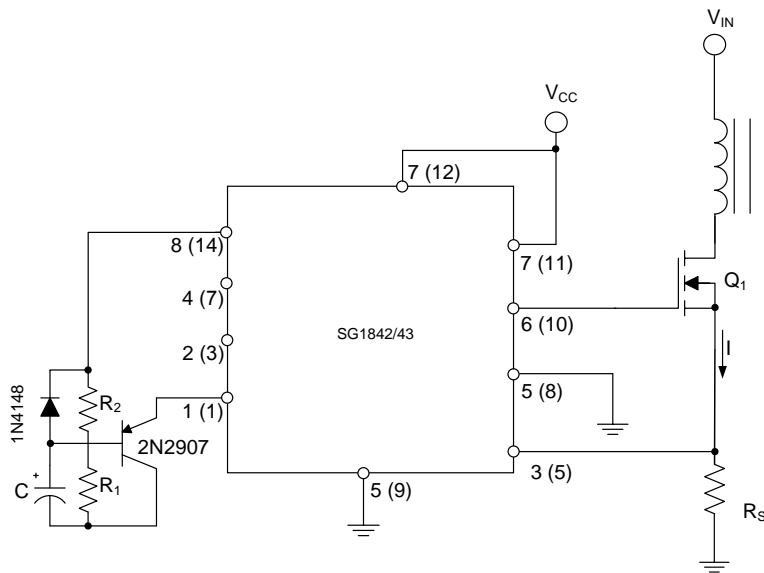
**Figure 19 - Bipolar Transistor Drive**

The 1842/43 output stage can provide negative base current to remove base charge of power transistor ( $Q_1$ ) for faster turn off. This is accomplished by adding a capacitor ( $C_1$ ) in parallel with a resistor ( $R_1$ ). The resistor ( $R_1$ ) is to limit the base current during turn on.



**Figure 20 - Isolated MOSFET Drive**

Current transformers can be used where isolation is required between PWM and Primary ground. A drive transformer is then necessary to interface the PWM output with the MOSFET.



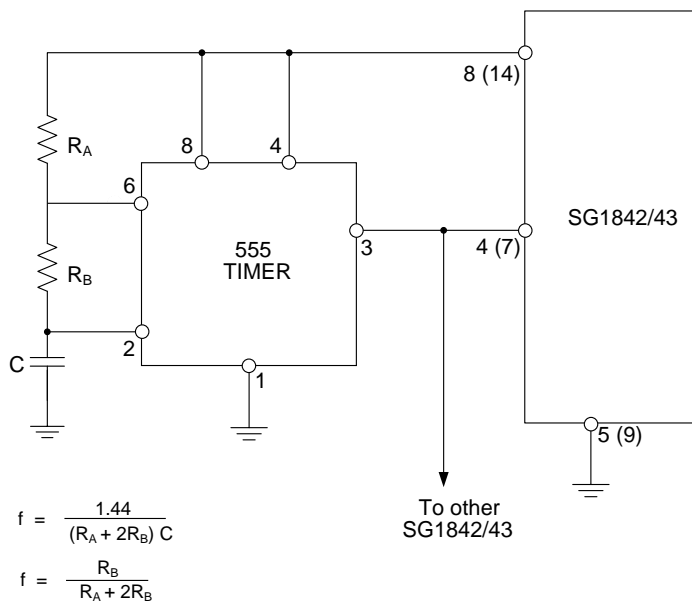
**Figure 21** • Adjustable Buffered Reduction of Clamp Level with Softstart

$$I_{PK} = \frac{V_{CS}}{R_S}$$

Where,  $V_{CS} = 1.67 \left( \frac{R_1}{R_1 + R_2} \right)$  and  $V_{C.S.MAX} = 1V$  (Typ.)

$$t_{SOFTSTART} = -\ln \left[ 1 - \frac{V_{EAO} - 1.3}{5 \left( \frac{R_1}{R_1 + R_2} \right)} \right] \left( \frac{R_1 R_2}{R_1 + R_2} \right) C$$

Where,  $V_{EAO} \equiv$  voltage at the Error Amp Output under minimum line and maximum load conditions  
Softstart and adjustable peak current can be done with the external circuitry shown above.

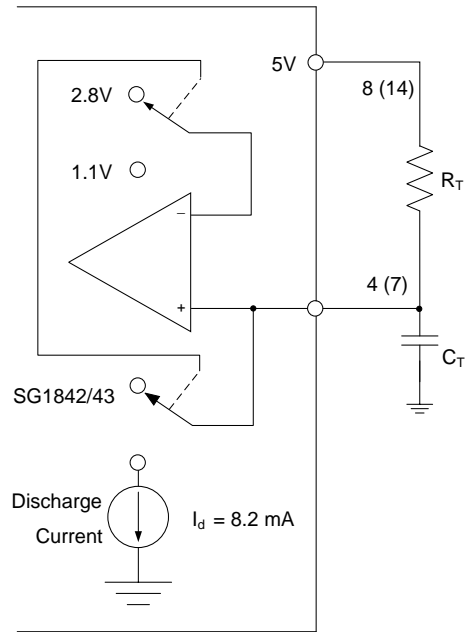


$$f = \frac{1.44}{(R_A + 2R_B) C}$$

$$f = \frac{R_B}{R_A + 2R_B}$$

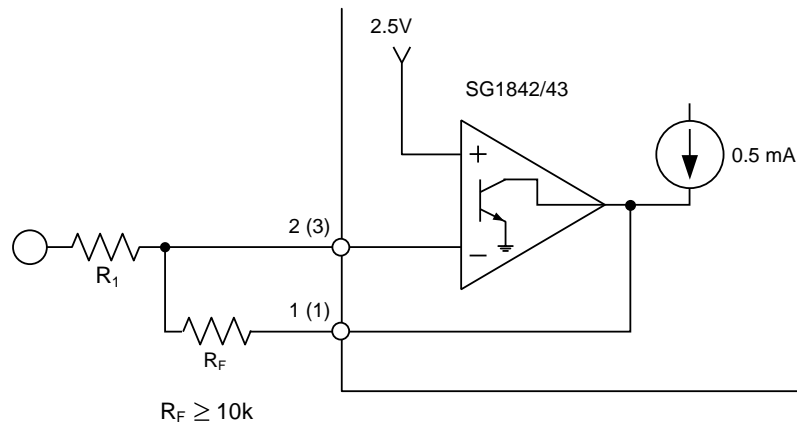
**Figure 22** • External Duty Cycle Clamp and Multi-Unit Synchronization

Precision duty cycle limiting as well as synchronizing several 1842/1843's is possible with the above circuitry.



**Figure 23** - Oscillator Connection

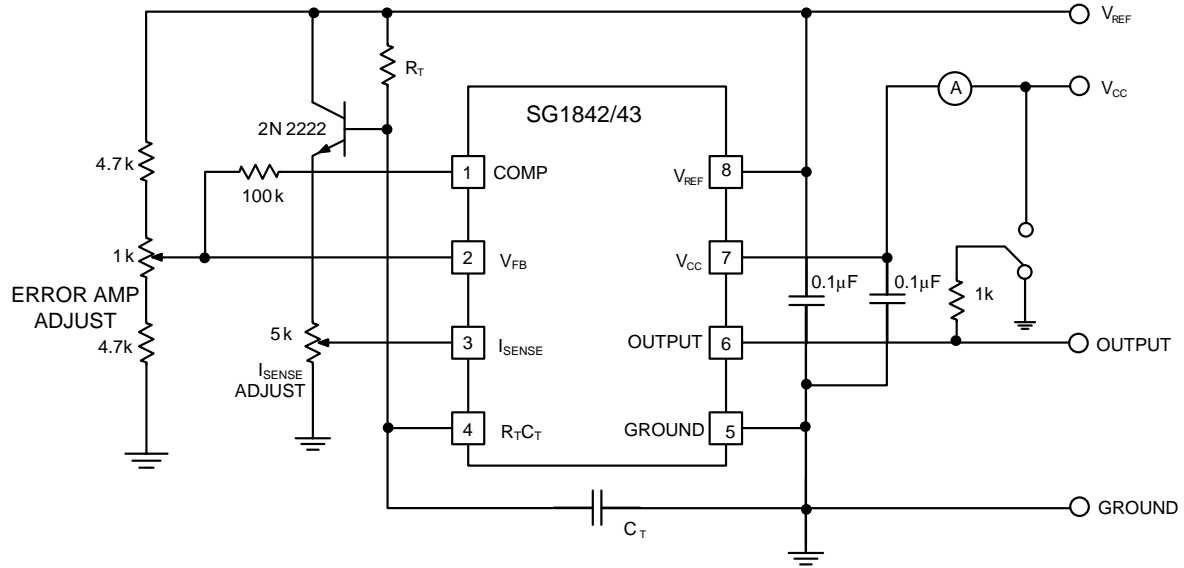
The oscillator is programmed by the values selected for the timing components  $R_T$  and  $C_T$ . Refer to application information for calculation of the component values.



**Figure 24** - Error Amplifier Connection

Error amplifier is capable of sourcing and sinking current up to 0.5mA.





**Figure 26** - Open Loop Laboratory Fixture

High-peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected to pin 5 in a single point ground.

The transistor and 5kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

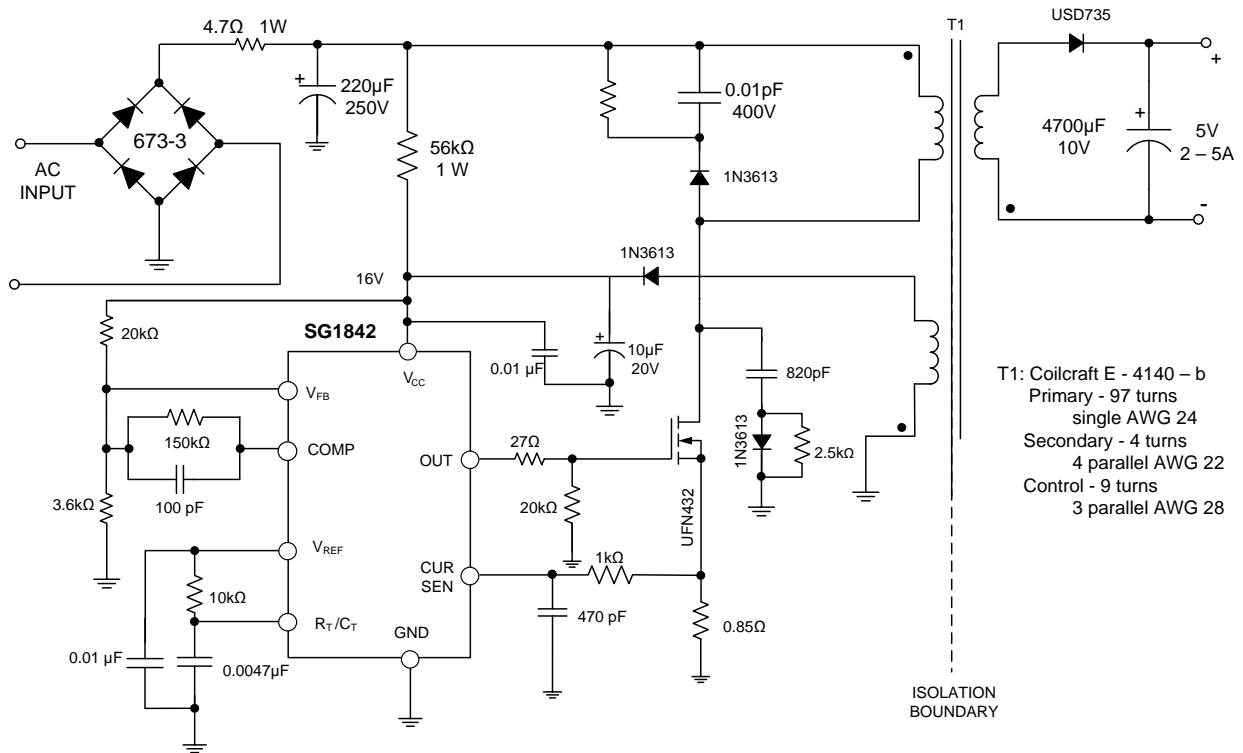


Figure 27 - Off-line Flyback Regulator

### SPECIFICATIONS

Input line voltage:	90VAC to 130VAC
Input frequency:	50 or 60Hz
Switching frequency:	40kHz $\pm$ 10%
Output power:	25W maximum
Output voltage:	5V $\pm$ 5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*
Efficiency @ 25 Watt:	
$V_{IN} = 90VAC$ :	70%
$V_{IN} = 130VAC$ :	65%
Output short-circuit current:	2.5 A average

\*This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the SG1842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance.

## Package Outline Dimensions

Controlling dimensions are in inches, metric equivalents are shown for general information.

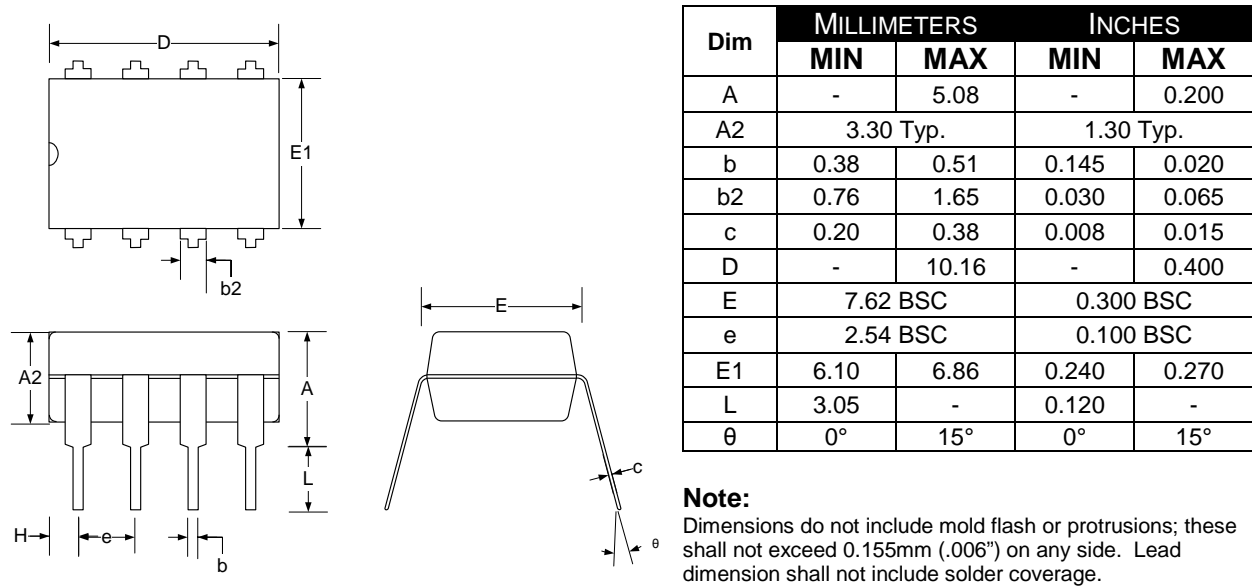


Figure 1 • M 8-Pin PDIP Package Dimensions

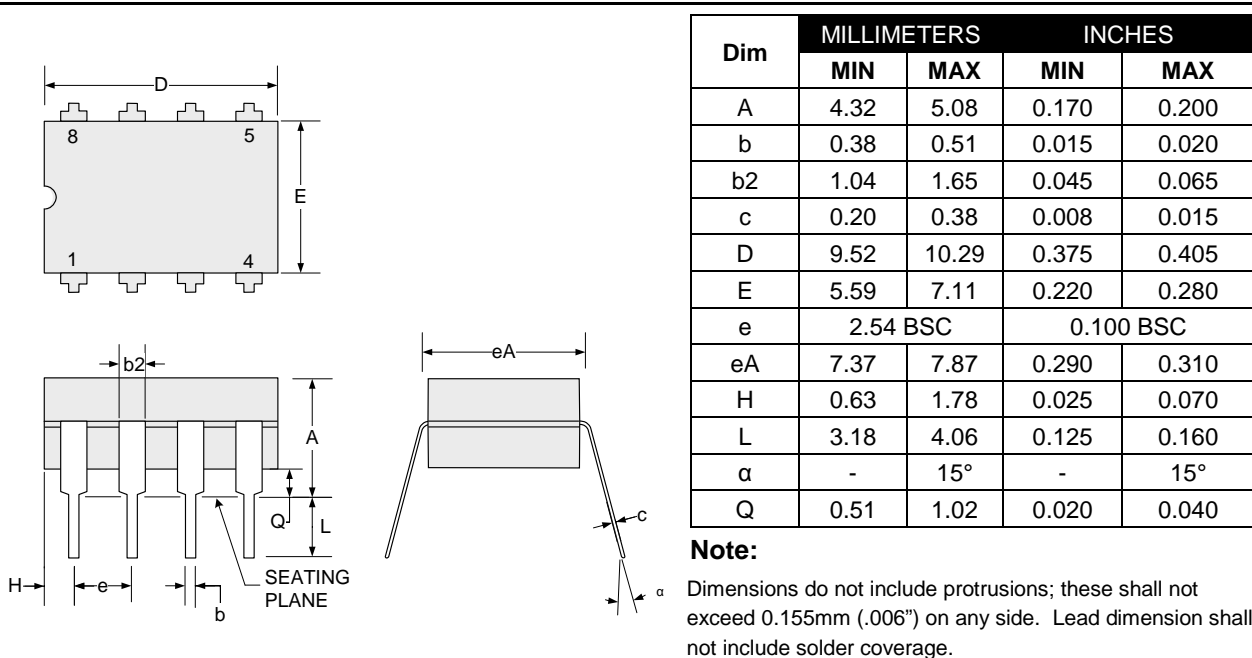
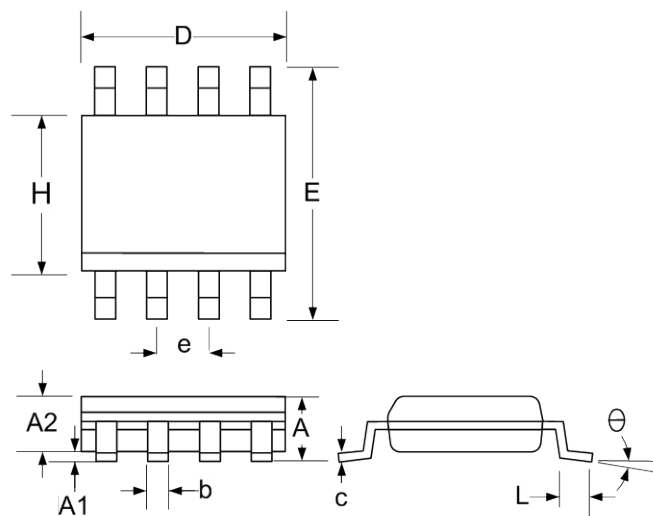


Figure 2 • Y 8-Pin CERDIP Package Dimensions

# Package Outline Dimensions

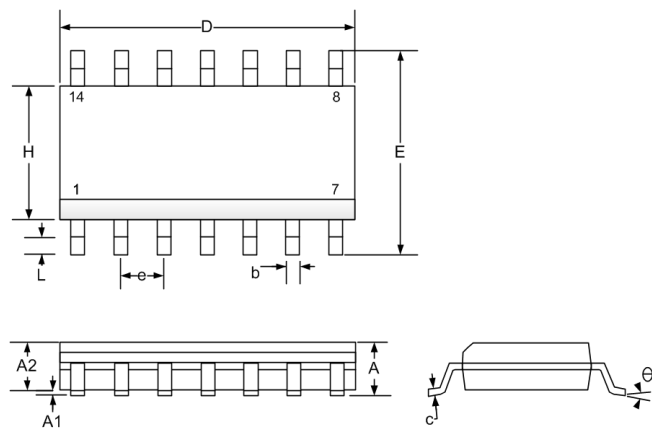


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	4.83	5.21	0.189	0.205
E	5.79	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
H	3.81	4.01	0.150	0.158
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
*LC	-	.010	-	0.004

\*Lead Co-planarity

**Note:** Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage

Figure 3 - DM 8-Pin SOIC Package Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	8.54	8.74	0.336	0.344
E	5.79	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
H	3.81	4.01	0.150	0.158
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
*LC	-	.010	-	0.004

\*Lead Co-planarity

**Note:** Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage

Figure 4 - D 14-Pin SOIC Package Dimensions

## Package Outline Dimensions

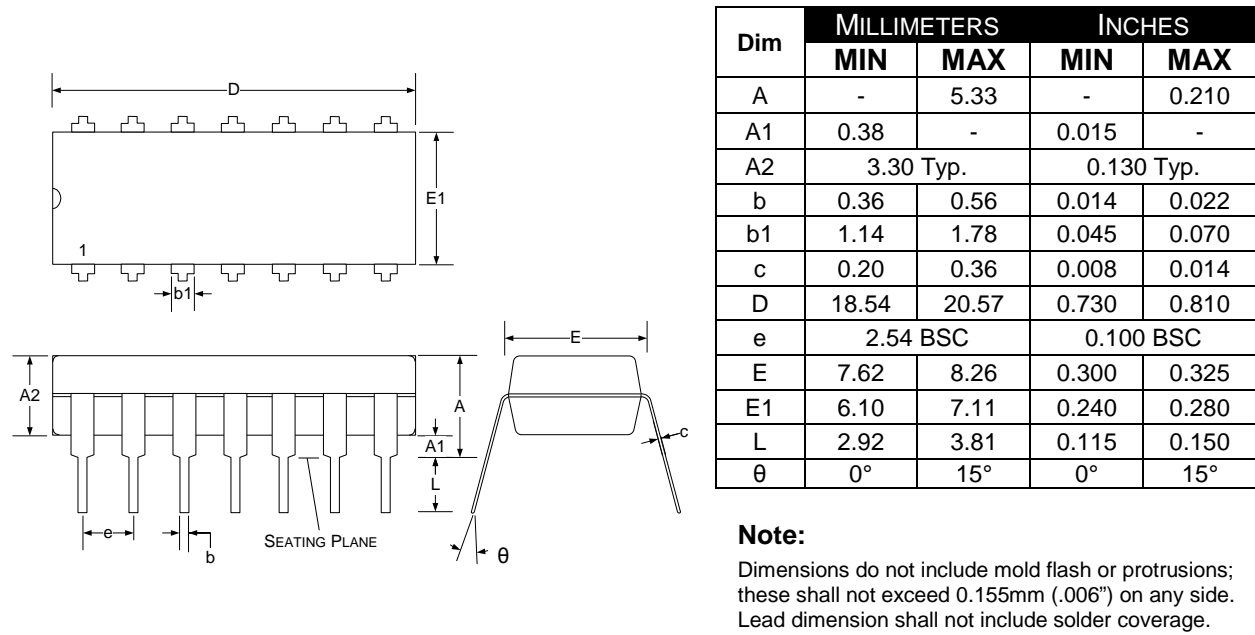


Figure 5 - N 14-Pin PDIP Package Dimensions

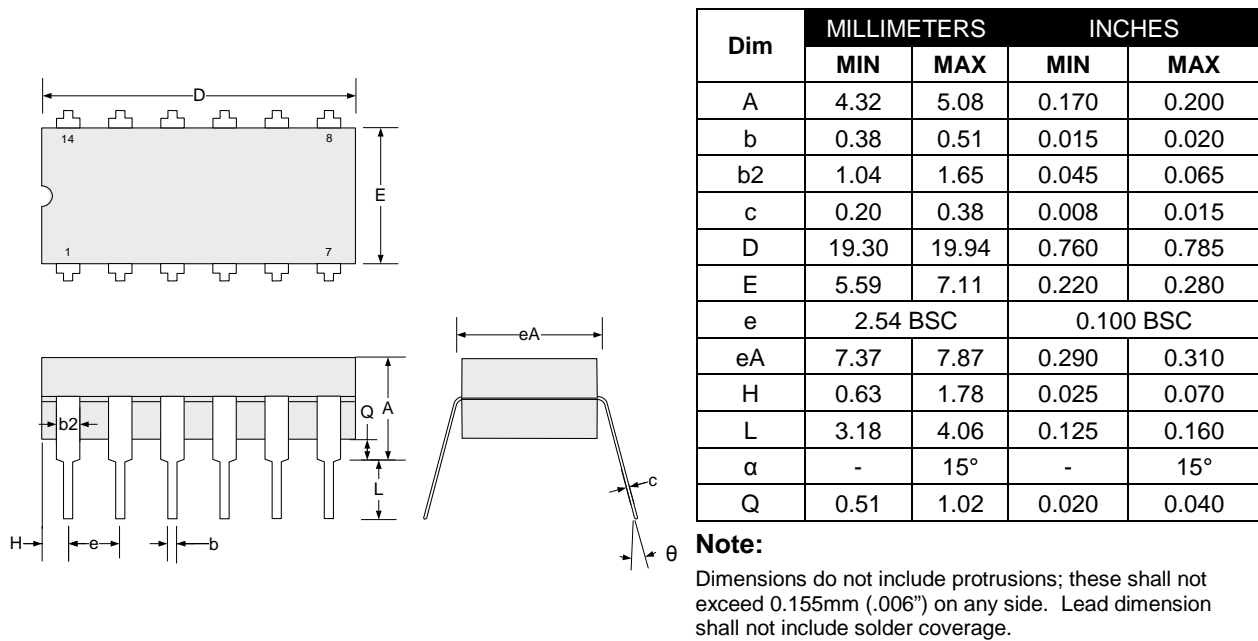
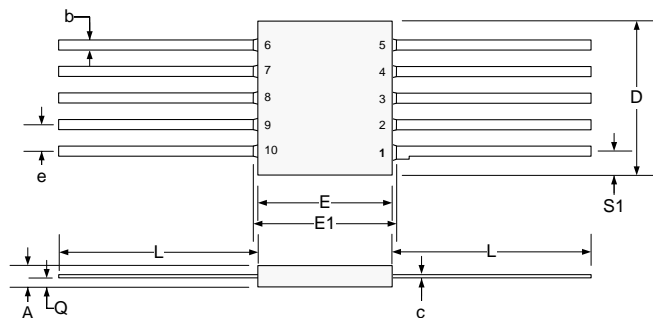


Figure 6 - J 14-Pin Cerdip Package Dimensions

# Package Outline Dimensions

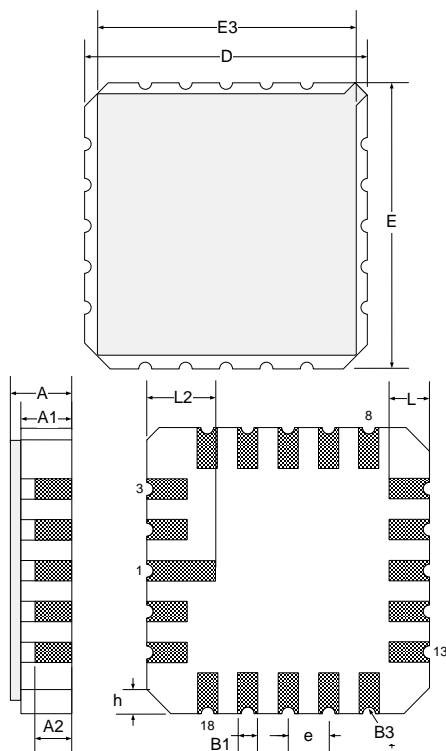


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.45	1.70	0.057	0.067
b	0.25	0.483	0.010	0.019
c	0.102	0.152	0.004	0.006
D	-	7.37	-	0.290
E	6.04	6.40	0.238	0.252
E1	-	6.91	-	0.272
e	1.27 BSC		0.050 BSC	
L	6.35	9.40	0.250	0.370
Q	0.51	1.02	0.020	0.040
S1	0.20	0.38	0.008	0.015

**Notes:**

1. Lead No. 1 is identified by tab on lead or dot on cover.
2. Leads are within 0.13mm (.0005") radius of the true position (TP) at maximum material condition.
3. Dimension "e" determines a zone within which all body and lead irregularities lie.

**Figure 7 - F 10-Pin Ceramic Flatpack Package Dimensions**



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

**Note:**

All exposed metallized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

**Figure 8 - L 20-Pin Leadless Chip Carrier Package Dimensions**



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