



**THE DATASHEET OF  
SN74ALVC04PW**



**FEATURES**

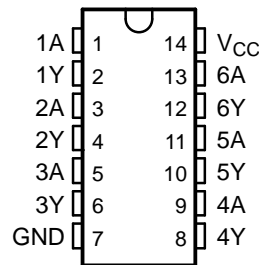
- Operates From 1.65 V to 3.6 V
- Max  $t_{pd}$  of 2.8 ns at 3.3 V
- $\pm 24$ -mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

**DESCRIPTION/ORDERING INFORMATION**

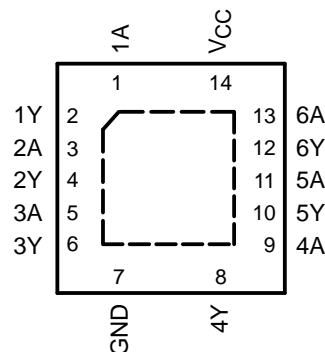
This hex inverter contains six independent inverters designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVC04 performs the Boolean function  $Y = \bar{A}$ .

**D, DGV, NS, OR PW PACKAGE (TOP VIEW)**



**RGY PACKAGE (TOP VIEW)**



**ORDERING INFORMATION**

| $T_A$         | PACKAGE <sup>(1)</sup> |                | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|----------------|-----------------------|------------------|
| -40°C to 85°C | QFN - RGY              | Tape and reel  | SN74ALVC04RGYR        | VA04             |
|               | SOIC - D               | Tube           | SN74ALVC04D           | ALVC04           |
|               |                        | Tape and reel  | SN74ALVC04DR          |                  |
|               | SOP - NS               | Tape and reel  | SN74ALVC04NSR         | ALVC04           |
|               | TSSOP - PW             | Tube           | SN74ALVC04PW          | VA04             |
|               |                        | Tape and reel  | SN74ALVC04PWR         |                  |
| TVSOP - DGV   | Tape and reel          | SN74ALVC04DGVR | VA04                  |                  |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE (each inverter)**

| INPUT<br>A | OUTPUT<br>Y |
|------------|-------------|
| H          | L           |
| L          | H           |

**LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74ALVC04 HEX INVERTER

SCES117J–JULY 1997–REVISED JULY 2004

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|   |  | MIN                        | MAX                   | UNIT    |
|---|--|----------------------------|-----------------------|---------|
| V <sub>CC</sub>                                   | Supply voltage range                   | -0.5                       | 4.6                   | V       |
| V <sub>I</sub>                                    | Input voltage range <sup>(2)</sup>     | -0.5                       | 4.6                   | V       |
| V <sub>O</sub>                                    | Output voltage range <sup>(2)(3)</sup> | -0.5                       | V <sub>CC</sub> + 0.5 | V       |
| I <sub>IK</sub>                                   | Input clamp current                    | V <sub>I</sub> < 0         |                       | -50 mA  |
| I <sub>OK</sub>                                   | Output clamp current                   | V <sub>O</sub> < 0         |                       | -50 mA  |
| I <sub>O</sub>                                    | Continuous output current              |                            |                       | ±50 mA  |
| Continuous current through V <sub>CC</sub> or GND |  |                            |                       | ±100 mA |
| θ <sub>JA</sub>                                   | Package thermal impedance              | D package <sup>(4)</sup>   |                       | 86      |
|   |  | DGV package <sup>(4)</sup> |                       | 127     |
|   |  | NS package <sup>(4)</sup>  |                       | 76      |
|   |  | PW package <sup>(4)</sup>  |                       | 113     |
|   |  | RGY package <sup>(5)</sup> |                       | 47      |
| T <sub>stg</sub>                                  | Storage temperature range              | -65                        | 150                   | °C      |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

|                 |                                    | MIN                                | MAX                    | UNIT   |
|-----------------|------------------------------------|------------------------------------|------------------------|--------|
| V <sub>CC</sub> | Supply voltage                     | 1.65                               | 3.6                    | V      |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.65 × V <sub>CC</sub> | V      |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                    |        |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2                      |        |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.35 × V <sub>CC</sub> | V      |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 0.7                    |        |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 0.8                    |        |
| V <sub>I</sub>  | Input voltage                      | 0                                  | 3.6                    | V      |
| V <sub>O</sub>  | Output voltage                     | 0                                  | V <sub>CC</sub>        | V      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V           | -4                     | mA     |
|                 |                                    | V <sub>CC</sub> = 2.3 V            | -12                    |        |
|                 |                                    | V <sub>CC</sub> = 2.7 V            | -12                    |        |
|                 |                                    | V <sub>CC</sub> = 3 V              | -24                    |        |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V           | 4                      | mA     |
|                 |                                    | V <sub>CC</sub> = 2.3 V            | 12                     |        |
|                 |                                    | V <sub>CC</sub> = 2.7 V            | 12                     |        |
|                 |                                    | V <sub>CC</sub> = 3 V              | 24                     |        |
| Δt/Δv           | Input transition rise or fall rate |                                    |                        | 5 ns/V |
| T <sub>A</sub>  | Operating free-air temperature     | -40                                | 85                     | °C     |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS  | V <sub>CC</sub> | MIN                   | TYP <sup>(1)</sup> | MAX  | UNIT |
|--------------------------|--|-----------------|-----------------------|--------------------|------|------|
| V <sub>OH</sub>          | I <sub>OH</sub> = -100 μA  | 1.65 V to 3.6 V | V <sub>CC</sub> - 0.2 |                    |      | V    |
|                          | I <sub>OH</sub> = -4 mA  | 1.65 V          | 1.2                   |                    |      |      |
|                          | I <sub>OH</sub> = -6 mA  | 2.3 V           | 2                     |                    |      |      |
|                          | I <sub>OH</sub> = -12 mA   | 2.3 V           | 1.7                   |                    |      |      |
|                          |  | 2.7 V           | 2.2                   |                    |      |      |
|                          |  | 3 V             | 2.4                   |                    |      |      |
| I <sub>OH</sub> = -24 mA | 3 V  | 2               |                       |                    |      |      |
| V <sub>OL</sub>          | I <sub>OL</sub> = 100 μA   | 1.65 V to 3.6 V |                       |                    | 0.2  | V    |
|                          | I <sub>OL</sub> = 4 mA   | 1.65 V          |                       |                    | 0.45 |      |
|                          | I <sub>OL</sub> = 6 mA   | 2.3 V           |                       |                    | 0.4  |      |
|                          | I <sub>OL</sub> = 12 mA  | 2.3 V           |                       |                    | 0.7  |      |
|                          |  | 2.7 V           |                       |                    | 0.4  |      |
|                          | I <sub>OL</sub> = 24 mA  | 3 V             |                       |                    | 0.55 |      |
| I <sub>I</sub>           | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           |                       |                    | ±5   | μA   |
| I <sub>CC</sub>          | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           |                       |                    | 10   | μA   |
| ΔI <sub>CC</sub>         | One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 3.6 V    |                       |                    | 750  | μA   |
| C <sub>i</sub>           | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           | 3.5                   |                    |      | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER       | FROM (INPUT) | TO (OUTPUT) | V <sub>CC</sub> = 1.8 V |     | V <sub>CC</sub> = 2.5 V ± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V ± 0.3 V |  | UNIT |
|-----------------|--------------|-------------|-------------------------|-----|---------------------------------|-----|-------------------------|-----|---------------------------------|--|------|
|                 |              |             | TYP                     | MIN | MAX                             | MIN | MAX                     | MIN | MAX                             |  |      |
| t <sub>pd</sub> | A            | Y           | (1)                     | 1   | 3                               |     | 3.3                     | 1   | 2.8                             |  | ns   |

(1) This information was not available at the time of publication.

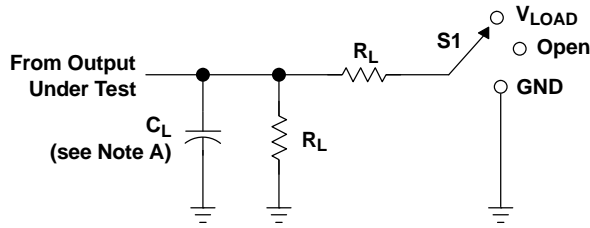
## OPERATING CHARACTERISTICS

T<sub>A</sub> = 25°C

| PARAMETER  | TEST CONDITIONS                | V <sub>CC</sub> = 1.8 V | V <sub>CC</sub> = 2.5 V | V <sub>CC</sub> = 3.3 V | UNIT |
|--|--------------------------------|-------------------------|-------------------------|-------------------------|------|
|  |                                | TYP                     | TYP                     | TYP                     |      |
| C <sub>pd</sub> Power dissipation capacitance per inverter | C <sub>L</sub> = 0, f = 10 MHz | (1)                     | 23                      | 27.5                    | pF   |

(1) This information was not available at the time of publication.

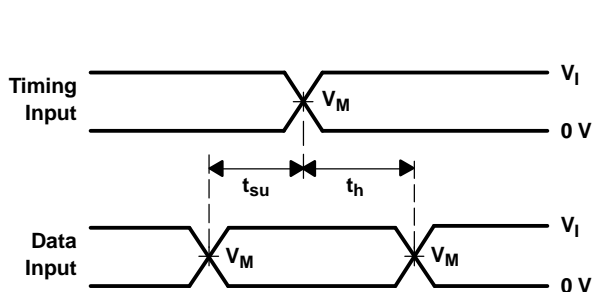
**PARAMETER MEASUREMENT INFORMATION**



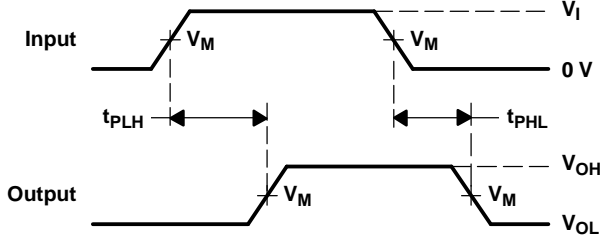
**LOAD CIRCUIT**

| TEST              | S1         |
|-------------------|------------|
| $t_{pd}$          | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

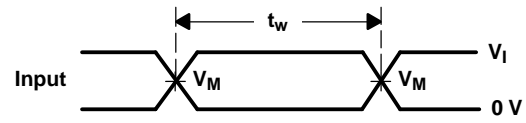
| $V_{CC}$                         | INPUT    |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |



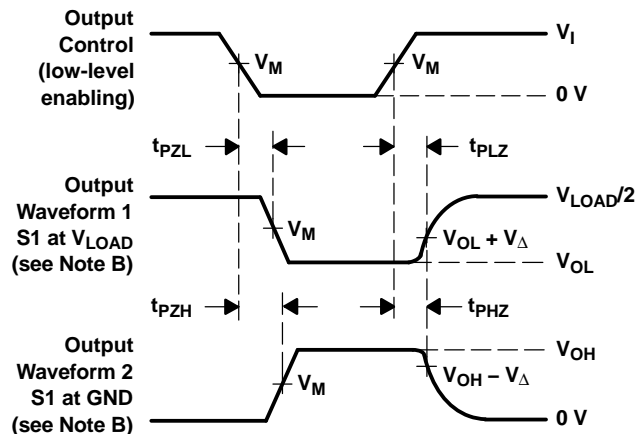
**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74ALVC04D      | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ALVC04                  | <a href="#">Samples</a> |
| SN74ALVC04DGVR   | ACTIVE        | TVSOP        | DGV             | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | VA04                    | <a href="#">Samples</a> |
| SN74ALVC04DR     | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ALVC04                  | <a href="#">Samples</a> |
| SN74ALVC04DRE4   | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ALVC04                  | <a href="#">Samples</a> |
| SN74ALVC04DRG4   | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ALVC04                  | <a href="#">Samples</a> |
| SN74ALVC04PW     | ACTIVE        | TSSOP        | PW              | 14   | 90          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | VA04                    | <a href="#">Samples</a> |
| SN74ALVC04PWR    | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | VA04                    | <a href="#">Samples</a> |
| SN74ALVC04PWRG4  | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | VA04                    | <a href="#">Samples</a> |
| SN74ALVC04RGYR   | ACTIVE        | VQFN         | RGY             | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | VA04                    | <a href="#">Samples</a> |
| SN74ALVC04RGYRG4 | ACTIVE        | VQFN         | RGY             | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | VA04                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALVC04DGVR | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74ALVC04DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74ALVC04PWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74ALVC04RGYR | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALVC04DGVR | TVSOP        | DGV             | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74ALVC04DR   | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |
| SN74ALVC04PWR  | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74ALVC04RGYR | VQFN         | RGY             | 14   | 3000 | 356.0       | 356.0      | 35.0        |

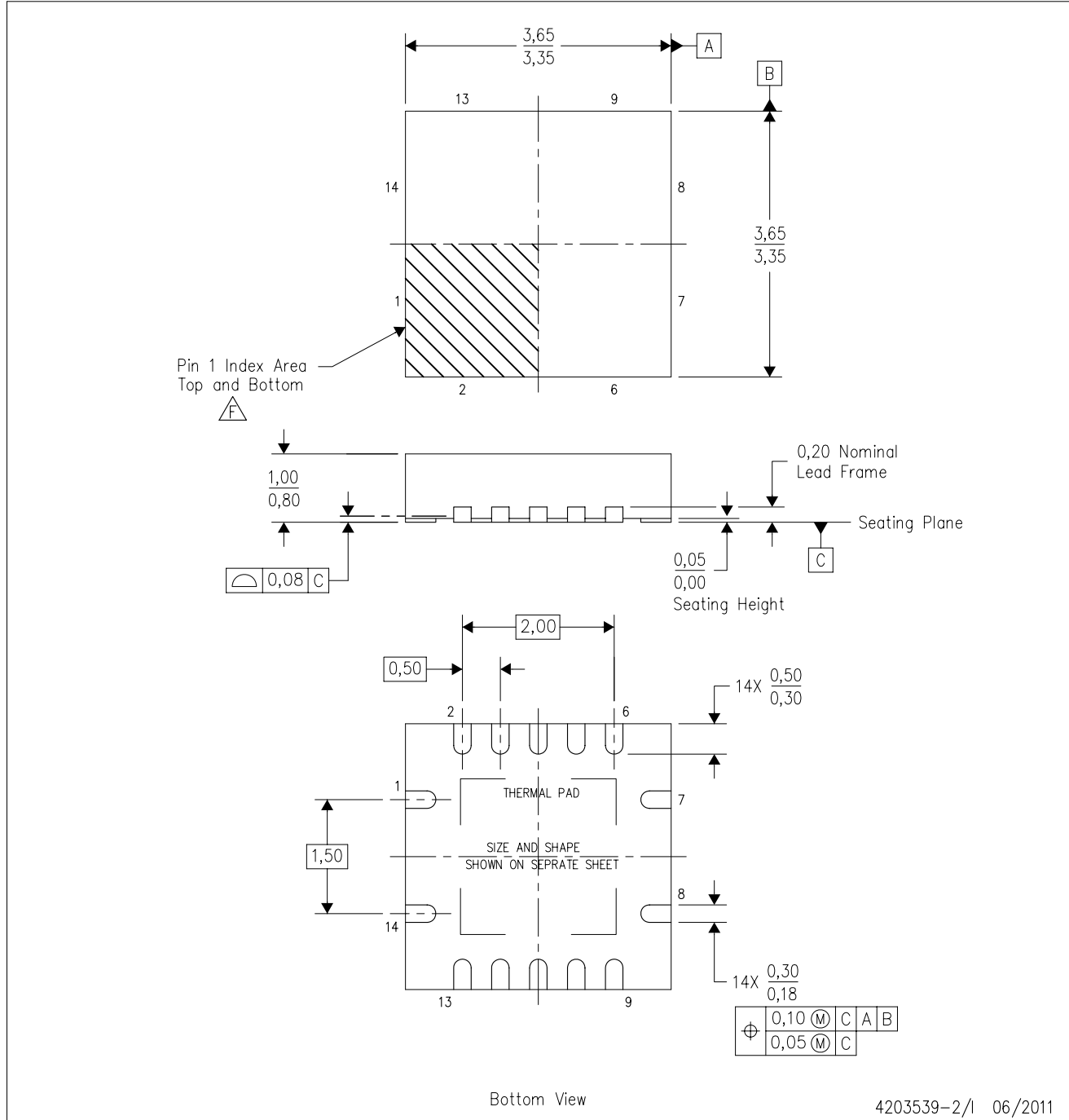
**TUBE**


\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ALVC04D  | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74ALVC04PW | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

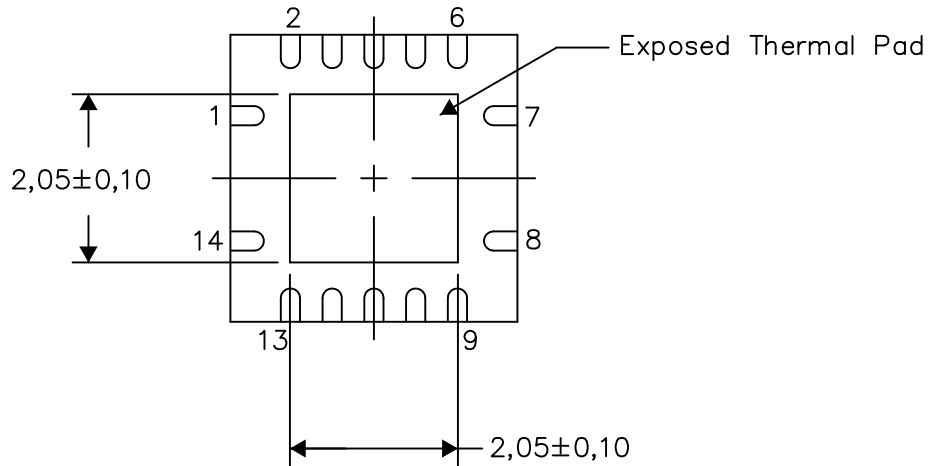
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN74ALVC04PW on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management