



**THE DATASHEET OF  
STL19N60DM2**



## N-channel 600 V, 0.280 $\Omega$ typ., 11 A MDmesh™ DM2 with fast diode Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - preliminary data

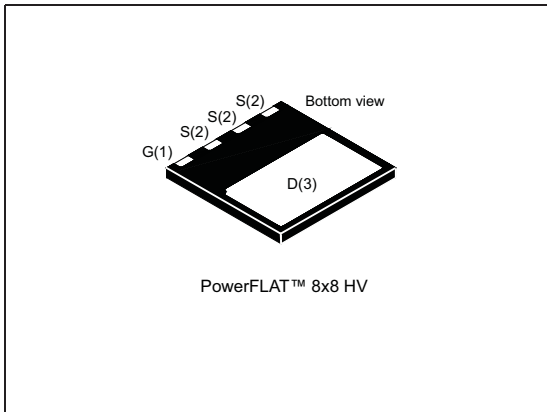
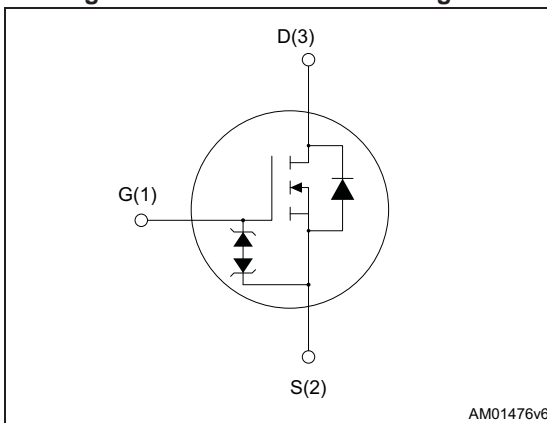


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on)max}$	$I_D$
STL19N60DM2	650 V	0.320 $\Omega$	11 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance  $R_{DS(on)}$
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high voltage N-channel Power MOSFET is part of the MDmesh DM2 fast recovery diode series. It offers very low recovery charge and time ( $Q_{rr}$ ,  $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL19N60DM2	19N60DM2	PowerFLAT™ 8x8 HV	Tape and reel

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	11	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6.8	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	44	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	90	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	TBD	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	TBD	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	40	V/ns
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to  $R_{thj-case}$  and limited by package.
2. Pulse width limited by safe operating area.
3.  $I_{SD} \leq 11\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
4.  $V_{DS} \leq 480\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.39	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient max	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 600\text{V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$		0.280	0.320	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	TBD	-	pF
$C_{oss}$	Output capacitance		-	TBD	-	pF
$C_{rss}$	Reverse transfer capacitance		-	TBD	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0$	-	TBD	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$		5.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 11\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 3</a> )	-	21	-	nC
$Q_{gs}$	Gate-source charge		-	TBD	-	nC
$Q_{gd}$	Gate-drain charge		-	TBD	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 5.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 2</a> and <a href="#">7</a> )	-	TBD	-	ns
$t_r$	Voltage rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
$t_f$	Current fall time		-	TBD	-	ns

Table 7. Source drain diode

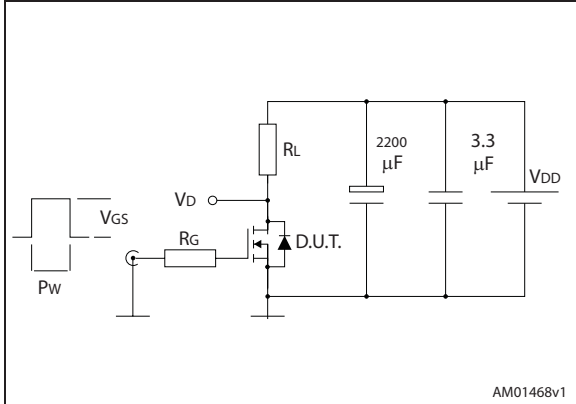
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		11	A
$I_{SDM}^{(1),(2)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 11\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}^{(4)}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 4</a> )	-	120		ns
$Q_{rr}^{(4)}$	Reverse recovery charge		-	TBD		$\mu\text{C}$
$I_{RRM}^{(4)}$	Reverse recovery current		-	TBD		A
$t_{rr}^{(4)}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 4</a> )	-	TBD		ns
$Q_{rr}^{(4)}$	Reverse recovery charge		-	TBD		$\mu\text{C}$
$I_{RRM}^{(4)}$	Reverse recovery current		-	TBD		A

1. The value is rated according to  $R_{thj-case}$  and limited by package.
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%
4. Typical values are referring to the test conditions of the same die housed in through hole package.

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

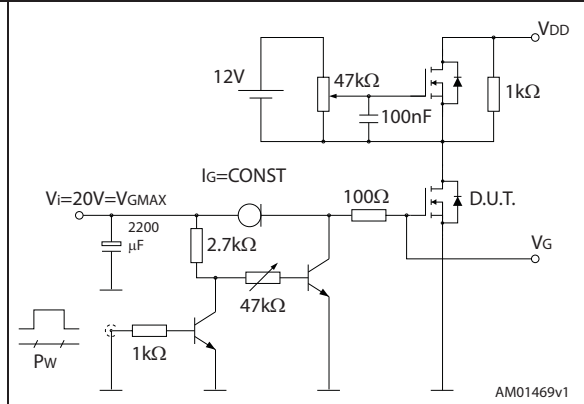
### 3 Test circuits

Figure 2. Switching times test circuit for resistive load



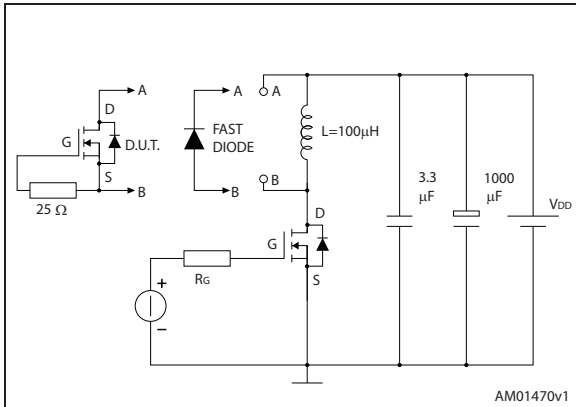
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Figure 3. Gate charge test circuit



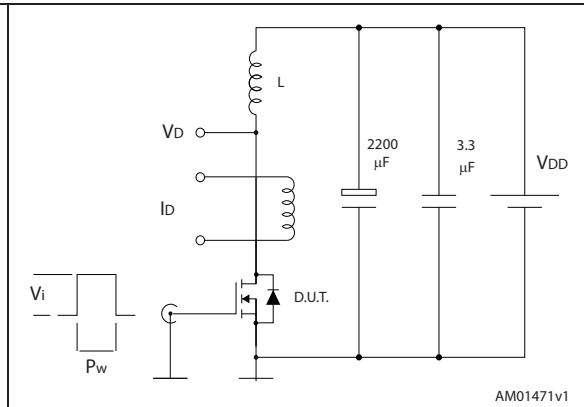
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Figure 4. Test circuit for inductive load switching and diode recovery times



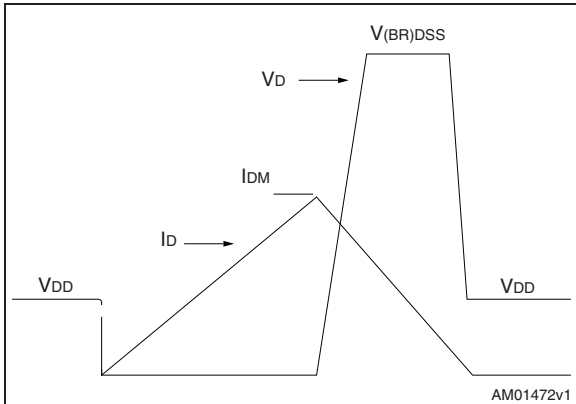
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Figure 5. Unclamped inductive load test circuit



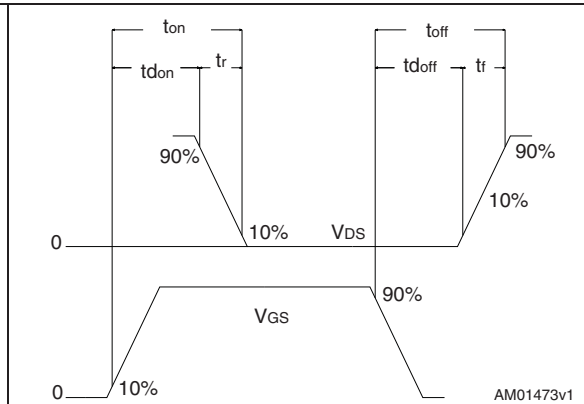
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Figure 6. Unclamped inductive waveform



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Figure 7. Switching time waveform



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## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 8. PowerFLAT™ 8x8 HV drawing mechanical data

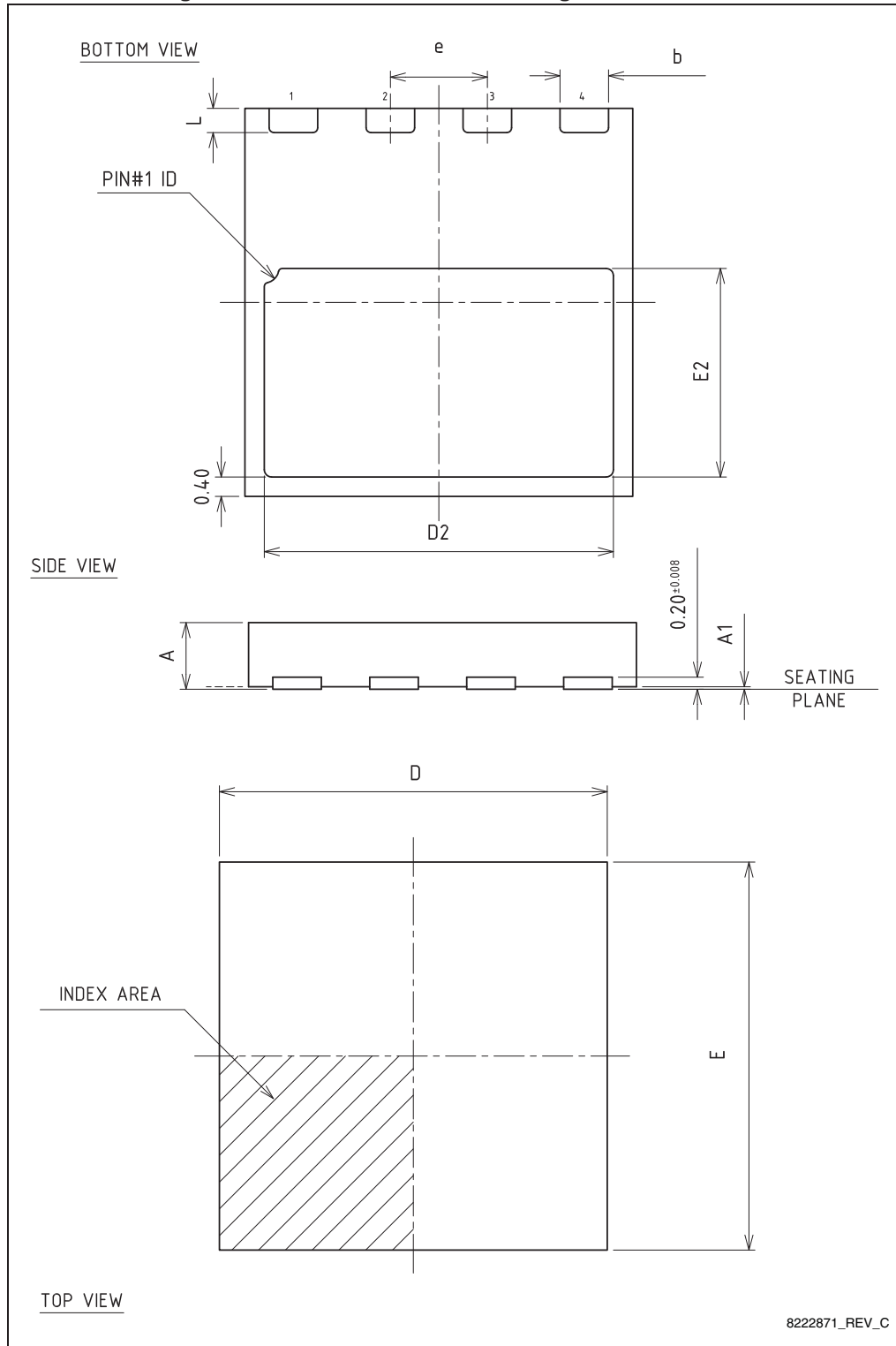
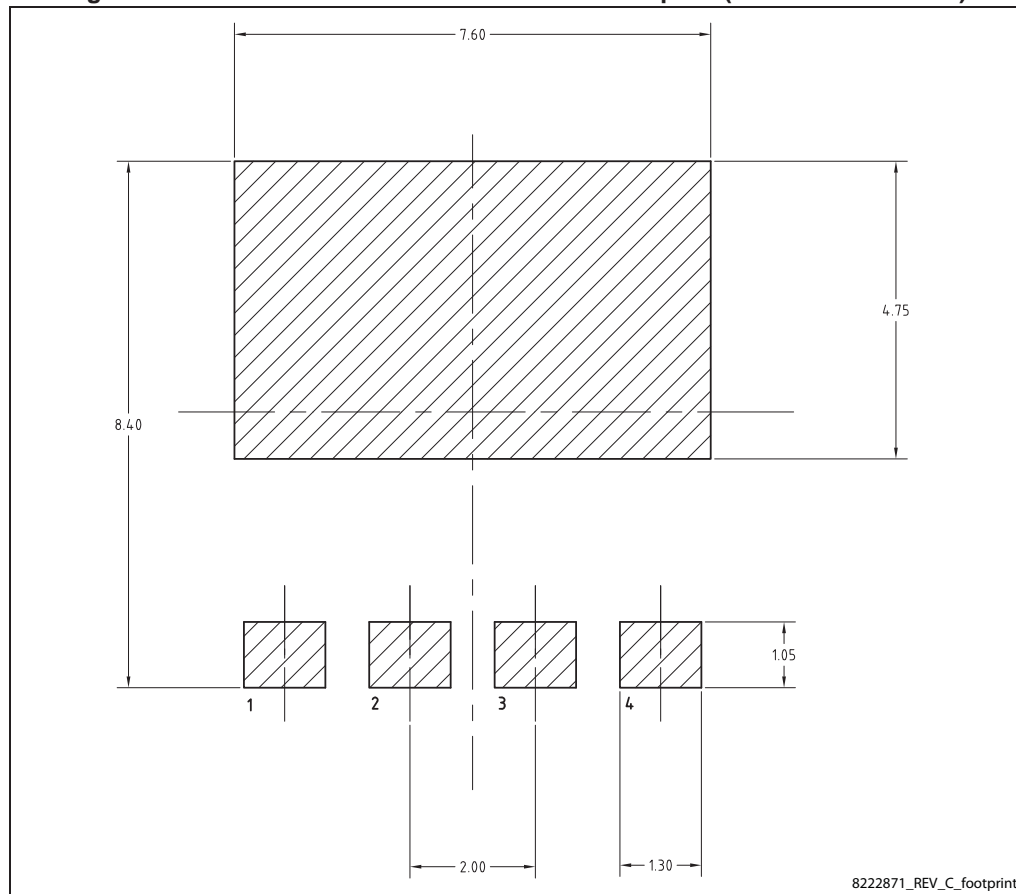


Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 9. PowerFLAT™ 8x8 HV recommended footprint (dimensions in mm.)



8222871\_REV\_C\_footprint

# 5 Packaging mechanical data

Figure 10. PowerFLAT™ 8x8 HV tape

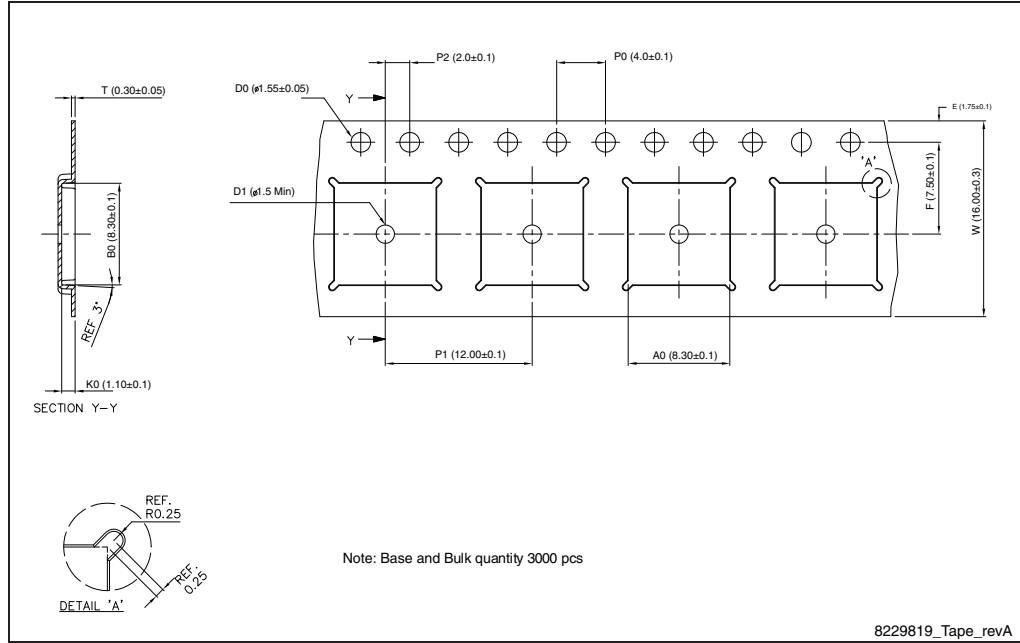


Figure 11. PowerFLAT™ 8x8 HV package orientation in carrier tape

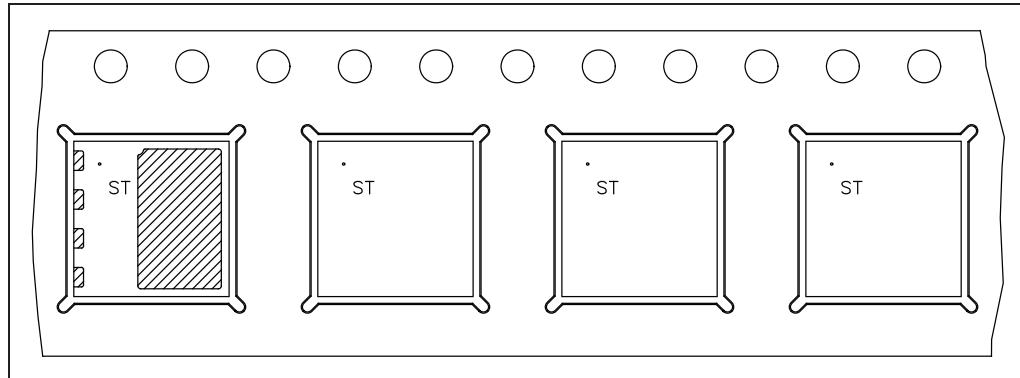
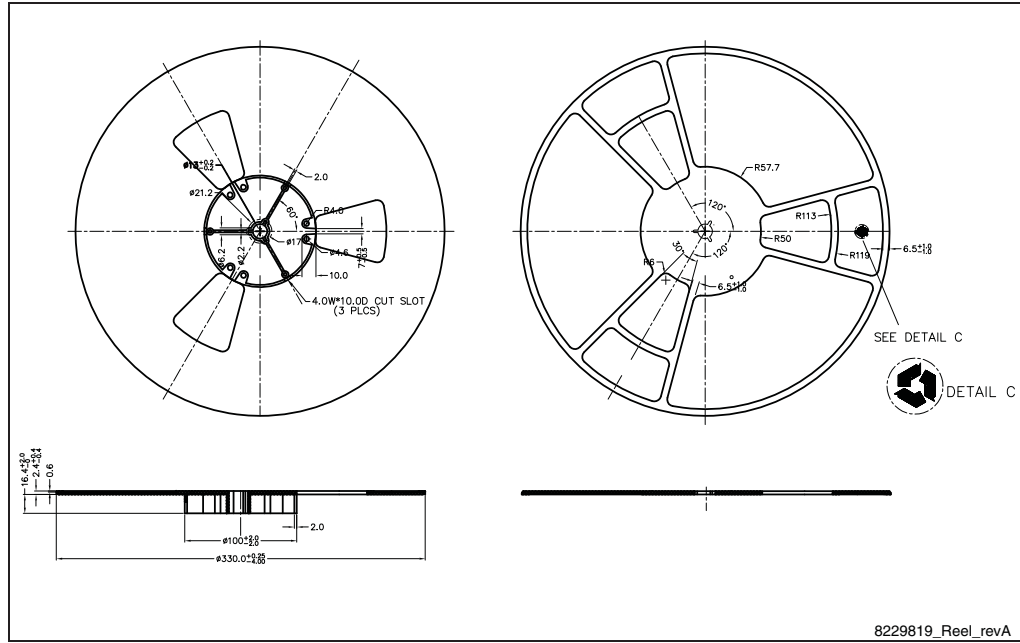


Figure 12. PowerFLAT™ 8x8 HV reel



## 6 Revision history

Table 9. Document revision history

Date	Revision	Changes
08-Aug-2014	1	First release.

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