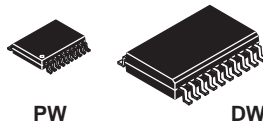




**THE DATASHEET OF  
TLV5633IPW**

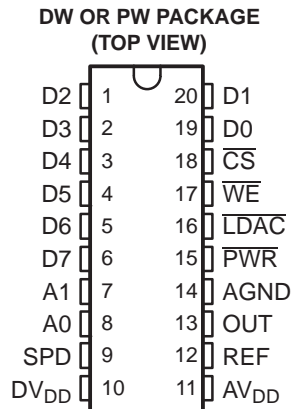




## 2.7 V TO 5.5 V LOW POWER 12-BIT DIGITAL-TO-ANALOG CONVERTERS WITH INTERNAL REFERENCE AND POWER DOWN

### FEATURES

- 12-Bit Voltage Output DAC
- Programmable Internal Reference
- Programmable Settling Time vs Power Consumption
  - 1  $\mu$ s in Fast Mode
  - 3.5  $\mu$ s in Slow Mode
- 8-Bit  $\mu$ Controller Compatible Interface
- Differential Nonlinearity . . . <0.5 LSB Typ
- Voltage Output Range . . . 2x the Reference Voltage
- Monotonic Over Temperature



### APPLICATIONS

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

### DESCRIPTION

The TLV5633 is a 12-bit voltage output digital- to-analog converter (DAC) with an 8-bit microcontroller compatible parallel interface. The 8 LSBs, the 4 MSBs, and 5 control bits are written using three different addresses. Developed for a wide range of supply voltages, the TLV5633 can be operated from 2.7 V to 5.5 V.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class A (slow mode: AB) output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed versus power dissipation. With its on-chip programmable precision voltage reference, the TLV5633 simplifies overall system design. Because of its ability to source up to 1 mA, the internal reference can also be used as a system reference. The settling time and the reference voltage can be chosen by a control register.

Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in 20-pin SOIC and TSSOP packages in standard commercial and industrial temperature ranges.

### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE <sup>(1)</sup>	
	SOIC (DW)	TSSOP (PW)
0°C to 70°C	TLV5633CDW	TLV5633CPW
-40°C to 85°C	TLV5633IDW	TLV5633IPW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).



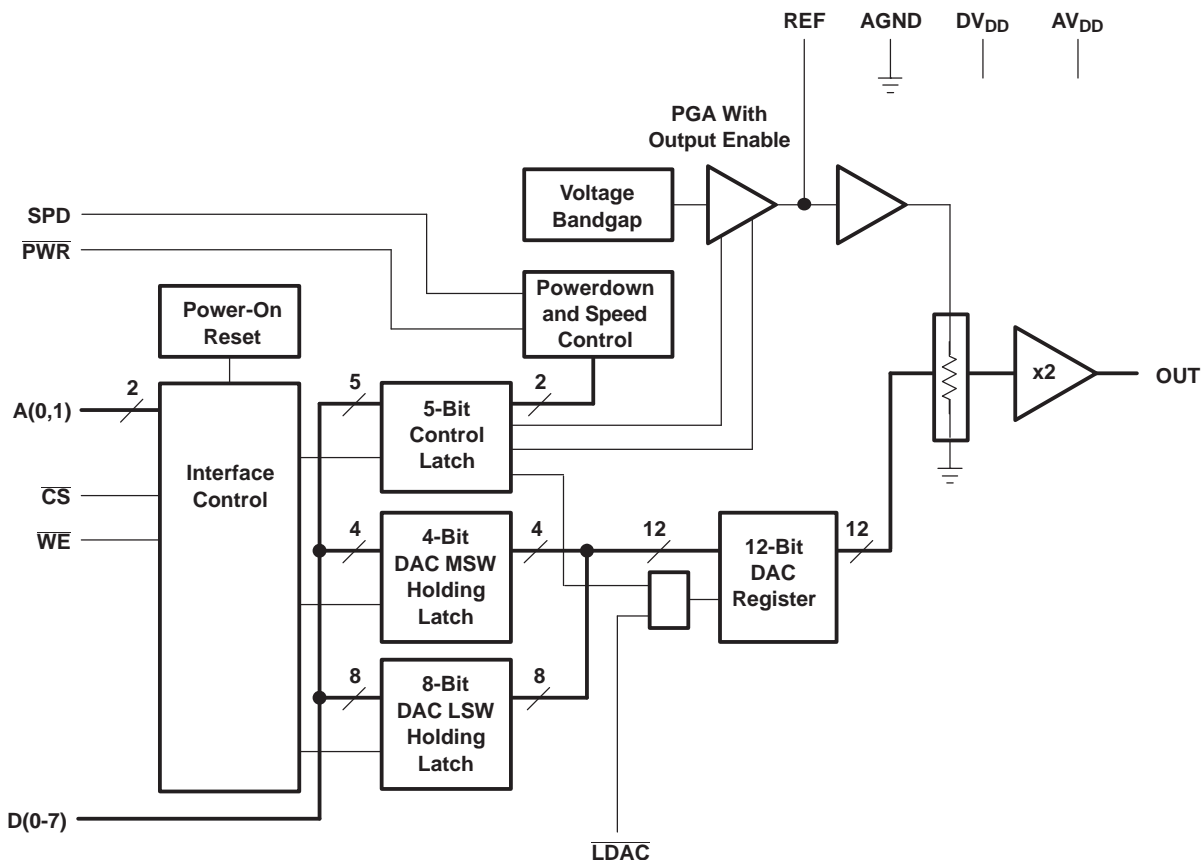
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### FUNCTIONAL BLOCK DIAGRAM



### Terminal Functions

TERMINAL NAME	NO.	I/O/P	DESCRIPTION
A1, A0	7, 8	I	Address input
AGND	14	P	Ground
AV <sub>DD</sub>	11	P	Positive power supply (analog part)
$\overline{CS}$	18	I	Chip select. Digital input active low, used to enable/disable inputs
D0-D1	19, 20	I	Data input
D2-D7	1-6	I	Data input
DV <sub>DD</sub>	10	P	Positive power supply (digital part)
$\overline{LDAC}$	16	I	Load DAC. Digital input active low, used to load DAC output
OUT	13	O	DAC analog voltage output
$\overline{PWR}$	15	I	Power down. Digital input active low
REF	12	I/O	Analog reference voltage input/output
SPD	9	I	Speed select. Digital input
$\overline{WE}$	17	I	Write enable. Digital input active low, used to latch data

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		UNIT
Supply voltage (DV <sub>DD</sub> , AV <sub>DD</sub> to AGND)		7 V
Supply voltage difference range, AV <sub>DD</sub> - DV <sub>DD</sub>		-2.8 V to 2.8 V
Reference input voltage range		-0.3 V to V <sub>DD</sub> + 0.3 V
Digital input voltage range		-0.3 V to V <sub>DD</sub> + 0.3 V
Operating free-air temperature range, T <sub>A</sub>	TLV5633C	0°C to 70°C
	TLV5633I	-40°C to 85°C
Storage temperature range, T <sub>stg</sub>		-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, DV <sub>DD</sub> , AV <sub>DD</sub>	5-V operation	4.5	5	5.5	V
	3-V operation	2.7	3	3.3	V
Supply voltage difference, $\Delta V_{DD} = AV_{DD} - DV_{DD}$		0	0	0	V
Power on reset voltage, POR		0.55		2	V
High-level digital input voltage, V <sub>IH</sub>	DV <sub>DD</sub> = 2.7 V	2			V
	DV <sub>DD</sub> = 5.5 V	2.4			
Low-level digital input voltage, V <sub>IL</sub>	DV <sub>DD</sub> = 2.7 V			0.6	V
	DV <sub>DD</sub> = 5.5 V			1	
Reference voltage, V <sub>ref</sub> to REF terminal (5-V supply) <sup>(1)</sup>		AGND	2.048	AV <sub>DD</sub> -1.5	V
Reference voltage, V <sub>ref</sub> to REF terminal (3-V supply) <sup>(1)</sup>		AGND	1.024	AV <sub>DD</sub> -1.5	V
Load resistance, R <sub>L</sub>		2			k $\Omega$
Load capacitance, C <sub>L</sub>				100	pF
Operating free-air temperature, T <sub>A</sub>	TLV5633C	0		70	°C
	TLV5633I	-40		85	

(1) Due to the x2 output buffer, a reference input voltage  $\geq AV_{DD}/2$  causes clipping of the transfer function. The output buffer of the internal reference must be disabled, if an external reference is used.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{ref} = 2.048\text{ V}$ ,  $V_{ref} = 1.024\text{ V}$  (unless otherwise noted)

POWER SUPPLY								
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{DD}$	Power supply current	No load, All inputs = AGND or DV <sub>DD</sub> , DAC latch = 0x800	$AV_{DD} = 5\text{ V}$ , $DV_{DD} = 5\text{ V}$	REF on	Fast	2.3	2.8	mA
				REF on	Slow	1.3	1.6	mA
			REF off	Fast	1.9	2.4	mA	
			REF off	Slow	0.9	1.2	mA	
		$AV_{DD} = 3\text{ V}$ , $DV_{DD} = 3\text{ V}$	REF on	Fast	2.1	2.6	mA	
			REF on	Slow	1.2	1.5	mA	
			REF off	Fast	1.8	2.3	mA	
			REF off	Slow	0.9	1.1	mA	
Power down supply current					0.01	1	$\mu\text{A}$	
PSRR	Power supply rejection ratio	Zero scale, external reference <sup>(1)</sup>			-60		dB	
		Full scale, external reference <sup>(2)</sup>			-60			
STATIC DAC SPECIFICATIONS								
Resolution					12		bits	
INL	Integral nonlinearity, end point adjusted	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ <sup>(3)</sup>			$\pm 1.2$	$\pm 3$	LSB	
DNL	Differential nonlinearity	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ <sup>(4)</sup>			$\pm 0.3$	$\pm 0.5$	LSB	
$E_{ZS}$	Zero-scale error (offset error at zero scale) <sup>(5)</sup>					20	mV	
$E_{ZS\text{TC}}$	Zero-scale-error temperature coefficient <sup>(6)</sup>					20	ppm/ $^{\circ}\text{C}$	
$E_G$	Gain error <sup>(7)</sup>					$\pm 0.3$	% full scale V	
$E_G\text{ TC}$	Gain error temperature coefficient <sup>(8)</sup>				20		ppm/ $^{\circ}\text{C}$	
OUTPUT SPECIFICATIONS								
$V_O$	Output voltage	$R_L = 10\text{ k}\Omega$				$AV_{DD}-0.4$	V	
	Output load regulation accuracy	$V_O = 4.096\text{ V}$ , $2.048\text{ V}$ , $R_L = 2\text{ k}\Omega$				$\pm 0.29$	% full scale V	

- (1) Power supply rejection ratio at zero scale is measured by varying  $AV_{DD}$  and is given by:  $PSRR = 20 \log [(E_{ZS}(AV_{DD\text{max}}) - E_{ZS}(AV_{DD\text{min}}))/AV_{DD\text{max}}]$
- (2) Power supply rejection ratio at full scale is measured by varying  $AV_{DD}$  and is given by:  $PSRR = 20 \log [(E_G(AV_{DD\text{max}}) - E_G(AV_{DD\text{min}}))/AV_{DD\text{max}}]$
- (3) The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text).
- (4) The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
- (5) Zero-scale error is the deviation from zero voltage output when the digital input code is zero (see text).
- (6) Zero-scale-error temperature coefficient is given by:  $E_{ZS\text{TC}} = [E_{ZS}(T_{\text{max}}) - E_{ZS}(T_{\text{min}})]/2V_{ref} \times 10^6/(T_{\text{max}} - T_{\text{min}})$ .
- (7) Gain error is the deviation from the ideal output ( $2V_{ref} - 1\text{ LSB}$ ) with an output load of  $10\text{ k}\Omega$  excluding the effects of the zero-error.
- (8) Gain temperature coefficient is given by:  $E_G\text{ TC} = [E_G(T_{\text{max}}) - E_G(T_{\text{min}})]/2V_{ref} \times 10^6/(T_{\text{max}} - T_{\text{min}})$ .

## ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range,  $V_{ref} = 2.048\text{ V}$ ,  $V_{ref} = 1.024\text{ V}$  (unless otherwise noted)

REFERENCE PIN CONFIGURED AS OUTPUT (REF)						
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{ref(OUTL)}$	Low reference voltage		1.003	1.024	1.045	V
$V_{ref(OUTH)}$	High reference voltage	$AV_{DD} = DV_{DD} > 4.75\text{ V}$	2.027	2.048	2.069	V
$I_{ref(source)}$	Output source current				1	mA
$I_{ref(sink)}$	Output sink current		-1			mA
PSRR	Power supply rejection ratio			-48		dB

REFERENCE PIN CONFIGURED AS INPUT (REF)						
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_I$	Input voltage		0		$AV_{DD-1.5}$	V
$R_I$	Input resistance			10		M $\Omega$
$C_I$	Input capacitance			5		pF
Reference input bandwidth		REF = 0.2 $V_{pp}$ + 1.024 V dc	Fast	900		kHz
			Slow	500		
Harmonic distortion, reference input		REF = 1 $V_{pp}$ + 2.048 V dc, $AV_{DD} = 5\text{ V}$	10 kHz	Fast	-87	dB
				Slow	-77	
			50 kHz	Fast	-74	dB
				Slow	-61	
			100 kHz	Fast	-66	dB
Reference feedthrough		REF = 1 $V_{pp}$ at 1 kHz + 1.024 V dc <sup>(1)</sup>		-80		dB

### DIGITAL INPUTS

$I_{IH}$	High-level digital input current	$V_I = DV_{DD}$			1	$\mu\text{A}$
$I_{IL}$	Low-level digital input current	$V_I = 0\text{ V}$	-1			$\mu\text{A}$
$C_I$	Input capacitance			8		pF

(1) Reference feedthrough is measured at the DAC output with an input code = 0x000.

## OPERATING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{ref} = 2.048\text{ V}$ , and  $V_{ref} = 1.024\text{ V}$ , (unless otherwise noted)

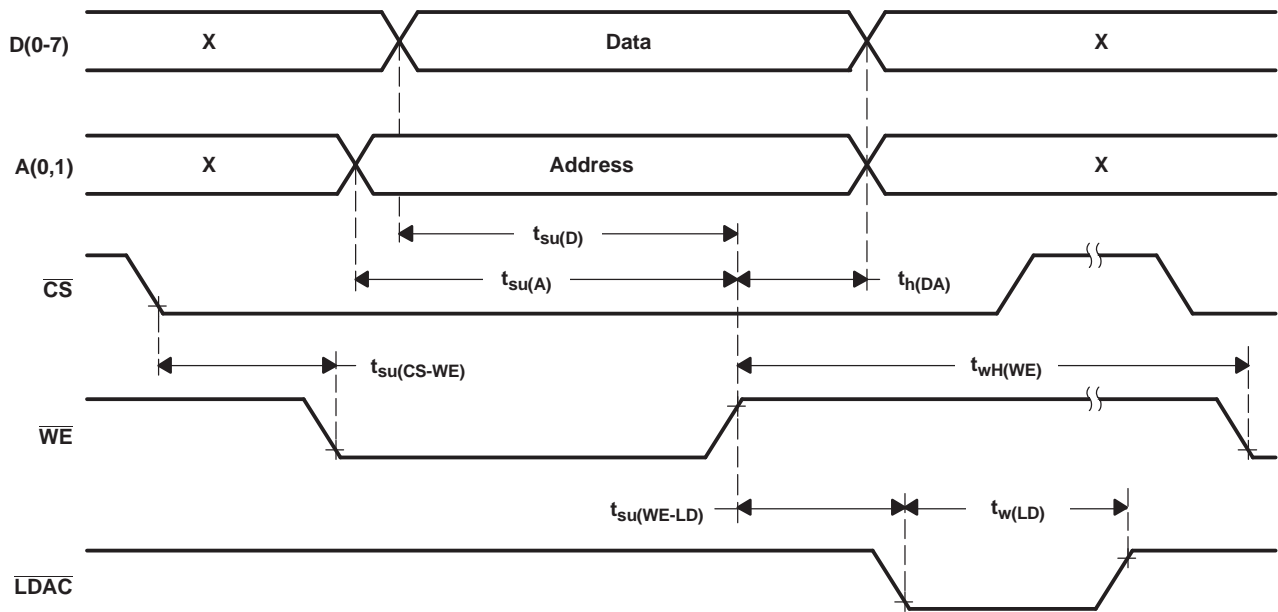
ANALOG OUTPUT DYNAMIC PERFORMANCE						
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ <sup>(1)</sup>	Fast	1	3	$\mu\text{s}$
			Slow	3.5	7	
$t_{s(CC)}$	Output settling time, code to code	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ <sup>(2)</sup>	Fast	0.5	1.5	$\mu\text{s}$
			Slow	1	2	
SR	Slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ <sup>(3)</sup>	Fast	6	10	V/ $\mu\text{s}$
			Slow	1.2	1.7	
	Glitch energy	$DIN = 0$ to 1, $f_{CLK} = 100\text{ kHz}$ , $\overline{CS} = V_{DD}$		5		nV-S
SNR	Signal-to-noise ratio	$f_s = 480\text{ kSPS}$ , $f_B = 20\text{ kHz}$ , $f_{out} = 1\text{ kHz}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$	73	78		dB
SINAD	Signal-to-noise + distortion		61	67		
THD	Total harmonic distortion			-69	-62	
SFDR	Spurious free dynamic range		63	74		

- Settling time is the time for the output signal to remain within  $\pm 0.5$  LSB of the final measured value for a digital input code change of 0x020 to 0xFDF or 0xFDF to 0x020 respectively.
- Settling time is the time for the output signal to remain within  $\pm 0.5$  LSB of the final measured value for a digital input code change of one count.
- Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

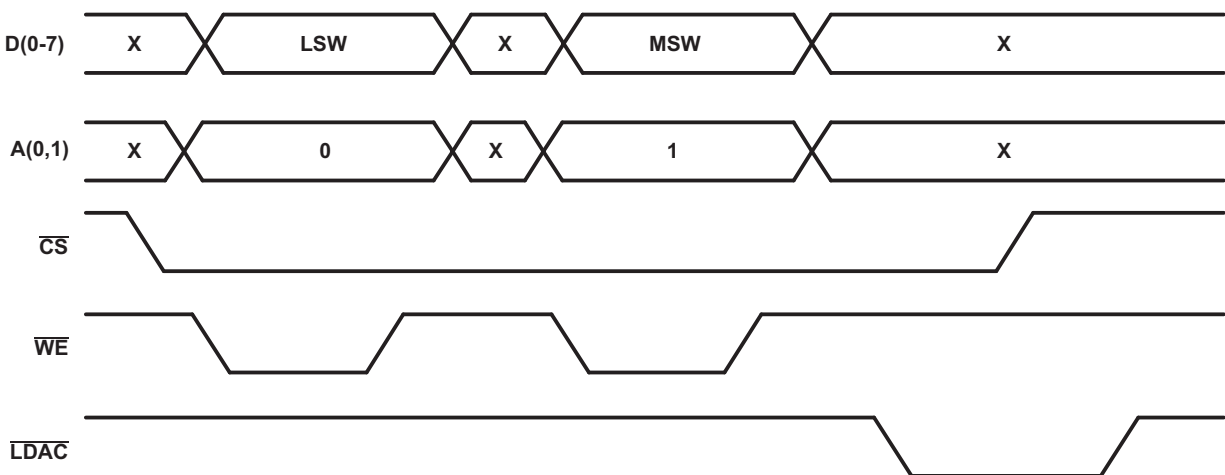
**DIGITAL INPUT TIMING REQUIREMENTS**

		MIN	NOM	MAX	UNIT
$t_{su(CS-WE)}$	Setup time, $\overline{CS}$ low before negative $\overline{WE}$ edge	15			ns
$t_{su(D)}$	Setup time, data ready before positive $\overline{WE}$ edge	10			ns
$t_{su(A)}$	Setup time, addresses ready before positive $\overline{WE}$ edge	20			ns
$t_{h(DA)}$	Hold time, data and addresses held valid after positive $\overline{WE}$ edge	5			ns
$t_{su(WE-LD)}$	Setup time, positive $\overline{WE}$ edge before $\overline{LDAC}$ low	5			ns
$t_{wH(WE)}$	Pulse duration, $\overline{WE}$ high	20			ns
$t_{w(LD)}$	Pulse duration, $\overline{LDAC}$ low	23			ns

**PARAMETER MEASUREMENT INFORMATION**

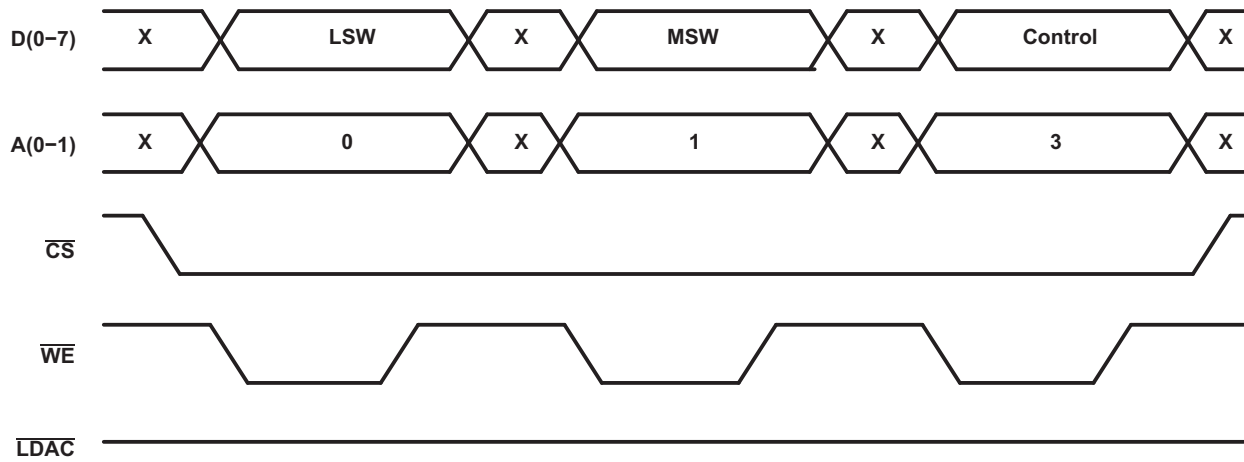


**Figure 1. Timing Diagram**



**Figure 2. Example of a Complete Write Cycle (MSW, LSW) Using  $\overline{LDAC}$  for Update**

**PARAMETER MEASUREMENT INFORMATION (continued)**



**Figure 3. Example of a Complete Write Cycle (MSW, LSW, Control)**

TYPICAL CHARACTERISTICS  
DIFFERENTIAL NONLINEARY ERROR

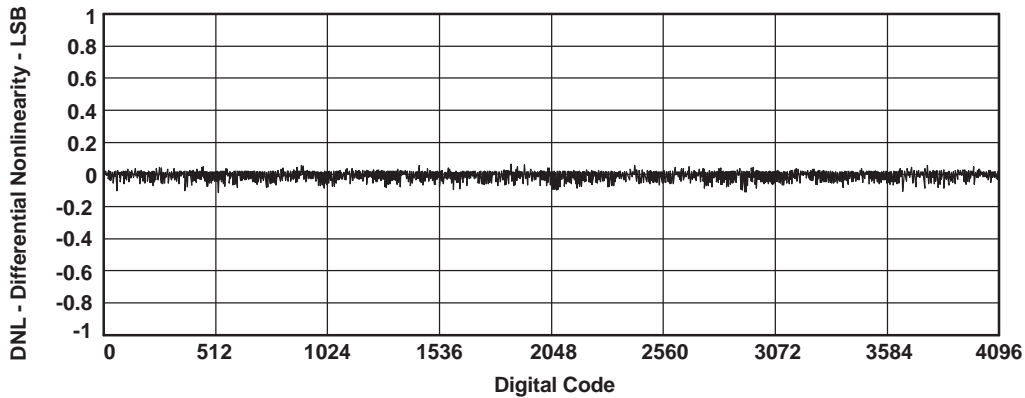


Figure 4.

INTEGRAL NONLINEARTIY ERROR

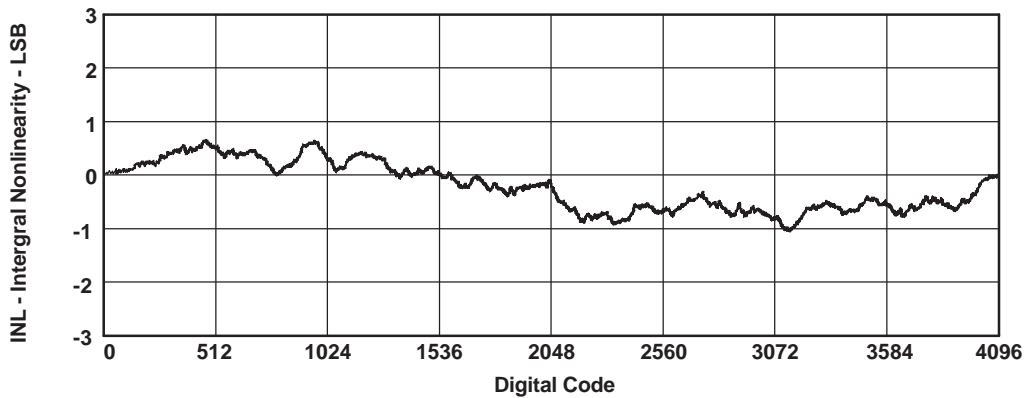


Figure 5.

MAXIMUM OUTPUT VOLTAGE  
vs  
LOAD CURRENT

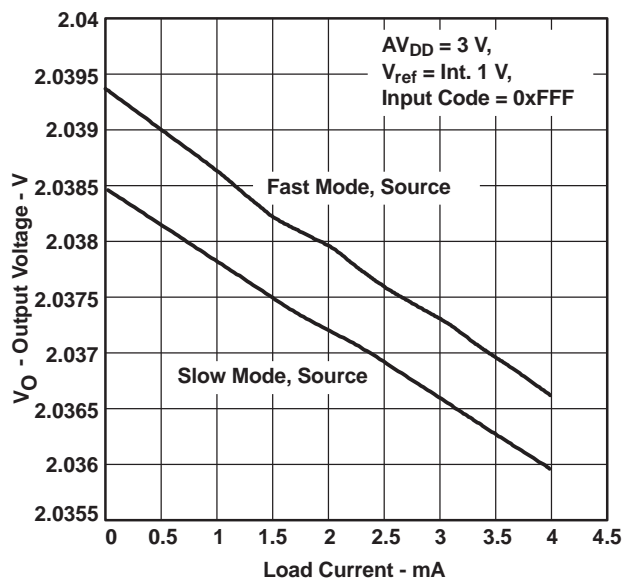


Figure 6.

MAXIMUM OUTPUT VOLTAGE  
vs  
LOAD CURRENT

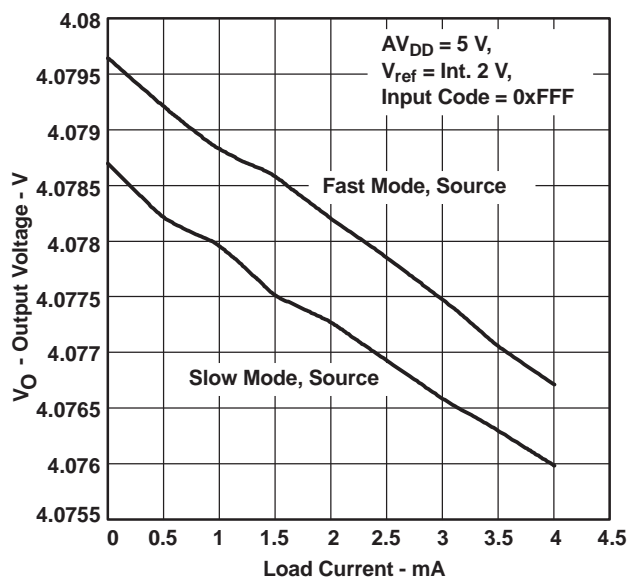
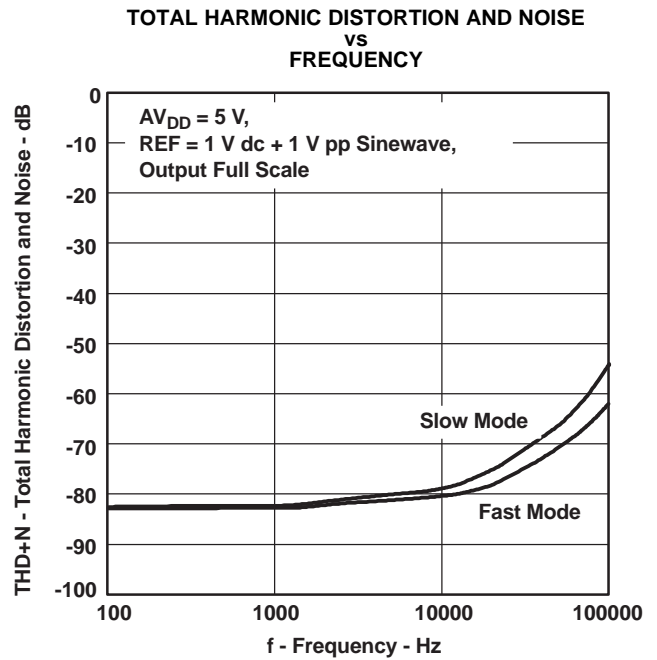
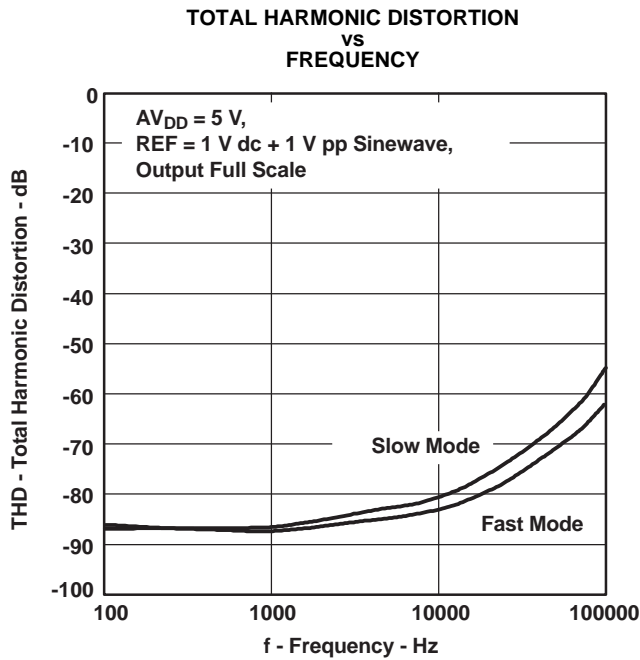
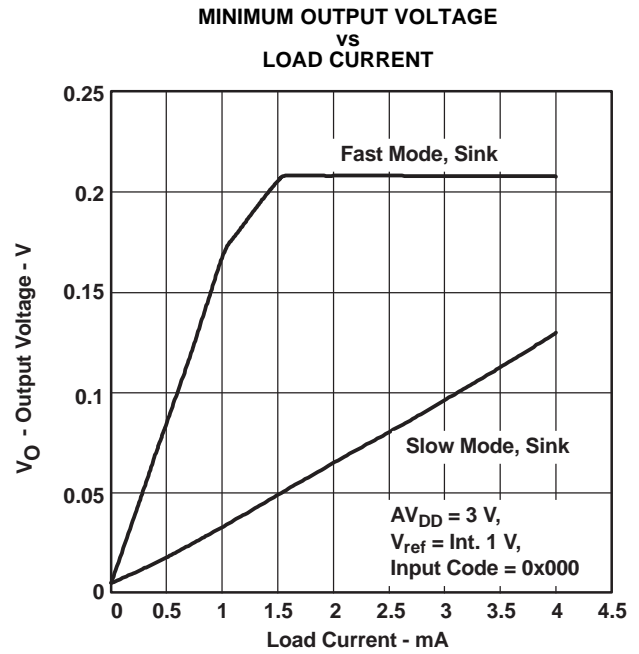
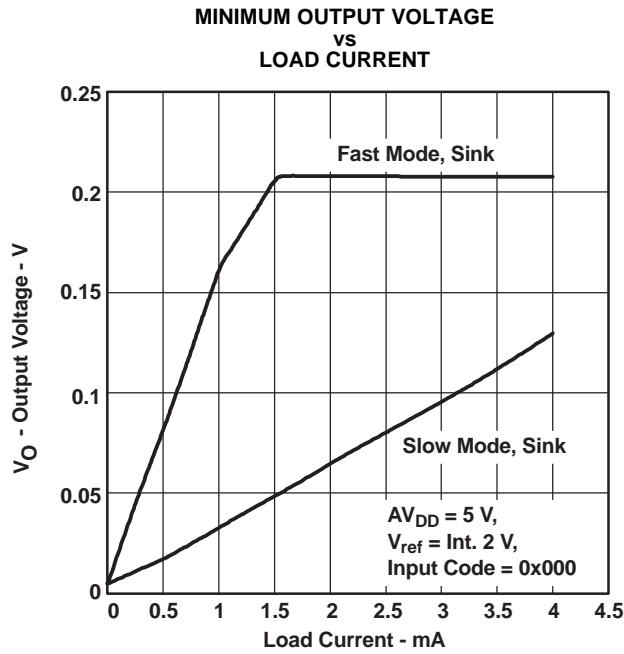


Figure 7.

**TYPICAL CHARACTERISTICS (continued)**



TYPICAL CHARACTERISTICS (continued)

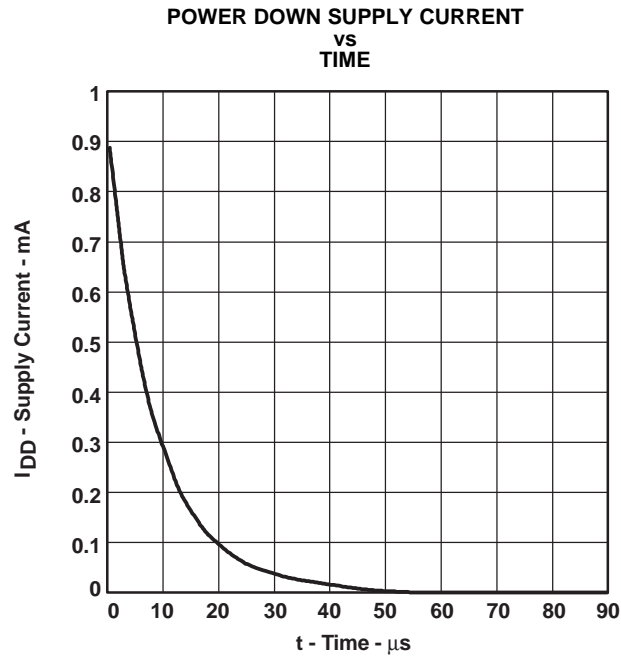


Figure 12.

## APPLICATION INFORMATION

### GENERAL FUNCTION

The TLV5633 is a 12-bit, single supply DAC, based on a resistor string architecture. It consists of a parallel interface, a speed and power down control logic, a programmable internal reference, a resistor string, and a rail-to-rail output buffer. The output voltage (full scale determined by reference) is given by:

$$2 \text{ REF } \frac{\text{CODE}}{0 \times 1000} \text{ [V]}$$

Where REF is the reference voltage and CODE is the digital input value in the range 0x000 to 0xFFFF. A power on reset initially puts the internal latches to a defined state (all bits zero).

### PARALLEL INTERFACE

The device latches data on the positive edge of  $\overline{\text{WE}}$ . It must be enabled with  $\overline{\text{CS}}$  low. Whether the data is written to one of the DAC holding latches (MSW, LSW) or the control register depends on the address bits A1 and A0.  $\overline{\text{LDAC}}$  low updates the DAC with the value in the holding latch.  $\overline{\text{LDAC}}$  is an asynchronous input and can be held low, if a separate update is not necessary. However, to control the DAC using the load feature, there should be approximately a 5 ns delay after the positive  $\overline{\text{WE}}$  edge before driving  $\overline{\text{LDAC}}$  low. Two more asynchronous inputs, SPD and  $\overline{\text{PWR}}$  control the settling times and the power-down mode:

SPD:    Speed control    1 → fast mode                    0 → slow mode  
 $\overline{\text{PWR}}$ :    Power control    1 → normal operation            0 → power down

It is also possible to program the different modes (fast, slow, power down) and the DAC update latch using the control register. The following tables list the possible combinations of control signals and control bits.

PIN	BIT	MODE
SPD	SPD	
0	0	Slow
0	1	Fast
1	0	Fast
1	1	Fast

PIN	BIT	POWER
$\overline{\text{PWR}}$	PWD	
0	0	Down
0	1	Down
1	0	Normal
1	1	Down

PIN	BIT	LATCH
$\overline{\text{LDAC}}$	RLDAC	
0	0	Transparent
0	1	Transparent
1	0	Hold
1	1	Transparent

## DATA FORMAT

The TLV5633 writes data either to one of the DAC holding latches or to the control register depending on the address bits A1 and A0.

### ADDRESS BITS

A1	A0	REGISTER
0	0	DAC LSW holding
0	1	DAC MSW holding
1	0	Reserved
1	1	Control

The following table lists the meaning of the bits within the control register.

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	REF1	REF0	RLDAC	PWR	SPD
X <sup>(1)</sup>	X <sup>(1)</sup>	X <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>

(1) Default values: X = Don't Care

SPD: Speed control bit    1 → fast mode            0 → slow mode

PWR: Power control bit    1 → power down            0 → normal operation

RLDAC: Load DAC latch    1 → latch transparent    0 → DAC latch controlled by  $\overline{\text{LDAC}}$  pin

REF1 and REF0 determine the reference source and the reference voltage.

### REFERENCE BITS

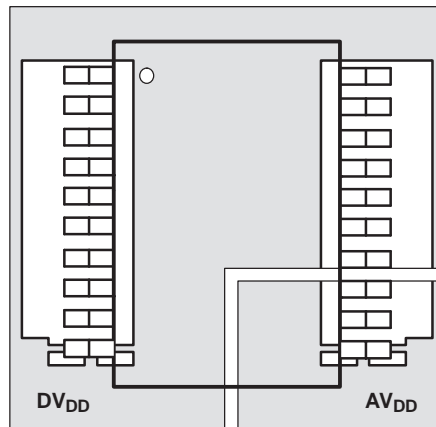
REF1	REF0	REFERENCE
0	0	External
0	1	1.024 V
1	0	2.048 V
1	1	External

If an external reference voltage is applied to the REF pin, external reference must be selected.

## LAYOUT CONSIDERATIONS

To achieve the best performance, it is recommended to have separate power planes for GND,  $AV_{DD}$ , and  $DV_{DD}$ . [Figure 13](#) shows how to lay out the power planes for the TLV5633. As a general rule, digital and analog signals should be separated as wide as possible. To avoid crosstalk, analog and digital traces must not be routed in parallel. The two positive power planes ( $AV_{DD}$  and  $DV_{DD}$ ) should be connected together at one point with a ferrite bead.

A 100-nF ceramic low series inductance capacitor between  $DV_{DD}$  and GND and a 1- $\mu\text{F}$  tantalum capacitor between  $AV_{DD}$  and GND placed as close as possible to the supply pins are recommended for optimal performance.



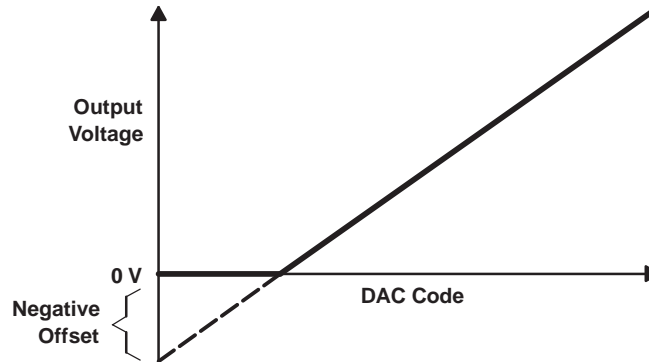
**Figure 13. TLV5633 Board Layout**

### LINEARITY, OFFSET, AND AGAIN ERROR USING SINGLE END SUPPLIES

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in [Figure 14](#).



**Figure 14. Effect of Negative Offset (Single Supply)**

The offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full scale code and the lowest code that produces a positive output voltage.

### TLV5633 INTERFACED to an Intel MCS<sup>®</sup>51 Controller

The circuit in Figure 15 shows how to interface the TLV5633 to an Intel MCS<sup>®</sup>51 microcontroller. The address bus and the data bus of the controller are multiplexed on port 0 (non page mode) to save port pins. To separate the address bits and the data bits, the controller provides a dedicated signal, address latch enable (ALE), which is connected to a latch at port 0.

An address decoder is required to generate the chip select signal for the TLV5633. In this example, a simple 3-to-8 decoder (74AC138) is used for the interface as shown in Figure 15. The DAC is memory mapped at addresses 0x8000/1/2/3 within the data memory address space and mirrored every 32 address locations (0x8020/1/2/3, 0x8040/1/2/3, etc.). In a typical microcontroller system, programmable logic should be used to generate the chip select signals for the entire system.

The data pins and the  $\overline{WE}$  pin of the TLV5633 can be connected directly to the multiplexed address and data bus and the  $\overline{WR}$  signal of the controller.

The application uses the TLV5633 device's internal reference at 2.048 V. The  $\overline{LDAC}$  pin is connected to P3.5 and is used to update the DAC after both data bytes have been written.

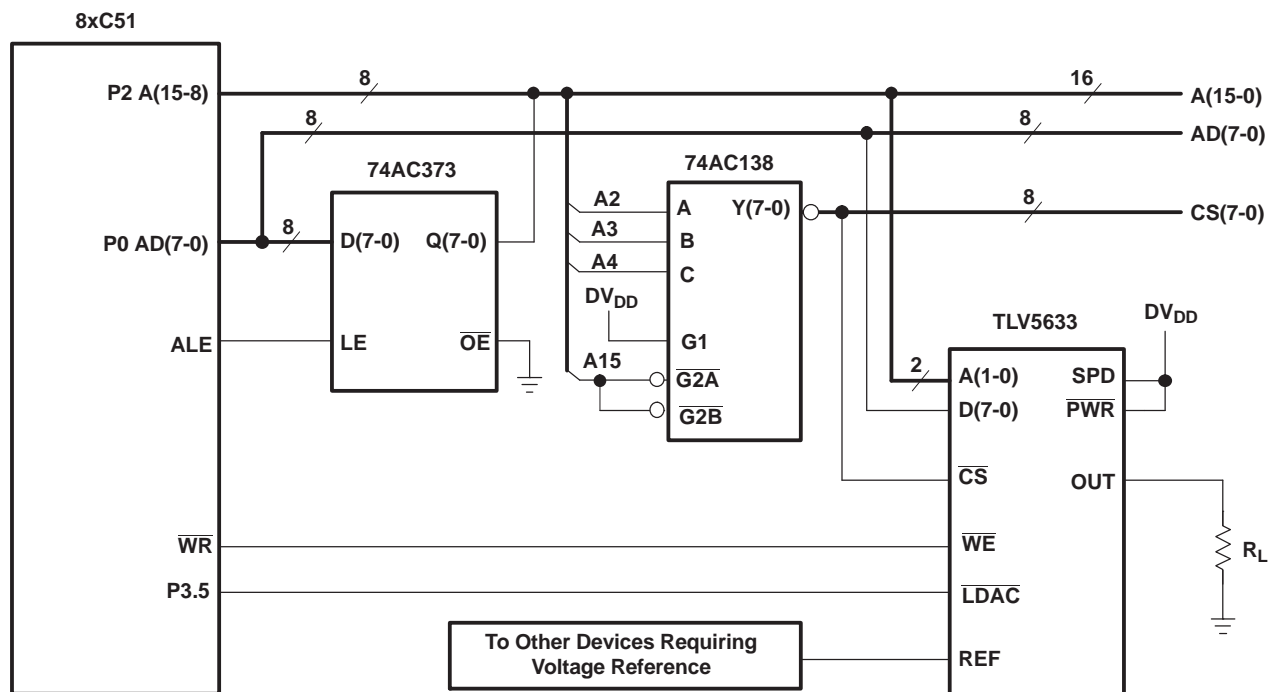


Figure 15. TLV5633 Interfaced to an Intel MCS<sup>®</sup>51 Controller

## SOFTWARE

In the following example, the code generates a waveform at 20 KSPS with 32 samples stored in a table within the program memory space of the microcontroller.

The waveform data is located in the program memory space at segment SINTBL beginning with the MSW of the first 16-bit word (the 4 MSBs are ignored), followed by the LSW. Two bytes are required for each DAC word (the table is not shown in the code example).

The program consists of two parts:

- A main routine, which is executed after reset and which initializes the timer and the interrupt system of the microcontroller.
- An interrupt service routine, which reads a new value from the waveform table and writes it to the DAC.

```

;-----
; File:          WAVE.A51
; Function:     wave generation with TLV5633
; Processors:  80C51 family (running at 12 MHz)
; Software:    ASM51 assembler, Keil BL51 code-banking linker
; (C) 1999 Texas Instruments
;-----
;-----
; Program function declaration
;-----
NAME      WAVE
MAIN      SEGMENT      CODE
ISR       SEGMENT      CODE
WAVTBL    SEGMENT      CODE
VAR1      SEGMENT      DATA
STACK     SEGMENT      IDATA
;-----
; Code start at address 0, jump to start
;-----
CSEG AT 0
    LJMP start          ; Execution starts at address 0 on power-up.
;-----
; Code in the timer0 interrupt vector
;-----
CSEG AT 0BH
    LJMP timer0ISR     ; Jump vector for timer 0 interrupt is 000Bh
;-----
; Define program variables
;-----
RSEG VAR1
rolling_ptr: DS 1
;-----
; Interrupt service routine for timer 0 interrupts
;-----
    RSEG ISR
TIMER0ISR:
    PUSH PSW
    PUSH ACC
    ; The signal to be output on the dac is stored in a table
    ; as 32 samples of msb, lsb pairs (64 bytes).
    ; The pointer, rolling_ptr, rolls round the table of samples
    ; incrementing by 2 bytes (1 sample) on each interrupt
    ; (at the end of this routine).
    MOV DPTR, #wavetable ; set DPTR to the start of the table
    MOV R0, #001H        ; R0 selects DAC MSW
    MOV A,rolling_ptr    ; ACC loaded with the pointer into the wave table
    MOVC A,@A+DPTR       ; get msb from the table
    MOVX @R0, A          ; write DAC MSW
    MOV R0, #000H        ; R0 selects DAC LSW
    MOV A,rolling_ptr    ; move rolling pointer back in to ACC
    INC A                ; increment ACC holding the rolling pointer
    MOVC A,@A+DPTR       ; which is the lsb of this sample, now in ACC
    MOVX @R0, A          ; write DAC LSW
    MOV A,rolling_ptr    ; load ACC with rolling pointer again
    INC A                ; increment the ACC twice, to get next sample
    INC A
    ANL A,#003FH         ; wrap back round to 0 if >64
    MOV rolling_ptr,A    ; move value held in ACC back to the rolling pointer

```

```

CLR T1          ; set LDACB = 0 (update DAC)
SETB T1         ; set LDACB = 1
POP ACC
POP PSW
RETI

;-----
; Set up stack
;-----
RSEG STACK
DS 10h ; 16 Byte Stack!
;-----
; Main Program
;-----
RSEG MAIN
start:
MOV SP,#STACK-1 ; first set Stack Pointer
CLR A
MOV rolling_ptr,A ; set rolling pointer to 0
MOV TMOD,#002H ; set timer 0 to mode 2 - auto-reload
MOV TH0,#0CEH ; set timer 2 re-load value for 20 kHz interrupts
MOV P2, #080H ; set A15 of address bus high to 'memory map'
; device up beyond used address space
SETB T1 ; set LDACB = 1 (on P3.5)
; TLV5633 setup
MOV R0, #003H ; R0 selects control register
MOV A, #011H ; LOAD ACC with control register value:
; REF1=1, REF0=0 -> 2.048V internal reference
; RLDAC=0 -> use LDACB pin to control DAC
; PD=0 -> DAC enabled
; SPD=1 -> FAST mode
; write control word:
MOVX @R0, A ; write DAC control word
SETB ET0 ; enable timer 0 interrupts
SETB EA ; enable all interrupts
SETB TR0 ; start timer 0
always:
SJMP always
RET
;-----
; Table of 32 wave samples used as DAC data
;-----
RSEG WAVTBL
wavetable:
;...insert 32 samples here...
.END

```

## **DEFINITIONS OF SPECIFICATIONS AND TERMINOLOGY**

### **Integral Nonlinearity (INL)**

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

### **Differential Nonlinearity (DNL)**

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1-LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

### **Zero-Scale Error ( $E_{ZS}$ )**

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

### **Gain Error ( $E_G$ )**

Gain error is the error in slope of the DAC transfer function.

### **Signal-To-Noise Ratio + Distortion (SINAD)**

Signal-to-noise ratio + distortion is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

### **Spurious Free Dynamic Range (SFDR)**

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

### **Total Harmonic Distortion (THD)**

Total harmonic distortion is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.

### Revision history

Revision	Date	Description
A	01/2001	Minor typographical changes.
B	08/2003	Changed the High-level and Low-level digital input voltage in the <i>Recommended Operating Conditions</i> table.
C	09/2006	Changed the positions of LSW and MSW in <a href="#">Figure 2</a> and <a href="#">Figure 3</a> .

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV5633CDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5633C	<a href="#">Samples</a>
TLV5633CPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5633	<a href="#">Samples</a>
TLV5633IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5633I	<a href="#">Samples</a>
TLV5633IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5633	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

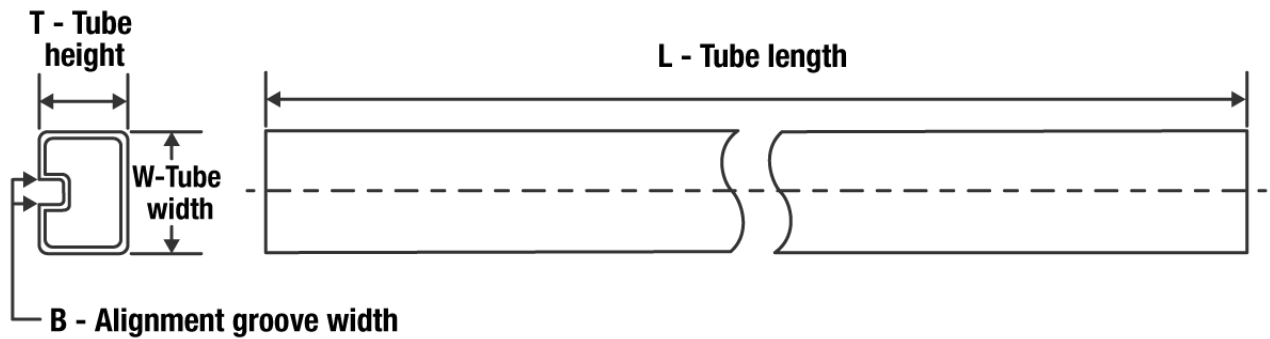
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV5633CDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV5633CPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TLV5633IDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLV5633IPW	PW	TSSOP	20	70	530	10.2	3600	3.5

# PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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