



**THE DATASHEET OF  
TPS40077PWPG4**



## OPA167x-Q1 Automotive, Low-Distortion Audio Operational Amplifiers

### 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
- Low noise:  $4.5\text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz
- Low distortion: 0.0001% at 1 kHz
- High open-loop gain: 114 dB
- Low quiescent current:
  - 2 mA per channel
- Low input bias current: 10 pA (typical)
- Slew rate:  $9\text{ V}/\mu\text{s}$
- Wide gain bandwidth: 16 MHz ( $G = 1$ )
- Rail-to-rail output
- Wide supply range:
  - $\pm 2.25\text{ V}$  to  $\pm 18\text{ V}$ , or  $4.5\text{ V}$  to  $36\text{ V}$
- Available packages:
  - Dual: SOIC-8 (Preview)
  - Quad: Small QFN-16

### 2 Applications

- [Telematics control unit](#)
- [Emergency call \(eCall\)](#)
- [Aftermarket telematics](#)
- [Automotive head unit](#)
- [Automotive active noise cancellation](#)
- [Automotive external amplifier](#)

### 3 Description

The dual-channel OPA1678-Q1 and quad-channel OPA1679-Q1 (OPA167x-Q1) operational amplifiers offer higher system-level performance over legacy op amps commonly used in audio circuitry. The OPA167x-Q1 amplifiers achieve a low  $4.5\text{-nV}/\sqrt{\text{Hz}}$  noise density and low distortion of 0.0001% at 1 kHz, which improves audio signal fidelity. These devices also offer rail-to-rail output swing to within 800 mV with a 2-k $\Omega$  load, which increases headroom and maximizes dynamic range.

To accommodate the power-supply constraints of many types of audio products, the OPA167x-Q1 operate over a very wide supply range of  $\pm 2.25\text{ V}$  to  $\pm 18\text{ V}$  (or  $4.5\text{ V}$  to  $36\text{ V}$ ) on only 2 mA of supply current. These op amps are unity-gain stable and have excellent dynamic behavior over a wide range of load conditions allowing the OPA167x-Q1 to be used in many audio circuits.

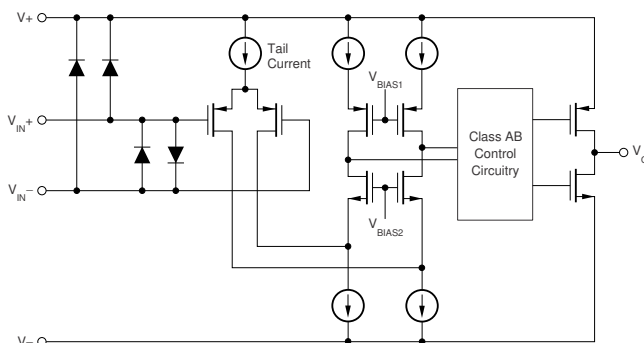
The OPA167x-Q1 temperature ranges are specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

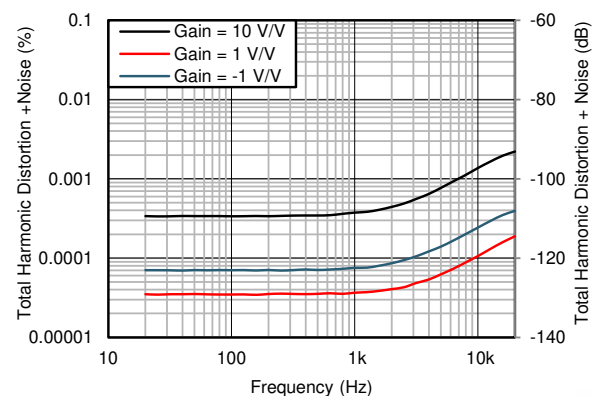
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1678-Q1 (Preview)	SOIC (8)	4.90 mm x 3.91 mm
OPA1679-Q1	QFN (16)	4.00 mm x 4.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

#### Simplified Internal Schematic



#### THD+N vs Frequency (2-k $\Omega$ Load)



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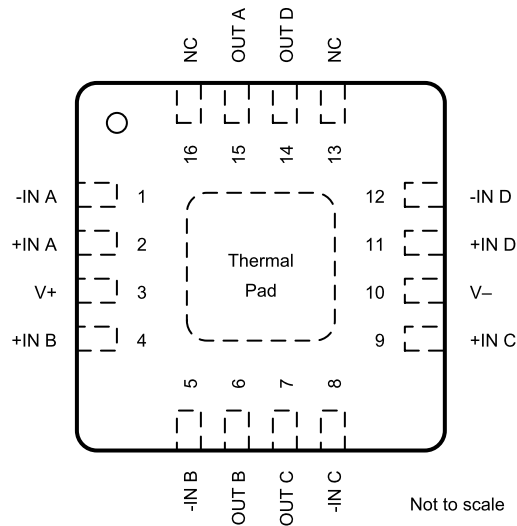
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## 4 Revision History

DATE	REVISION	NOTES
June 2020	*	Initial release.

## 5 Pin Configuration and Functions

**OPA1679-Q1 RUM Package  
16-Pin QFN With Exposed Thermal Pad  
Top View**



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	1	I	Inverting input, channel A
+IN A	2	I	Noninverting input, channel A
-IN B	5	I	Inverting input, channel B
+IN B	4	I	Noninverting input, channel B
-IN C	8	I	Inverting input, channel C
+IN C	9	I	Noninverting input, channel C
-IN D	12	I	Inverting input, channel D
+IN D	11	I	Noninverting input, channel D
NC	13	—	No connect
NC	16	—	No connect
OUT A	15	O	Output, channel A
OUT B	6	O	Output, channel B
OUT C	7	O	Output, channel C
OUT D	14	O	Output, channel D
V+	3	—	Positive (highest) power supply
V-	10	—	Negative (lowest) power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage, V <sub>S</sub> = (V+) – (V–)		40	V
	Input voltage	(V–) – 0.5	(V+) + 0.5	V
	Input current (all pins except power-supply pins)	–10	10	mA
	Output short-circuit current <sup>(2)</sup>	Continuous		
T <sub>A</sub>	Operating temperature	–55	125	°C
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	–65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Short-circuit to V<sub>S</sub> / 2 (ground asymmetrical dual-supply setups), one amplifier per package.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 HBM ESD classification level 2 <sup>(1)</sup>	±2000	V
		Charge device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	

- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>S</sub>	Supply voltage	Single-supply, V <sub>S</sub> = (V+)	4.5		36	V
		Dual-supply, V <sub>S</sub> = (V+) – (V–)	±2.25		±18	
T <sub>A</sub>	Operating temperature		–40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		OPA1679-Q1	UNIT
		RUM (QFN)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	38.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	34.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	17.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.6	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	7.1	°C/W

- For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 2\text{ k}\Omega$ , and  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
<b>AUDIO PERFORMANCE</b>								
THD+N	Total harmonic distortion + noise	$G = 1$ , $R_L = 600\ \Omega$ , $f = 1\text{ kHz}$ , $V_O = 3\ V_{RMS}$			0.0001%			
					-120		dB	
IMD	Intermodulation distortion	$G = 1$ , $V_O = 3\ V_{RMS}$	SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz)		0.0001%			
					-120		dB	
			DIM 30 (3-kHz square wave and 15 kHz sine wave)		0.0001%			
					-120		dB	
			CCIF twin-tone (19 kHz and 20 kHz)		0.0001%			
					-120		dB	
<b>FREQUENCY RESPONSE</b>								
GBW	Gain-bandwidth product	$G = 1$			16		MHz	
SR	Slew rate	$G = -1$			9		V/ $\mu\text{s}$	
	Full power bandwidth <sup>(1)</sup>	$V_O = 1\ V_P$			1.4		MHz	
	Overload recovery time	$G = -10$			1		$\mu\text{s}$	
	Channel separation (dual and quad)	$f = 1\text{ kHz}$			-130		dB	
<b>NOISE</b>								
$e_n$	Input voltage noise	$f = 20\text{ Hz to } 20\text{ kHz}$			5.4		$\mu\text{V}_{RMS}$	
		$f = 0.1\text{ Hz to } 10\text{ Hz}$			1.74		$\mu\text{V}_{PP}$	
	Input voltage noise density	$f = 1\text{ kHz}$			4.5		$\text{nV}/\sqrt{\text{Hz}}$	
$i_n$	Input current noise density	$f = 1\text{ kHz}$			3		$\text{fA}/\sqrt{\text{Hz}}$	
<b>OFFSET VOLTAGE</b>								
$V_{OS}$	Input offset voltage	$V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$			$\pm 0.5$	$\pm 2$	mV	
		$V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$ , $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ <sup>(2)</sup>			2		$\mu\text{V}/^\circ\text{C}$	
PSRR	Power-supply rejection ratio	$V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$			3	8	$\mu\text{V}/\text{V}$	
<b>INPUT BIAS CURRENT</b>								
$I_B$	Input bias current	$V_{CM} = 0\text{ V}$			$\pm 10$		pA	
$I_{OS}$	Input offset current	$V_{CM} = 0\text{ V}$			$\pm 10$		pA	
<b>INPUT VOLTAGE RANGE</b>								
$V_{CM}$	Common-mode voltage range			$(V-) + 0.6$		$(V+) - 2$	V	
CMRR	Common-mode rejection ratio			100	110		dB	
<b>INPUT IMPEDANCE</b>								
	Differential				100    6		$\text{M}\Omega    \text{pF}$	
	Common-mode				6000    2		$\text{G}\Omega    \text{pF}$	
<b>OPEN-LOOP GAIN</b>								
$A_{OL}$	Open-loop voltage gain	$(V-) + 0.8\text{ V} \leq V_O \leq (V+) - 0.8\text{ V}$ , $R_L = 2\text{ k}\Omega$			94	114	dB	

(1) Full-power bandwidth =  $SR / (2\pi \times V_P)$ , where SR = slew rate.

(2) Specified by design and characterization.

**Electrical Characteristics (continued)**

 at  $T_A = 25^\circ\text{C}$ ,  $R_L = 2\text{ k}\Omega$ , and  $V_{CM} = V_{OUT} = \text{mid supply}$ , unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT</b>						
$V_O$	Voltage output	$R_L = 2\text{ k}\Omega$	(V-) + 0.8		(V+) – 0.8	V
$I_{OUT}$	Output Current					mA
$Z_O$	Open-loop output impedance					$\Omega$
$I_{SC}$	Short-circuit current <sup>(3)</sup>			$\pm 50$		mA
$C_L$	Capacitive load drive			100		pF
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current (per channel)	$I_O = 0\text{ A}$		2	2.5	mA
		$I_O = 0\text{ A}$ , $T_A = -40^\circ\text{C to } +125^\circ\text{C}^{(2)}$			2.8	

(3) One channel at a time.

## 6.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , (unless otherwise noted)

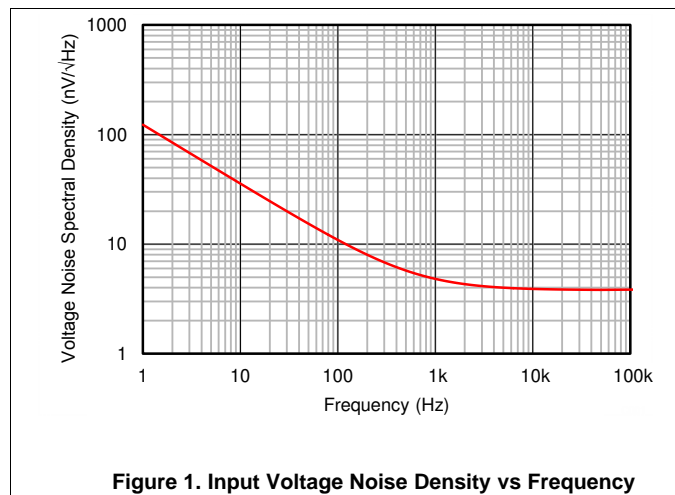


Figure 1. Input Voltage Noise Density vs Frequency

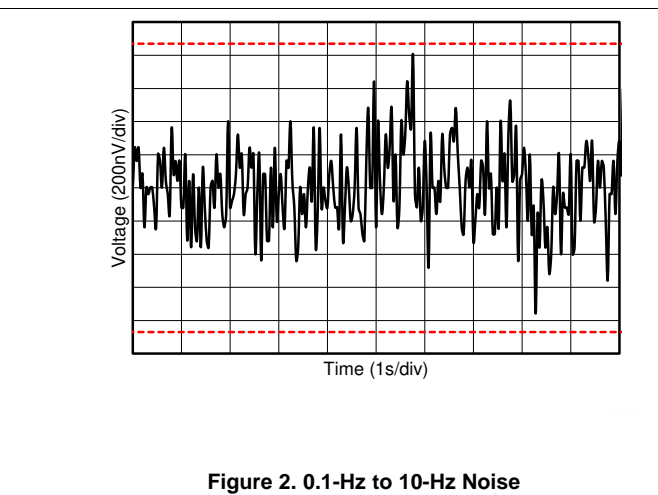


Figure 2. 0.1-Hz to 10-Hz Noise

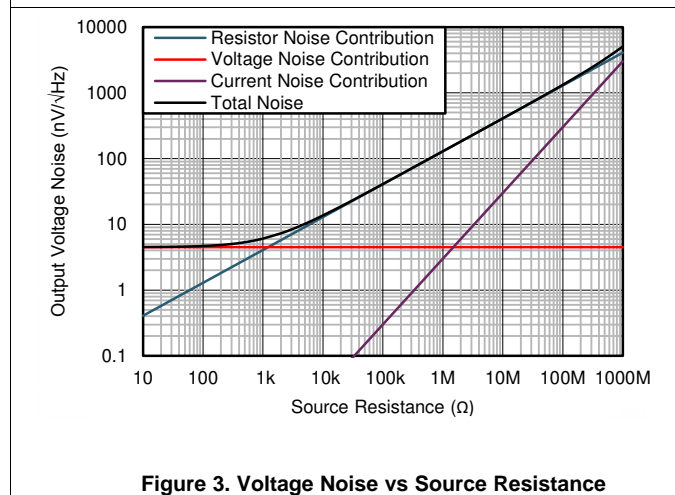


Figure 3. Voltage Noise vs Source Resistance

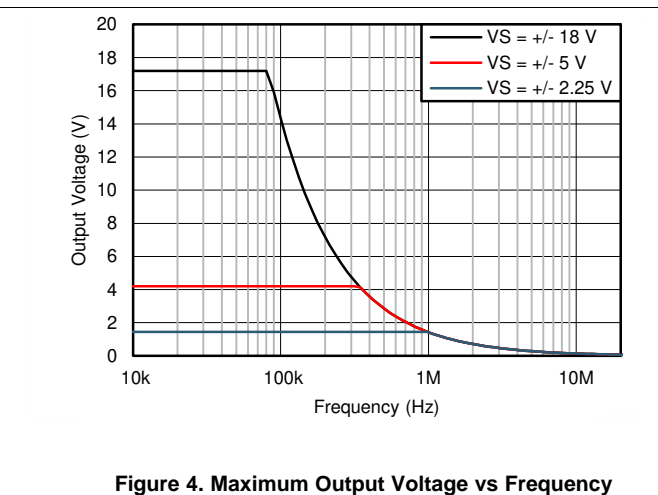


Figure 4. Maximum Output Voltage vs Frequency

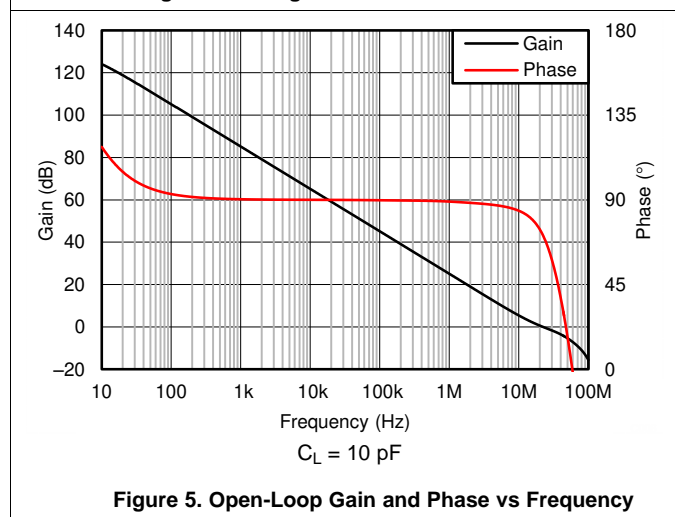


Figure 5. Open-Loop Gain and Phase vs Frequency

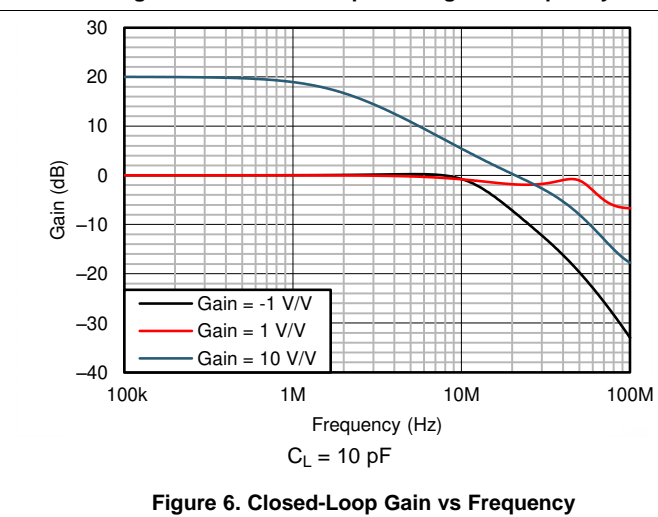


Figure 6. Closed-Loop Gain vs Frequency

### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , (unless otherwise noted)

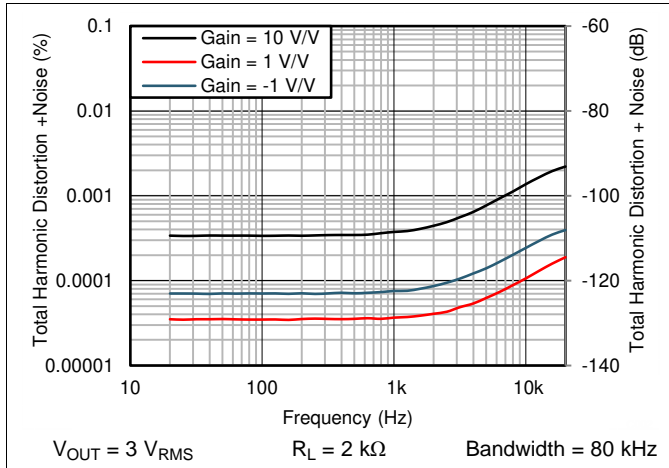


Figure 7. THD+N Ratio vs Frequency

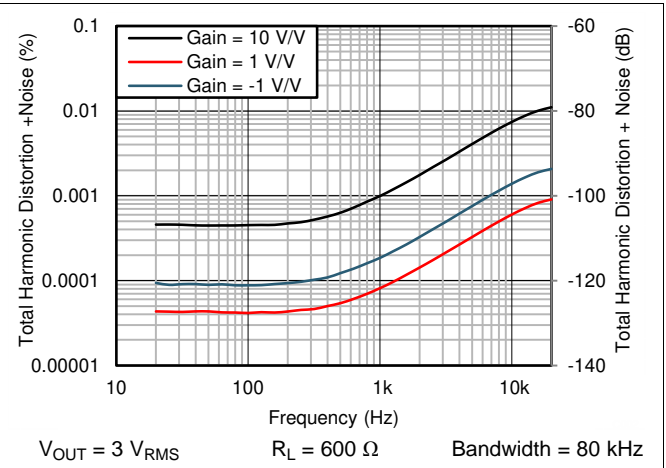


Figure 8. THD+N Ratio vs Frequency

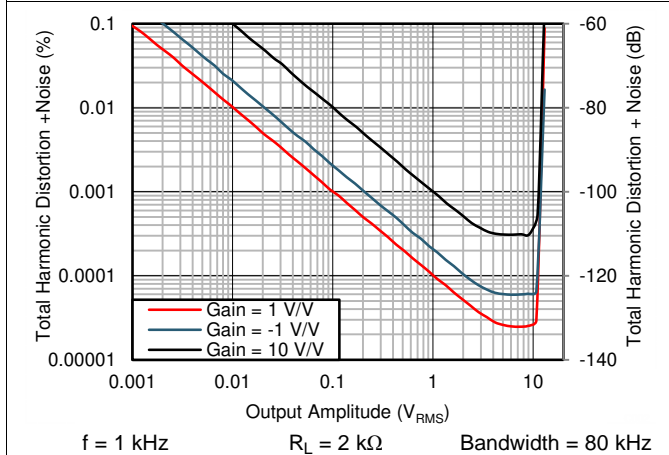


Figure 9. THD+N Ratio vs Output Amplitude

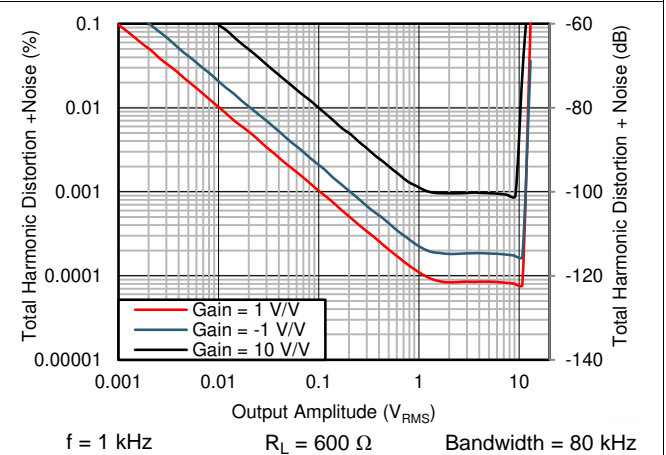


Figure 10. THD+N Ratio vs Output Amplitude

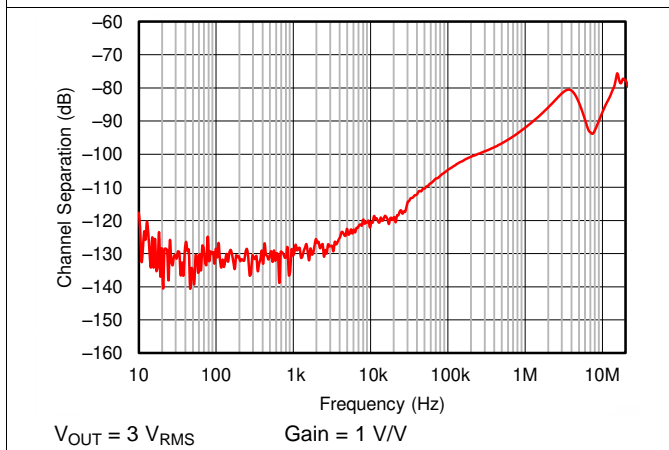


Figure 11. Channel Separation vs Frequency

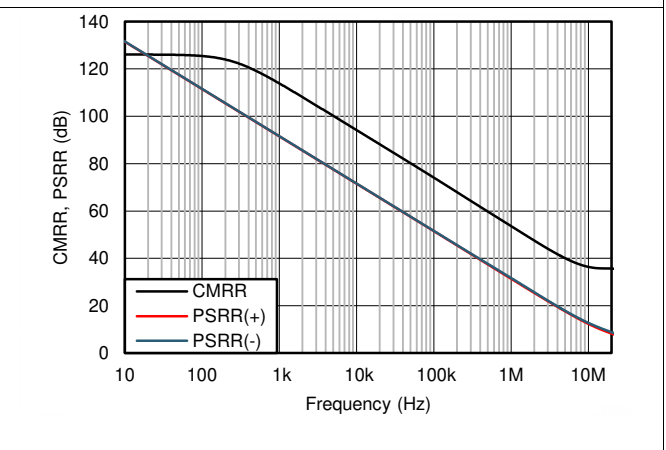
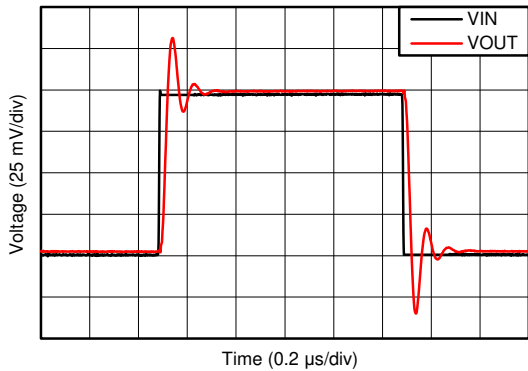


Figure 12. CMRR and PSRR vs Frequency (Referred to Input)

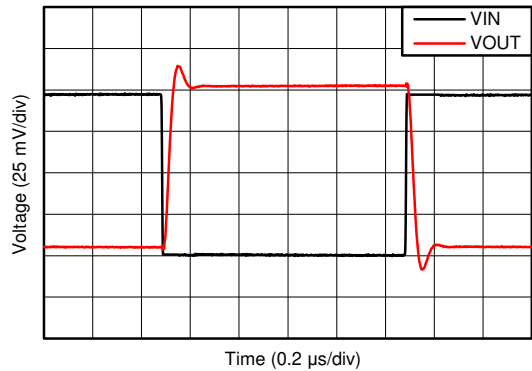
Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , (unless otherwise noted)



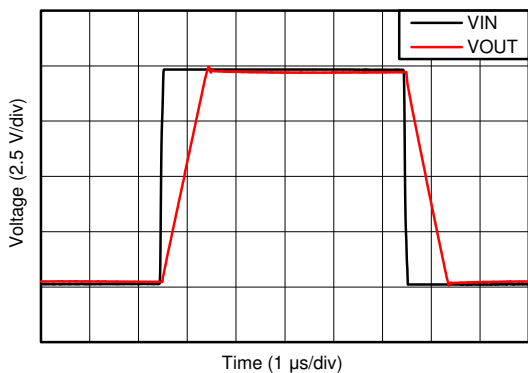
Gain = 1 V/V  $C_L = 100\text{ pF}$

Figure 13. Small-Signal Step Response (100 mV)



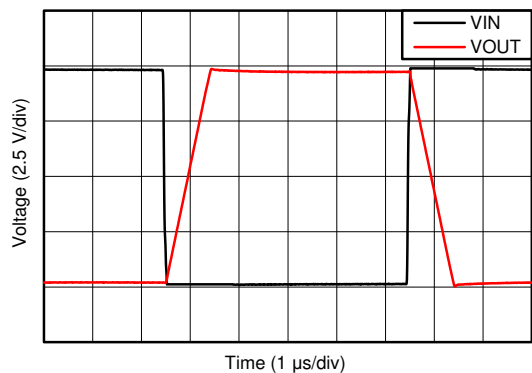
Gain = -1 V/V  $C_L = 100\text{ pF}$

Figure 14. Small-Signal Step Response (100 mV)



Gain = +1 V/V  $R_F = 2\text{ k}\Omega$   $C_L = 100\text{ pF}$

Figure 15. Large-Signal Step Response



Gain = -1 V/V  $C_L = 100\text{ pF}$

Figure 16. Large-Signal Step Response

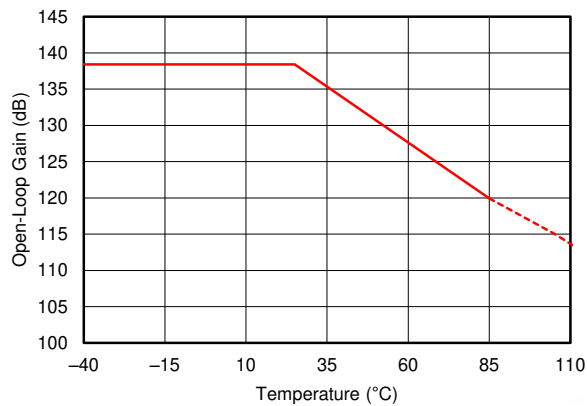


Figure 17. Open-Loop Gain vs Temperature

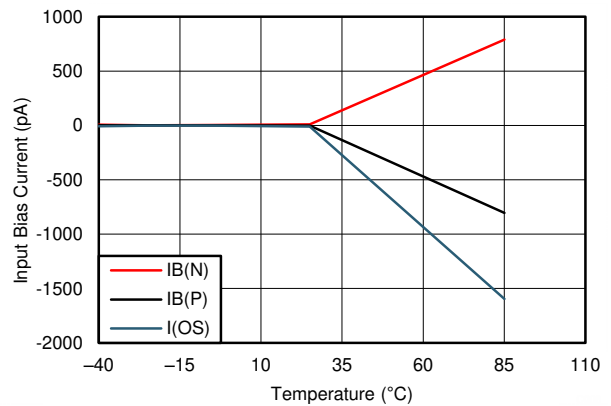


Figure 18.  $I_B$  and  $I_{OS}$  vs Temperature

### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , (unless otherwise noted)

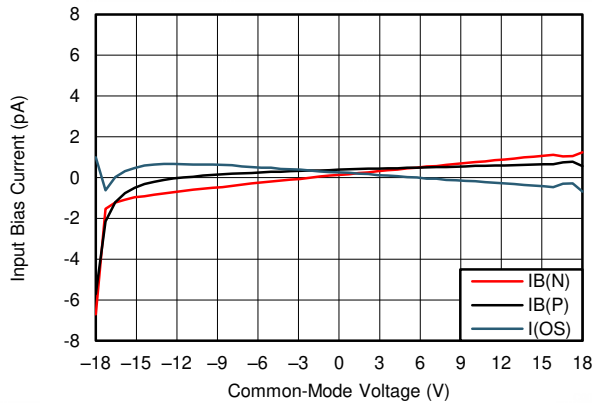


Figure 19.  $I_B$  and  $I_{OS}$  vs Common-Mode Voltage

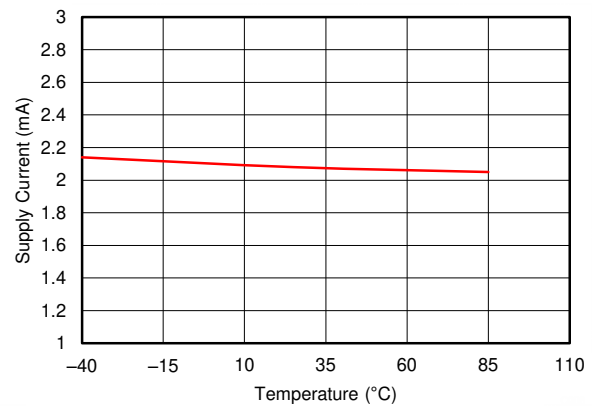


Figure 20. Supply Current vs Temperature

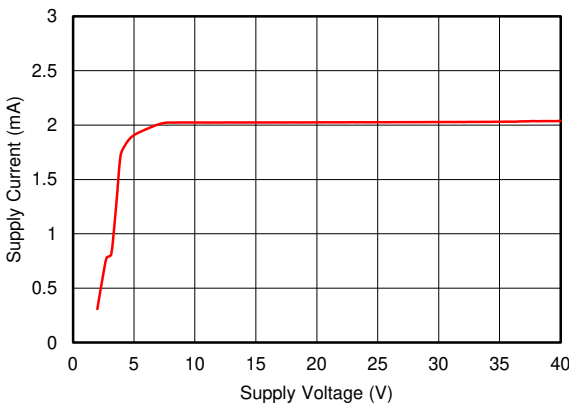


Figure 21. Supply Current vs Supply Voltage

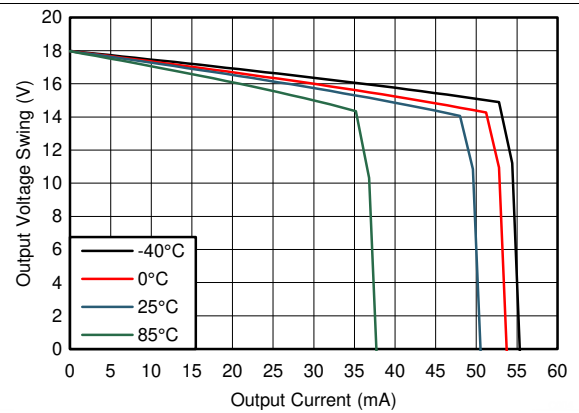


Figure 22. Output Voltage vs Output Current (Sourcing)

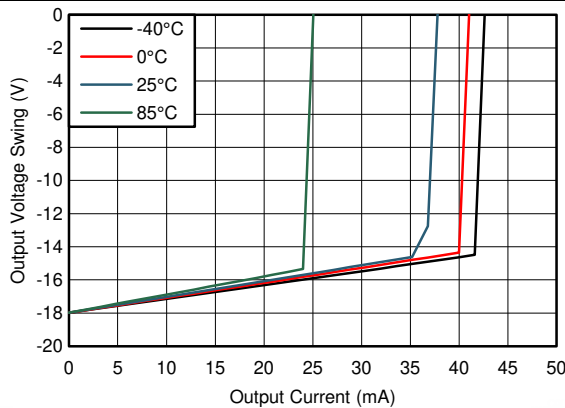


Figure 23. Output Voltage vs Output Current (Sinking)

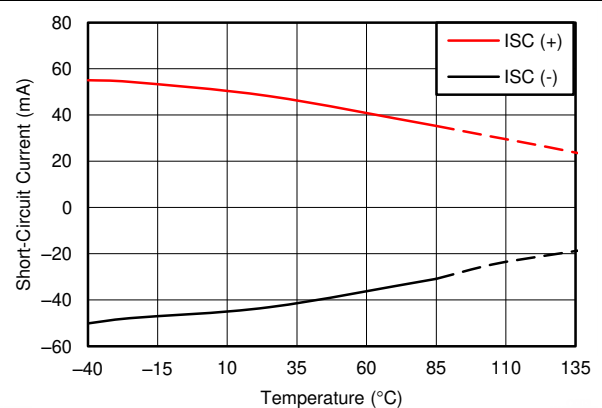


Figure 24. Short-Circuit Current vs Temperature

### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , (unless otherwise noted)

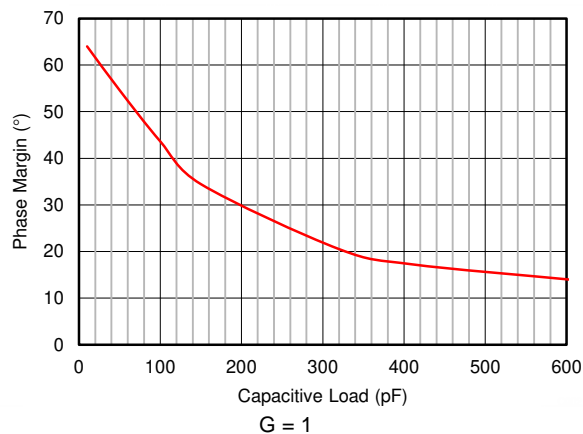


Figure 25. Phase Margin vs Capacitive Load

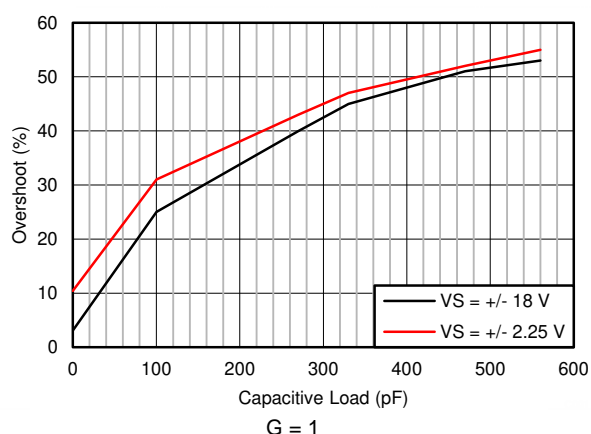


Figure 26. Percent Overshoot vs Capacitive Load

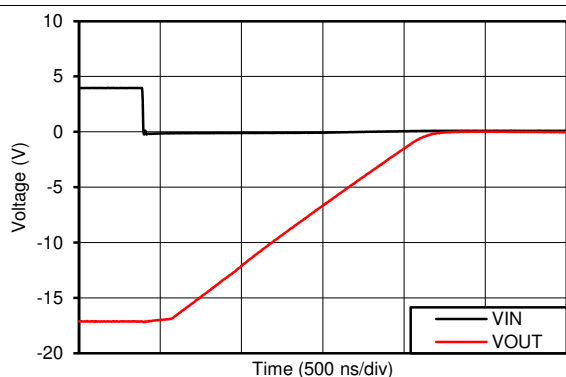


Figure 27. Negative Overload Recovery

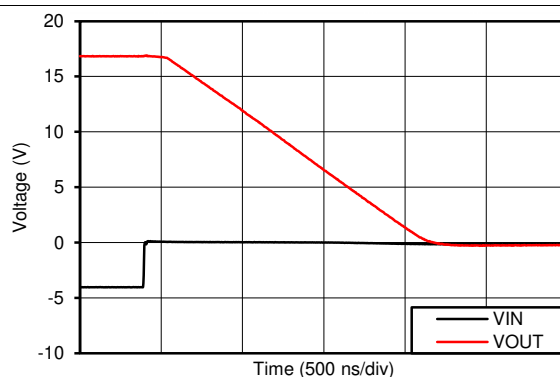


Figure 28. Positive Overload Recovery

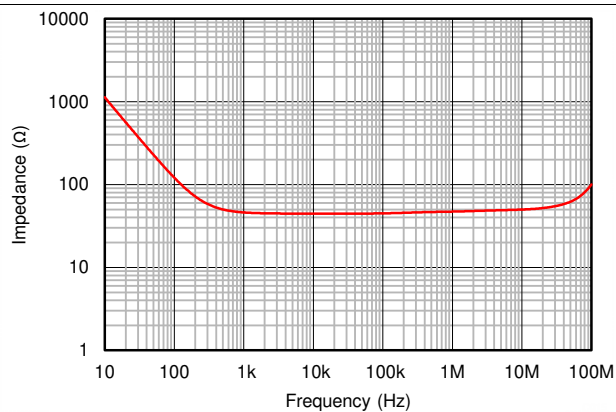


Figure 29. Open-Loop Output Impedance vs Frequency

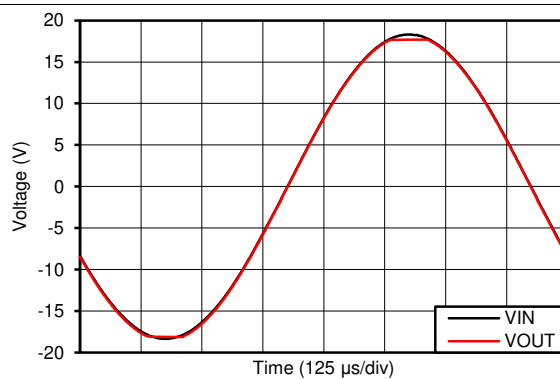


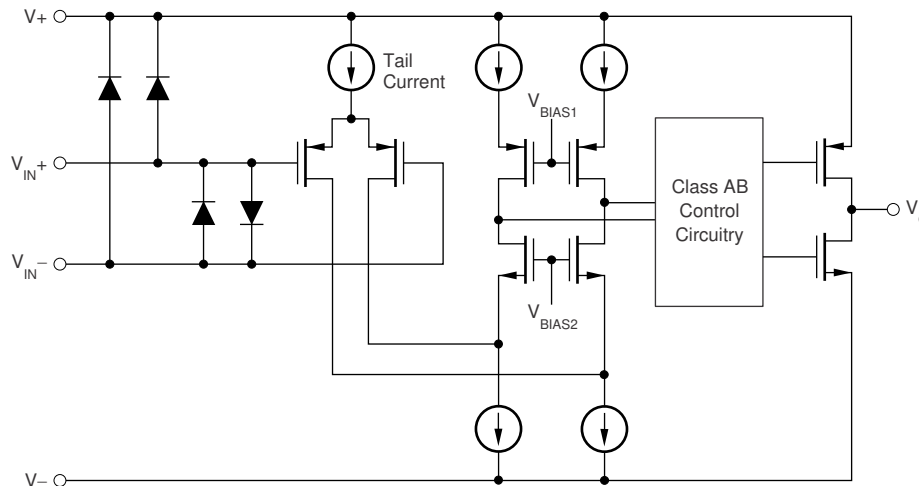
Figure 30. No Phase Reversal

## 7 Detailed Description

### 7.1 Overview

The OPA167x-Q1 automotive devices are unity-gain stable, dual-channel and quad-channel op amps with low noise and distortion. The [Functional Block Diagram](#) shows a simplified schematic of the OPA167x-Q1 (one channel shown). These devices consist of a low-noise input stage with a folded cascode and a rail-to-rail output stage. This topology exhibits superior noise and distortion performance across a wide range of supply voltages that are not delivered by legacy commodity audio operational amplifiers.

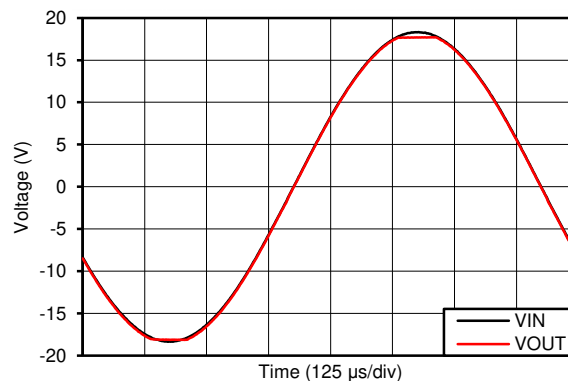
### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Phase Reversal Protection

The OPA167x-Q1 family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA167x-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in [Figure 31](#).



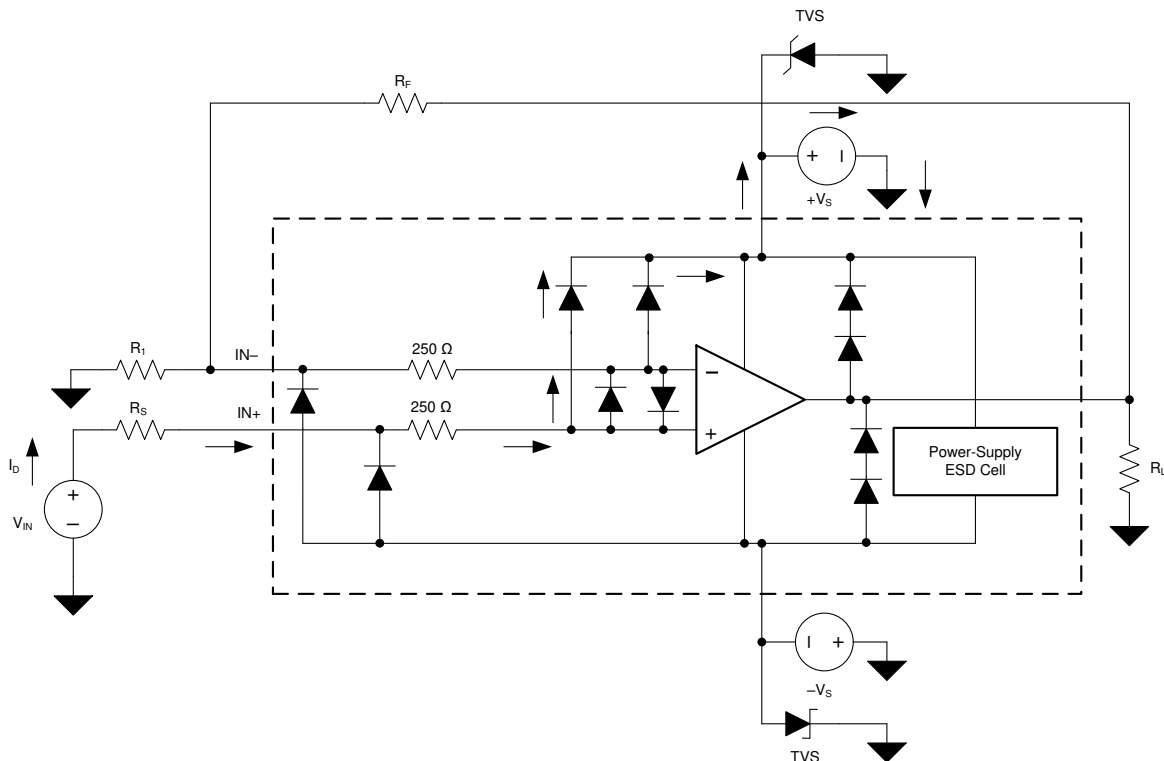
**Figure 31. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition**

## Feature Description (continued)

### 7.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 32 illustrates the ESD circuits contained in the OPA167x-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



**Figure 32. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is greater than the normal operating voltage of the OPA167x-Q1 but less than the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (see Figure 32), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

## Feature Description (continued)

Figure 32 shows a specific example where the input voltage ( $V_{IN}$ ) exceeds the positive supply voltage ( $V+$ ) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If  $V+$  can sink the current, one of the upper input steering diodes conducts and directs current to  $V+$ . Excessively high current levels can flow with increasingly higher  $V_{IN}$ . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current,  $V_{IN}$  can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies ( $V+$  or  $V-$ ) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level less than the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see Figure 32. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

### 7.3.3 EMI Rejection Ratio (EMIRR)

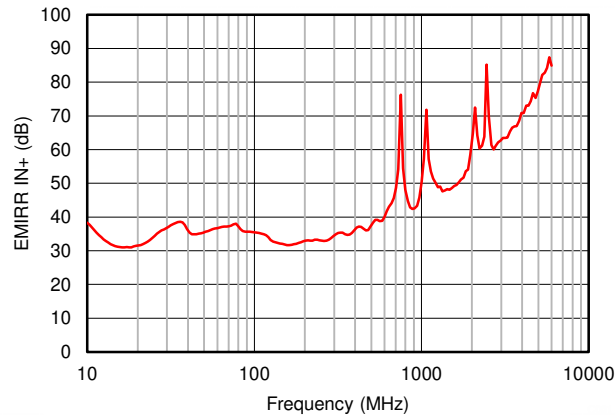
The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this document provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is shown in the [EMI Rejection Ratio of Operational Amplifiers application report](#), available for download at [www.ti.com](http://www.ti.com).

The EMIRR IN+ of the OPA167x-Q1 is plotted versus frequency in Figure 33. The dual and quad operational amplifier device versions have approximately identical EMIRR IN+ performance. The OPA167x-Q1 unity-gain bandwidth is 16 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

**Feature Description (continued)**



**Figure 33. OPA167x-Q1 EMIRR vs Frequency**

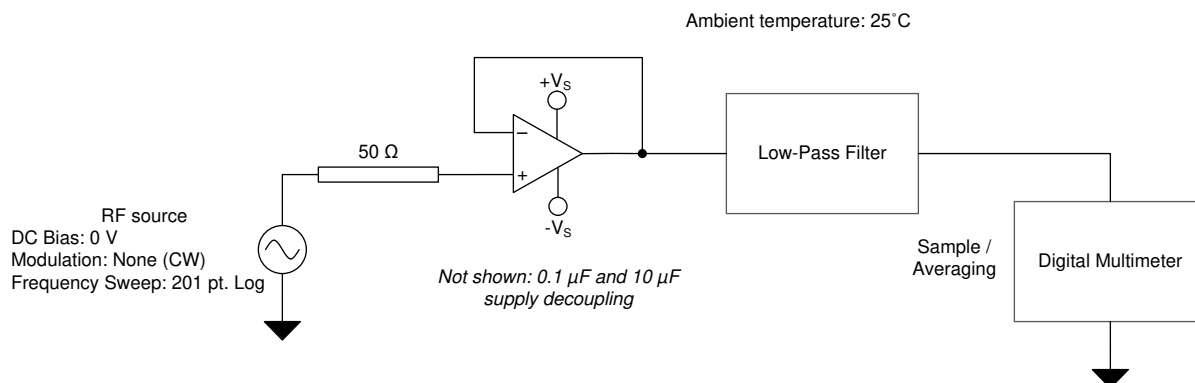
Table 1 lists the EMIRR IN+ values for the OPA167x-Q1 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 can be centered on or operated near the particular frequency shown. This information can be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

**Table 1. OPA167x-Q1 EMIRR IN+ for Frequencies of Interest**

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, UHF	36 dB
900 MHz	GSM, radio communication and navigation, GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	42 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	52 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio and satellite, S-band	64 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	67 dB
5 GHz	802.11a/n, aero communication and navigation, mobile communication, space and satellite operation, C-band	77 dB

### 7.3.3.1 EMIRR IN+ Test Configuration

Figure 34 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input pin using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy. See the [EMI Rejection Ratio of Operational Amplifiers application report](#) for more details.



**Figure 34. EMIRR IN+ Test Configuration Schematic**

## 7.4 Device Functional Modes

### 7.4.1 Operating Voltage

The OPA167x-Q1 series op amps operate from  $\pm 2.25$  V to  $\pm 18$  V supplies while maintaining excellent performance. The OPA167x-Q1 series can operate with as little as 4.5 V between the supplies and with up to 36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA167x-Q1 series, power-supply voltages are not required to be equal. For example, the positive supply can be set to 25 V with the negative supply at  $-5$  V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are specified over the temperature range of  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Parameters that vary significantly with operating voltage or temperature are shown in the [Typical Characteristics](#) section.

## 8 Application and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 8.1 Application Information

#### 8.1.1 Capacitive Loads

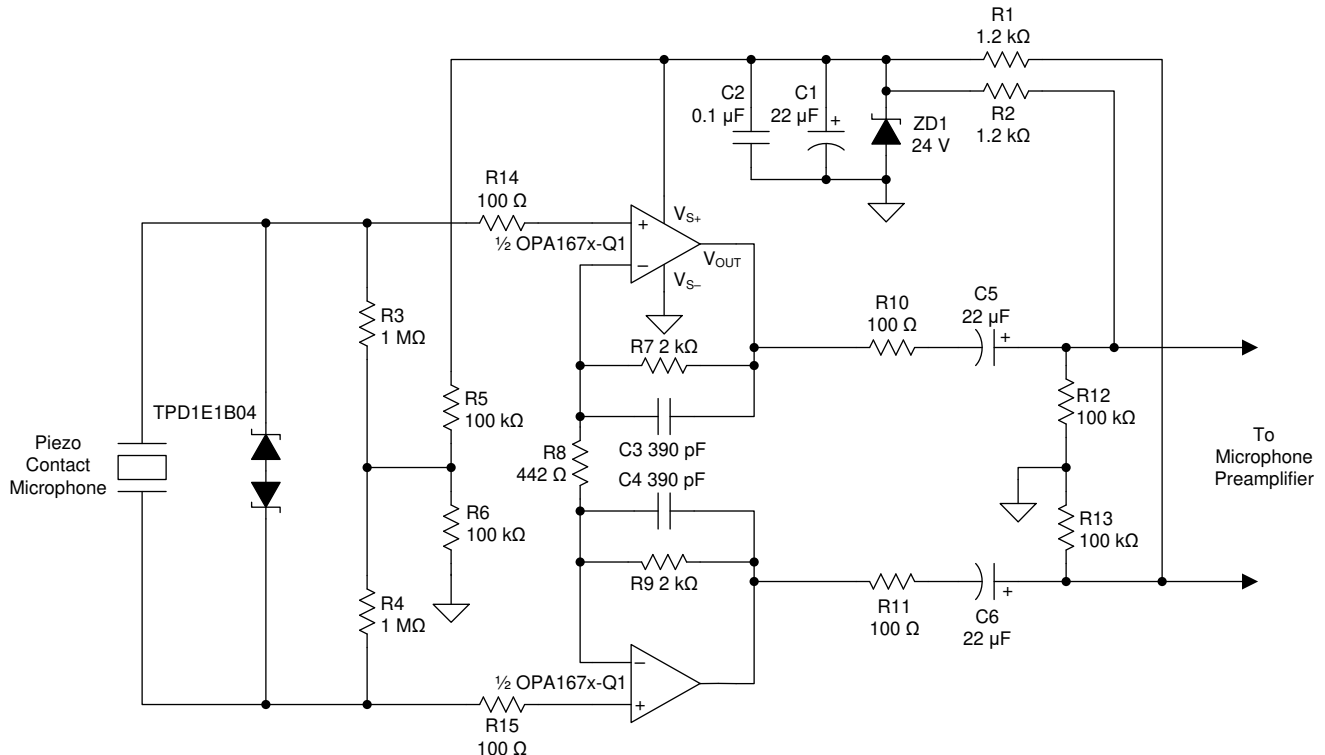
The dynamic characteristics of the OPA167x-Q1 series are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier, and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor ( $R_S$  equal to 50  $\Omega$ , for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device short-circuits. For more details about analysis techniques and application circuits, see the [Feedback Plots Define Op Amp AC Performance](#) application report, available for download from the TI website ([www.ti.com](http://www.ti.com)).

## 8.2 Typical Application

Contact or surface microphones are useful for measuring surface pressure in automotive test applications. Most contact microphones use a piezo element to convert vibrations in the body of the musical instrument to a voltage which may be amplified or recorded. The low noise and low input bias current of the OPA167x-Q1 make the device an excellent choice for high impedance preamplifiers for piezo elements. This preamplifier circuit provides high input impedance for the piezo element but has low output impedance for driving long cable runs. The circuit is also designed to be powered from 48-V phantom power which is commonly available in professional microphone preamplifiers and recording consoles.

A TINA-TI™ simulation schematic of the circuit below is available in the *Tools and Software* section of the OPA1679-Q1 product folder.



**Figure 35. Phantom-Powered Preamplifier for Piezo Contact Microphones**

### 8.2.1 Design Requirements

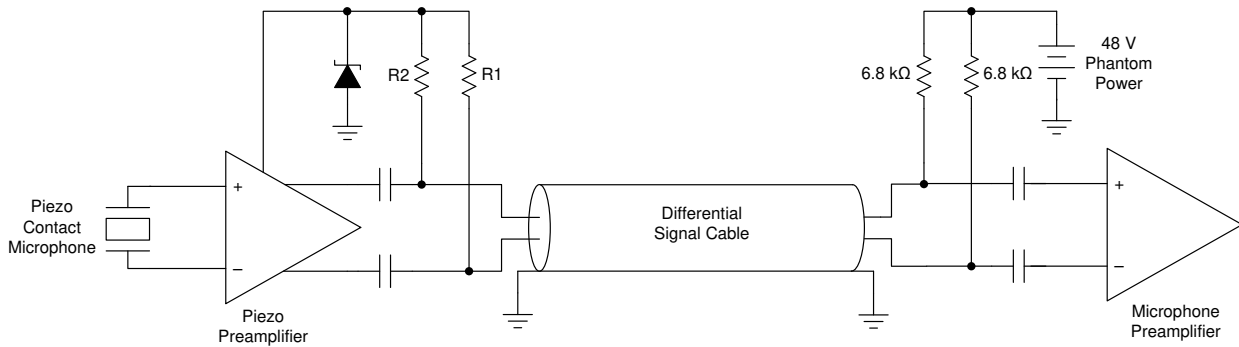
- –3-dB bandwidth: 20 Hz to 20 kHz
- Gain: 20 dB (10 V/V)
- Piezo element capacitance: 8 nF (9-kHz resonance)

## Typical Application (continued)

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Power Supply

In professional audio systems, phantom power is applied to the two signal lines that carry a differential audio signal from the microphone. Figure 36 is a diagram of the system showing 48-V phantom power applied to the differential signal lines between the piezo preamplifier output and the input of a professional microphone preamplifier.



**Figure 36. System Diagram Showing the Application of Phantom Power to the Audio Signal Lines**

A voltage divider is used to extract the common-mode phantom power from the differential audio signal in this type of system. The voltage at center point of the voltage divider formed by R1 and R2 does not change when audio signals are present on the signal lines (assuming R1 and R2 are matched). A Zener diode forces the voltage at the center point of R1 and R2 to a regulated voltage. The values of R1 and R2 are determined by the allowable voltage drop across these resistors from the current delivered to both op amp channels and the Zener diode. There are two power supply current pathways in parallel, each sharing half the total current of the op amp and Zener diode. Resistors R1 and R2 can be calculated using Equation 1:

$$R_1 = R_2 = R_{PS}$$

$$\frac{V_{ZD}}{\left(\frac{I_{OPA}}{2} + \frac{I_{ZD}}{2}\right)} - 6.8 \text{ k}\Omega = R_{PS} \quad (1)$$

A 24-V Zener diode is selected for this design, and 1 mA of current flows through the diode at idle conditions to maintain the reverse-biased condition of the Zener diode. The maximum idle power supply current of both op amp channels is 5 mA. Inserting these values into Equation 1 gives the values for R1 and R2 shown in Equation 2.

$$\frac{24V}{\left(\frac{I_{OPA}}{2} + \frac{I_{ZD}}{2}\right)} - 6.8 \text{ k}\Omega = \frac{24V}{\left(\frac{5.0 \text{ mA}}{2} + \frac{1.0 \text{ mA}}{2}\right)} - 6.8 \text{ k}\Omega = 1.2 \text{ k}\Omega = R_{PS} \quad (2)$$

Using a value of 1.2 kΩ for resistors R1 and R2 establishes a 1-mA current through the Zener diode and properly regulate the node to 24 V. Capacitor C1 forms a low-pass filter with resistors R1 and R2 to filter the Zener diode noise and any residual differential audio signals. Mismatch in the values of R1 and R2 causes a portion of the audio signal to appear at the voltage divider center point. The corner frequency of the low-pass filter must be set below the audio band, as shown in Equation 3.

$$C_1 \geq \frac{1}{2 \cdot \pi \cdot R_1 \parallel R_2 \cdot f_{-3dB}} \geq \frac{1}{2 \cdot \pi \cdot 600 \Omega \cdot 20 \text{ Hz}} \geq 13 \mu\text{F} \rightarrow 22 \mu\text{F} \quad (3)$$

A 22-μF capacitor is selected because the capacitor meets the requirements for power supply filtering and is a widely available denomination. A 0.1-μF capacitor (C2) is added in parallel with C1 as a high-frequency bypass capacitor.

## Typical Application (continued)

### 8.2.2.2 Input Network

Resistors R3 and R4 provide a pathway for the input bias current of the OPA167x-Q1 while maintaining the high input impedance of the circuit. The contact microphone capacitance and the required low-frequency response determine the values of R3 and R4. The –3-dB frequency formed by the microphone capacitance and amplifier input impedance is shown in [Equation 4](#):

$$F_{-3dB} = \frac{1}{2 \cdot \pi \cdot (R_3 + R_4) \cdot C_{MIC}} \leq 20 \text{ Hz} \quad (4)$$

A piezo element with 8 nF of capacitance was selected for this design because the 9-kHz resonance is towards the upper end of the audible bandwidth, and is less likely to affect the frequency response of many musical instruments. The minimum value for resistors R3 and R4 is then calculated with [Equation 5](#):

$$R_3 = R_4 = R_{IN}$$

$$R_{IN} \geq \frac{1}{4 \cdot \pi \cdot F_{-3dB} \cdot C_{MIC}} \geq \frac{1}{4 \cdot \pi \cdot 20 \text{ Hz} \cdot 8 \text{ nF}} \geq 497.4 \text{ k}\Omega \quad (5)$$

1-M $\Omega$  resistors are selected for R3 and R4 to make sure the circuit meets the design requirements for –3-dB bandwidth. The center point of resistors R3 and R4 is biased to half the supply voltage through the voltage divider formed by R5 and R6. This sets the input common-mode voltage of the circuit to a value within the input voltage range of the OPA167x-Q1. Piezo elements can produce very large voltages if the elements are struck with sufficient force. To prevent damage, the input of the OPA167x-Q1 is protected by a transient voltage suppressor (TVS) diode placed across the preamplifier inputs. The TPD1E1B04 TVS was selected due to low capacitance and the 6.4-V clamping voltage does not clamp the desired low amplitude vibration signals. Resistors R14 and R15 limit current flow into the amplifier inputs in the event that the internal protection diodes of the amplifier are forward-biased.

### 8.2.2.3 Gain

R7, R8, and R9 determines the gain of the preamplifier circuit. The gain of the circuit is shown in [Equation 6](#):

$$A_V = 1 + \frac{R_7 + R_9}{R_8} = 10 \text{ V/V} \quad (6)$$

Resistors R7 and R9 are selected with a value of 2 k $\Omega$  to avoid loading the output of the OPA167x-Q1 and producing distortion. The value of R8 is then calculated in [Equation 7](#):

$$R_8 = \frac{R_7 + R_9}{A_V - 1} = \frac{2 \text{ k}\Omega + 2 \text{ k}\Omega}{10 - 1} = 444.4 \text{ }\Omega \rightarrow 442 \text{ }\Omega \quad (7)$$

Capacitors C3 and C4 limit the bandwidth of the circuit so that signals outside the audio bandwidth are not amplified. The corner frequency produced by capacitors C3 and C4 is shown in [Equation 8](#). This corner frequency must be above the desired –3-dB bandwidth point to avoid attenuating high-frequency audio signals.

$$C_3 = C_4 = C_{FB}$$

$$C_{FB} \leq \frac{1}{2 \cdot \pi \cdot F_{-3dB} \cdot R_{7/9}} \leq \frac{1}{2 \cdot \pi \cdot 20 \text{ kHz} \cdot 2 \text{ k}\Omega} \leq 3.98 \text{ nF} \quad (8)$$

C3 and C4 are 390-pF capacitors, which places the corner frequency approximately 1 decade above the desired –3-dB bandwidth point. Capacitors C3 and C4 must be NP0 or C0G type ceramic capacitors or film capacitors. Other ceramic dielectrics, such as X7R, are not suitable for these capacitors and produces distortion.

## Typical Application (continued)

### 8.2.2.4 Output Network

The audio signal is ac-coupled onto the microphone signal lines through capacitors C5 and C6. The value of capacitors C5 and C6 are determined by the low-frequency design requirements and the input impedance of the microphone preamplifier that connect to the output of the circuit. Equation 9 shows an approximation of the capacitor value requirements, and neglects the effects of R10, R11, R12, and R13 on the frequency response. The microphone preamplifier input impedance ( $R_{IN\_MIC}$ ) uses a typical value of 4.4 k $\Omega$  for the calculation.

$$C_5 = C_6 = C_{OUT}$$

$$C_{OUT} \geq \frac{2}{2 \cdot \pi \cdot R_{IN\_MIC} \cdot 20 \text{ Hz}} \geq \frac{2}{2 \cdot \pi \cdot 4.4 \text{ k}\Omega \cdot 20 \text{ Hz}} \geq 3.6 \mu\text{F} \quad (9)$$

For simplicity, the same 22- $\mu\text{F}$  capacitors selected for the power supply filtering are selected for C5 and C6 to satisfy Equation 9. At least 50-V rated capacitors must be used for C5 and C6. If polarized capacitors are used, the positive terminal must be oriented towards the microphone preamplifier. Resistors R10 and R11 isolate the op amp outputs from the capacitances of long cables that may cause instability. R12 and R13 discharge ac-coupling capacitors C4 and C5 when phantom power is removed.

### 8.2.3 Application Curves

The frequency response of the preamplifier circuit is shown in Figure 37. The –3-dB frequencies are 15.87 Hz and 181.1 kHz, which meet the design requirements. The gain within the passband of the circuit is 18.9 dB, slightly less than the design goal of 20 dB. The reduction in gain is a result of the voltage division between the output resistors of the piezo preamplifier circuit and the input impedance of the microphone preamplifier. The A-weighted noise of the circuit (referred to the input) is 842.2 nV<sub>RMS</sub> or –119.27 dBu.

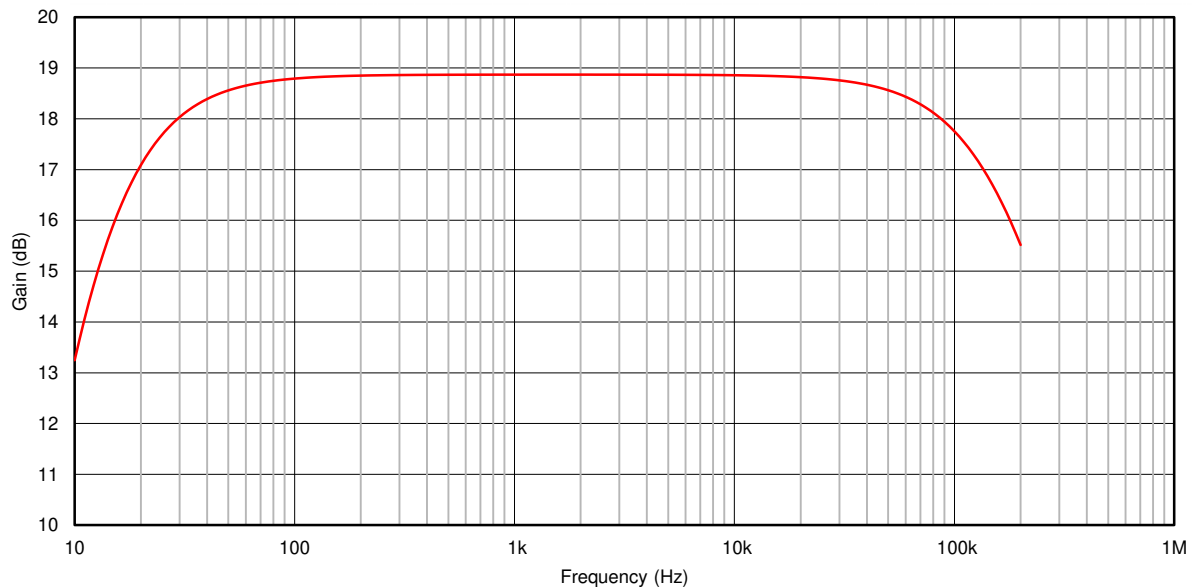


Figure 37. Frequency Response of the Preamplifier Circuit for a 8-nF Piezo Element

## 9 Power Supply Recommendations

The OPA167x-Q1 devices are specified for operation from 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the [Typical Characteristics](#) section. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1- $\mu\text{F}$  capacitors are adequate.

## 10 Layout

### 10.1 Layout Guidelines

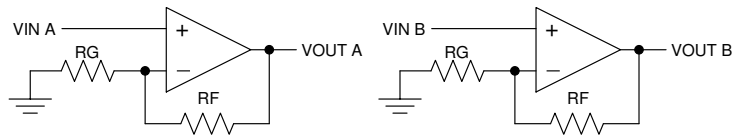
For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V+$  to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Physically separate digital and analog grounds, observing the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 38](#), keeping  $R_F$  and  $R_G$  close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at  $85^{\circ}\text{C}$  for 30 minutes is sufficient for most circumstances.

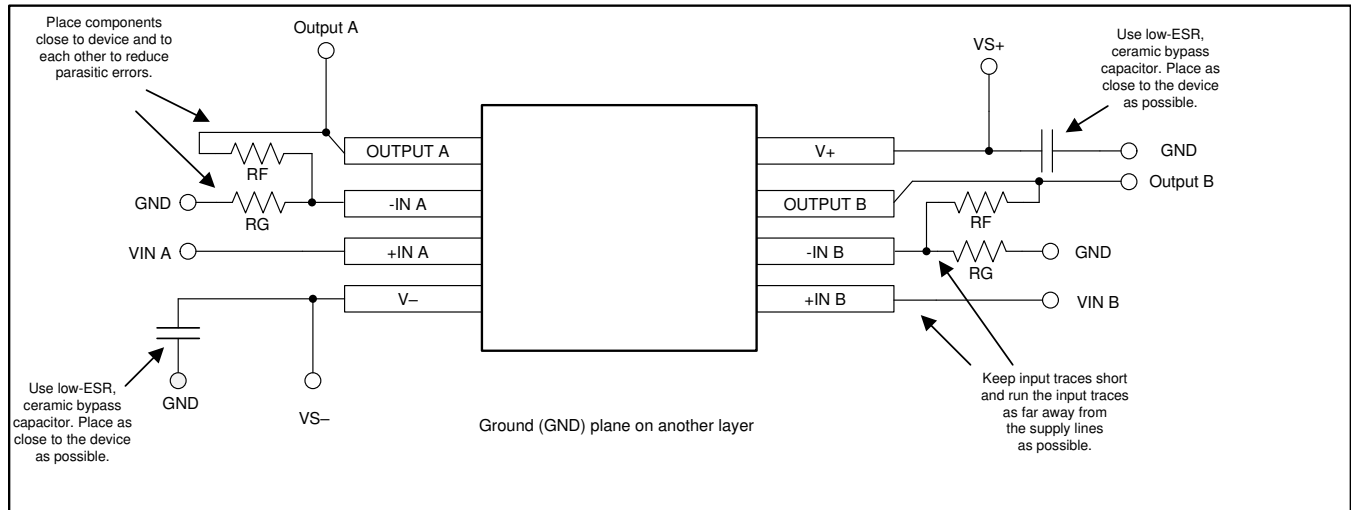
#### 10.1.1 Power Dissipation

The OPA167x-Q1 series op amps are capable of driving 2-k $\Omega$  loads with a power-supply voltage up to  $\pm 18$  V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA167x-Q1 series op amps improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

## 10.2 Layout Example



(Schematic Representation)



**Figure 38. Operational Amplifier Board Layout for Noninverting Configuration**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the WEBENCH® Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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#### NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

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##### 11.1.1.2 DIP Adapter EVM

The [DIP Adapter EVM](#) tool provides an easy, low-cost way to prototype small surface mount devices. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT-23-6, SOT-23-5 and SOT-23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

##### 11.1.1.3 Universal Operational Amplifier EVM

The [Universal Op Amp EVM](#) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of device package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP and SOT-23 packages are all supported.

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#### NOTE

These boards are unpopulated, so users must provide their own devices. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

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##### 11.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at <http://www.ti.com/ww/en/analog/precision-designs/>.

##### 11.1.1.5 WEBENCH® Filter Designer

[WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, [WEBENCH® Filter Designer](#) allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

The following documents are relevant to using the OPA167x, and are recommended for reference. All are available for download at [www.ti.com](http://www.ti.com) unless otherwise noted.

- Texas Instruments, [Source resistance and noise considerations in amplifiers technical brief](#)
- Burr Brown, [Single-Supply Operation of Operational Amplifiers application bulletin](#)
- Burr Brown, [Op Amp Performance Analysis application bulletin](#)
- Texas Instruments, [Compensate Transimpedance Amplifiers Intuitively application report](#)
- Burr Brown, [Tuning in Amplifiers application bulletin](#)
- Burr Brown, [Feedback Plots Define Op Amp AC Performance application bulletin](#)
- Texas Instruments, [Active Volume Control for Professional Audio precision design](#)

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1679QRUMRQ1	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 1679Q	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF OPA1679-Q1 :**

- Catalog: [OPA1679](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1679QRUMRQ1	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1679QRUMRQ1	WQFN	RUM	16	3000	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

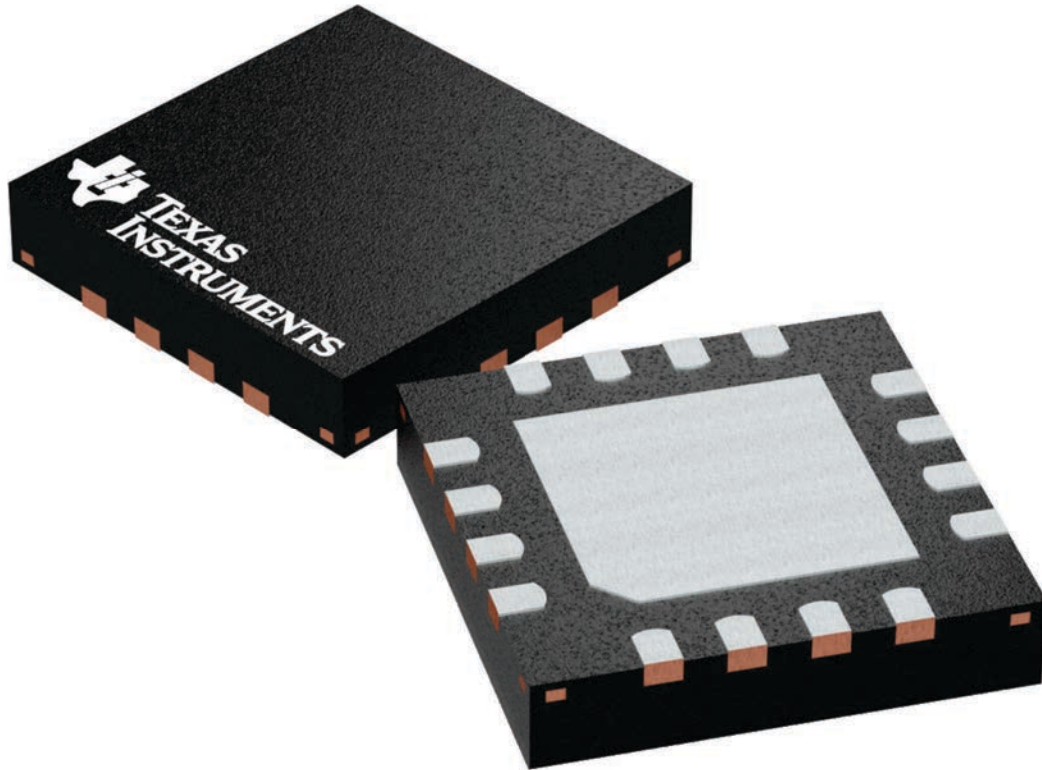
**RUM 16**

**WQFN - 0.8 mm max height**

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

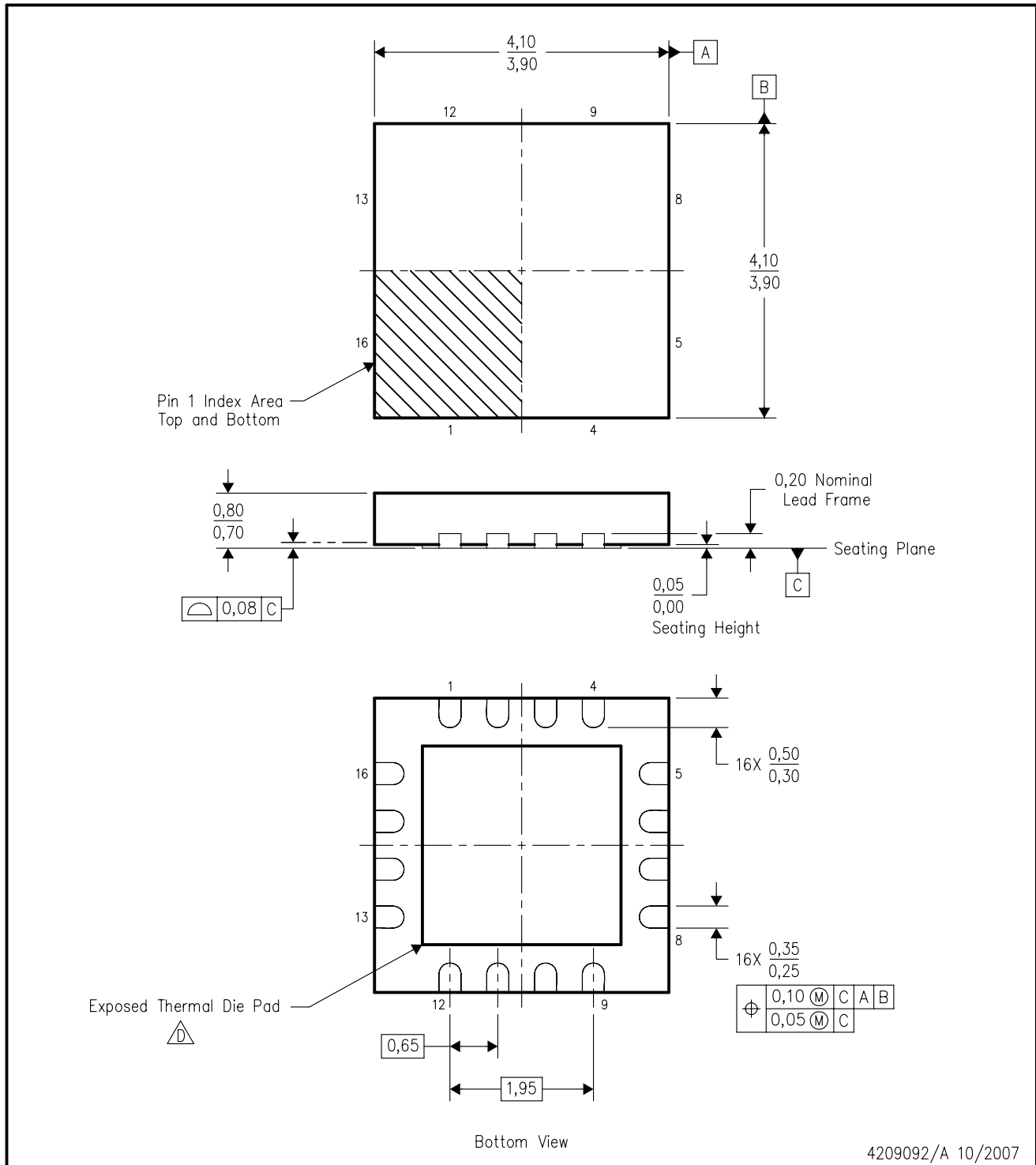
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224843/A

RUM (S-PQFP-N16)

PLASTIC QUAD FLATPACK



4209092/A 10/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Package complies to JEDEC MO-220 variation WGGC-3.

RUM (S-PWQFN-N16)

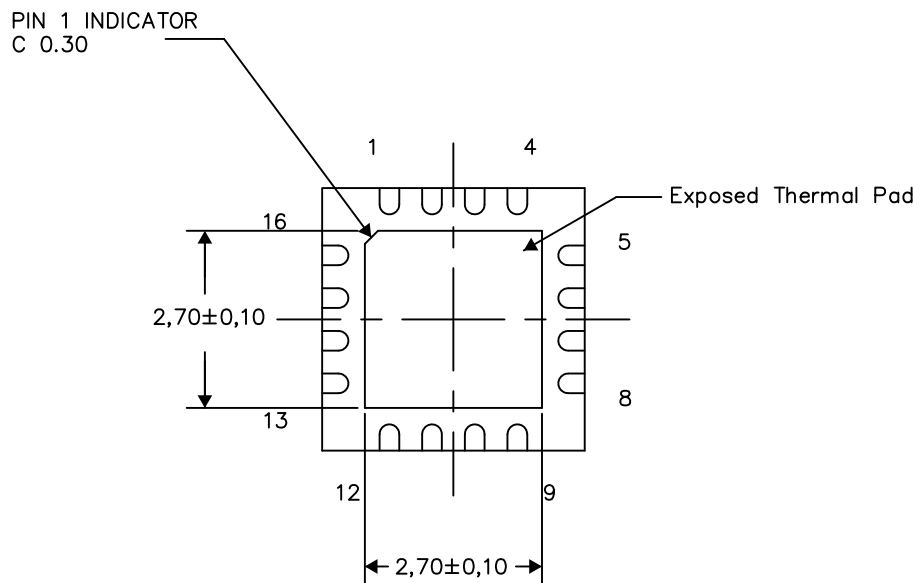
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4209093-2/F 09/15

NOTES: All linear dimensions are in millimeters



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