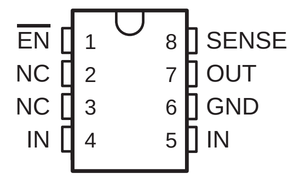
THE DATASHEET OF

TPS7433D

- **Fast Transient Response Using Small Output Capacitor (10 μF)**
- **200-mA Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, 3-V and 3.3-V**
- **Dropout Voltage Down to 170 mV at 200 mA (TPS7433)**
- **3% Tolerance Over Specified Conditions**
- **8-Pin SOIC Package**
- **Thermal Shutdown Protection**

D PACKAGE
(TOP VIEW)



NC – No internal connection

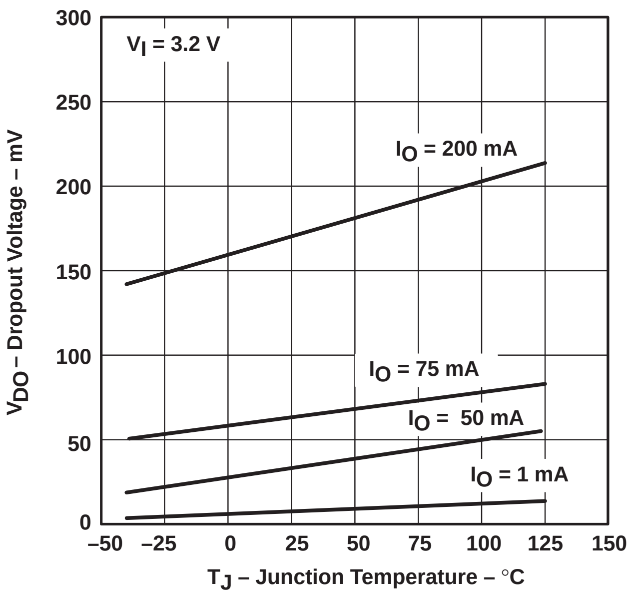
description

This device is designed to have a fast transient response and be stable with 1-μF capacitors. This combination provides high performance at a reasonable cost.

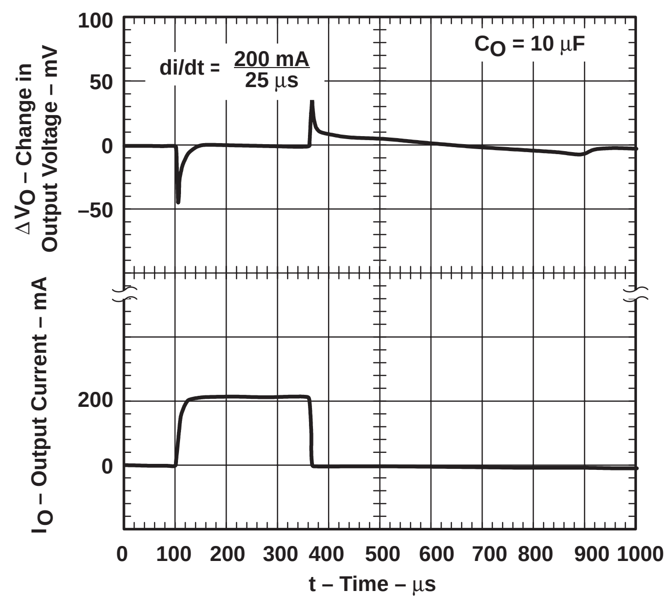
Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 170 mV at an output current of 200-mA for the TPS7433). This LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 μA at T_J = 25°C.

The TPS74xx is offered in 1.5-V, 1.8-V, 2.5-V, 3-V, and 3.3-V. Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS74xx family is available in 8 pin SOIC package.

TPS7433
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE



TPS7418
LOAD TRANSIENT RESPONSE

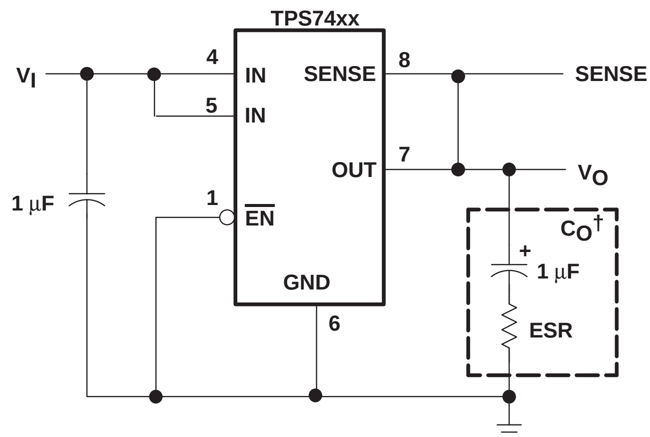


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES
	TYP	SOIC (D)
–40°C to 125°C	3.3	TPS7433D
	3	TPS7430D
	2.5	TPS7425D
	1.8	TPS7418D
	1.5	TPS7415D

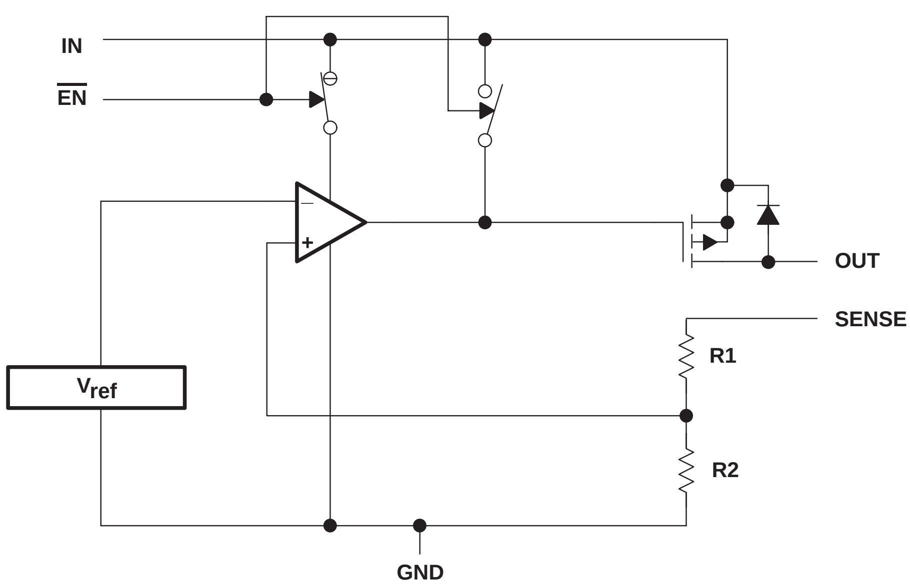
The D package is available taped and reeled. Add an R suffix to the device type (e.g., TPS7433DR).



† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{EN}$	1	I	Enable input
GND	6		Regulator ground
IN	4, 5	I	Input voltage
NC	2, 3		Not connected
OUT	7	O	Regulated output voltage
SENSE	8	I	Sense

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I . . . . –0.3 V to 8 V
Voltage range at $\overline{EN}$ . . . . –0.3 V to V_I + 0.3 V
Peak output current . . . . Internally limited
Continuous total power dissipation . . . . See dissipation rating tables
Operating virtual junction temperature range, T_J . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I§	2.5	7	V
Output current, I_O (see Note 1)	0	200	mA
Operating virtual junction temperature, T_J (see Note 1)	–40	125	°C

§ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.
NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

electrical characteristics over recommended operating free-air temperature range, $V_i = V_{O(typ)} + 1\ V$, $I_O = 1\ mA$, $\overline{EN} = 0\ V$, $C_O = 1\ \mu F$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 µA to 200 mA load) (see Note 2)	TPS7415	$2.5\ V < V_I < 7\ V$	$T_J = 25°C$		1.5		V
			$T_J = –40°C$ to 125°C	1.455		1.545	
	TPS7418	$2.8\ V < V_I < 7\ V$	$T_J = 25°C$		1.8		
			$T_J = –40°C$ to 125°C	1.746		1.854	
	TPS7425	$3.5\ V < V_I < 7\ V$	$T_J = 25°C$		2.5		
			$T_J = –40°C$ to 125°C	2.425		2.575	
	TPS7430	$4.0\ V < V_I < 7\ V$	$T_J = 25°C$		3.0		
			$T_J = –40°C$ to 125°C	2.910		3.090	
	TPS7433	$4.3\ V < V_I < 7\ V$	$T_J = 25°C$		3.3		
			$T_J = –40°C$ to 125°C	3.201		3.399	
Quiescent current (GND current) (See Note 2)		$I_O = 1\ mA$, EN = 0 V	$T_J = 25°C$		80		µA
			$T_J = –40°C$ to 125°C			115	
		$I_O = 100\ mA$, EN = 0 V	$T_J = 25°C$		550		µA
			$T_J = –40°C$ to 125°C			850	
		$I_O = 200\ mA$, EN = 0 V	$T_J = 25°C$		1300		µA
			$T_J = –40°C$ to 125°C			1500	
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)		$V_O + 1\ V < V_I \le 7\ V$,	$T_J = 25°C$		0.06		%/V
Load regulation					5		mV
Output noise voltage		BW = 300 Hz to 50 kHz, $T_J = 25°C$	$C_O = 1\ \mu F$,		190		µVrms
Output current Limit		$V_O = 0\ V$			500	750	mA
Thermal shutdown junction temperature					150		°C
Standby current		$2.5\ V < V_I < 7\ V$, $T_J = 25°C$	$\overline{EN} = V_I$,			1	µA
		$2.5\ V < V_I < 7\ V$, $T_J = –40°C$ to 125°C	$\overline{EN} = V_I$,			3	µA
High level enable input voltage				2			V
Low level enable input voltage						0.7	V
Input current (EN)		$\overline{EN} = 0\ V$		–1		1	µA
		$\overline{EN} = V_I$		–1		1	
Power supply ripple rejection (see Note 2)		f = 100 Hz, $T_J = 25°C$	$C_O = 1\ \mu F$,		55		dB
Dropout voltage (see Note 4)	TPS7430	$I_O = 200\ mA$,	$T_J = 25°C$		180		mV
		$I_O = 200\ mA$,	$T_J = –40°C$ to 125°C			350	
	TPS7433	$I_O = 200\ mA$,	$T_J = 25°C$		170		
		$I_O = 200\ mA$,	$T_J = –40°C$ to 125°C			315	

NOTES: 2. Minimum IN operating voltage is 2.5 V or $V_{O(typ)} + 1\ V$, whichever is greater. Maximum IN voltage 7 V.

3. If $V_O = 1.5\ V$ then $V_{imax} = 7\ V$, $V_{imin} = 2.5\ V$:

4. IN voltage equals $V_O(Typ) – 100\ mV$; TPS7430 and TPS7433 dropout limited by input voltage range limitations (i.e., TPS7430 input voltage needs to drop to 2.9 V for purpose of this test).

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{imax} - 2.5\ V\right)}{100} \times 1000$$

If $V_O \ge 2.5\ V$ then $V_{imax} = 7\ V$, $V_{imin} = V_O + 1\ V$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{imax} - \left(V_O + 1\ V\right)\right)}{100} \times 1000$$

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3, 4
		vs Junction temperature	5, 6
	Ground current	vs Junction temperature	7, 8
	Power supply ripple rejection	vs Frequency	12
	Output noise	vs Frequency	9
Z_O	Output impedance	vs Frequency	10
V_{DO}	Dropout voltage	vs Junction temperature	11
	Line transient response		13, 15
	Load transient response		14, 16
	Output voltage	vs Time	17
	(Stability) Equivalent series resistance (ESR)	vs Output current	19

TYPICAL CHARACTERISTICS

TPS7418
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

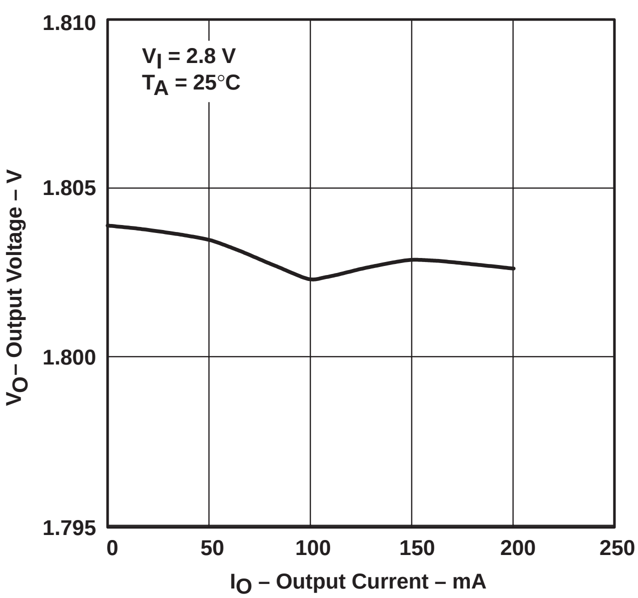


Figure 2

TPS7433
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

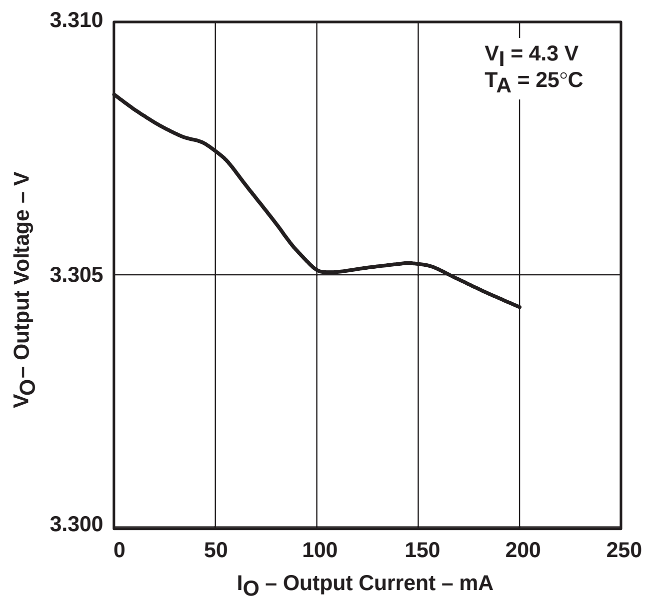


Figure 3

TYPICAL CHARACTERISTICS

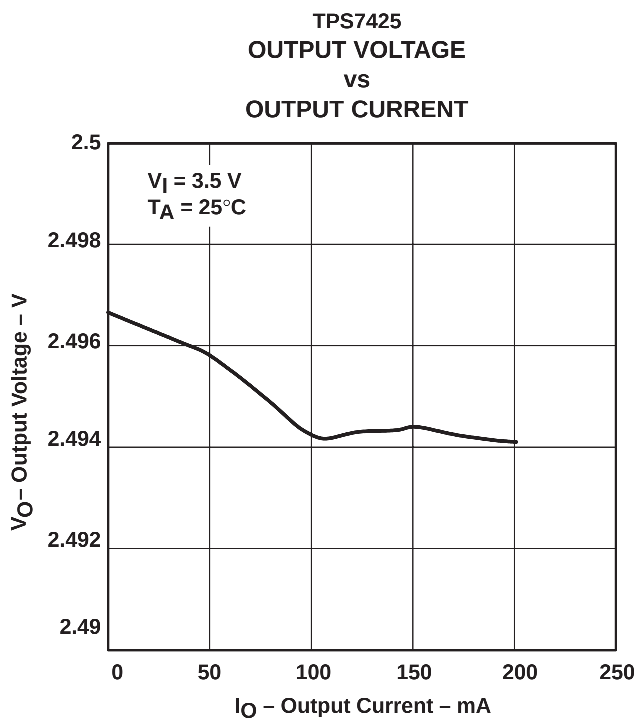


Figure 4

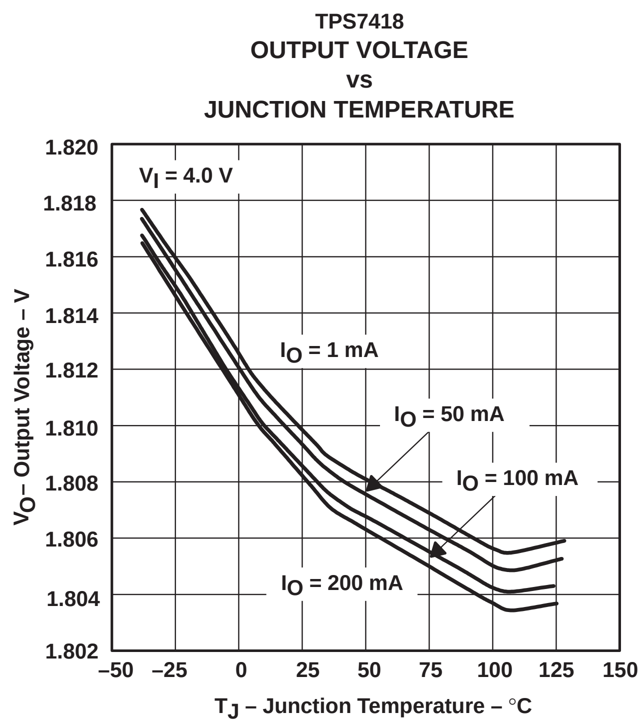


Figure 5

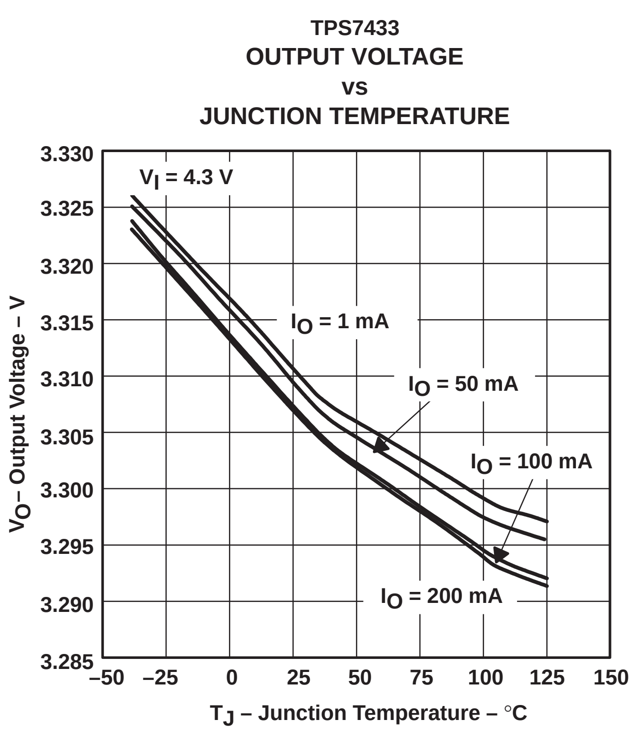


Figure 6

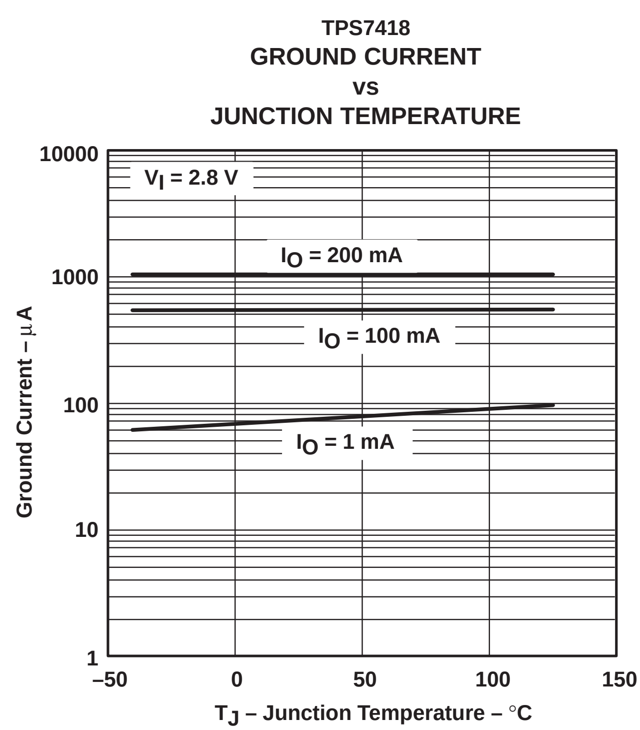


Figure 7

TYPICAL CHARACTERISTICS

TPS7433
GROUND CURRENT
vs
JUNCTION TEMPERATURE

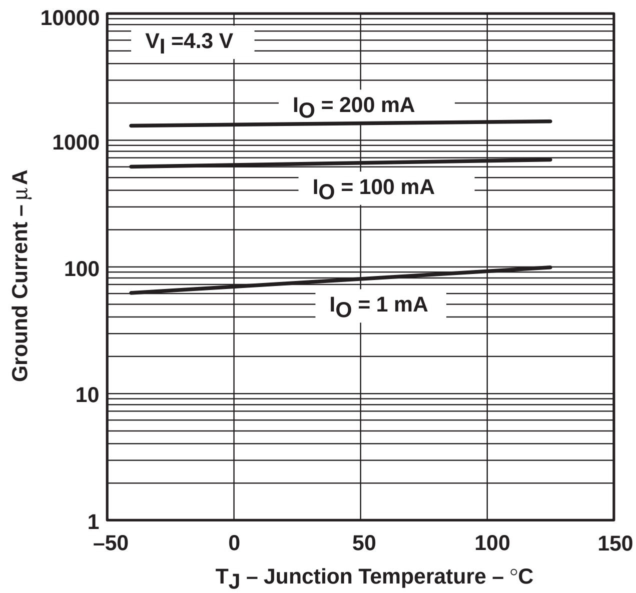


Figure 8

OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

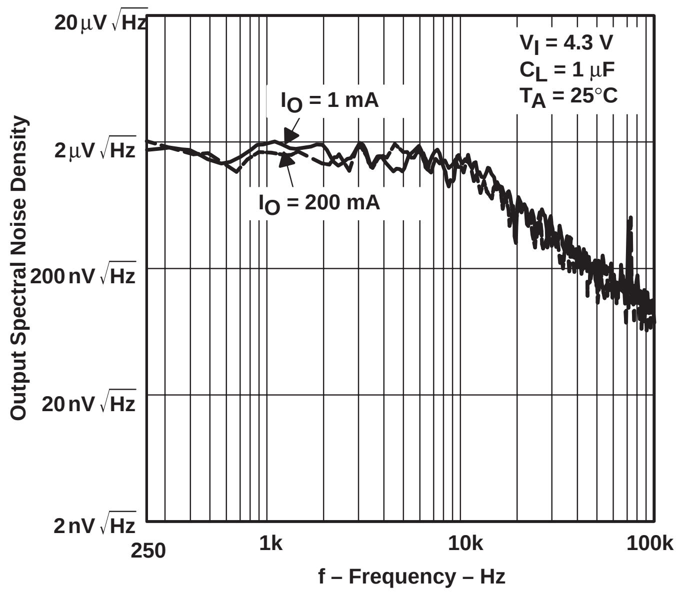


Figure 9

OUTPUT IMPEDANCE
vs
FREQUENCY

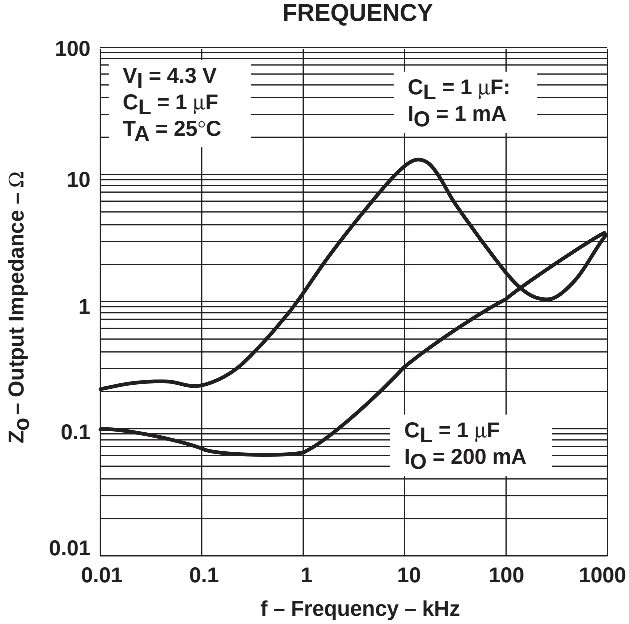


Figure 10

TPS7430
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

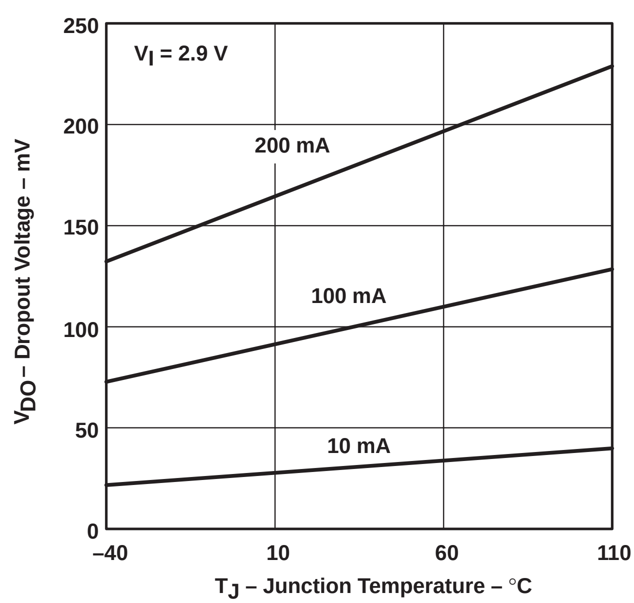


Figure 11

TYPICAL CHARACTERISTICS

RIPPLE REJECTION vs FREQUENCY

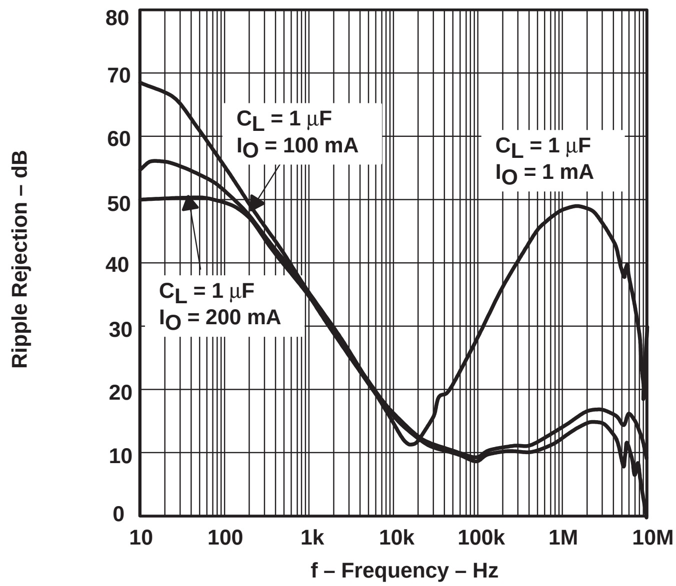


Figure 12

TPS7418 LINE TRANSIENT RESPONSE

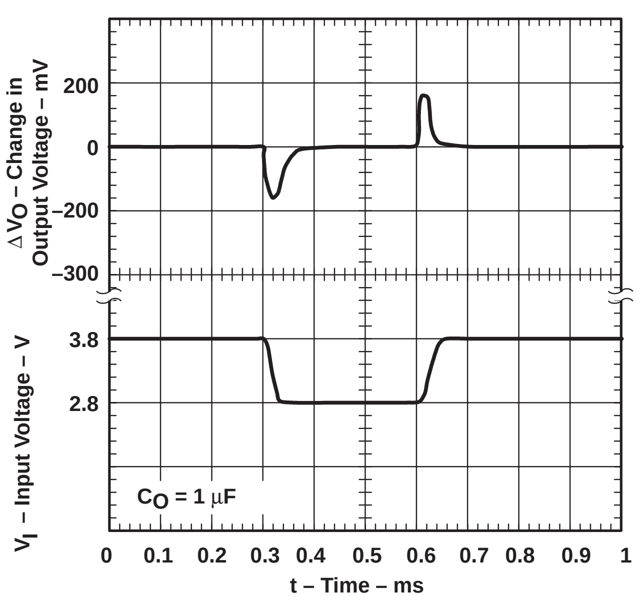


Figure 13

TPS7418 LOAD TRANSIENT RESPONSE

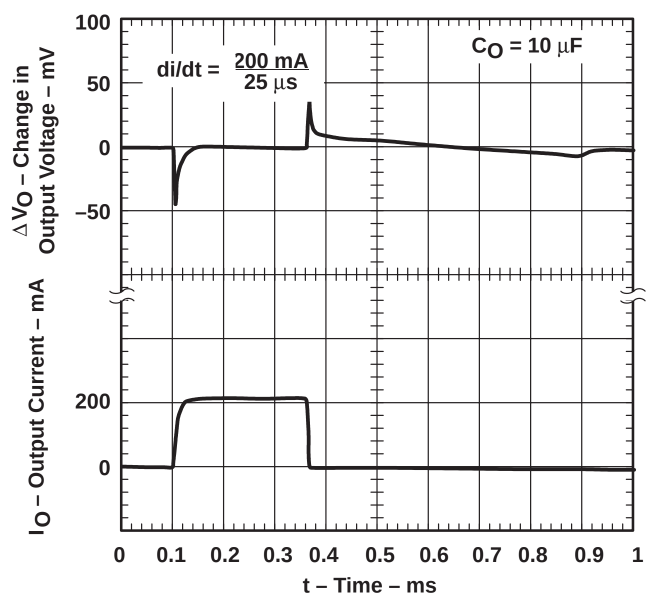


Figure 14

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TYPICAL CHARACTERISTICS

TPS7433
LINE TRANSIENT RESPONSE

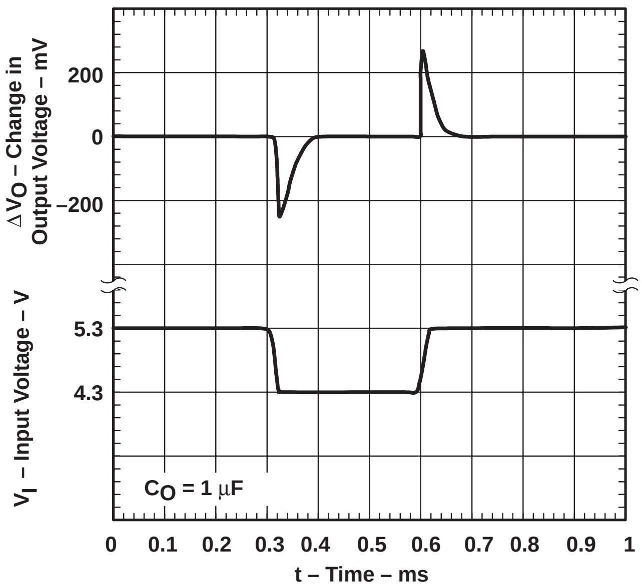

Figure 15

TPS7433
LOAD TRANSIENT RESPONSE

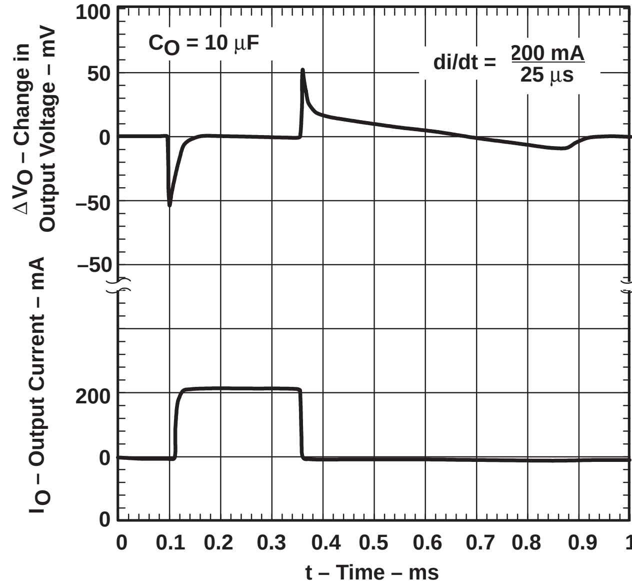

Figure 16

TPS7433
OUTPUT VOLTAGE
vs
TIME (AT STARTUP)

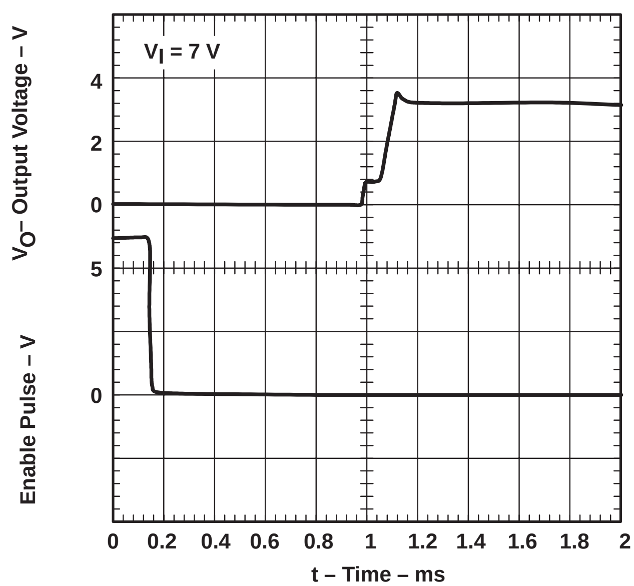

Figure 17

TYPICAL CHARACTERISTICS

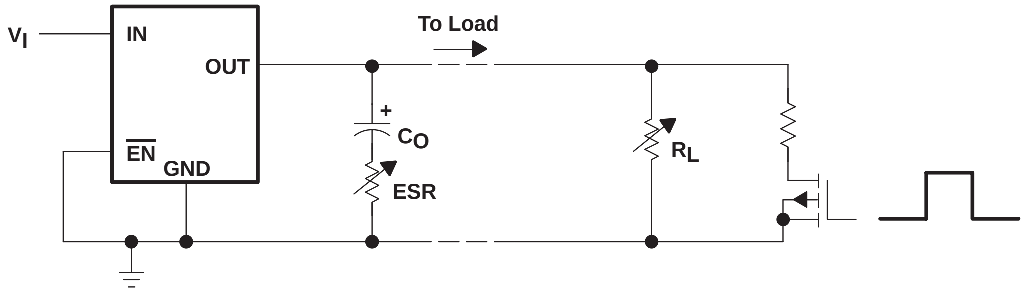

Figure 18. Test Circuit for Typical Regions of Stability (Figure 19)

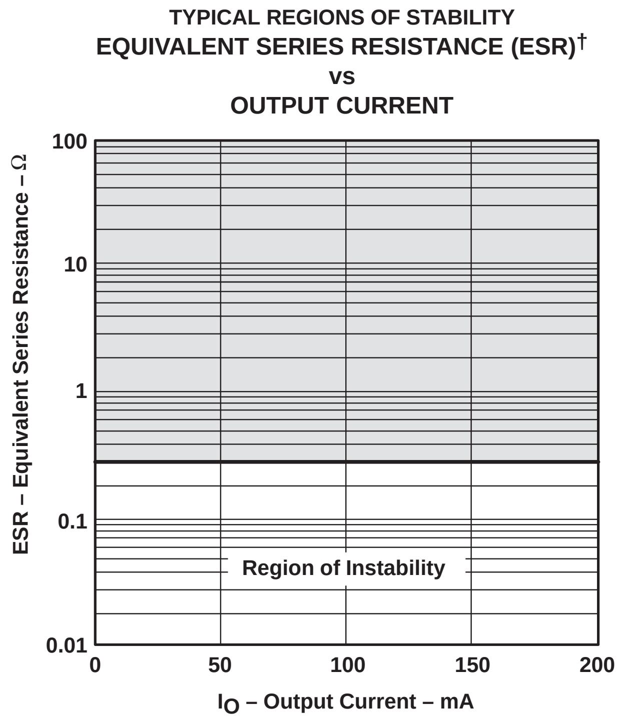

Figure 19

† ESR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The TPS74xx family includes five voltage regulators (1.5 V, 1.8 V, 2.5 V, 3 V, and 3.3 V).

minimum load requirements

The TPS74xx family is stable even at zero load; no minimum load is required for operation.

SENSE terminal connection

The SENSE terminal must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (1 μF or larger) improves load transient response and noise rejection if the TPS74xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS74xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 1 μF and the ESR (equivalent series resistance) must be at least 300 mΩ. Solid tantalum electrolytic and aluminum electrolytic are all suitable, provided they meet the requirements described previously.

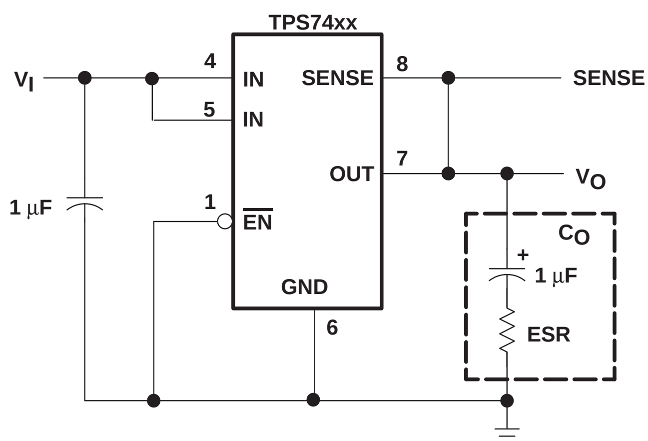

Figure 20. Typical Application Circuit

regulator protection

The TPS74xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

APPLICATION INFORMATION

regulator protection (continued)

The TPS74xx also features internal current limiting and thermal protection. During normal operation, the TPS74xx limits output current to approximately 500 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7415D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7415	Samples
TPS7418D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7418	Samples
TPS7418DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7418	Samples
TPS7425D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7425	Samples
TPS7430D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7430	Samples
TPS7433D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7433	Samples
TPS7433DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7433	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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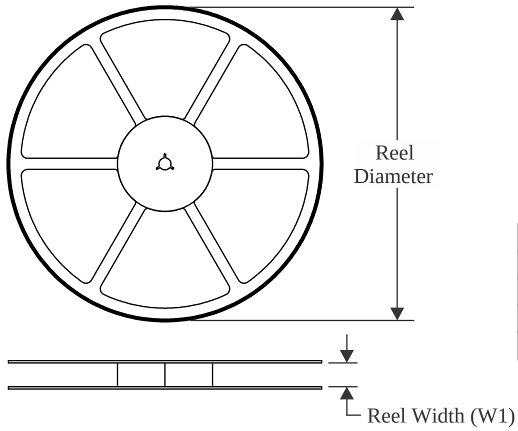
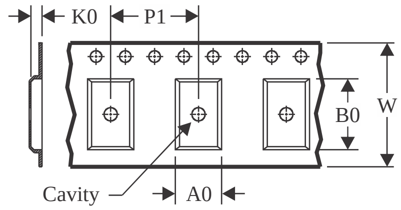
TAPE AND REEL INFORMATION

REEL DIMENSIONS

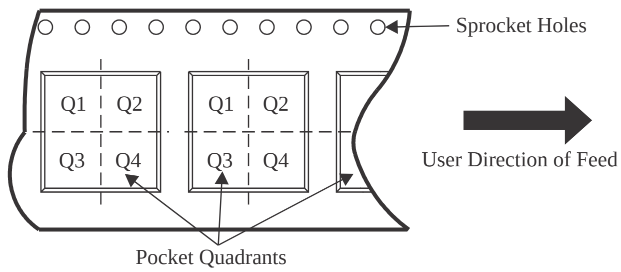


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

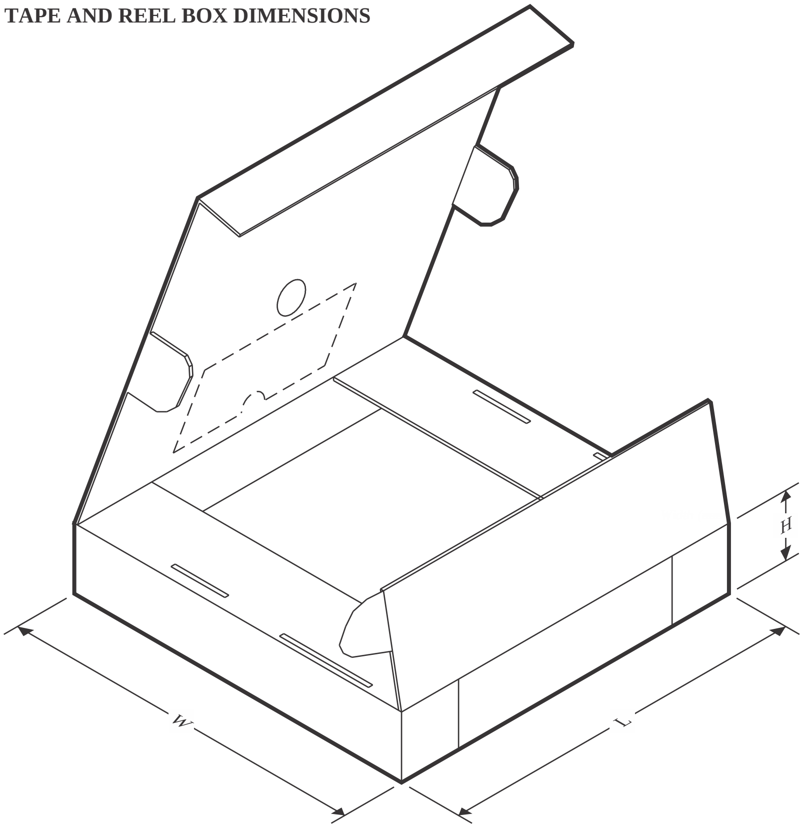
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7433DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

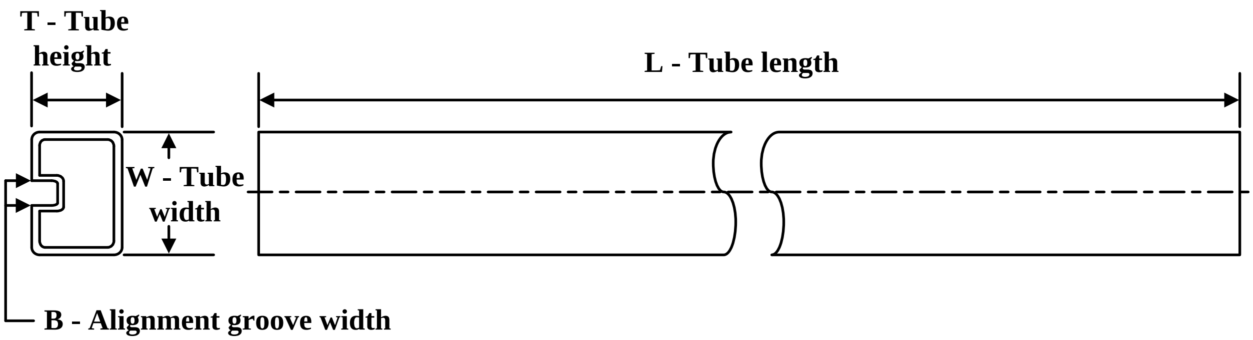
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

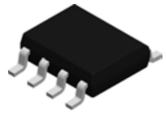
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7433DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

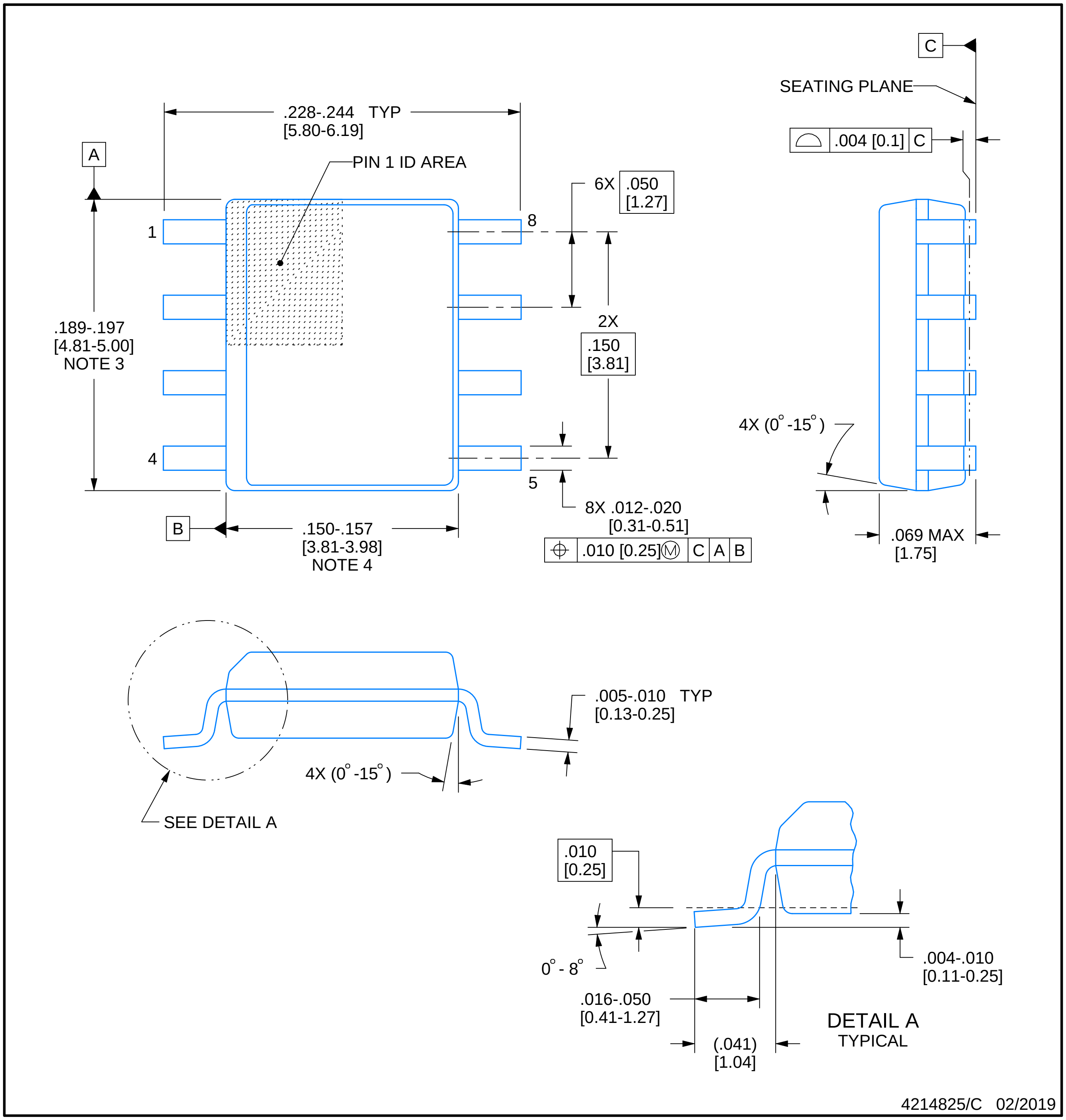
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS7415D	D	SOIC	8	75	505.46	6.76	3810	4
TPS7418D	D	SOIC	8	75	505.46	6.76	3810	4
TPS7418DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS7425D	D	SOIC	8	75	505.46	6.76	3810	4
TPS7430D	D	SOIC	8	75	505.46	6.76	3810	4
TPS7433D	D	SOIC	8	75	505.46	6.76	3810	4



D0008A

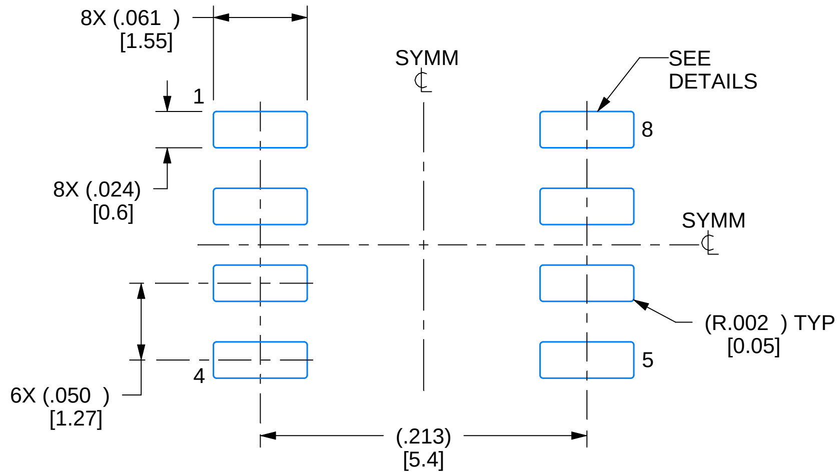
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

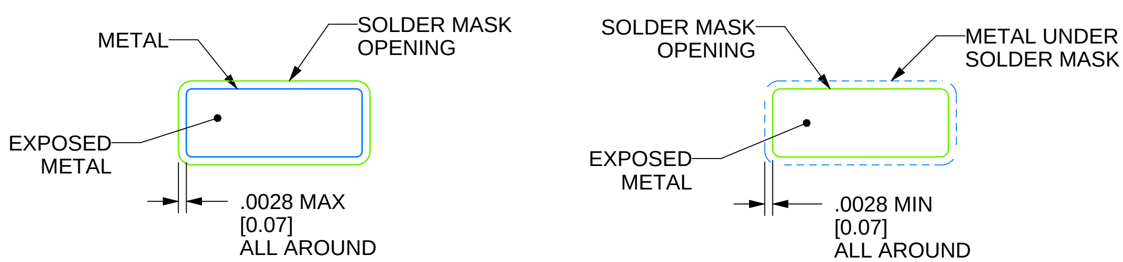


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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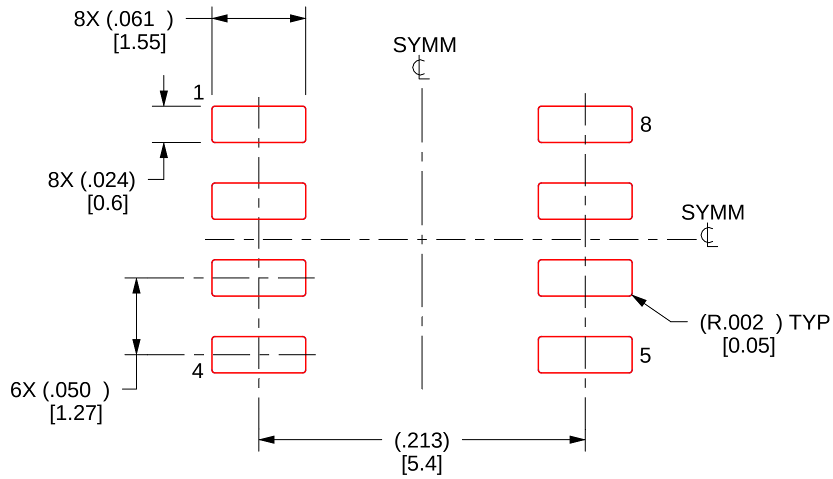
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.