

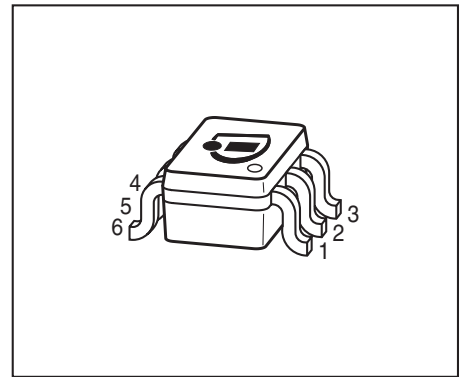


**THE DATASHEET OF  
BG5412KE6327HTSA1**

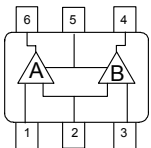


**Dual N-Channel MOSFET Tetrode**

- Designed for input stages of 2 band tuners
- Two AGC amplifiers in one single package, with on-chip internal switch
- Only one switching line to control both FETs
- Integrated gate protection diodes
- Ultra low noise figure
- Excellent cross modulation at gain reduction
- Integrated ESD gate protection diodes
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101



Detailed functional diagram on page 5


**BG5412K**


**ESD (Electrostatic discharge) sensitive device, observe handling precaution!**

Type	Package	Pin Configuration						Marking
BG5412K	SOT363	1=G1*	2=G2	3=G1**	4=D**	5=S	6=D*	K2s

\* For amp. A; \*\* for amp. B

180° rotated tape loading orientation available

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Drain-source voltage	$V_{DS}$	8	V
Continuous drain current amp. A	$I_D$	25	mA
amp. B		25	
Gate 1/ gate 2-source current	$I_{G1S}, I_{G2S}$	$\pm 1$	mA
Gate 1/ gate 2-source voltage	$V_{G1S}, V_{G2S}$	$\pm 6$	V
Total power dissipation $T_S \leq 94 \text{ }^\circ\text{C}$	$P_{tot}$	200	mW
Storage temperature	$T_{stg}$	-55 ... 150	$^\circ\text{C}$
Channel temperature	$T_{ch}$	150	

**Thermal Resistance**

Parameter	Symbol	Value	Unit
Channel - soldering point <sup>1)</sup>	$R_{thchs}$	$\leq 280$	K/W

<sup>1)</sup>For calculation of  $R_{thJA}$  please refer to Application Note Thermal Resistance

**Electrical Characteristics** at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

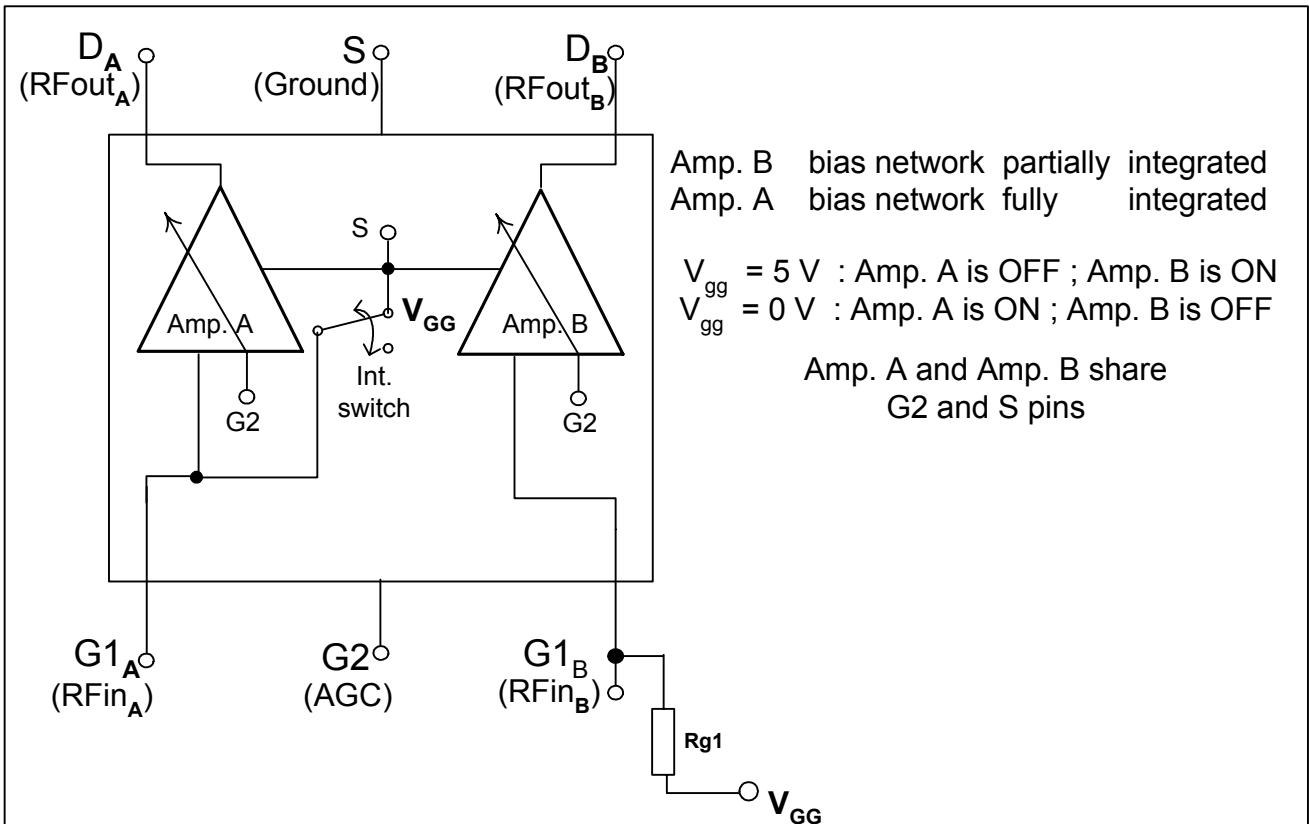
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>DC Characteristics</b>					
Drain-source breakdown voltage $I_D = 100 \mu\text{A}$ , $V_{G1S} = 0$ , $V_{G2S} = 0$	$V_{(BR)DS}$	12	-	-	V
Gate1-source breakdown voltage $+I_{G1S} = 10 \text{ mA}$ , $V_{G2S} = 0$ , $V_{DS} = 0$	$+V_{(BR)G1SS}$	6	-	15	
Gate2-source breakdown voltage $+I_{G2S} = 10 \text{ mA}$ , $V_{G1S} = 0$ , $V_{DS} = 0$	$+V_{(BR)G2SS}$	6	-	15	
Gate1-source leakage current $V_{G1S} = 6 \text{ V}$ , $V_{G2S} = 0$ , $V_{DS} = 0$	$+I_{G1SS}$	-	-	50	nA
Gate2-source leakage current $V_{G2S} = 8 \text{ V}$ , $V_{G1S} = 0$	$+I_{G2SS}$	-	-	50	
Drain current $V_{DS} = 5 \text{ V}$ , $V_{G1S} = 0$ , $V_{G2S} = 4 \text{ V}$	$I_{DSS}$	-	-	100	$\mu\text{A}$
Drain-source current $V_{DS} = 5 \text{ V}$ , $V_{G2S} = 4 \text{ V}$ , $R_{G1} = 120 \text{ k}\Omega$ , amp. B $V_{DS} = 5 \text{ V}$ , $V_{G2S} = 4 \text{ V}$ , selfbiased, amp. A	$I_{DSX}$	-	14 18	-	mA
Gate1-source pinch-off voltage $V_{DS} = 5 \text{ V}$ , $V_{G2S} = 4 \text{ V}$ , $I_D = 100 \mu\text{A}$	$V_{G1S(p)}$	-	0.7	-	V
Gate2-source pinch-off voltage $V_{DS} = 5 \text{ V}$ , $I_D = 100 \mu\text{A}$	$V_{G2S(p)}$	-	0.7	-	

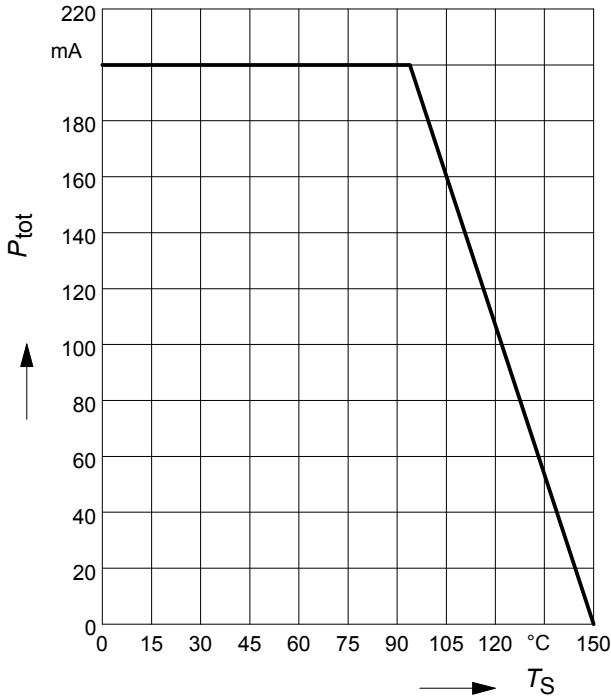
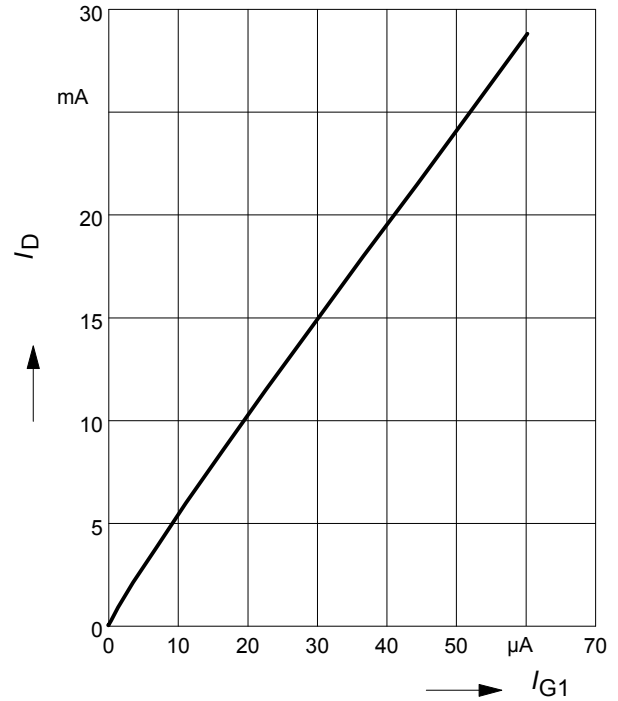
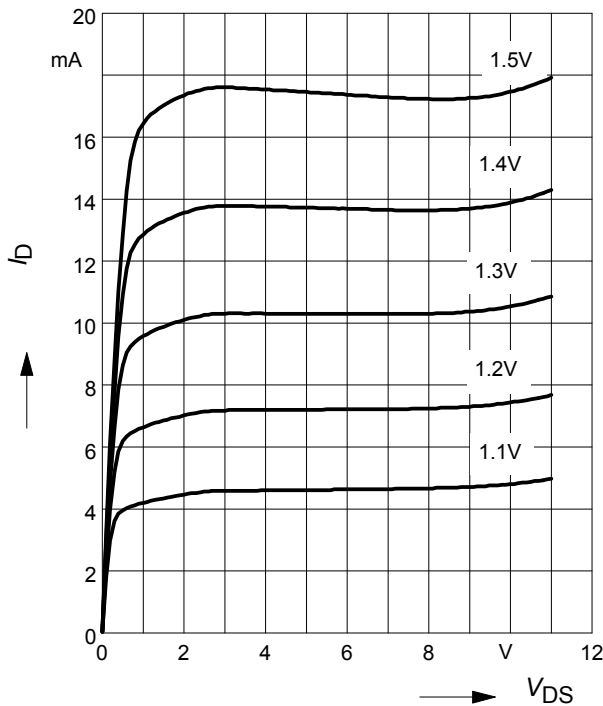
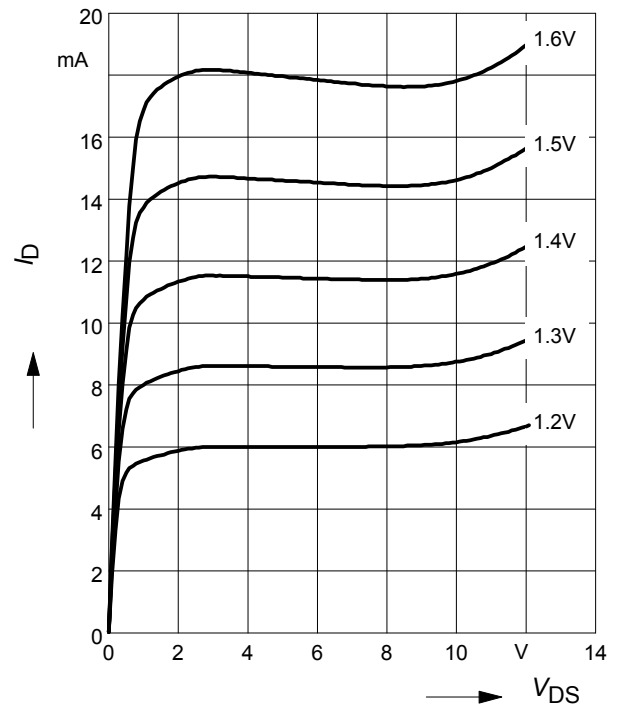
**Electrical Characteristics at  $T_A = 25^\circ\text{C}$ , unless otherwise specified**

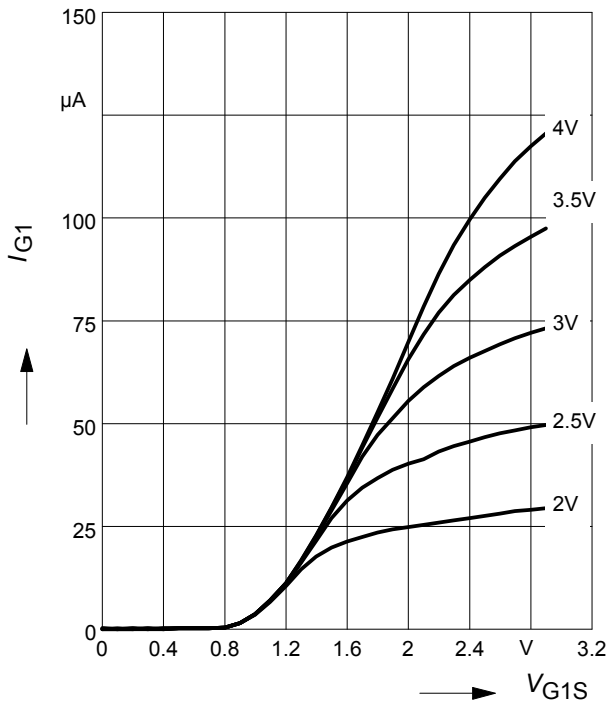
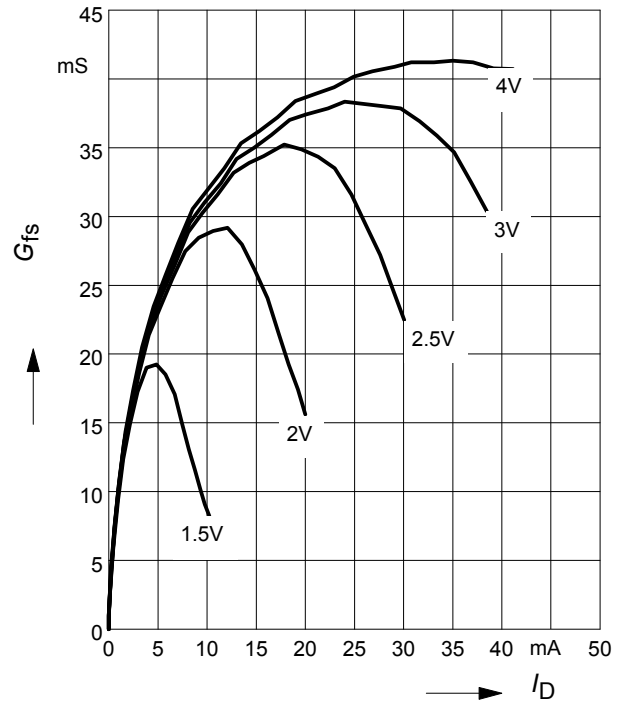
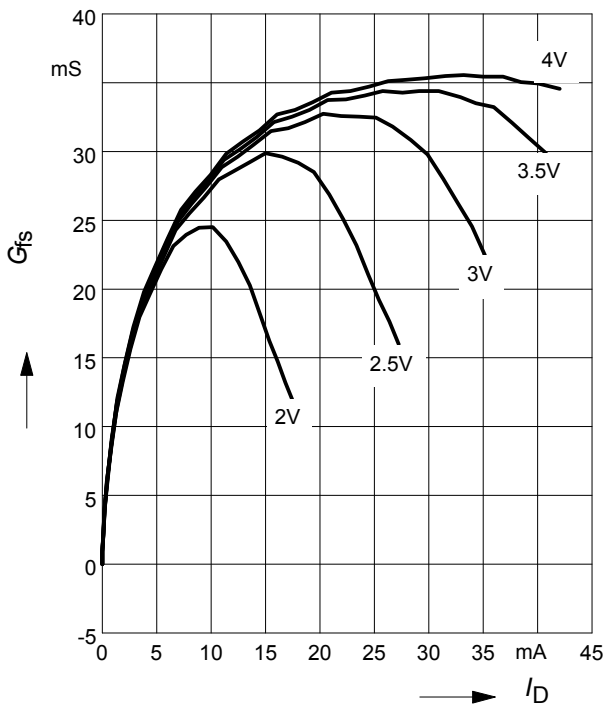
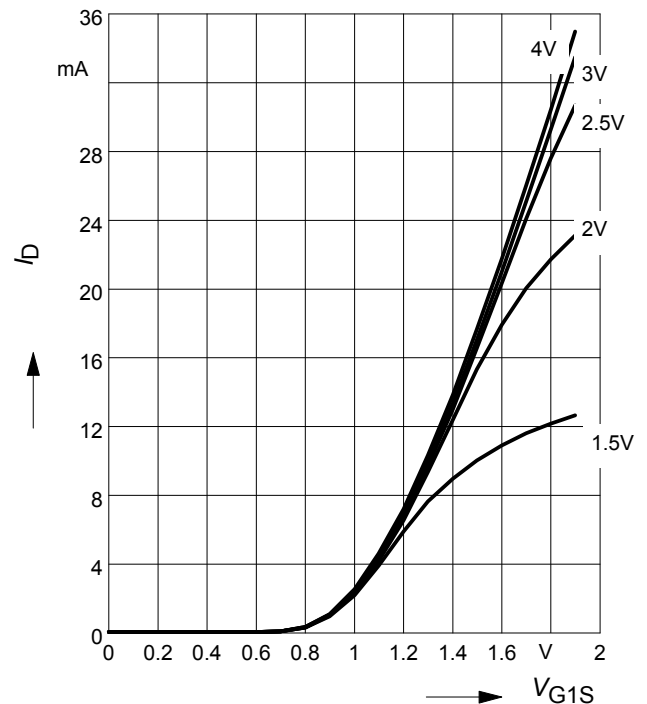
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>AC Characteristics <math>V_{DS} = 5\text{ V}</math>, <math>V_{G2} = 4\text{ V}</math>, <math>I_D = 10\text{ mA}</math> (verified by random sampling)</b>					
Forward transconductance amp. A amp. B	$g_{fs}$	- - -	33 30	- - -	mS
Gate1 input capacitance amp. A amp. B	$C_{g1ss}$	- -	2.2 2	- -	pF
Output capacitance amp. A amp. B	$C_{dss}$	- -	0.9 0.8	- -	
Power gain $f = 800\text{ MHz}$ , amp. A $f = 800\text{ MHz}$ , amp. B $f = 45\text{ MHz}$ , amp. A $f = 45\text{ MHz}$ , amp. B	$G_p$	- - - -	24 24 34 31	- - - -	dB
Noise figure $f = 800\text{ MHz}$ , amp. A $f = 800\text{ MHz}$ , amp. B $f = 45\text{ MHz}$ , amp. A $f = 45\text{ MHz}$ , amp. B	$F$	- - - -	1.1 1.2 0.8 0.9	- - - -	dB
Gain control range $V_{G2S} = 4\dots 0\text{ V}$ , $f = 800\text{ MHz}$	$\Delta G_p$	-	45	-	
Cross-modulation $k=1\%$ , $f_W=50\text{MHz}$ , $f_{unw}=60\text{MHz}$ amp. A, AGC = 0 dB amp. B, AGC = 0 dB amp. A, AGC = 10 dB amp. B, AGC = 10 dB amp. A, AGC = 40 dB amp. B, AGC = 40 dB	$X_{mod}$	- - - - - -	97 96 94 91 105 103	- - - - - -	-

**Functional diagram**

shows pinning of BG5412K, switching pin at PIN 3



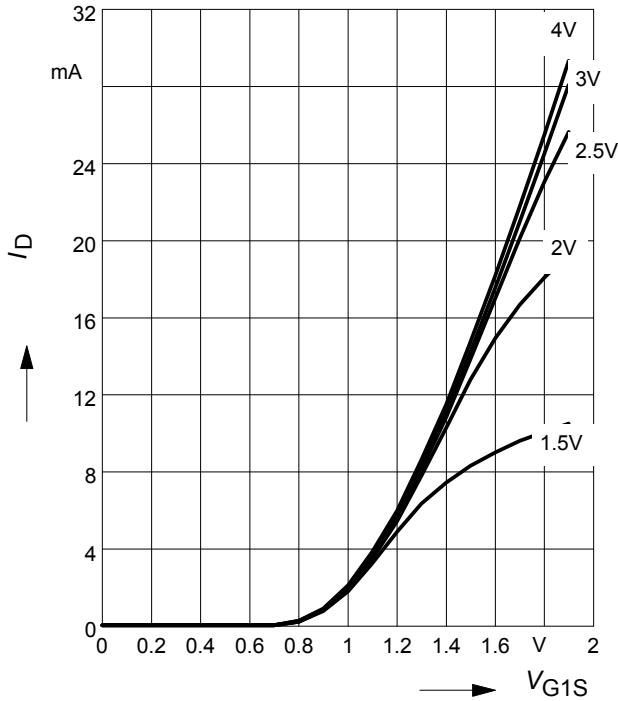
**Total power dissipation  $P_{\text{tot}} = f(T_S)$** 

**Drain current  $I_D = f(I_{G1})$** 
 $V_{G2S} = 4V, \text{ amp. B}$ 
 $V_{DS} = 5V$ 

**Output characteristics  $I_D = f(V_{DS})$** 
 $V_{G2} = 4V, \text{ amp. A}$ 
 $V_{G1} = \text{Parameter}$ 

**Output characteristics  $I_D = f(V_{DS})$** 
 $V_{G2} = 4V, \text{ amp. B}$ 
 $V_{G1} = \text{Parameter}$ 


**Gate 1 current  $I_{G1} = f(V_{G1S})$** 
 $V_{DS} = 5V$ 
 $V_{G2S} = \text{Parameter}$ 

**Gate 1 forward transconductance**
 $g_{fs} = f(I_D); \text{ amp. A}$ 
 $V_{DS} = 5V, V_{G2S} = \text{Parameter}$ 

**Gate 1 forward transconductance**
 $g_{fs} = f(I_D), \text{ amp. B}$ 
 $V_{DS} = 5V, V_{G2S} = \text{Parameter}$ 

**Drain current  $I_D = f(V_{G1S})$** 
 $V_{DS} = 5V, \text{ amp. A}$ 
 $V_{G2S} = \text{Parameter}$ 


**Drain current  $I_D = f(V_{G1S})$**

$V_{DS} = 5V$ , amp. B

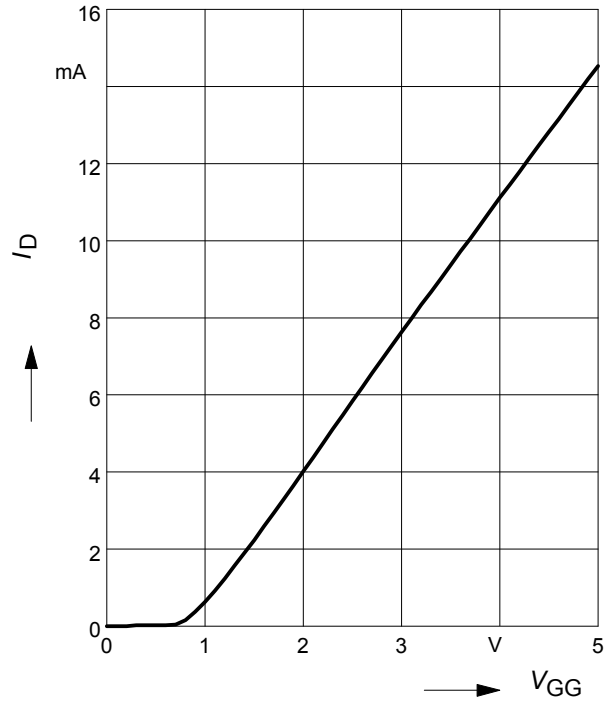
$V_{G2S} =$  Parameter



**Drain current  $I_D = f(V_{GG})$ , amp. B**

$V_{DS} = 5V$ ,  $V_{G2S} = 4V$ ,  $R_{G1} = 100k\Omega$

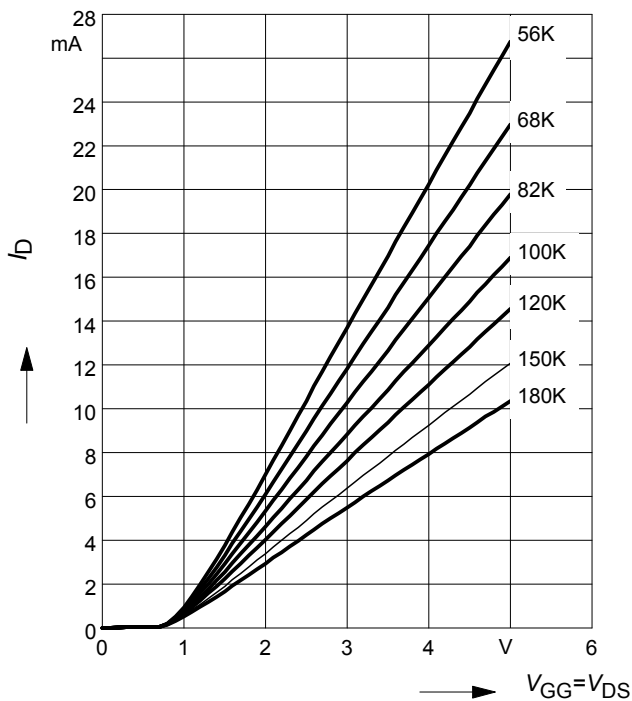
(connected to  $V_{GG}$ ,  $V_{GG} = \text{gate1 supply voltage}$ )



**Drain current  $I_D = f(V_{GG})$ , amp. B**

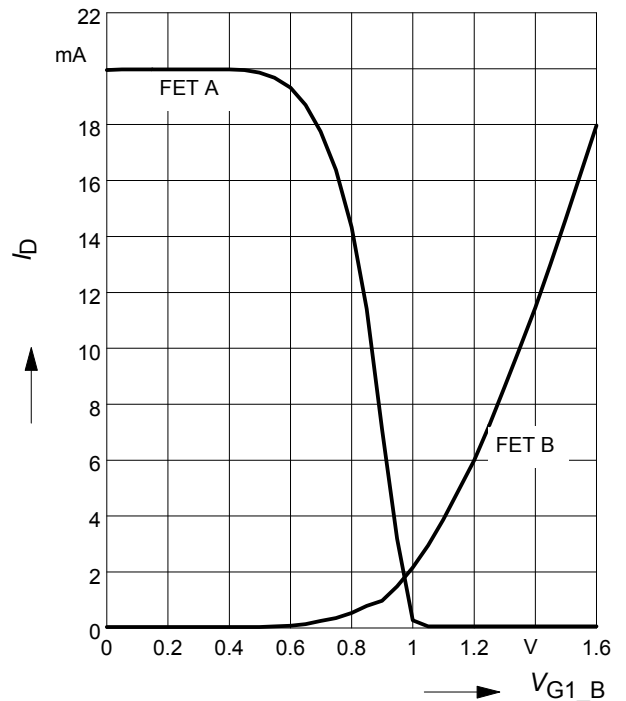
$V_{DS} = 5V$ ,  $V_{G2S} = 4V$

(connected to  $V_{GG}$ ,  $V_{GG} = \text{gate1 supply voltage}$ )



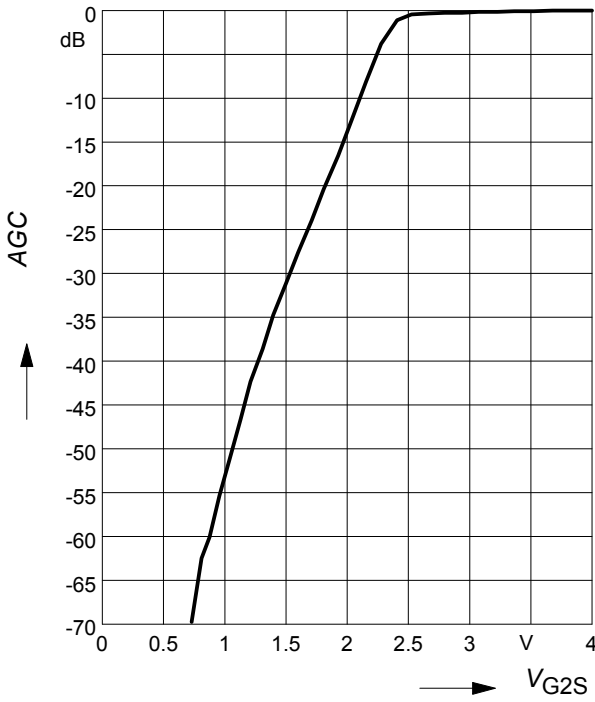
**Drain current of FET A and FET B**

as function of Gate 1 FET B



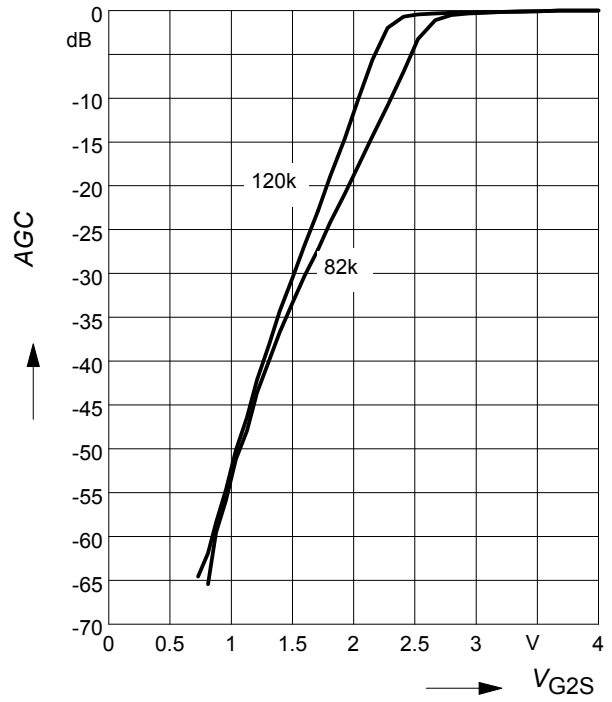
**AGC characteristic  $AGC = f(V_{G2S})$**

$f = 45 \text{ MHz, amp. A}$



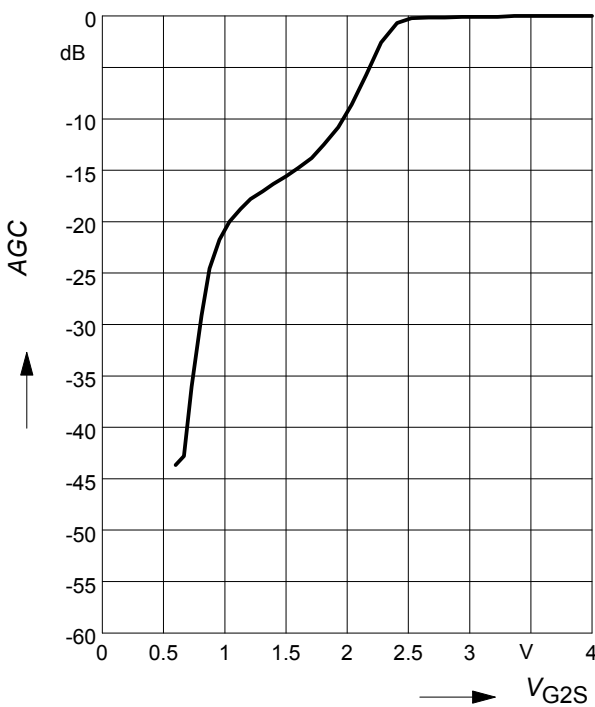
**AGC characteristic  $AGC = f(V_{G2S})$**

$f = 45 \text{ MHz, amp. B}$



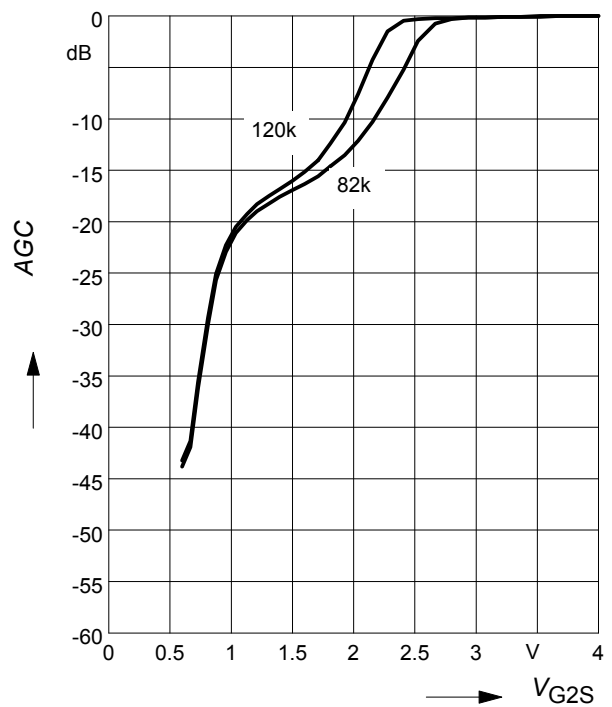
**AGC characteristic  $AGC = f(V_{G2S})$**

$f = 800 \text{ MHz, amp. A}$



**AGC characteristic  $AGC = f(V_{G2S})$**

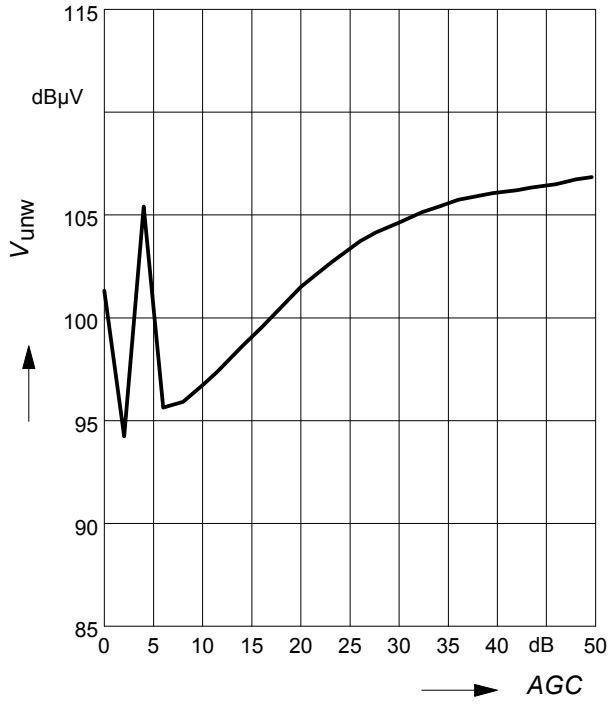
$f = 800 \text{ MHz, amp. B}$



**Crossmodulation  $V_{unw} = (AGC)$**

$V_{DS} = 5\text{ V}$ ,  $R_{g1} = 120\text{ k}\Omega$

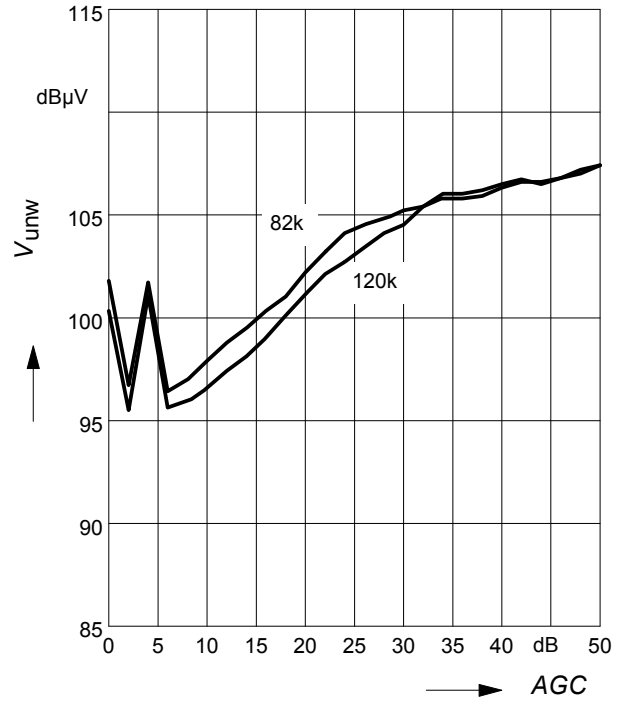
amp.A



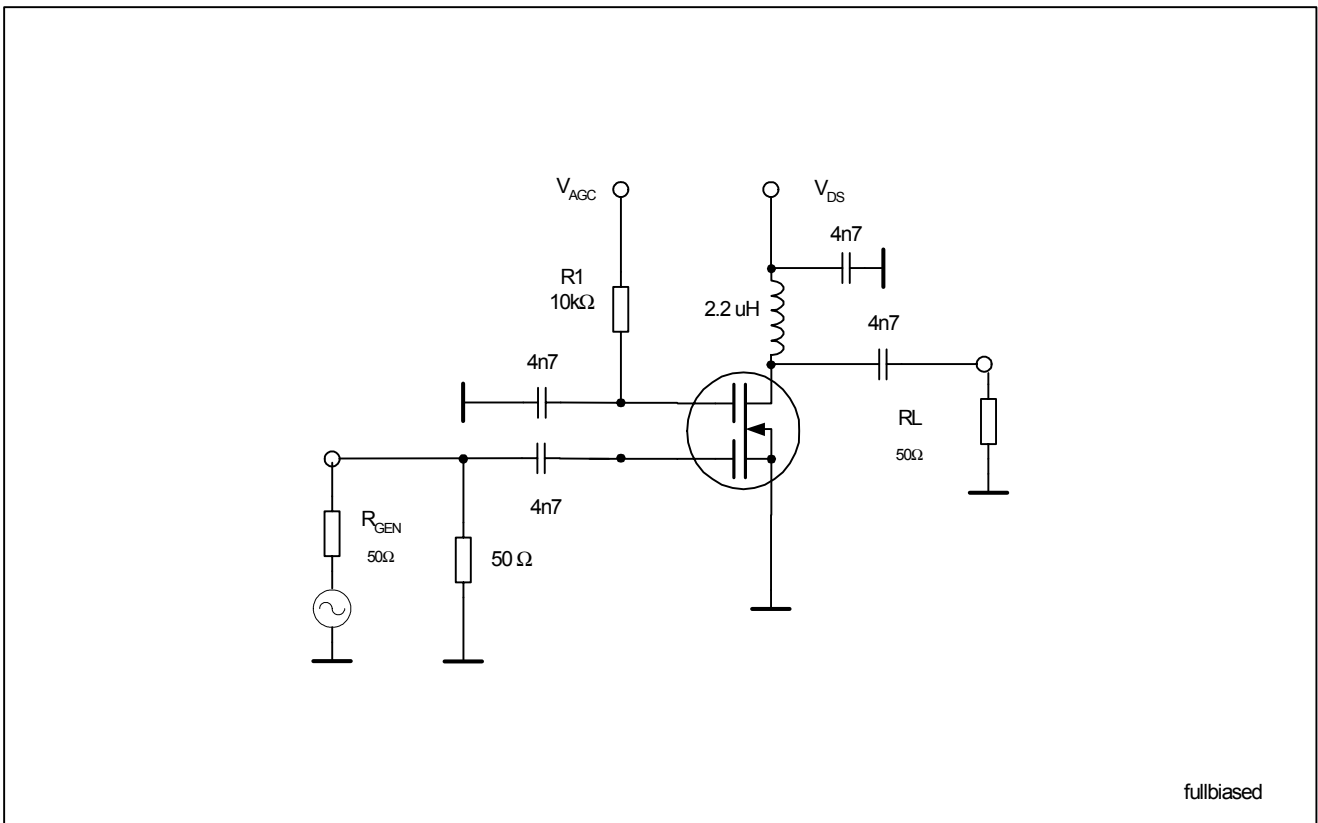
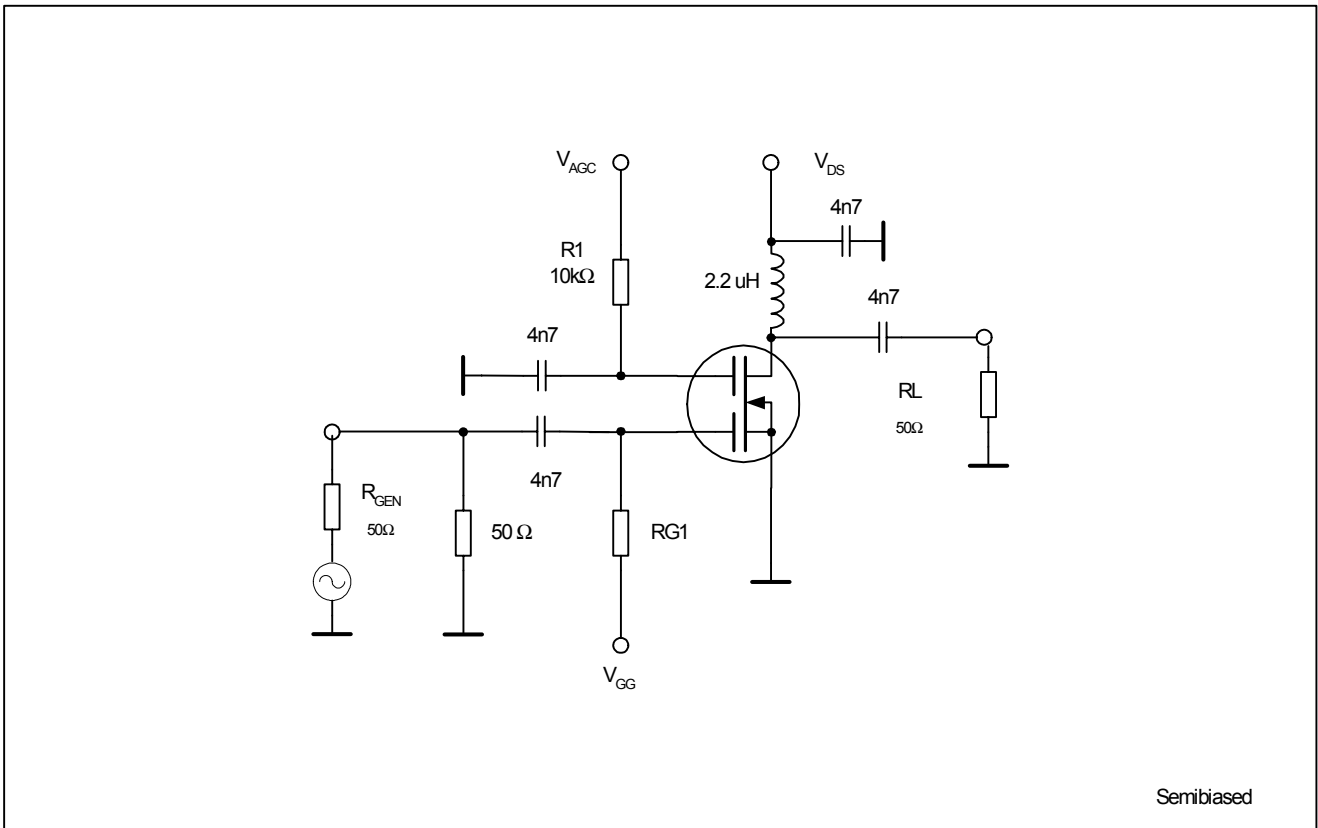
**Crossmodulation  $V_{unw} = (AGC)$**

$V_{DS} = 5\text{ V}$ ,  $R_{g1} = 56\text{ k}\Omega$

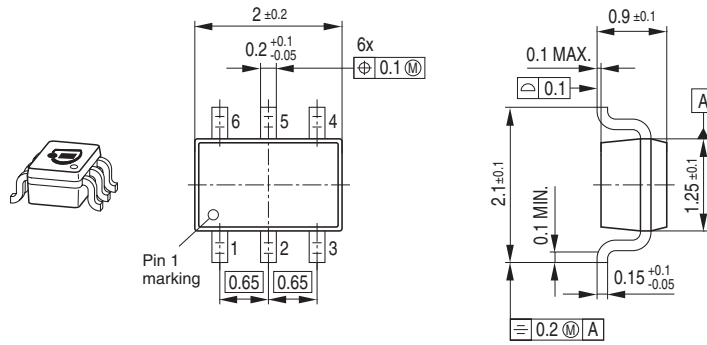
amp.B



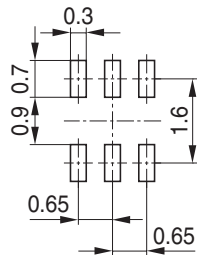
Crossmodulation test circuit



Package Outline

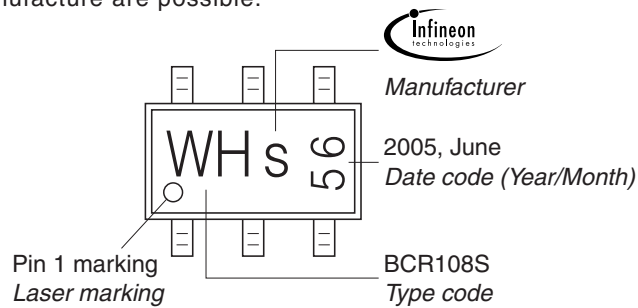


Foot Print



Marking Layout (Example)

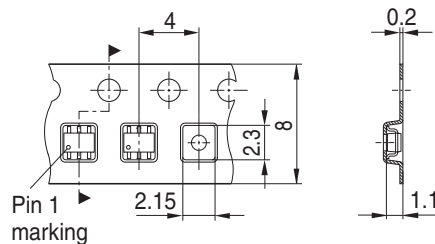
Small variations in positioning of Date code, Type code and Manufacture are possible.



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel  
 Reel ø330 mm = 10.000 Pieces/Reel

For symmetric types no defined Pin 1 orientation in reel.



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