

Structure	Silicon monolithic integrated circuit
Product	Color TV signal encoder
Type	BH7236AF
Features	Analog RGB signal is converted into video signals. It corresponds to both the systems of NTSC and PAL format.

○ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	VCC1, VCC2	7.0	V
Power dissipation	Pd	550 ^{*1}	mW
Storage temperature range	Tstg	-55 ~ +125	°C

^{*1} A measured value at mounting on 50 × 50 × 1.6mm glass epoxy substrate.
In the case of exceeding Ta=25°C, 5.5mW should be reduced per 1°C.

- * The radiation-resistance design is not carried out.
- * Operation is not guaranteed.

○ Operating Conditions (Ta=-20~+70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VCC1, VCC2	4.5	5.0	5.5	V
Input "H" voltage (SYNCIN,NT/PAL)	VIH	2.2	-	5.0 ^{*2}	V
Input "L" voltage (SYNCIN,NT/PAL)	VIL	0.0	-	0.8 ^{*2}	V
Input level (SCIN)	Vsci	0.4	-	5.0	Vpp
Input level (R,G,B)	Vrgbi	0	-	1.0	Vpp

^{*2} VCC1=VCC2=5.0V

Application example

- ROHM cannot provide adequate confirmation of patents.
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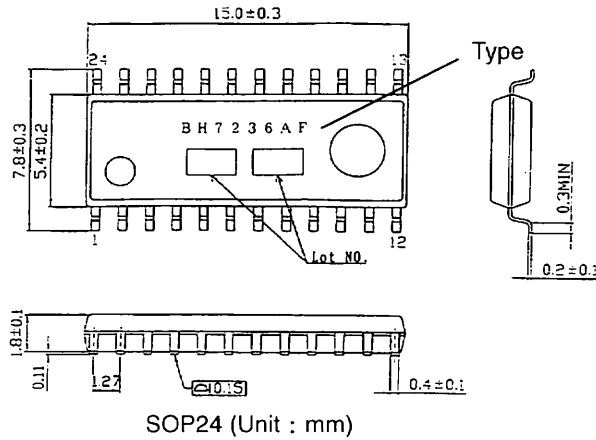
○ Electrical Characteristics (Ta=25°C, VCC1=VCC2=5.0V unless otherwise noted.)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Consumption current	Icc	-	42	55	mA	RIN=GIN=BIN=0.0Vpp input
Luminance level (Vout,Yout)						
White level	Vlwhite	0.63	0.70	0.77	Vpp	RIN=GIN=BIN=1.0Vpp input
Red level	Vlred	0.19	0.21	0.23	Vpp	RIN= 1.0Vpp input
Green level	Vlgreen	0.37	0.41	0.45	Vpp	GIN= 1.0Vpp input
Blue level	Vlblue	0.07	0.08	0.09	Vpp	BIN= 1.0Vpp input
Sync level	Vsync	0.27	0.30	0.33	Vpp	
Sync/White level ratio	Rs/w	0.38	0.43	0.48		Rs/w = Vsync/Vlwhite
Chroma level (Vout,Cout)						
Red/Burst level ratio	Vcr/Vbur	2.84	3.16	3.48	-	RIN= 1.0Vpp input *3
Green/Burst level ratio	Vcg/Vbur	2.65	2.95	3.25	-	GIN= 1.0Vpp input *3
Blue/Burst level ratio	Vcb/Vbur	2.01	2.24	2.47	-	BIN= 1.0Vpp input *3
Burst level	Vbur	0.23	0.29	0.35	Vpp	*4
Red phase	θ red	94	104	114	deg	RIN= 1.0Vpp input *3
Green phase	θ green	231	241	251	deg	GIN= 1.0Vpp input *3
Blue phase	θ blue	337	347	357	deg	BIN= 1.0Vpp input *3
PAL burst phase	θ bur+	125	135	145	deg	Color subcarrier =4.433619MHz (NT/PAL = L) *3
	θ bur-	215	225	235	deg	
PAL burst level ratio	Rbur	0.9	1.0	1.1	-	Level ratio per every 1 line
Carrier leak	Vcl	-	-	35	mVpp	*4
RGB level (Rout,Gout,Bout)						
Red level	Vro	0.63	0.70	0.77	Vpp	RIN= 1.0Vpp input
Green level	Vgo	0.63	0.70	0.77	Vpp	GIN= 1.0Vpp input
Blue level	Vbo	0.63	0.70	0.77	Vpp	BIN= 1.0Vpp input
SYNCOUT High level	Vhsync	3.90	-	-	V	
SYNCOUT Low level	Vlsync	-	-	0.80	V	
Output DC voltage						
YOUT	Vyo	1.30	1.70	2.10	V	
COUT	Vco	2.00	2.40	2.80	V	
VOUT	Vvo	1.15	1.55	1.95	V	
ROUT	Vro	1.40	1.80	2.20	V	
GOUT	Vgo	1.40	1.80	2.20	V	
BOUT	Vbo	1.40	1.80	2.20	V	

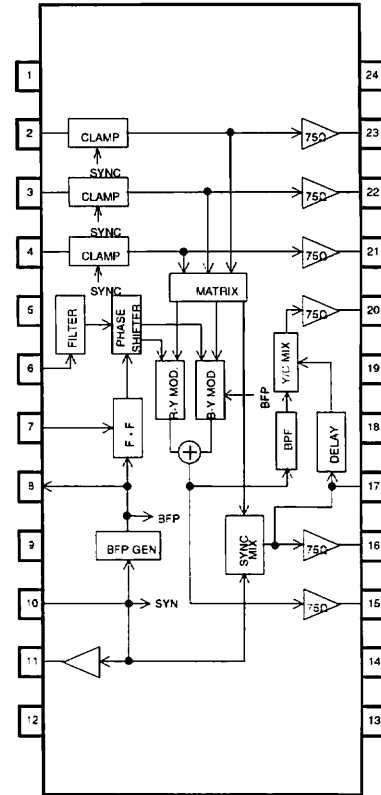
*3 This specification is design target.

*4 This specification is measured with 3.58MHz BPF.

○ Package outline



○ Block diagram



○ Terminal functions

Terminal No.	Terminal name	Description of terminals	Terminal No.	Terminal name	Description of terminals
1	GND1	Ground terminal except 75Ω driver	13	N.C.	No Connection
2	RIN	Analog Red signal input terminal.	14	N.C.	No Connection
3	GIN	Analog Green signal input terminal.	15	COUT	Chroma signal output terminal.
4	BIN	Analog Blue signal input terminal.	16	YOUT	Luminance signal output terminal.
5	N.C.	No Connection	17	YTRAP	Luminance trap filter terminal.
6	SCIN	Color subcarrier input terminal.	18	N.C.	No Connection
7	NT/PAL	Input terminal for the selection of TV format.	19	VCC2	Power supply terminal for 75Ω driver.
8	BFPOUT	Burst timing signal output terminal.	20	VOUT	Composite video output terminal.
9	N.C.	No Connection	21	BOUT	Analog B signal output terminal.
10	SYNCIN	Composite sync input terminal.	22	GOUT	Analog G signal output terminal.
11	SYNCOUT	Composite sync output terminal.	23	ROUT	Analog R signal output terminal.
12	VCC1	Power supply terminal except 75Ω driver.	24	GND2	Ground terminal for 75Ω driver

○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as power-supply voltage, operating temperature range, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(1 0) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(1 1) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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