THE DATASHEET OF

BLF7G20LS-140P,118

BLF7G20LS-140P

Power LDMOS transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

140 W LDMOS power transistor for base station applications at frequencies from 1800 MHz to 2000 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Mode of operation	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	$ACPR_{400k}$ (dBc)	$ACPR_{600k}$ (dBc)	EVM_{rms} (%)
CW	1805 to 1880	850	28	125	17	54	-	-	-
GSM EDGE	1805 to 1880	850	28	60	17.5	41	–61	–75	2.7

1.2 Features and benefits

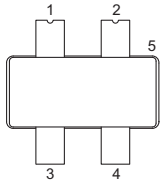
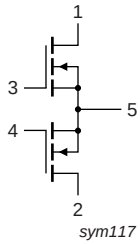
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (1800 MHz to 2000 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1800 MHz to 2000 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G20LS-140P	-	earless flanged LDMOST ceramic package; 4 leads	SOT1121B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 100 W	0.41	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.9 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 90 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	14	-	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	200	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2.5 A	-	6.45	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 3.15 A	-	0.15	-	Ω

7. Test information

Table 7. Application information

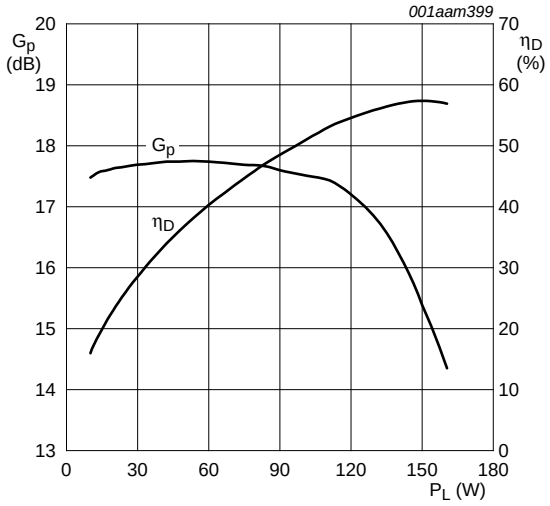
f = 1805 MHz and 1880 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 850 mA; T_{case} = 25 °C; 2 sections combined unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mode of operation: GSM EDGE; $P_{L(AV)}$ = 60 W						
G_p	power gain		16.3	17.5	-	dB
RL_{in}	input return loss		-	–15	–8	dB
η_D	drain efficiency		37	41	-	%
$ACPR_{400k}$	adjacent channel power ratio (400 kHz)		-	–61	–56.5	dBc
$ACPR_{600k}$	adjacent channel power ratio (600 kHz)		-	–75	–69.5	dBc
EVM_{rms}	RMS EDGE signal distortion error		-	2.7	4.0	%
EVM_M	peak EDGE signal distortion error		-	8.5	12.5	%
Mode of operation: CW; $P_{L(AV)}$ = 125 W						
G_p	power gain		16	17	-	dB
η_D	drain efficiency		48	54	-	%

7.1 Ruggedness in class-AB operation

The BLF7G20LS-140P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 850 mA; P_L = 140 W (CW); f = 1805 MHz.

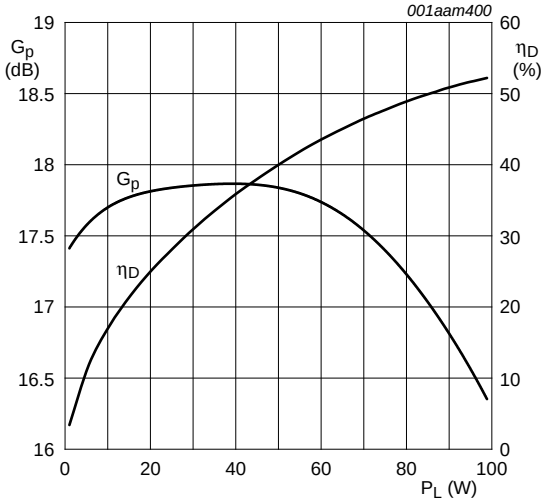
7.2 One-tone CW



V_{DS} = 28 V; I_{Dq} = 850 mA; f = 1880 MHz.

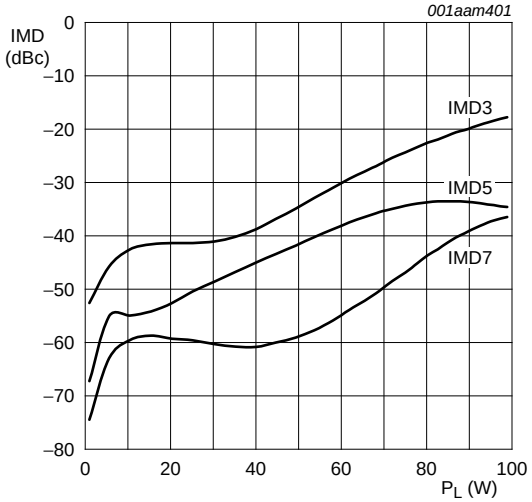
Fig 1. One-tone CW power gain and drain efficiency as function of load power; typical values

7.3 Two-tone CW



V_{DS} = 28 V; I_{Dq} = 850 mA; f_1 = 1879.95 MHz; f_2 = 1880.05 MHz.

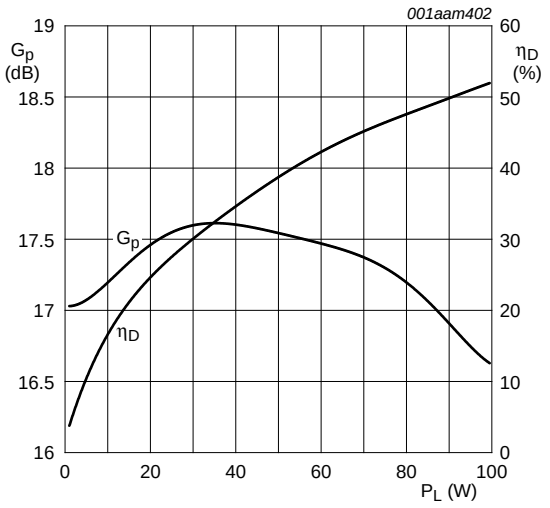
Fig 2. Two-tone CW power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 850 mA; f_1 = 1879.95 MHz; f_2 = 1880.05 MHz.

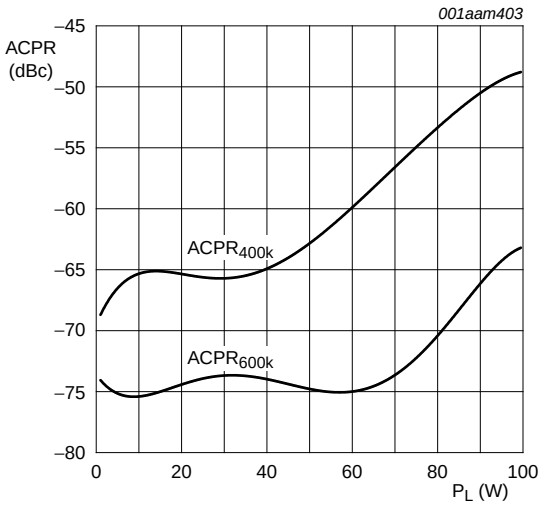
Fig 3. Two-tone CW intermodulation distortion as a function of load power; typical values

7.4 GSM EDGE



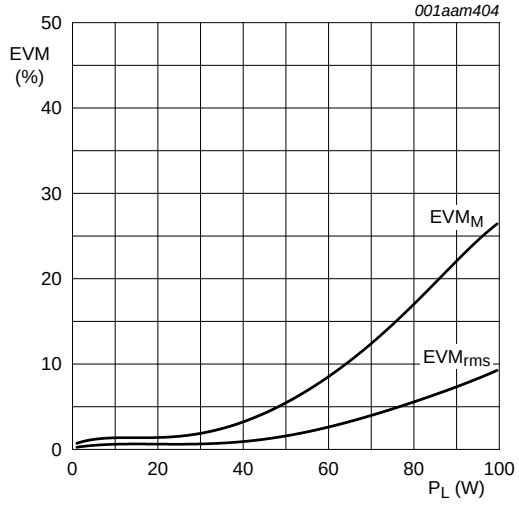
V_{DS} = 28 V; I_{Dq} = 850 mA; f = 1880 MHz.

Fig 4. GSM EDGE power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 850 mA; f = 1880 MHz.

Fig 5. GSM EDGE ACPR at 400 kHz and at 600 kHz as function of load power; typical values

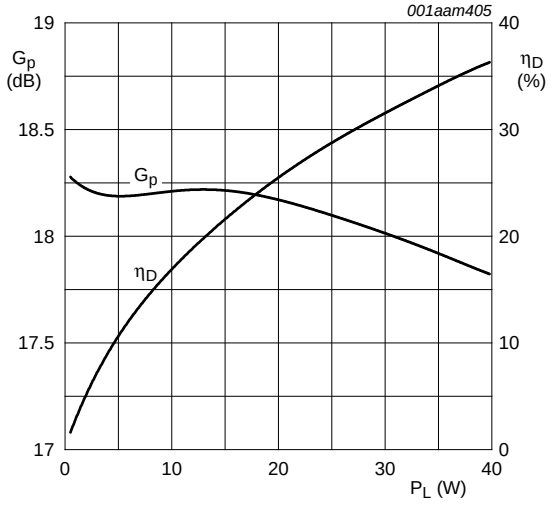


V_{DS} = 28 V; I_{Dq} = 850 mA; f = 1880 MHz.

Fig 6. GSM-EDGE RMS EVM and peak EVM as function of load power; typical values

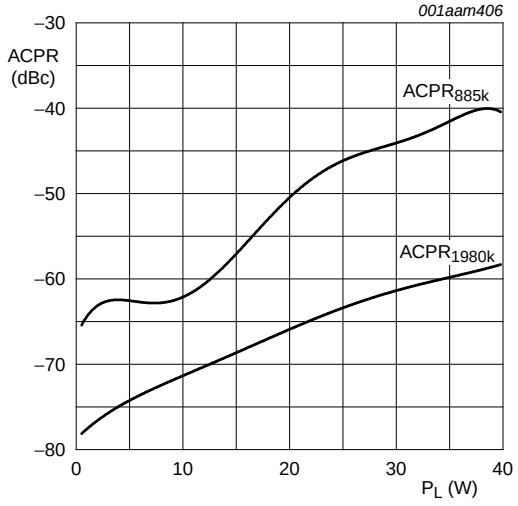
7.5 Single carrier IS-95

Single carrier IS-95 with pilot, paging, sync and 6 traffic channels (Walsh codes 8 - 13). PAR = 9.7 dB at 0.01 % probability on the CCDF. Channel bandwidth is 1.2288 MHz.



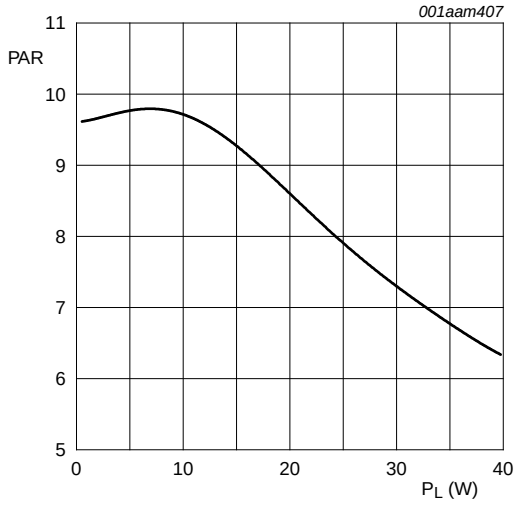
V_{DS} = 28 V; I_{Dq} = 1080 mA; f = 1880 MHz.

Fig 7. Single carrier IS-95 power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 1080 mA; f = 1880 MHz.

Fig 8. Single carrier IS-95 ACPR at 885 kHz and at 1980 kHz as function of load power; typical values

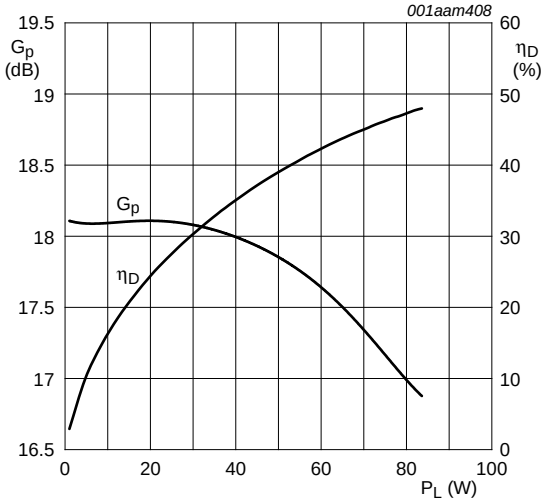


V_{DS} = 28 V; I_{Dq} = 1080 mA; f = 1880 MHz.

Fig 9. Single carrier IS-95 peak-to-average power ratio as a function of load power; typical values

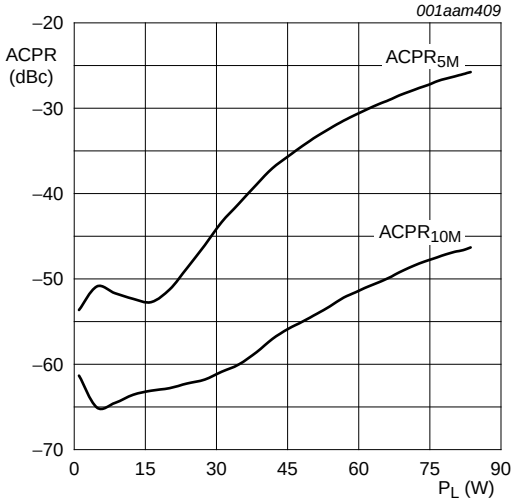
7.6 Single carrier W-CDMA

3GPP; test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF. Channel bandwidth is 3.84 MHz.



V_{DS} = 28 V; I_{Dq} = 1080 mA; f = 1880 MHz.

Fig 10. Single carrier W-CDMA power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 1080 mA; f = 1880 MHz.

Fig 11. Single carrier W-CDMA ACPR at 5 MHz and at 10 MHz as function of load power; typical values

7.7 Test circuit

Table 8. List of components

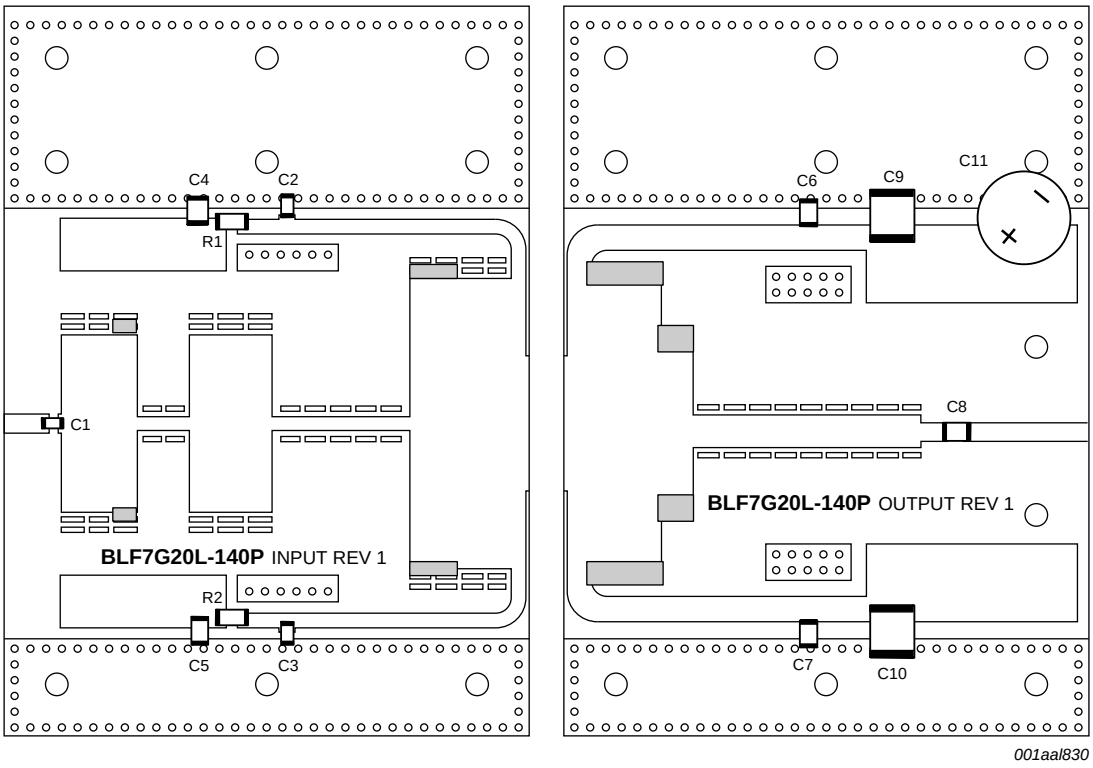
For test circuit see Figure 12.

Component	Description	Value		Remarks
C1, C2, C3	multilayer ceramic chip capacitor	24 pF	[1]	
C4, C5	multilayer ceramic chip capacitor	4.7 μF	[2]	
C6, C7, C8	multilayer ceramic chip capacitor	11 pF	[3]	
C9, C10	multilayer ceramic chip capacitor	10 μF	[2]	
C11	electrolytic capacitor	470 μF; 63 V		
R1, R2	SMD resistor	12 Ω		Philips 1206

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] TDK or capacitor of same quality.

[3] American Technical Ceramics type 100B or capacitor of same quality.



Printed-Circuit Board (PCB): Taconic RF35; ε_r = 3.5 F/m; thickness = 0.76 mm; thickness copper plating = 35 μm.
See Table 8 for a list of components.

Fig 12. Component layout for class-AB production test circuit

7.8 Impedance information

Table 9. Typical impedance

Typical values valid for both section in parallel unless otherwise specified.

f	Z_S	Z_L
MHz	Ω	Ω
1800	1.1 – j3.8	1.8 – j2.8
1840	1.3 – j3.7	1.7 – j2.6
1880	1.2 – j3.8	1.6 – j2.5

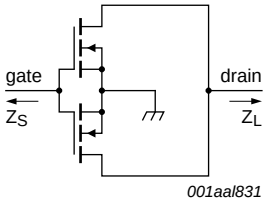
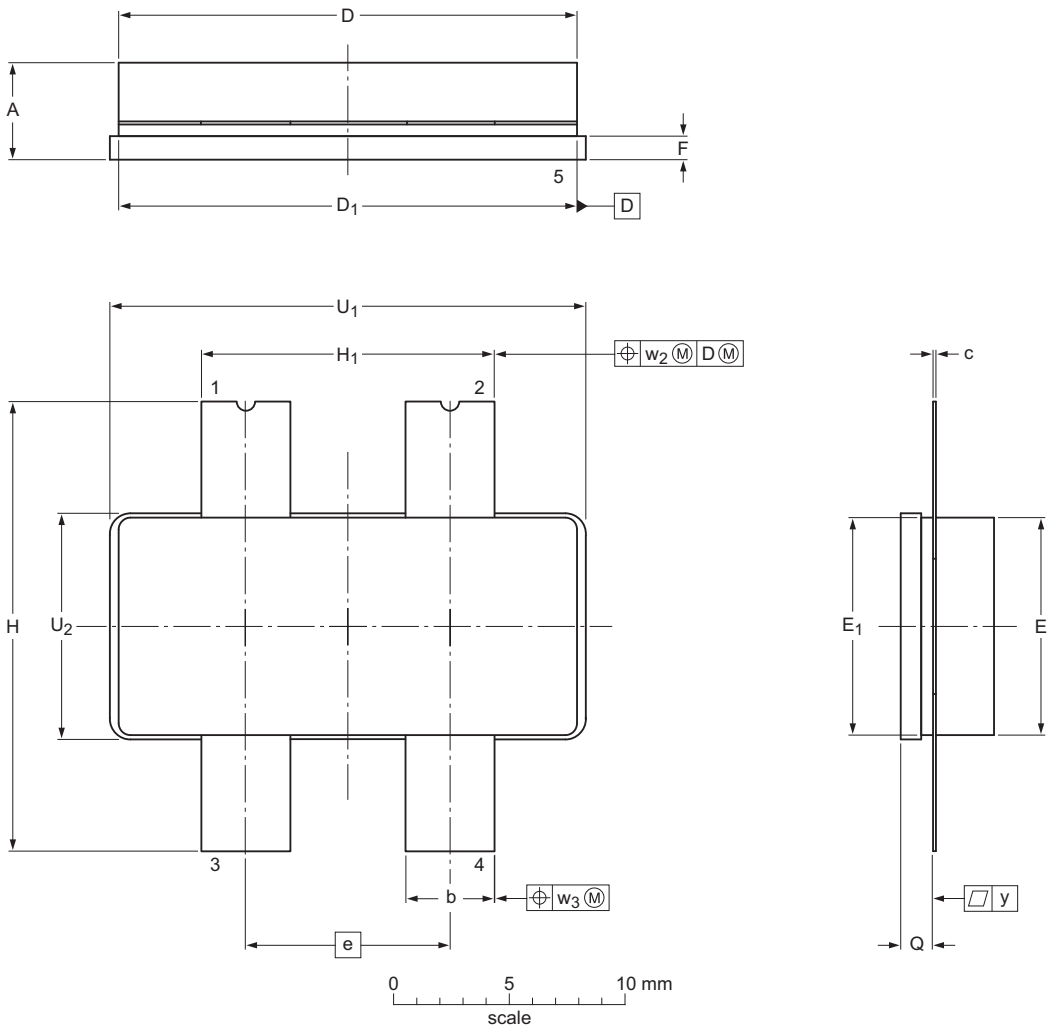


Fig 13. Definition of transistor impedance

8. Package outline

Earless flanged ceramic package; 4 leads **SOT1121B**



Dimensions

Unit(1)		A	b	c	D	D_1	e	E	E_1	F	H	H_1	Q	U_1	U_2	w_2	w_3	y
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	1.70	20.70	9.91	0.51	0.25	0.25
	nom						8.89											
	min	3.45	3.68	0.08	19.61	19.66		9.27	9.27	0.89	18.92	12.57	1.45	20.45	9.65			
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.067	0.815	0.39	0.02	0.01	0.01
	nom						0.35											
	min	0.136	0.145	0.003	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.057	0.805	0.38			

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121B						~~09-12-14~~ 12-06-07

Fig 14. Package outline SOT1121B

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
ESD	ElectroStatic Discharge
GSM	Global System for Mobile communications
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G20LS-140P#3	20150901	Product data sheet	-	BLF7G20LS-140P v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLF7G20LS-140P v.2	20100817	Product data sheet	-	BLF7G20L-140P_ 7G20LS-140P v.1
BLF7G20L-140P_7G20LS-140P v.1	20100421	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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13. Contents

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