



**THE DATASHEET OF
74ABT16240ADGG,118**





74ABT16240A

16-bit inverting buffer/line driver; 3-state

Rev. 9 — 24 June 2024

Product data sheet

1. General description

The 74ABT16240A is a 16-bit inverting buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The device features four output enables (1OE, 2OE, 3OE and 4OE), each controlling four of the 3-state outputs. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 4.5 V to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- 3-state buffers
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Output capability: +64 mA and -32 mA
- Live insertion and extraction permitted
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ABT16240ADGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

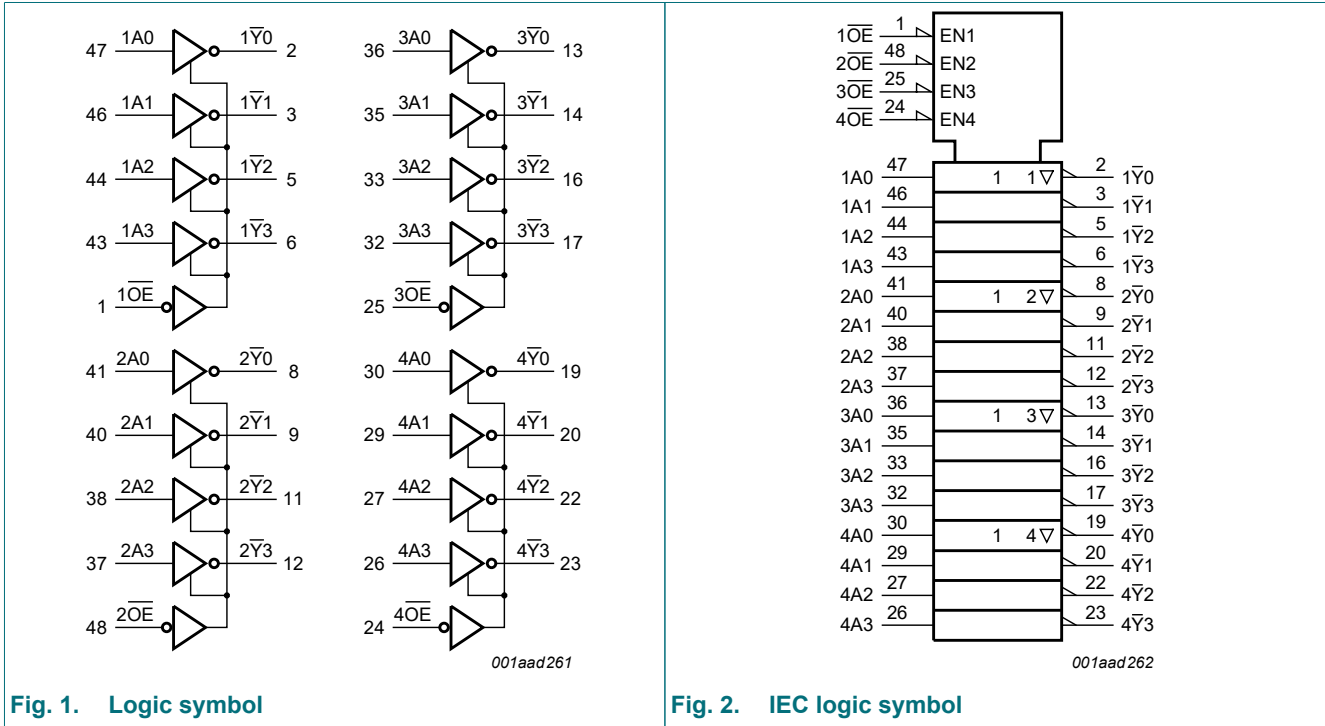
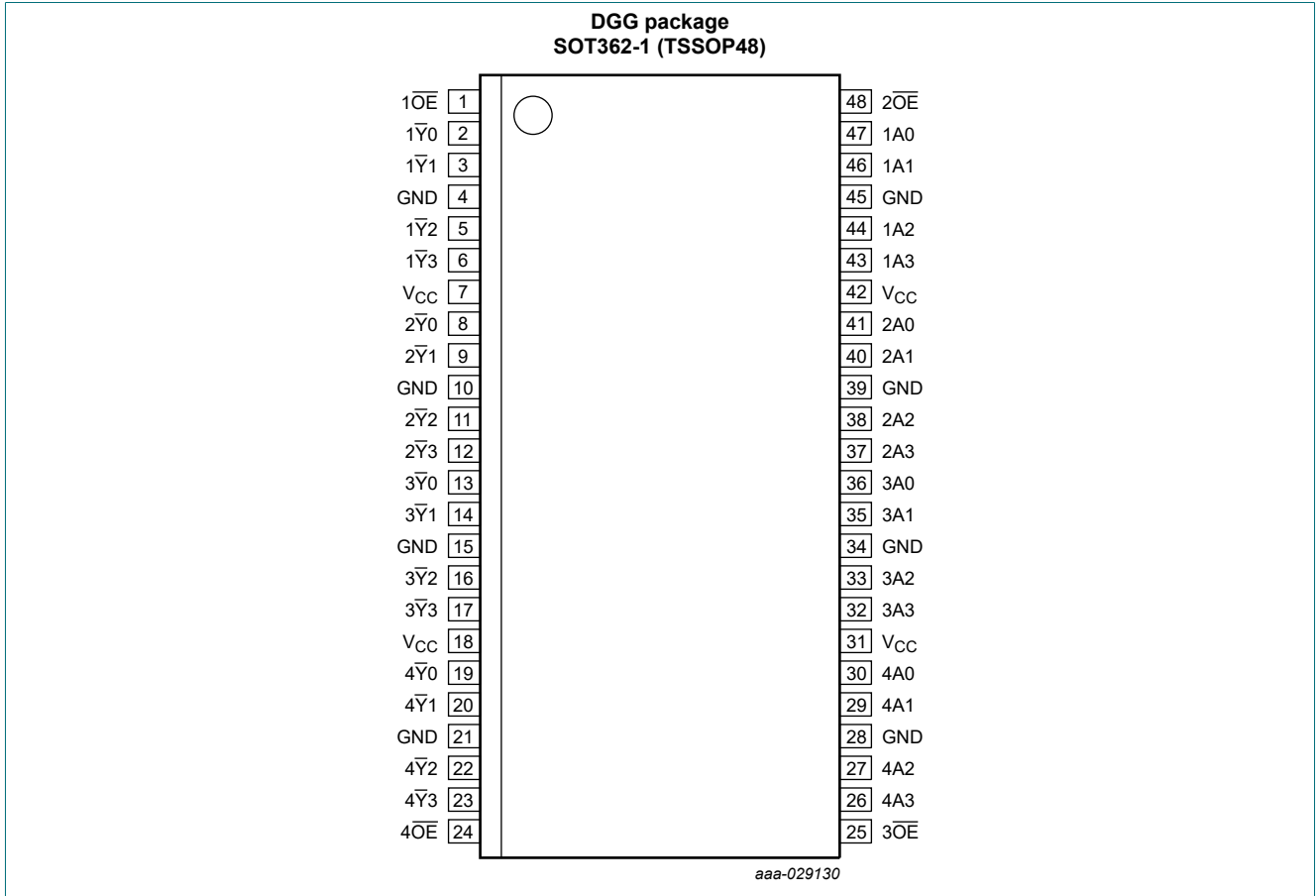


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 48, 25, 24	1 to 4 output enable (LOW active)
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	1 data output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC}	7, 18, 31, 42	supply voltage
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	2 data output
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	3 data output
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	4 data output
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	4 data input
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	3 data input
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	2 data input
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	1 data input

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nAn	nYn
L	L	H
L	H	L
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		[1] -1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T_j	junction temperature		[2] -	150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level Input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current		-	-	32	mA
		duty cycle ≤ 50 %; $f_i \geq 1$ kHz	-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		-	-	10	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$	-1.2	-0.9	-	-1.2	-	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IL} \text{ or } V_{IH}$						
		$V_{CC} = 4.5 \text{ V}; I_{OH} = -3 \text{ mA}$	2.5	2.9	-	2.5	-	V
		$V_{CC} = 5.0 \text{ V}; I_{OH} = -3 \text{ mA}$	3.0	3.4	-	3.0	-	V
		$V_{CC} = 4.5 \text{ V}; I_{OH} = -32 \text{ mA}$	2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 4.5 \text{ V}; I_{OL} = 64 \text{ mA};$ $V_I = V_{IL} \text{ or } V_{IH}$	-	0.42	0.55	-	0.55	V
I_I	input leakage current	$V_{CC} = 5.5 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}$	-	± 0.01	± 1.0	-	± 1.0	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_I \text{ or } V_O \leq 4.5 \text{ V}$	-	± 5.0	± 100	-	± 100	μA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.0 \text{ V}; V_O = 0.5 \text{ V};$ $V_I = \text{GND or } V_{CC}; n\overline{OE} = \text{HIGH}$ [1]	-	± 5.0	± 50	-	± 50	μA
I_{OZ}	OFF-state output current	$V_{CC} = 5.5 \text{ V}; V_I = V_{IL} \text{ or } V_{IH}$						
		output HIGH-state at $V_O = 5.5 \text{ V}$	-	1.0	10	-	10	μA
		output LOW-state at $V_O = 0.5 \text{ V}$	-	-1.0	-10	-	-10	μA
I_{CEX}	output high leakage current	HIGH-state; $V_O = 5.5 \text{ V};$ $V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } V_{CC}$	-	1.0	50	-	50	μA
I_O	output current	$V_{CC} = 5.5 \text{ V}; V_O = 2.5 \text{ V}$ [2]	-180	-70	-50	-180	-50	mA
I_{CC}	supply current	$V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } V_{CC}$						
		outputs HIGH-state	-	0.5	1.0	-	1.0	mA
		outputs LOW-state	-	8	19	-	19	mA
		outputs 3-state	-	0.5	1.0	-	1.0	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 5.5 \text{ V};$ one input at 3.4 V and other inputs at $V_{CC} \text{ or } \text{GND}$ [3] [4]	-	10	200	-	200	μA
C_I	input capacitance	$V_I = 0 \text{ V or } V_{CC}$	-	4	-	-	-	pF
$C_{I/O}$	input/output capacitance	outputs disabled; $V_O = 0 \text{ V or } V_{CC}$	-	6	-	-	-	pF

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms.

From $V_{CC} = 2.1 \text{ V}$ to $V_{CC} = 5 \text{ V} \pm 10 \%$, a transition time of up to 100 μs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

[4] This data sheet limit may vary among suppliers.

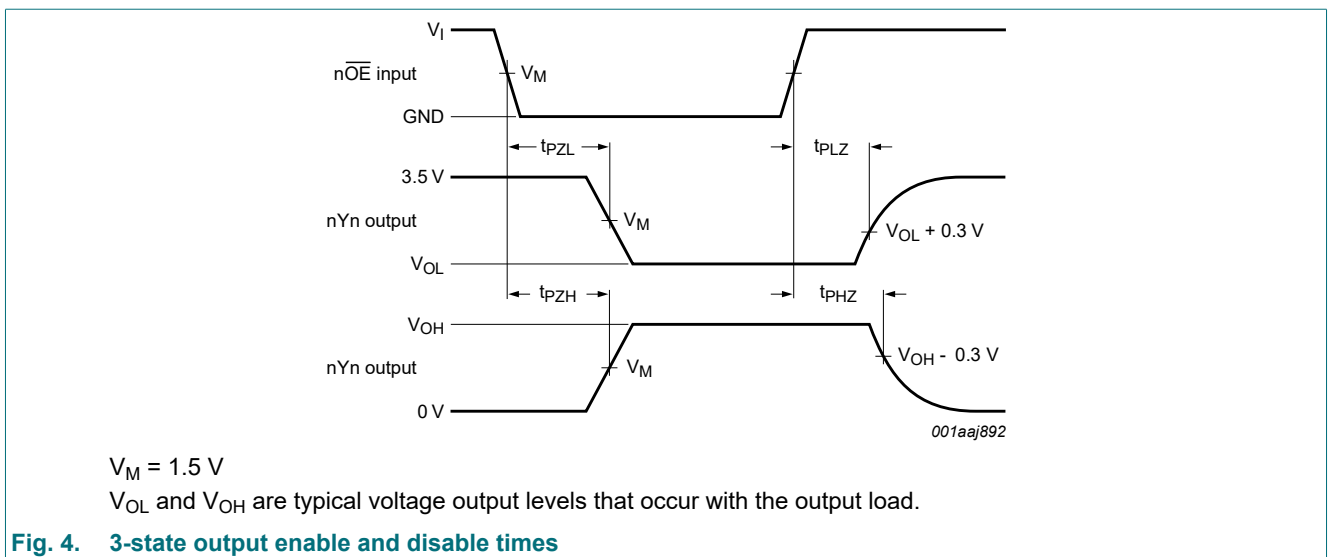
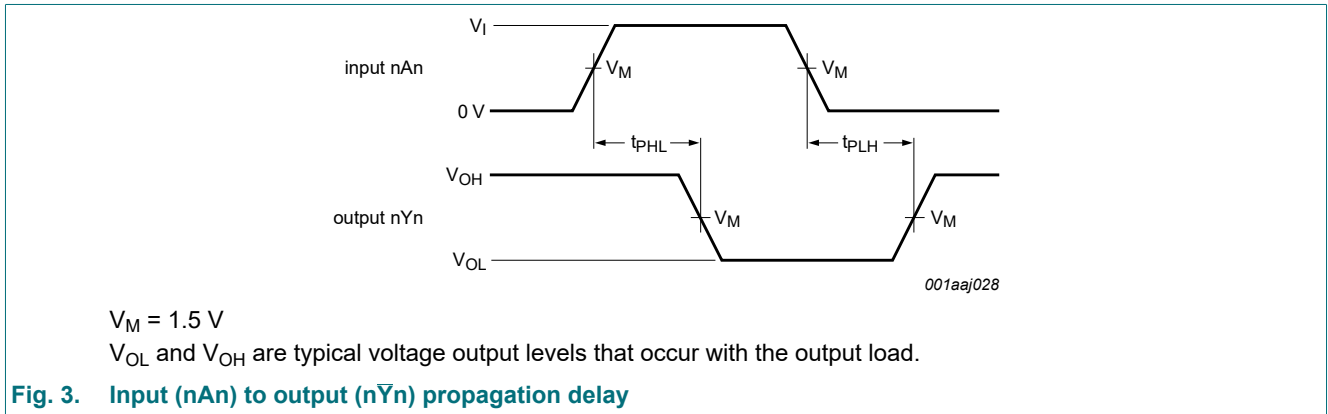
10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$. For test circuit, see Fig. 5.

Symbol	Parameter	Conditions	25 °C; $V_{CC} = 5.0\text{ V}$			-40 °C to +85 °C; $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	nAn to $n\bar{Y}n$, see Fig. 3	1.0	2.0	3.0	1.0	3.7	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to $n\bar{Y}n$, see Fig. 3	1.0	1.5	3.0	1.0	3.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\bar{OE}$ to $n\bar{Y}n$; see Fig. 4	1.2	2.4	3.3	1.2	4.2	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\bar{OE}$ to $n\bar{Y}n$; see Fig. 4	1.2	2.3	3.2	1.0	4.2	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\bar{OE}$ to $n\bar{Y}n$; see Fig. 4	1.3	2.7	4.1	1.6	4.7	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\bar{OE}$ to $n\bar{Y}n$; see Fig. 4	1.3	2.5	3.6	1.4	4.1	ns

10.1. Waveforms and test circuit



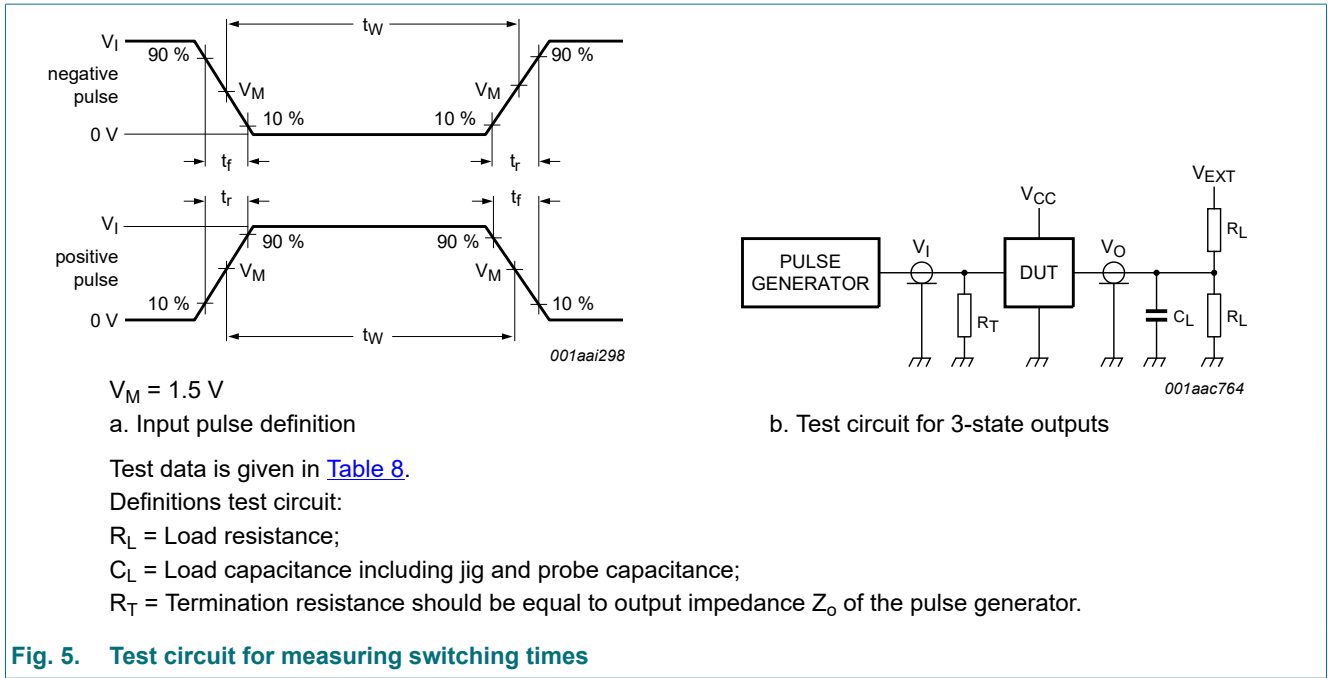


Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_w	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 Ω	open	7.0 V	open

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

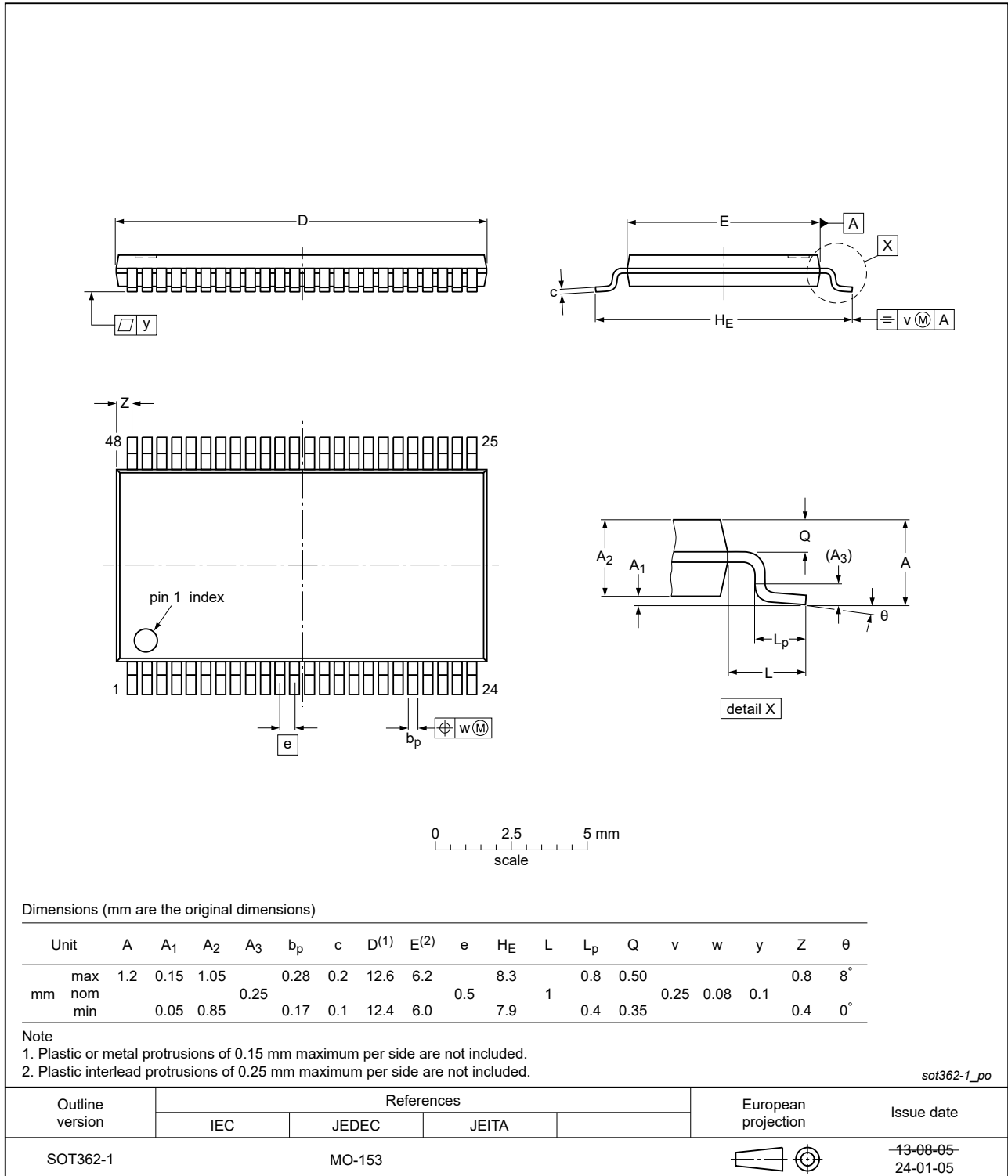


Fig. 6. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar CMOS
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT16240A v.9	20240624	Product data sheet	-	74ABT16240A v.8
Modifications:	<ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74ABT16240A v.8	20240419	Product data sheet	-	74ABT16240A v.7
Modifications:	<ul style="list-style-type: none"> • Fig. 6: Updated package outline drawing SOT362-1 (TSSOP48). 			
74ABT16240A v.7	20210707	Product data sheet	-	74ABT16240A v.6
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Fig. 6: Package outline drawing SOT362-1 (TSSOP48) updated. • Type number 74ABT16240ADL (SOT370-1/SSOP48) removed. • Section 1 and Section 2 updated. 			
74ABT16240A v.6	20111103	Product data sheet	-	74ABT16240A v.5
Modifications:	<ul style="list-style-type: none"> • Legal pages updated 			
74ABT16240A v.5	20100525	Product data sheet	-	74ABT16240A v.4
74ABT16240A v.4	20090325	Product data sheet	-	74ABT16240A v.3
74ABT16240A v.3	20040212	Product specification	01-A15420	74ABT_H16240A v.2
74ABT_H16240A v.2	19980225	Product specification	853-1880 19019	74ABT_H16240A
74ABT_H16240A	19961001	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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