



**THE DATASHEET OF
74AVCH16244DGG,112**



74AVCH16244

16-bit buffer/line driver; 3.6 V tolerant; 3-state

Rev. 2 — 20 February 2018

Product data sheet

1 General description

The 74AVCH16244 is a 16-bit non-inverting buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-state outputs are controlled by the output enable inputs \overline{nOE} . A HIGH on \overline{nOE} causes the outputs to assume a high impedance OFF-state.

The 74AVCH16244 is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance output state during power-up or power-down, \overline{nOE} should be tied to V_{CC} through a pull-up resistor (Live Insertion).

A dynamic controlled output (DCO) circuitry is implemented to support termination line drive during transient (see [Figure 4](#)).

The 74AVCH16244 has active bus-hold circuitry to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2 Features and benefits

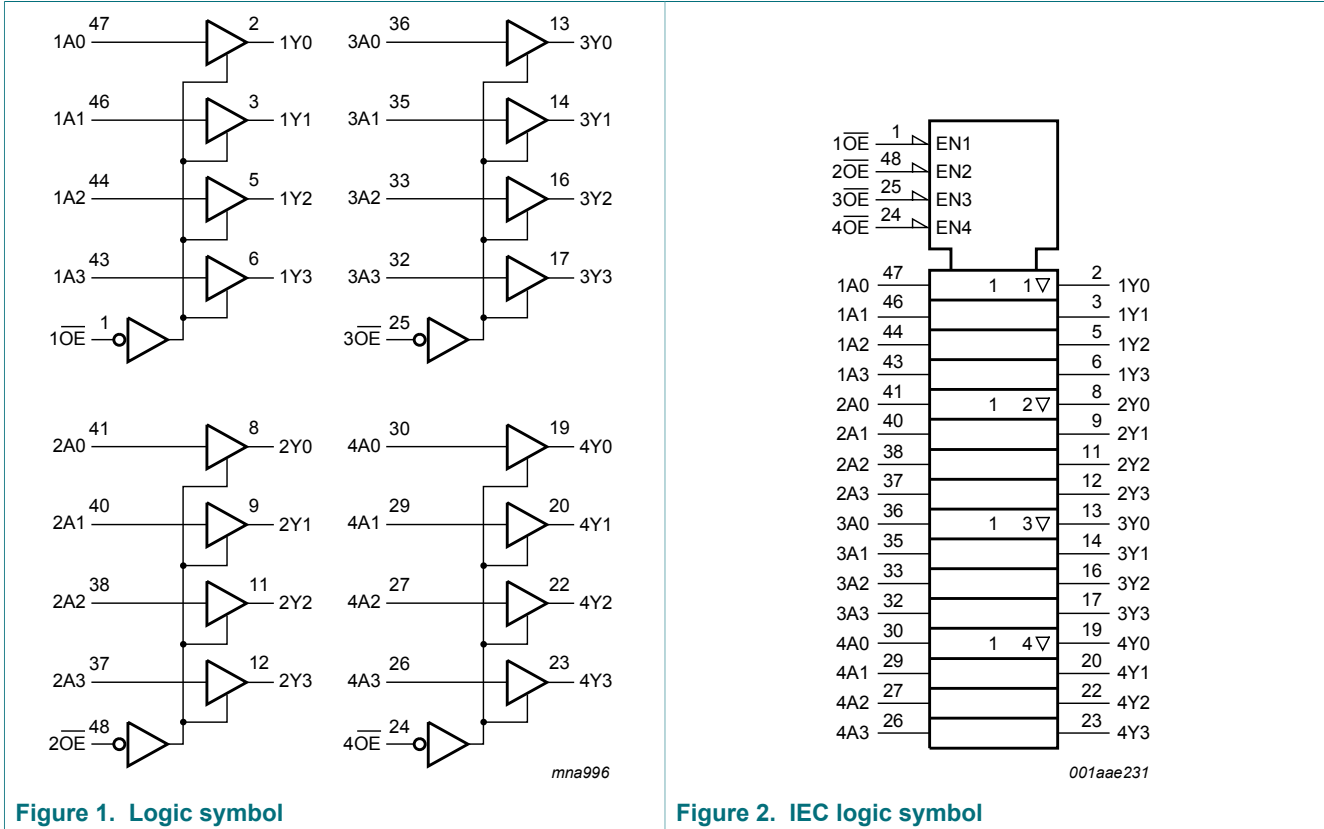
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Input/output tolerant up to 3.6 V
- Dynamic controlled output (DCO) circuit dynamically changes the output impedance, resulting in noise reduction without speed degradation
- Bus hold on all data inputs
- Supports Live Insertion
- Complies with JEDEC standards:
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-1A (2.7 V to 3.6 V)

3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AVCH16244DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4 Functional diagram



5 Pinning information

5.1 Pinning

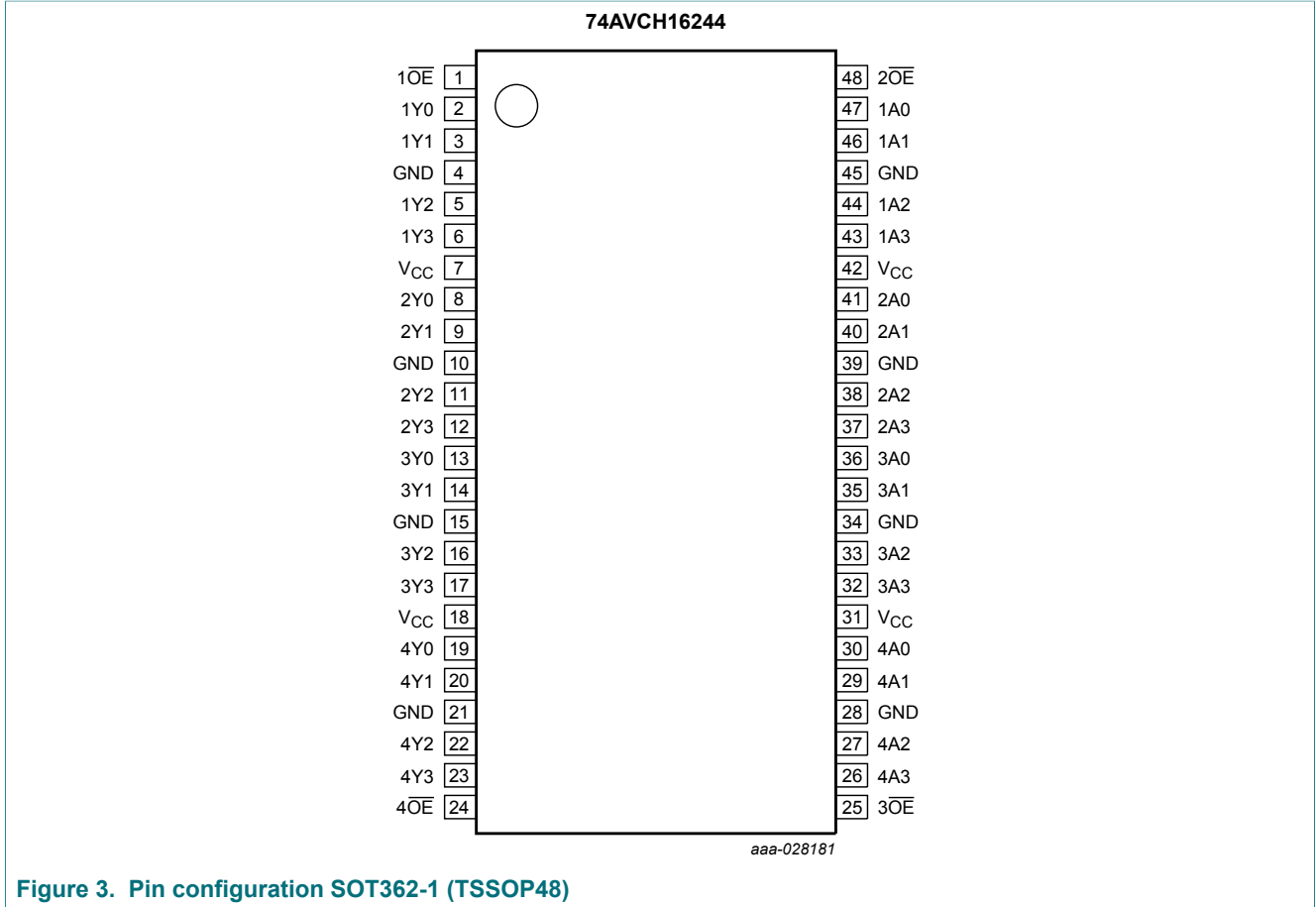


Figure 3. Pin configuration SOT362-1 (TSSOP48)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 48, 25, 24	output enable inputs (active LOW)
1A0, 1A1, 1A2, 1A3 2A0, 2A1, 2A2, 2A3 3A0, 3A1, 3A2, 3A3 4A0, 4A1, 4A2, 4A3	47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	data inputs
1Y0, 1Y1, 1Y2, 1Y3 2Y0, 2Y1, 2Y2, 2Y3 3Y0, 3Y1, 3Y2, 3Y3 4Y0, 4Y1, 4Y2, 4Y3	2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	data outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
VCC	7, 18, 31, 42	supply voltage

6 Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-	-50	mA
V_I	input voltage		[1] -0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-	-50	mA
V_O	output voltage	output HIGH or LOW	[1] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[1] -0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	+50	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for low-voltage applications	1.2	-	3.6	V
		according to JEDEC Low Voltage Standards	1.4	-	1.6	V
			1.65	-	1.95	V
			2.3	-	2.7	V
			3.0	-	3.6	V
V_I	input voltage		0	-	3.6	V
V_O	output voltage	output HIGH or LOW	0	-	V_{CC}	V
		output 3-state	0	-	3.6	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$	0	-	40	ns/V
		$V_{CC} = 1.65 \text{ V to } 2.3 \text{ V}$	0	-	30	ns/V
		$V_{CC} = 2.3 \text{ V to } 3.0 \text{ V}$	0	-	20	ns/V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0	-	10	ns/V

9 Static characteristics

Table 6. Static characteristics

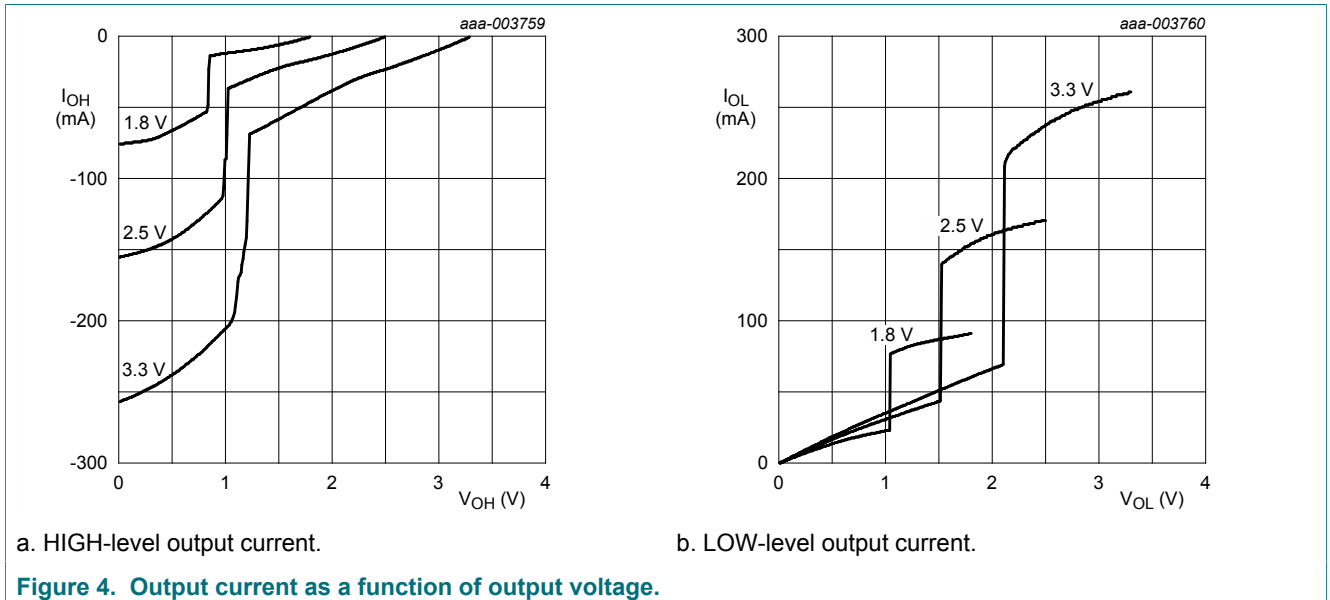
At recommended operating conditions. $T_{amb} = -40 \text{ °C to } +85 \text{ °C}$; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2 \text{ V}$	V_{CC}	-	-	V
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$	$0.65 \times V_{CC}$	0.9	-	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	0.9	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	1.2	-	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2 \text{ V}$	-	-	GND	V
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$	-	0.9	$0.35 \times V_{CC}$	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	0.9	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	1.2	0.7	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$; see Figure 4				
		$I_O = -100 \text{ }\mu\text{A}$; $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	$V_{CC} - 0.20$	V_{CC}	-	V
		$I_O = -3 \text{ mA}$; $V_{CC} = 1.4 \text{ V}$	$V_{CC} - 0.35$	$V_{CC} - 0.21$	-	V
		$I_O = -4 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$	$V_{CC} - 0.45$	$V_{CC} - 0.25$	-	V
		$I_O = -8 \text{ mA}$; $V_{CC} = 2.3 \text{ V}$	$V_{CC} - 0.55$	$V_{CC} - 0.37$	-	V
		$I_O = -12 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	$V_{CC} - 0.70$	$V_{CC} - 0.47$	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$; see Figure 4				
		$I_O = 100 \text{ }\mu\text{A}$; $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	GND	0.20	V
		$I_O = 3 \text{ mA}$; $V_{CC} = 1.4 \text{ V}$	-	0.22	0.35	V
		$I_O = 4 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$	-	0.24	0.45	V
		$I_O = 8 \text{ mA}$; $V_{CC} = 2.3 \text{ V}$	-	0.38	0.55	V
		$I_O = 12 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	-	0.53	0.70	V
I_I	input leakage current	per input pin; $V_I = V_{CC} \text{ or } \text{GND}$; $V_{CC} = 1.4 \text{ V to } 3.6 \text{ V}$	-	0.1	2.5	μA
I_{OFF}	power-off leakage current	$V_I \text{ or } V_O = 3.6 \text{ V}$; $V_{CC} = 0 \text{ V}$	-	0.1	± 10	μA
I_{BHL}	bus hold LOW current	$V_{CC} = 1.65 \text{ V}$; $V_I = 0.35 \times V_{CC}$	25	-	-	μA
		$V_{CC} = 2.3 \text{ V}$; $V_I = 0.7 \text{ V}$	45	-	-	μA
		$V_{CC} = 3.0 \text{ V}$; $V_I = 0.8 \text{ V}$	75	-	-	μA

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I _{BHH}	bus hold HIGH current	V _{CC} = 1.65 V; V _I = 0.65 × V _{CC}	-25	-	-	μA
		V _{CC} = 2.3 V; V _I = 0.65 × V _{CC}	-45	-	-	μA
		V _{CC} = 3.0 V; V _I = 0.65 × V _{CC}	-75	-	-	μA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 1.95 V	200	-	-	μA
		V _{CC} = 2.7 V	300	-	-	μA
		V _{CC} = 3.6 V	450	-	-	μA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 1.95 V	-200	-	-	μA
		V _{CC} = 2.7 V	-300	-	-	μA
		V _{CC} = 3.6 V	-450	-	-	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND				
		V _{CC} = 1.4 V to 2.7 V	-	0.1	5	μA
		V _{CC} = 3.0 V to 3.6 V	-	0.1	10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A				
		V _{CC} = 1.4 V to 2.7 V	-	0.1	20	μA
		V _{CC} = 3.0 V to 3.6 V	-	0.2	40	μA
C _I	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

9.1 Dynamic controlled output graphs



10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
t _{pd}	propagation delay	nAn to nYn; see Figure 5 ^[2]				
		V _{CC} = 1.2 V	-	5.2	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	2.9	-	ns
		V _{CC} = 1.65 V to 1.95 V	0.8	2.1	3.4	ns
		V _{CC} = 2.3 V to 2.7 V	0.7	1.5	2.2	ns
		V _{CC} = 3.0 V to 3.6 V	0.6	1.3	2.0	ns
t _{en}	enable time	n $\overline{O}E$ to nYn; see Figure 6 ^[2]				
		V _{CC} = 1.2 V	-	5.7	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	4.0	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.3	3.3	6.8	ns
		V _{CC} = 2.3 V to 2.7 V	0.9	2.2	4.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.7	1.9	3.5	ns
t _{dis}	disable time	n $\overline{O}E$ to nYn; see Figure 6 ^[2]				
		V _{CC} = 1.2 V	-	5.9	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	4.2	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.6	3.7	6.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	1.9	4.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.1	2.2	3.5	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ^[3]				
		outputs enabled	-	34	-	pF
		outputs disabled	-	1	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz

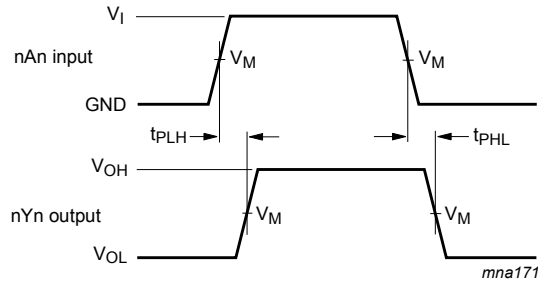
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

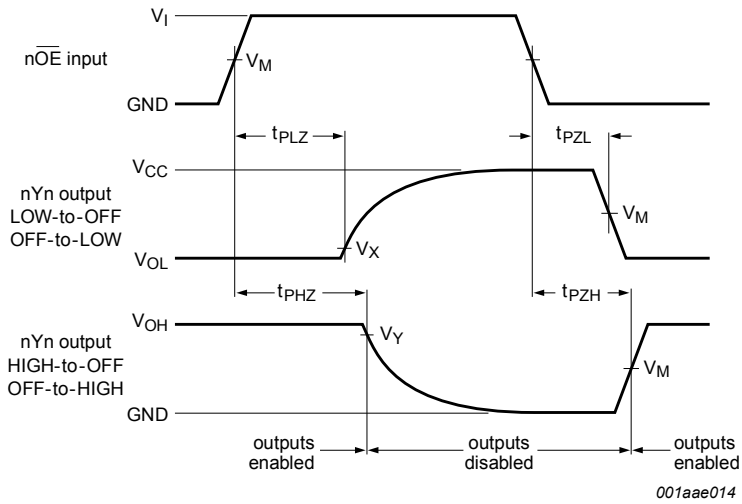
10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. Inputs nAn to output nYn propagation delays



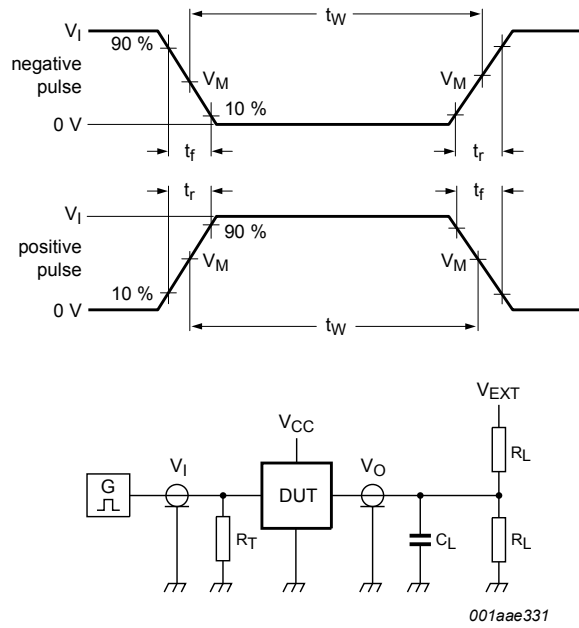
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output			
V_{CC}	V_I	V_M	V_M	V_X	V_Y
$\leq 2.3\text{ V}$	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.0 V to 3.6 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Figure 7. Test circuit for measuring switching times

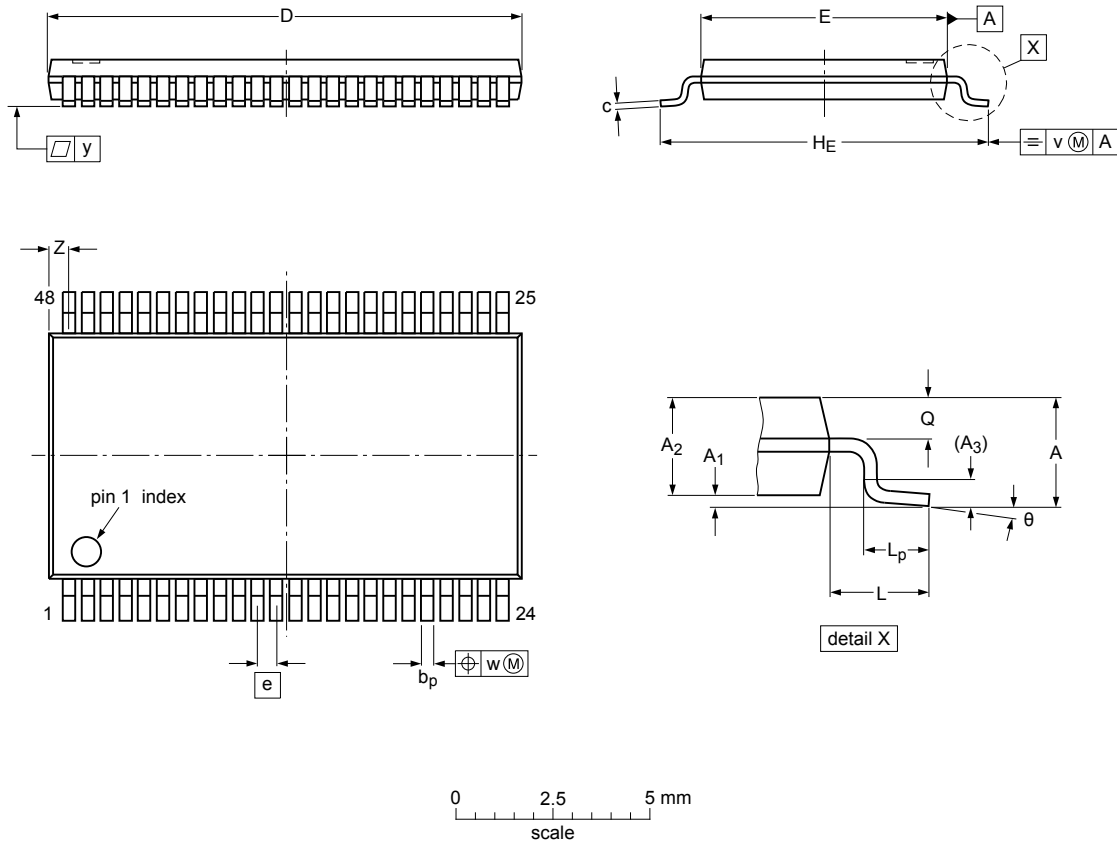
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2.0 ns	15 pF	2000 Ω	open	$2 \times V_{CC}$	GND
1.4 V to 1.6 V	V_{CC}	≤ 2.0 ns	15 pF	2000 Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1000 Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND

11 Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



Dimensions (mm are the original dimensions)

Unit	A	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ	
max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50		0.25	0.08	0.1	0.8	8°
nom	1.2			0.25					0.5		1								
min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT362-1		MO-153			03-02-19 13-08-05

Figure 8. Package outline SOT362-1 (TSSOP48)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DCO	Dynamic Controlled Output
DUT	Device Under Test

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVCH16244 v.2	20180220	Product data sheet	-	74AVCH16244 v.1
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.			
74AVCH16244 v.1	20000307	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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