THE DATASHEET OF

74FCT162511CTPVG

FAST CMOS 16-BIT REGISTERED/LATCHED TRANSCEIVER WITH PARITY

IDT54/74FCT162511AT/CT

FEATURES:

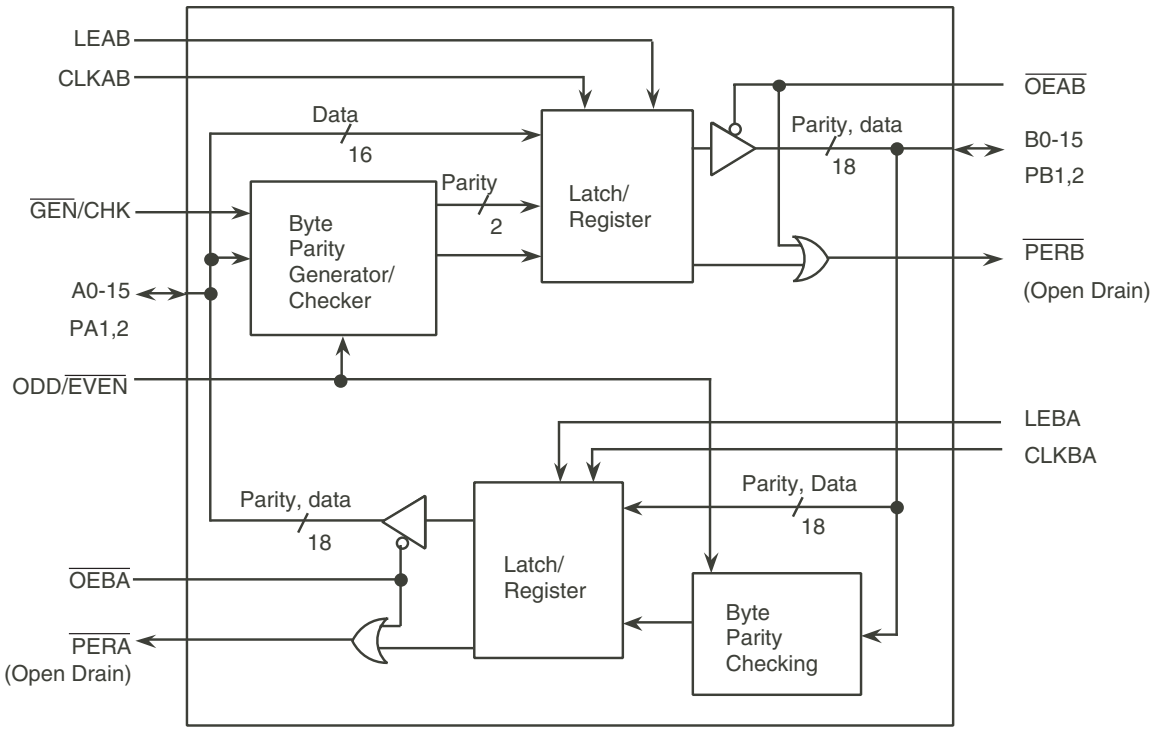
- **0.5 MICRON CMOS Technology**
- **Typical $t_{sk(o)}$ (Output Skew) < 250ps, clocked mode**
- **Low input and output leakage ≤1µA (max)**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Vcc = 5V ±10%**
- **Balanced Output Drivers:**
  - *±24mA (industrial)*
  - *±16mA (military)*
- **Series current limiting resistors**
- **Generate/Check, Check/Check modes**
- **Open drain parity error allows wire-OR**
- **Available in the following packages:**
  - *Industrial: SSOP, TSSOP*
  - *Military: CERPACK*

DESCRIPTION:

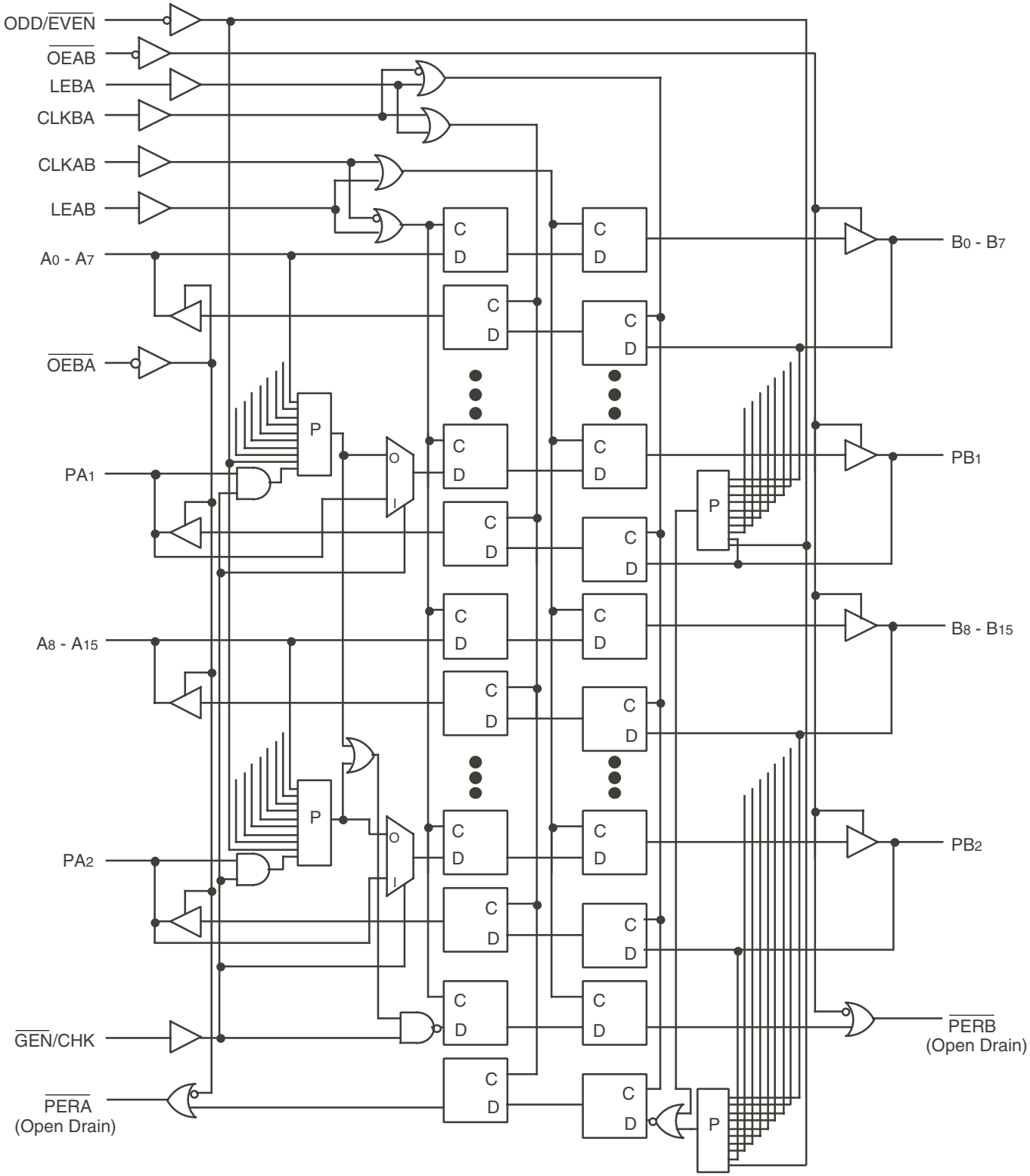
The FCT162511T 16-bit registered/latched transceiver with parity is built using advanced dual metal CMOS technology. This high-speed, low-power transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The device has a parity generator/checker in the A-to-B direction and a parity checker in the B-to-A direction. Error checking is done at the byte level with separate parity bits for each byte. Separate error flags exits for each direction with a single error flag indicating an error for either byte in the A-to-B direction and a second error flag indicating an error for either byte in the B-to-A direction. The parity error flags are open drain outputs which can be tied together and/or tied with flags from other devices to form a single error flag or interrupt. The parity error flags are enabled by the $\overline{OExx}$ control pins allowing the designer to disable the error flag during combinational transitions.

The control pins LEAB, CLKAB, and $\overline{OEAB}$ control operation in the A-to-B direction while LEBA, CLKBA, and $\overline{OEBA}$ control the B-to-A direction. $\overline{GEN}$/CHK is only for the selection of A-to-B operation. The B-to-A direction is always in checking mode. The ODD/$\overline{EVEN}$ select is common between the two directions. Except for the ODD/$\overline{EVEN}$ control, independent operation can be achieved between the two directions by using the corresponding control lines.

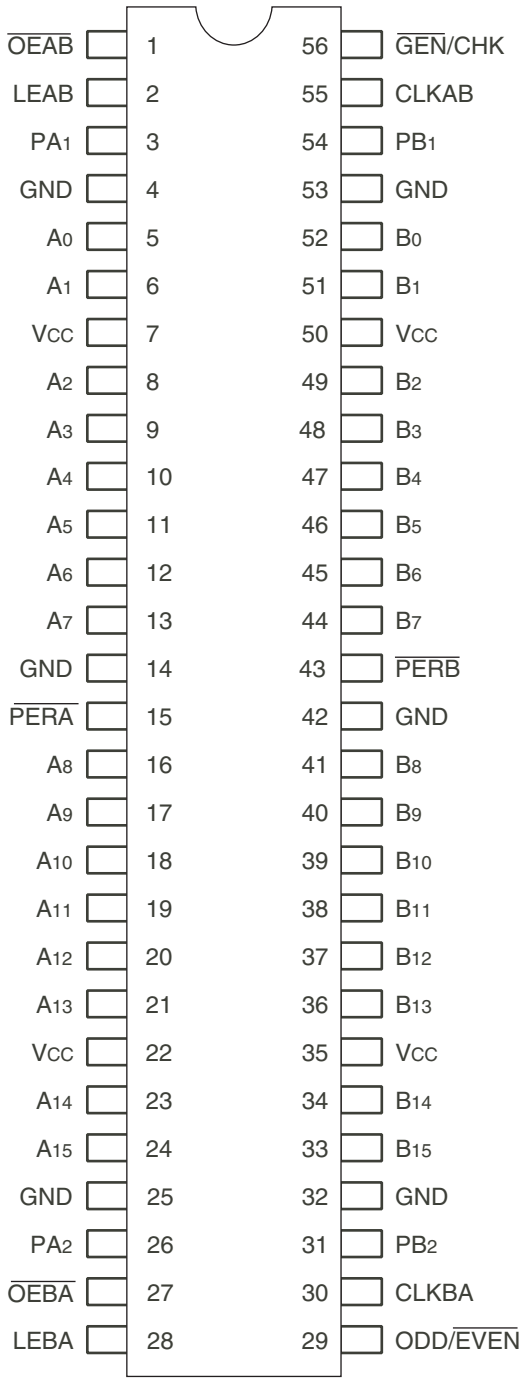
FUNCTIONAL BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ CERPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to 7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Output and I/O terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8	pF
C_O	Open Drain Capacitance	V_{OUT} = 0V	3.5	6	pF

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs
$\overline{PERA}$	Parity Error (Open Drain) on A Outputs
$\overline{PERB}$	Parity Error (Open Drain) on B Outputs
PAx(1)	A-to-B Parity Input, B-to-A Parity Output
PBx	B-to-A Parity Input, A-to-B Parity Output
ODD/$\overline{EVEN}$	Parity Mode Selection Input
$\overline{GEN}$/CHK	A to B Port Generate or Check Mode Input

NOTE:
1. The PAx pin input is internally disabled during parity generation. This means that when generating parity in the A to B direction there is no need to add a pull up resistor to guarantee state. The pin will still function properly as the parity output for the B to A direction.

FUNCTION TABLE[1, 4]

Inputs				Outputs
$\overline{OEAB}$	LEAB	CLKAB	Ax	Bx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	B[2]
L	L	H	X	B[3]

NOTES:
1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-impedance
   ↑ = LOW-to-HIGH Transition

FUNCTION TABLE (PARITY CHECKING) [1, 2, 3, 4]

$A_0 - A_7$ and P_{A1}[5] Number of inputs that are high	ODD/$\overline{EVEN}$	$\overline{PERB}$
1, 3, 5, 7 or 9	L	L
1, 3, 5, 7 or 9	H	H[6]
0, 2, 4, 6 or 8	L	H[6]
0, 2, 4, 6 or 8	H	L

NOTES:
1. Conditions shown are for $\overline{GEN}$/CHK = H, $\overline{OEAB}$ = L, $\overline{OEBA}$ = H.
2. A-to-B parity checking is shown. B-to-A parity checking is similar but uses $\overline{OEBA}$ = L, $\overline{OEAB}$ = H and errors will be indicated on $\overline{PERA}$.
3. In parity checking mode the parity bits will be transmitted unchanged along with the corresponding data regardless of parity errors (PB1 = PA1).
4. The response shown is for LEAB = H. If LEAB = L then CLKAB will control as an edge triggered clock.
5. Conditions shown are for the byte A0–A7 and PA1. The byte A8–A15 and PA2 is similiar.
6. The parity error flag $\overline{PERB}$ is a combined flag for both bytes A0–A7 and A8–A15. If a parity error occurs on either byte $\overline{PERB}$ will go low. $\overline{PERB}$ is an open drain output which must be externally pulled up to achieve a logic HIGH.

FUNCTION TABLE (PARITY GENERATION) [1, 2, 3, 4, 5]

A0 – A7 Number of inputs that are high	ODD/$\overline{EVEN}$	PB1
1, 3, 5 or 7	L	H
1, 3, 5 or 7	H	L
0, 2, 4, 6 or 8	L	L
0, 2, 4, 6 or 8	H	H

NOTES:
1. Conditions shown are for $\overline{GEN}$/CHK = L, $\overline{OEAB}$ = L, $\overline{OEBA}$ = H.
2. A-to-B parity checking is shown. B-to-A is capable of parity checking while A-to-B is performing generation. B-to-A will not generate parity.
3. The response shown is for LEAB = H. If LEAB = L then CLKAB will control as an edge triggered clock.
4. Conditions shown are for the byte A–A7. The byte A8–A15 is similiar but will output the parity on PB2.
5. The error flag $\overline{PERB}$ will remain in a high state during parity generation.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	5	500	µA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter		Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	(I/O pins)	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		60	115	200	mA
		(Open Drain)			—	250	—	mA
I_{ODH}	Output HIGH Current		V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–60	–115	–200	mA
I_{OFF}	Output Power Off Leakage Current (Open Drain)[5]		V_{CC} = 0, V_O ≤ 5.5V		—	—	±1	µA
V_{OH}	Output HIGH Voltage (I/O pins)		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL I_{OH} = –24mA IND	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	(I/O pins)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL I_{OL} = 24mA IND	—	0.3	0.55	V
		(Open Drain)		I_{OL} = 48mA MIL I_{OL} = 64mA IND	—	0.3	0.55	V

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]	All other Input Pins	—	0.5	1.5	mA
			Parity Input Pins (PAx, PBx)	—	1	2.5	
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OEAB}$ = GND, $\overline{OEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle $\overline{OEAB}$ = GND, $\overline{OEBA}$ = V_{CC}	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
		LEAB = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = GND, $\overline{OEBA}$ = V_{CC}	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
		LEAB = GND Eighteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	9	21.8[5]	

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (PROPAGATION DELAYS)

Symbol	Parameter	Condition[1]	FCT162511AT				FCT162511CT				Unit
			Ind.		Mil.		Ind.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay, PAx to PBx Ax to Bx or Bx to Ax, PBx to PAx	C_L = 50pF R_L = 500Ω	1.5	5	1.5	5.3	1.5	4.2	1.5	4.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{GEN}$/CHK LOW Ax to PBx		1.5	7.5	1.5	8	1.5	6.5	1.5	6.8	ns
t_{PLH}[3]	Propagation Delay		1.5	9	1.5	9	1.5	7.5	1.5	7.8	ns
t_{PHL}	Ax to PERB, PAx to $\overline{PERB}$		1.5	8	1.5	8	1.5	6.5	1.5	6.8	ns
t_{PLH}[3]	Propagation Delay		1.5	9	1.5	9	1.5	7.5	1.5	7.8	ns
t_{PHL}	Bx to PERA, PBx to $\overline{PERA}$		1.5	8	1.5	8	1.5	6.5	1.5	6.8	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to Ax and PAx LEAB to Bx and PBx		1.5	5.6	1.5	6	1.5	5.3	1.5	5.5	ns
t_{PLH}[3]	Propagation Delay		1.5	7	1.5	7	1.5	6	1.5	6.3	ns
t_{PHL}	LEBA to $\overline{PERA}$, LEAB to $\overline{PERB}$		1.5	6	1.5	6	1.5	5	1.5	5.3	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to Ax and PAx CLKAB to Bx and PBx		1.5	5.6	1.5	6	1.5	5.3	1.5	5.5	ns
t_{PLH}[3]	Propagation Delay		1.5	7	1.5	7	1.5	6	1.5	6.3	ns
t_{PHL}	CLKBA to $\overline{PERA}$ CLKAB to $\overline{PERB}$		1.5	6	1.5	6	1.5	5	1.5	5.3	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to Ax and PAx $\overline{OEAB}$ to Bx and PBx		1.5	6	1.5	6.5	1.5	5.6	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to Ax and PAx $\overline{OEAB}$ to Bx and PBx		1.5	5.6	1.5	6	1.5	5.2	1.5	5.5	ns
t_{PLZ}[3]	Parity ERROR Enable		1.5	6	1.5	6.3	1.5	6	1.5	6.3	ns
t_{PZL}	$\overline{OEBA}$ to $\overline{PERA}$, $\overline{OEAB}$ to $\overline{PERB}$		1.5	6	1.5	6.3	1.5	6	1.5	6.3	ns
t_{PLH}[3]	ODD/$\overline{EVEN}$ to $\overline{PERx}$		1.5	10	1.5	10	1.5	10	1.5	10	ns
t_{PHL}			1.5	10	1.5	10	1.5	10	1.5	10	ns
t_{PLH} t_{PHL}	ODD/$\overline{EVEN}$ to PBx		1.5	10	1.5	10	1.5	10	1.5	10	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. On Open Drain Outputs t_{PLH} is measured at $V_{OUT} = V_{OL} + 0.3V$.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (SET UP TIMES)

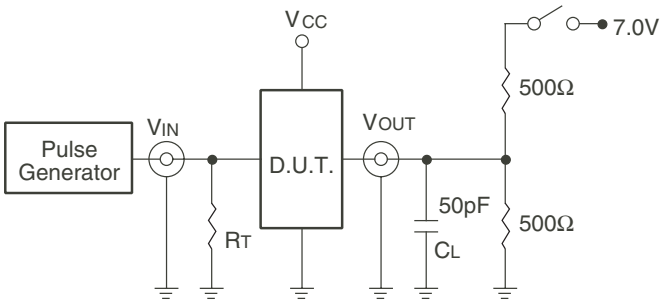
Symbol	Parameter	Test Conditions[1, 3]			FCT162511AT Ind. Min.	FCT162511AT Ind. Max.	FCT162511AT Mil. Min.	FCT162511AT Mil. Max.	FCT162511CT Ind. Min.	FCT162511CT Ind. Max.	FCT162511CT Mil. Min.	FCT162511CT Mil. Max.	Unit
t_{SU}	Set-up Time HIGH or LOW Ax to CLKAB	$\overline{GEN}$/CHK LOW	PBx valid	C_L = 50pF	4	—	4	—	3	—	3.5	—	ns
			PBx not valid	R_L = 500Ω	3	—	3	—	3	—	3	—	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid		4	—	4	—	3	—	3	—	ns
			$\overline{PERB}$ not valid		3	—	3	—	3	—	3	—	ns
t_{SU}	Set-up Time PAx to CLKAB	$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid		4	—	4	—	3	—	3	—	ns
			$\overline{PERB}$ not valid		3	—	3	—	3	—	3	—	ns
t_{SU}	Set-up Time Bx to CLKBA, PBx to CLKBA		$\overline{PERA}$ valid		4	—	4	—	3	—	3	—	ns
			$\overline{PERA}$ not valid		3	—	4	—	3	—	3	—	ns
t_{SU}	Set-up Time Ax to LEAB	CLKAB LOW	PBx valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{GEN}$/CHK LOW	PBx not valid		3	—	3	—	3	—	3	—	ns
		CLKAB LOW	$\overline{PERB}$ valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ not valid		3	—	3	—	3	—	3	—	ns
		CLKAB HIGH	PBx valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{GEN}$/CHK LOW	PBx not valid		3	—	3	—	3	—	3	—	ns
		CLKAB HIGH	$\overline{PERB}$ valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ not valid		3	—	3	—	3	—	3	—	ns
t_{SU}	Set-up Time PAx to LEAB	CLKAB LOW	$\overline{PERB}$ valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ not valid		3	—	3	—	3	—	3	—	ns
		CLKAB HIGH	$\overline{PERB}$ valid		3.5	—	3.5	—	3	—	3	—	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ not valid		3	—	3	—	3	—	3	—	ns
t_{SU}	Set-up Time Bx to LEBA PBx to LEBA	CLKBA LOW	$\overline{PERA}$ valid		3.5	—	3.5	—	3	—	3	—	ns
			$\overline{PERA}$ not valid		3	—	3	—	3	—	3	—	ns
		CLKBA HIGH	$\overline{PERA}$ valid		3.5	—	3.5	—	3	—	3	—	ns
			$\overline{PERA}$ not valid		3	—	3	—	3	—	3	—	ns
$t_{SK(O)}$	Output Skew[4]				—	0.5	—	0.5	—	0.5	—	0.5	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (HOLD TIMES)

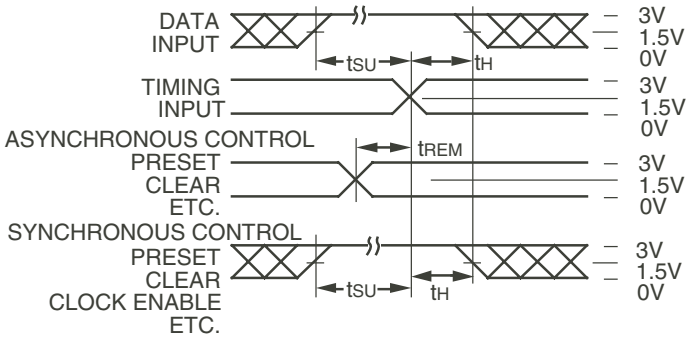
Symbol	Parameter	Condition[1]	FCT162511AT Ind. Min.	FCT162511AT Ind. Max.	FCT162511AT Mil. Min.	FCT162511AT Mil. Max.	FCT162511CT Ind. Min.	FCT162511CT Ind. Max.	FCT162511CT Mil. Min.	FCT162511CT Mil. Max.	Unit
t_H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	C_L= 50pF	1	—	1	—	1	—	1	—	ns
t_H	Hold Time HIGH or LOW PAx to LEAB	R_L = 500Ω	1	—	1	—	1	—	1	—	ns
t_H	Hold Time HIGH or LOW PBx to LEBA		1	—	1	—	1	—	1	—	ns
t_H	Hold Time Ax to CLKAB, PAx to CLKAB		1	—	1	—	0	—	0	—	ns
t_H	Hold Time Bx to CLKBA, PBx to CLKBA		1	—	1	—	0	—	0	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[2]		3	—	3	—	3	—	3	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[2]		3	—	3	—	3	—	3	—	ns

NOTES:
1. See test circuits and waveforms.
2. This parameter is guaranteed but not tested.
3. "Not valid" means the set-up time indicated is not sufficient to assure proper functioning of this output; however, the set-up time indicated will assure proper functioning of the A to B or B to A port respective to the indicated direction.
4. Skew between any two outputs of the same package, switching in the same direction, excluding $\overline{PERx}$ in clocked mode, and Pxx (parity bits) and $\overline{PERx}$ in transparent/ latched mode. This parameter is guaranteed by design.

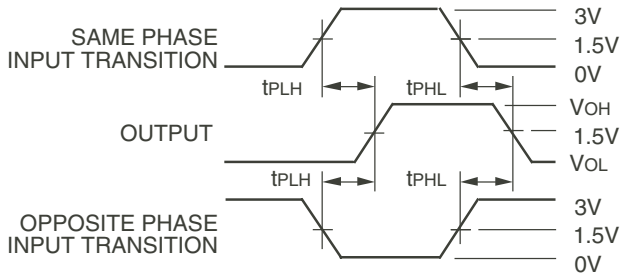
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

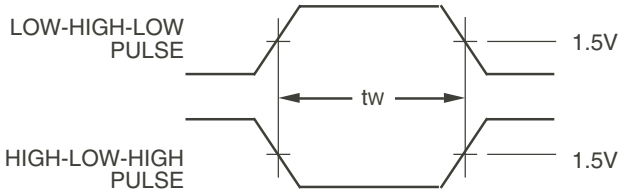
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

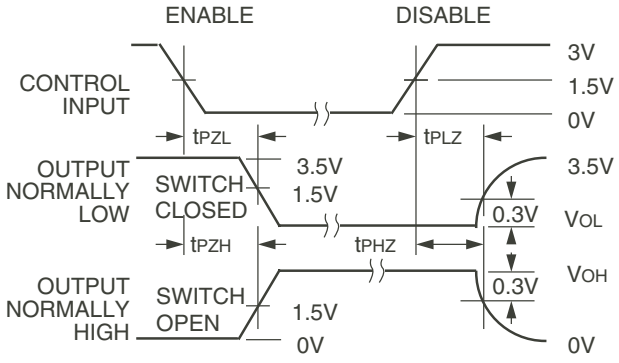
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

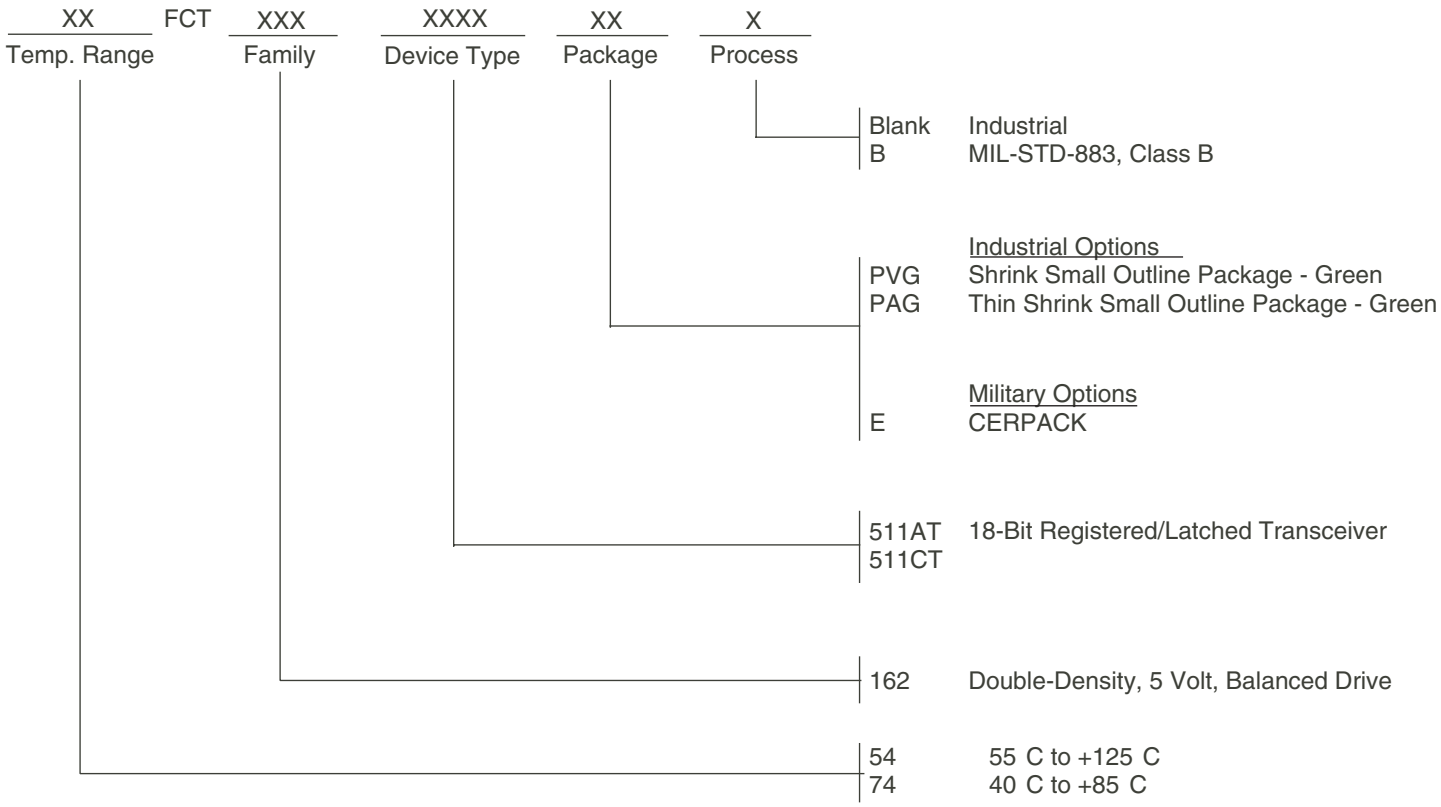


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



Datasheet Document History

09/06/09 Pg.6 Updated the ordering information by removing the "IDT" notation and non RoHS part.

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