



**THE DATASHEET OF
74HC1G04GW/AU125**



74HC1G04; 74HCT1G04

Inverter

Rev. 7 — 17 November 2023

Product data sheet

1. General description

The 74HC1G04; 74HCT1G04 is a single inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - For 74HC1G04: CMOS level
 - For 74HCT1G04: TTL level
- Symmetrical output impedance
- High noise immunity
- CMOS low power dissipation
- Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC1G04GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74HCT1G04GW				
74HC1G04GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74HCT1G04GV				

4. Marking

Table 2. Marking codes

Type number	Marking ^[1]
74HC1G04GW	HC
74HCT1G04GW	TC
74HC1G04GV	H04
74HCT1G04GV	T04

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

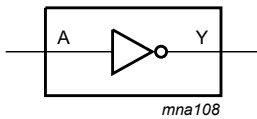


Fig. 1. Logic symbol

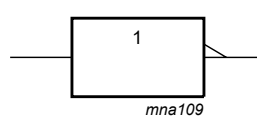


Fig. 2. IEC logic symbol

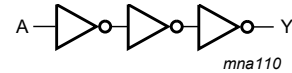


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning

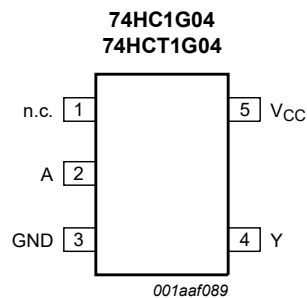


Fig. 4. Pin configuration for SOT353-1 (TSSOP5) and SOT753 (SC-74A)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
A	Y
L	H
H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ [1]	-	± 12.5	mA
I_{CC}	supply current	[1]	-	25	mA
I_{GND}	ground current		-25	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC1G04			74HCT1G04			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	-	139	-	-	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC1G04								
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I _O = -2.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I _O = 2.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	1.0	-	1.0	μA
		V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	10	-	20	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	10	-	20	μA
C _I	input capacitance		-	1.5	-	-	-	pF
74HCT1G04								
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -2.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 2.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	1.0	-	1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	10	-	20	μA
ΔI _{CC}	additional supply current	per input; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A	-	-	500	-	850	μA
C _I	input capacitance		-	1.5	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f \leq 6.0\text{ ns}$; All typical values are measured at $T_{amb} = 25\text{ }^\circ\text{C}$. For test circuit, see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC1G04								
t_{pd}	propagation delay	A to Y; see Fig. 5 [1]						
		$V_{CC} = 2.0\text{ V}$; $C_L = 50\text{ pF}$	-	25	105	-	135	ns
		$V_{CC} = 4.5\text{ V}$; $C_L = 50\text{ pF}$	-	9	21	-	27	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	7	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$; $C_L = 50\text{ pF}$	-	8	18	-	23	ns
C_{PD}	power dissipation capacitance	$V_I = GND\text{ to }V_{CC}$ [2]	-	16	-	-	-	pF
74HCT1G04								
t_{pd}	propagation delay	A to Y; see Fig. 5 [1]						
		$V_{CC} = 4.5\text{ V}$; $C_L = 50\text{ pF}$	-	10	24	-	27	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	8	-	-	-	ns
C_{PD}	power dissipation capacitance	$V_I = GND\text{ to }V_{CC} - 1.5\text{ V}$ [2]	-	18	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

11.1. Waveforms and test circuit

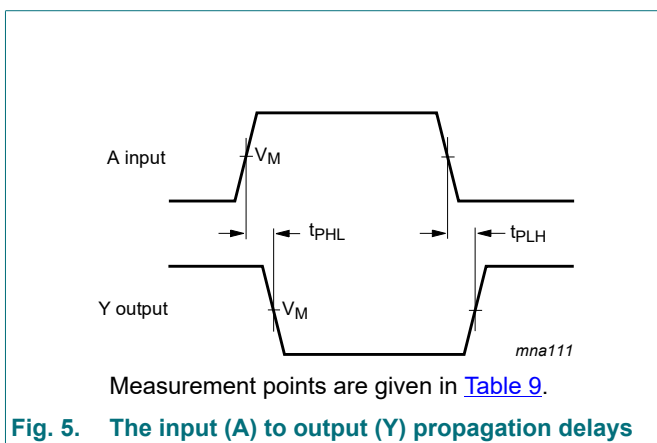


Fig. 5. The input (A) to output (Y) propagation delays

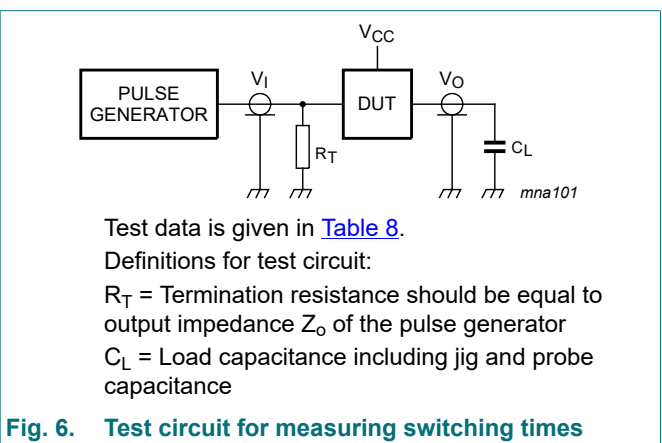


Fig. 6. Test circuit for measuring switching times

Table 9. Measurement points

Type	V_I	V_M
74HC1G04	GND to V_{CC}	$0.5 \times V_{CC}$
74HCT1G04	GND to 3.0 V	1.3 V

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

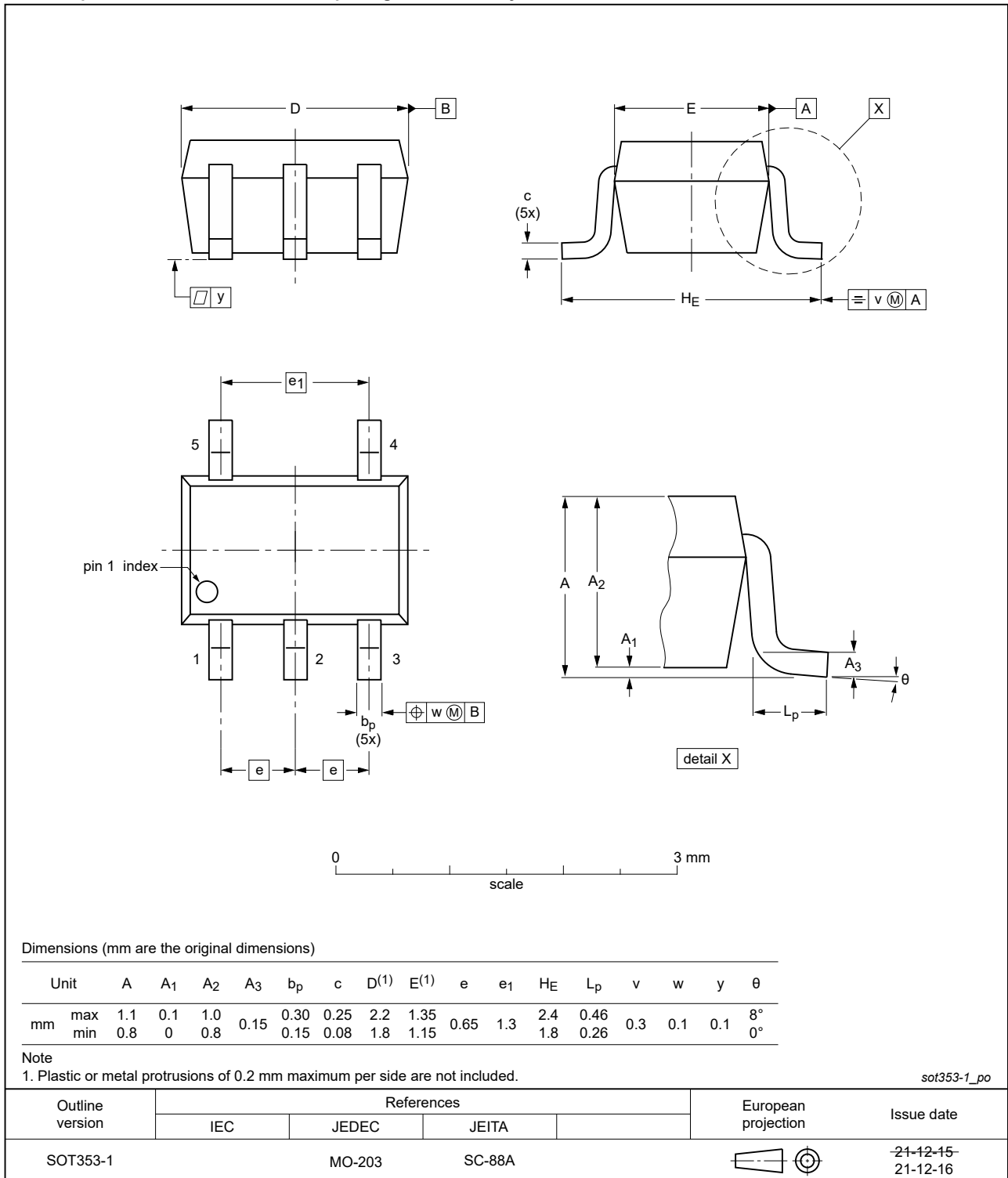


Fig. 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

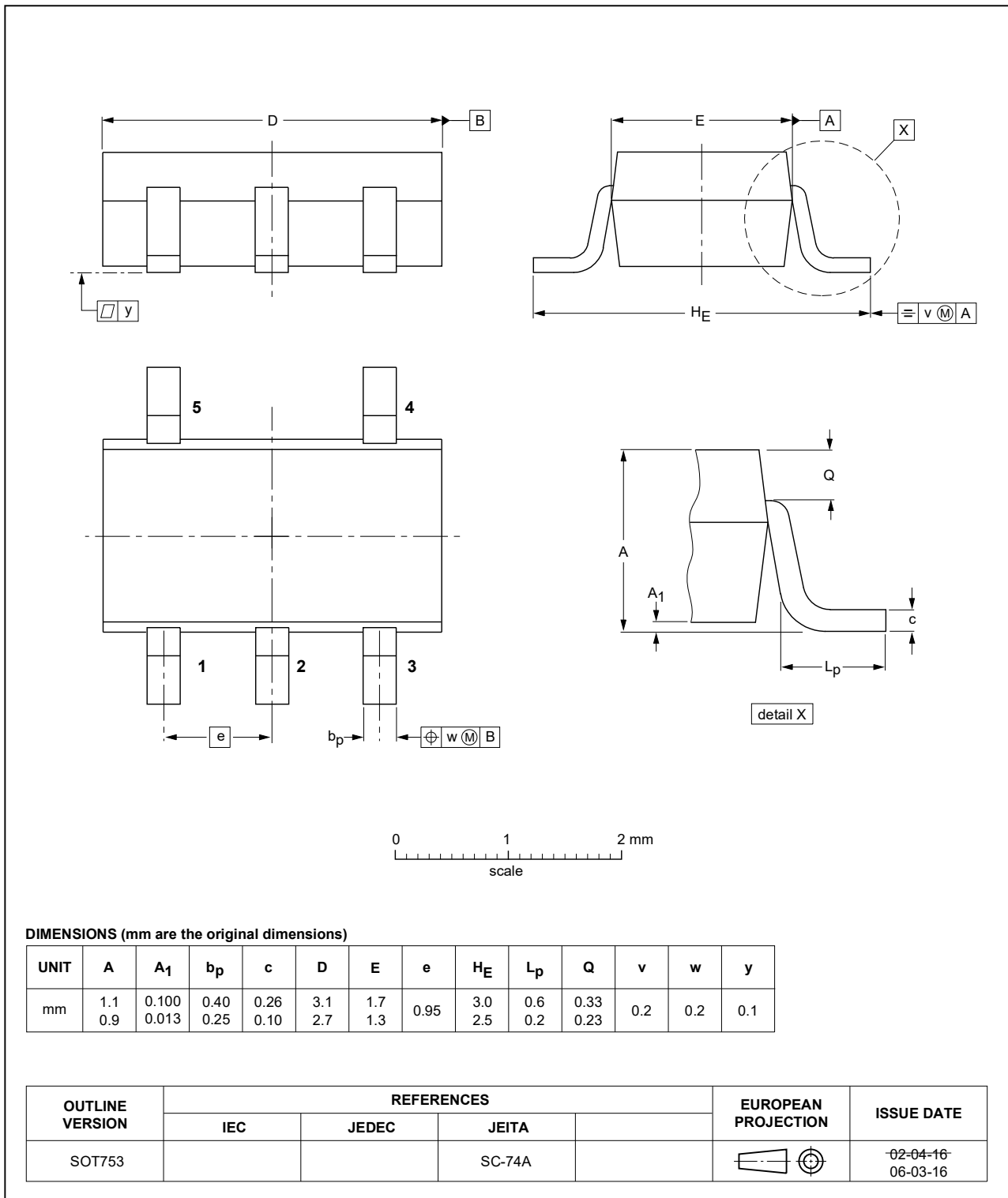


Fig. 8. Package outline SOT753 (SC-74A)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT1G04 v.7	20231117	Product data sheet	-	74HC_HCT1G04 v.6
Modifications:	<ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74HC_HCT1G04 v.6	20220121	Product data sheet	-	74HC_HCT1G04 v.5
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Table 5: Derating values for P_{tot} total power dissipation updated. • Fig. 7: Package outline drawing SOT353-1 (TSSOP5) has changed. 			
74HC_HCT1G04 v.5	20130925	Product data sheet	-	74HC_HCT1G04 v.4
Modifications:	<ul style="list-style-type: none"> • Section 1 updated. 			
74HC_HCT1G04 v.4	20070716	Product data sheet	-	74HC_HCT1G04 v.3
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Package SOT353 changed to SOT353-1 in Table 1 and Fig. 7. • Quick Reference Data and Soldering sections removed. • Section 2 updated. 			
74HC_HCT1G04 v.3	20020517	Product specification	-	74HC_HCT1G04 v.2
74HC_HCT1G04 v.2	20010302	Product specification	-	74HC_HCT1G04 v.1
74HC_HCT1G04 v.1	19980831	Preliminary specification	-	-

15. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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