



**THE DATASHEET OF
74LV4094DB,118**





74LV4094

8-stage shift-and-store bus register

Rev. 9 — 28 May 2024

Product data sheet

1. General description

The 74LV4094 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (D) and two serial outputs (QS1 and QS2) to enable cascading. Data is shifted on the LOW-to-HIGH transitions of the CP input. Data is available at QS1 on the LOW-to-HIGH transitions of the CP input to allow cascading when clock edges are fast. The same data is available at QS2 on the next HIGH-to-LOW transition of the CP input to allow cascading when clock edges are slow. The data in the shift register is transferred to the storage register when the STR input is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) is HIGH. A LOW on OE causes the outputs to assume a high-impedance OFF-state. Operation of the OE input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess V_{CC} .

2. Features and benefits

- Optimized for low voltage applications over a wide supply voltage range from 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical output ground bounce < 0.8 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- CMOS low power dissipation
- Direct interface with TTL levels
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Applications

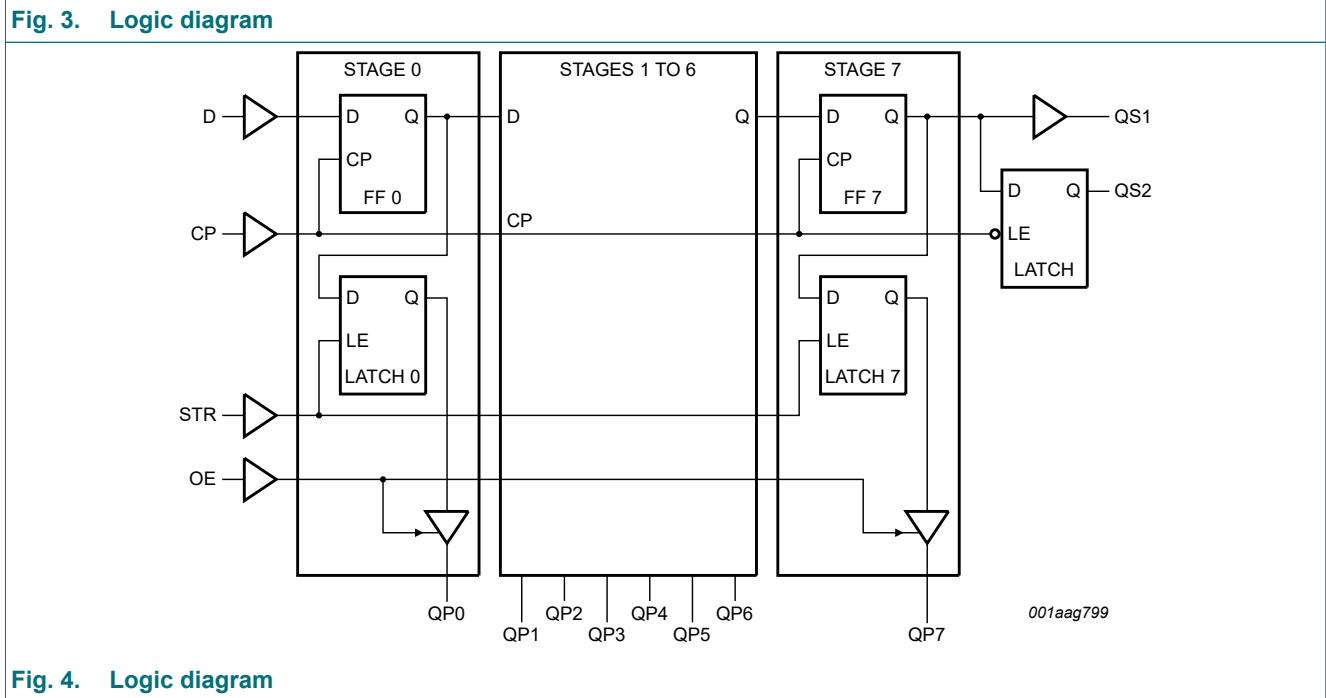
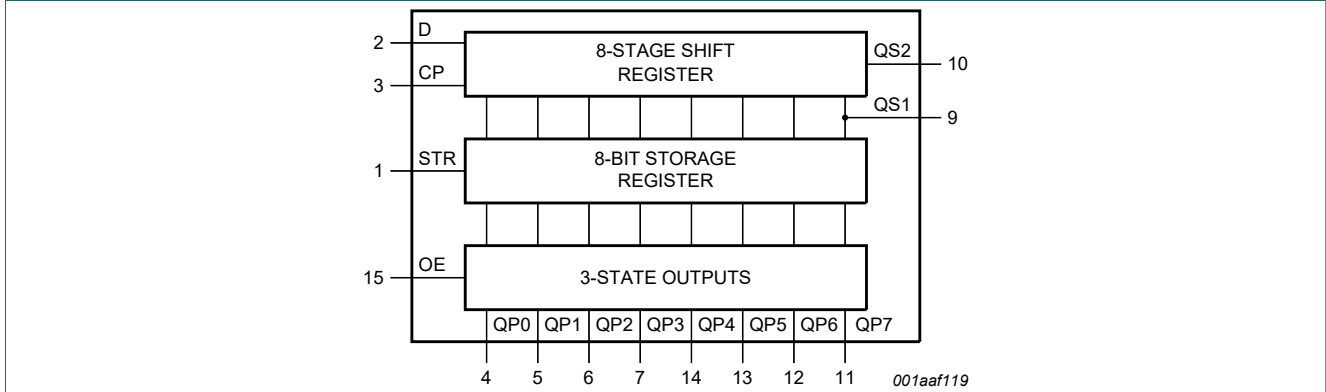
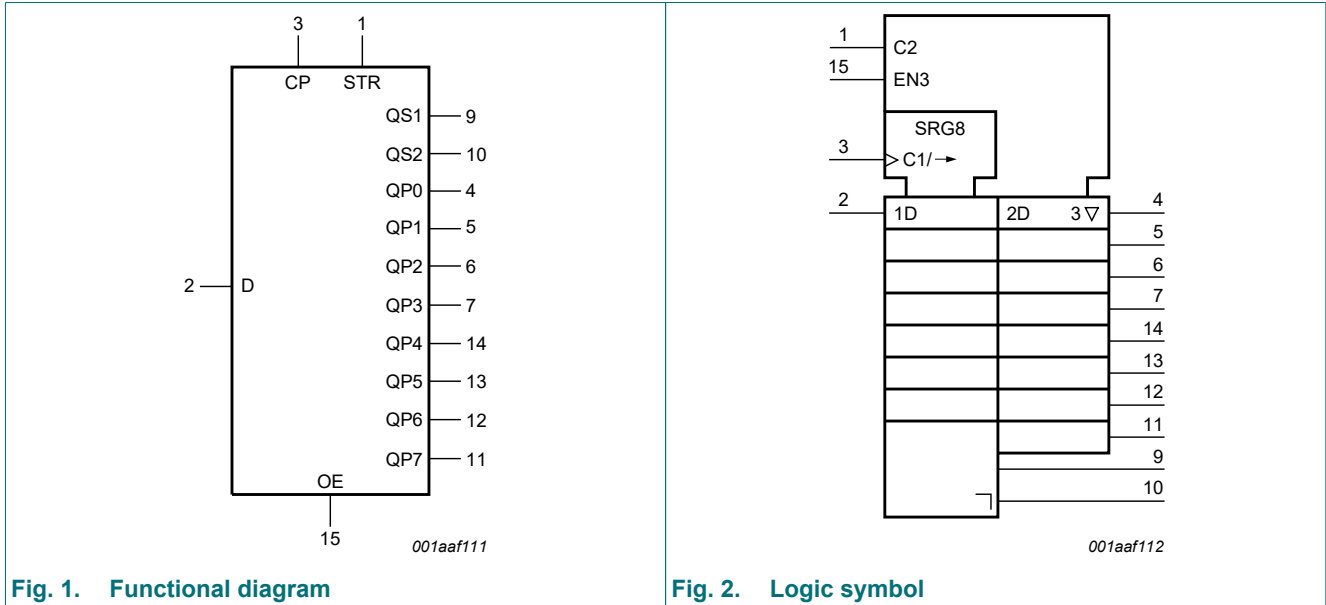
- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

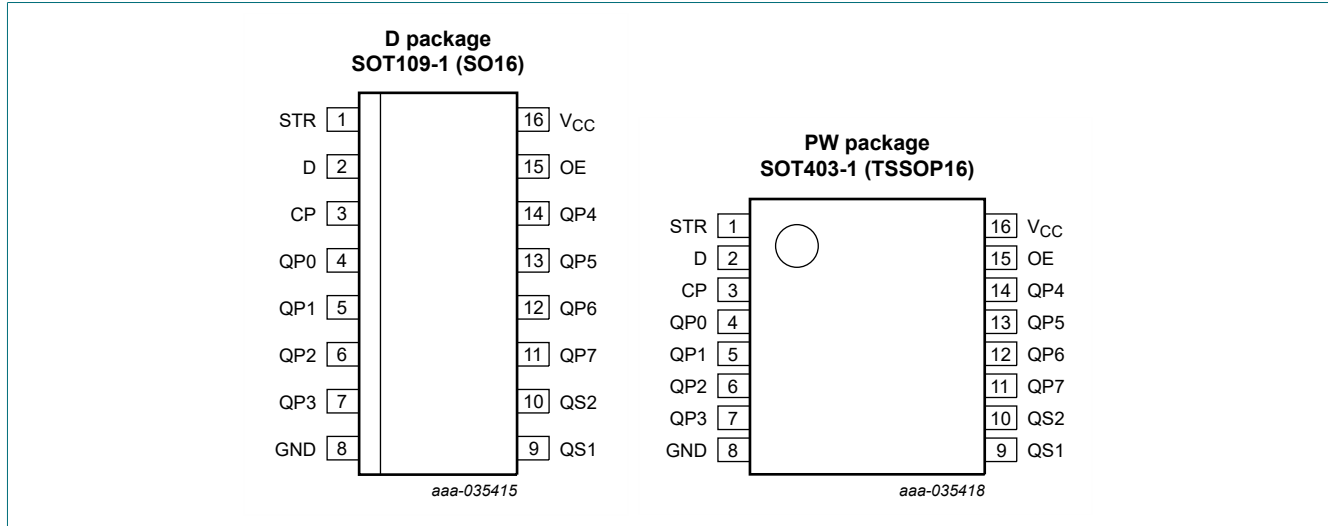
Type number	Package			Version
	Temperature range	Name	Description	
74LV4094D	-40 °C to $+125$ °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4094PW	-40 °C to $+125$ °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
STR	1	strobe input
D	2	data input
CP	3	clock input
QP0 to QP7	4, 5, 6, 7, 14, 13, 12, 11	parallel output
GND	8	ground supply voltage
QS1, QS2	9, 10	serial output
OE	15	output enable input
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = HIGH-impedance OFF-state; NC = no change;
 ↑ = positive-going transition; ↓ = negative-going transition;
 Q6S = the data in register stage 6 before the LOW to HIGH clock transition;
 Q7S = the data in register stage 7 before the HIGH to LOW clock transition.

Inputs				Parallel outputs		Serial outputs	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q6S	NC
↓	L	X	X	Z	Z	NC	Q7S
↑	H	L	X	NC	NC	Q6S	NC
↑	H	H	L	L	QPn - 1	Q6S	NC
↑	H	H	H	H	QPn - 1	Q6S	NC
↓	H	H	H	NC	NC	NC	Q7S

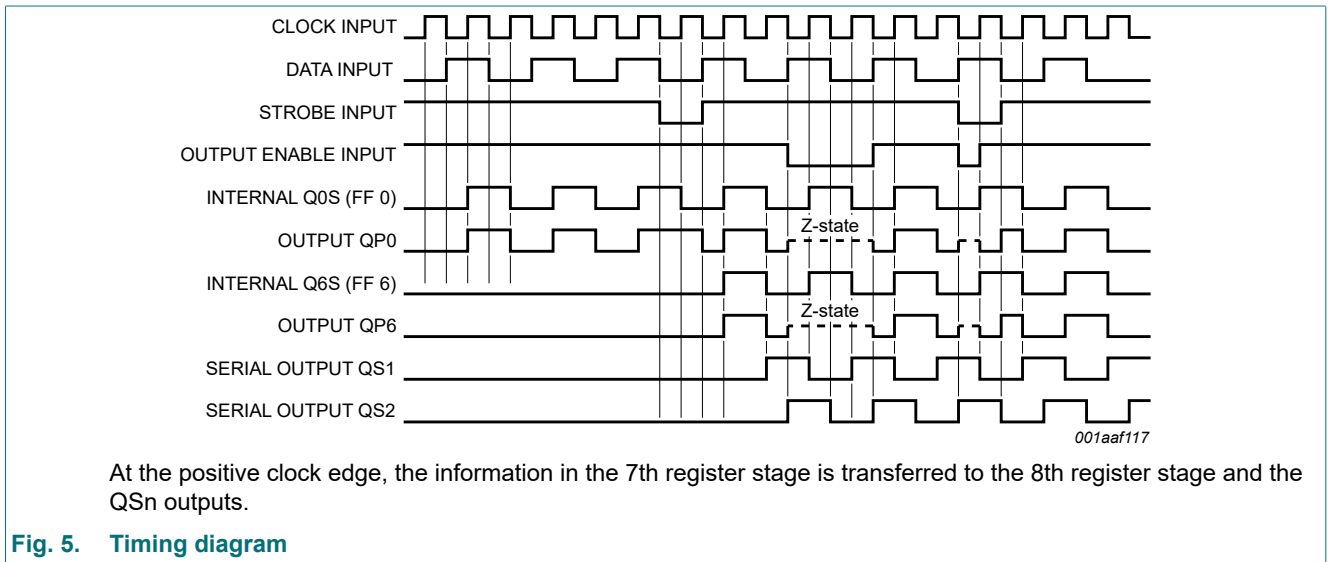


Fig. 5. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 50	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	± 25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [1]	-	500	mW

- [1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	1.0	3.3	3.6	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V}$ to 2.0 V	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V}$ to 2.7 V	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	-	-	100	ns/V

- [1] The static characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 5.5\text{ V}$, but LV devices are guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (with input levels GND or V_{CC}).

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to 85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	V _{CC}	0.6	-	V _{CC}	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	0.4	GND	-	GND	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; all pins						
		I _O = -100 μA; V _{CC} = 1.2 V	-	1.2	-	-	-	V
		I _O = -100 μA; V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I _O = -100 μA; V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I _O = -100 μA; V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		V _I = V _{IH} or V _{IL} ; pins QPn						
V _{OL}	LOW-level output voltage	I _O = -6 mA; V _{CC} = 3.0 V	2.40	2.82	-	2.20	-	V
		V _I = V _{IH} or V _{IL} ; all pins						
		I _O = 100 μA; V _{CC} = 1.2 V	-	0	-	-	-	V
		I _O = 100 μA; V _{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 3.0 V	-	0	0.2	-	0.2	V
		V _I = V _{IH} or V _{IL} ; pins QPn						
I _O = 6 mA; V _{CC} = 3.0 V	-	0.25	0.40	-	0.50	V		
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 3.6 V	-	-	±1.0	-	±1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 3.6 V	-	-	±5.0	-	±10.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 3.6 V	-	-	20.0	-	160	μA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} - 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500.0	-	850	μA
C _I	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40 °C to 85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to QS1; see Fig. 6 [2]						
		$V_{CC} = 1.2$ V	-	90	-	-	-	ns
		$V_{CC} = 2.0$ V	-	31	58	-	70	ns
		$V_{CC} = 2.7$ V	-	23	43	-	51	ns
		$V_{CC} = 3.0$ V to 3.6 V [3]	-	17	34	-	41	ns
		$V_{CC} = 3.3$ V; $C_L = 15$ pF	-	14	-	-	-	ns
		CP to QS2; see Fig. 6 [2]						
		$V_{CC} = 1.2$ V	-	80	-	-	-	ns
		$V_{CC} = 2.0$ V	-	27	51	-	61	ns
		$V_{CC} = 2.7$ V	-	20	38	-	45	ns
		$V_{CC} = 3.0$ V to 3.6 V	-	14	30	-	36	ns
		$V_{CC} = 3.3$ V; $C_L = 15$ pF [3]	-	13	-	-	-	ns
		CP to QPn; see Fig. 6 [2]						
		$V_{CC} = 1.2$ V	-	115	-	-	-	ns
		$V_{CC} = 2.0$ V	-	39	75	-	90	ns
		$V_{CC} = 2.7$ V	-	29	55	-	66	ns
		$V_{CC} = 3.0$ V to 3.6 V [3]	-	22	44	-	53	ns
		$V_{CC} = 3.3$ V; $C_L = 15$ pF	-	18	-	-	-	ns
		STR to QPn; see Fig. 7 [2]						
		$V_{CC} = 1.2$ V	-	105	-	-	-	ns
$V_{CC} = 2.0$ V	-	36	68	-	82	ns		
$V_{CC} = 2.7$ V	-	26	50	-	60	ns		
$V_{CC} = 3.0$ V to 3.6 V [3]	-	20	40	-	48	ns		
$V_{CC} = 3.3$ V; $C_L = 15$ pF	-	17	-	-	-	ns		
t_{en}	enable time	OE to QPn; see Fig. 8 [2]						
		$V_{CC} = 1.2$ V	-	100	-	-	-	ns
		$V_{CC} = 2.0$ V	-	34	65	-	77	ns
		$V_{CC} = 2.7$ V	-	25	48	-	56	ns
		$V_{CC} = 3.0$ V to 3.6 V [3]	-	19	38	-	45	ns
t_{dis}	disable time	OE to QPn; see Fig. 8 [2]						
		$V_{CC} = 1.2$ V	-	65	-	-	-	ns
		$V_{CC} = 2.0$ V	-	24	40	-	49	ns
		$V_{CC} = 2.7$ V	-	18	32	-	37	ns
		$V_{CC} = 3.0$ V to 3.6 V [3]	-	14	26	-	30	ns

8-stage shift-and-store bus register

Symbol	Parameter	Conditions	-40 °C to 85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _w	pulse width	CP HIGH or LOW; see Fig. 6						
		V _{CC} = 2.0 V	34	9	-	41	-	ns
		V _{CC} = 2.7 V	25	6	-	30	-	ns
		V _{CC} = 3.0 V to 3.6 V [3]	20	5	-	24	-	ns
		STR HIGH; see Fig. 7						
		V _{CC} = 2.0 V	34	9	-	41	-	ns
		V _{CC} = 2.7 V	25	6	-	30	-	ns
V _{CC} = 3.0 V to 3.6 V [3]	20	5	-	24	-	ns		
t _{su}	set-up time	D to CP; see Fig. 9						
		V _{CC} = 1.2 V	-	25	-	-	-	ns
		V _{CC} = 2.0 V	22	9	-	26	-	ns
		V _{CC} = 2.7 V	16	6	-	19	-	ns
		V _{CC} = 3.0 V to 3.6 V [3]	13	5	-	15	-	ns
		CP to STR; see Fig. 7						
		V _{CC} = 1.2 V	-	50	-	-	-	ns
		V _{CC} = 2.0 V	43	17	-	51	-	ns
		V _{CC} = 2.7 V	31	13	-	38	-	ns
V _{CC} = 3.0 V to 3.6 V [3]	25	10	-	30	-	ns		
t _h	hold time	D to CP; see Fig. 9						
		V _{CC} = 1.2 V	-	-10	-	-	-	ns
		V _{CC} = 2.0 V	5	-4	-	+5	-	ns
		V _{CC} = 2.7 V	5	-3	-	+5	-	ns
		V _{CC} = 3.0 V to 3.6 V [3]	5	-2	-	+5	-	ns
		CP to STR; see Fig. 7						
		V _{CC} = 1.2 V	-	-25	-	-	-	ns
		V _{CC} = 2.0 V	5	-9	-	+5	-	ns
		V _{CC} = 2.7 V	5	-6	-	+5	-	ns
V _{CC} = 3.0 V to 3.6 V [3]	5	-5	-	+5	-	ns		
f _{max}	maximum frequency	CP; see Fig. 6						
		V _{CC} = 2.0 V	14	52	-	12	-	MHz
		V _{CC} = 2.7 V	19	70	-	16	-	MHz
		V _{CC} = 3.0 V to 3.6 V [3]	24	87	-	20	-	MHz
		V _{CC} = 3.3 V; C _L = 15 pF	-	95	-	-	-	MHz
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [4]	-	83	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZH} and t_{PZL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] All typical values are measured at V_{CC} = 3.3 V.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz;

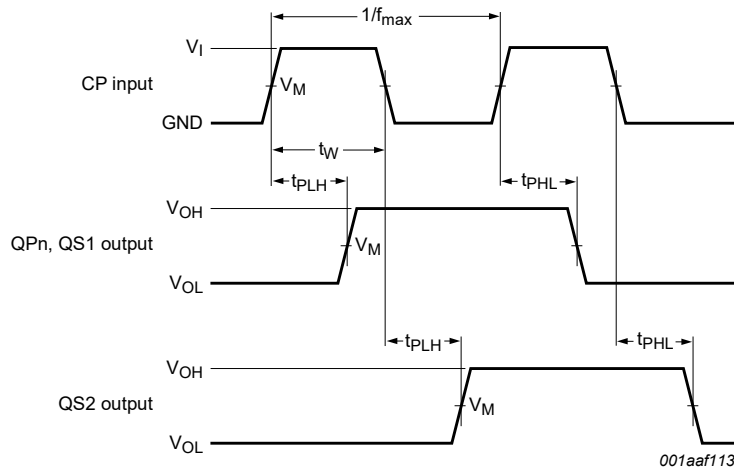
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

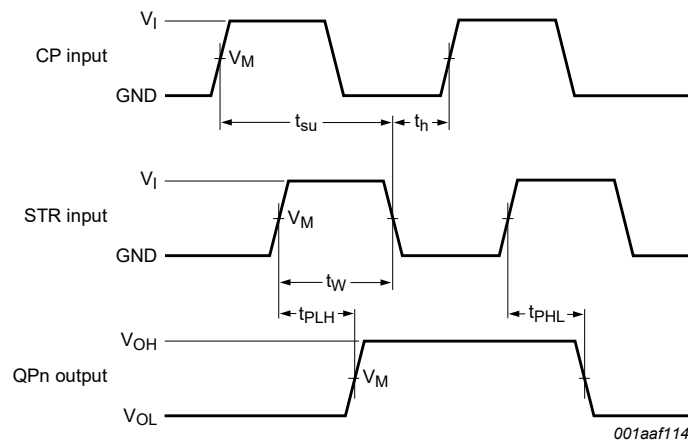
11.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

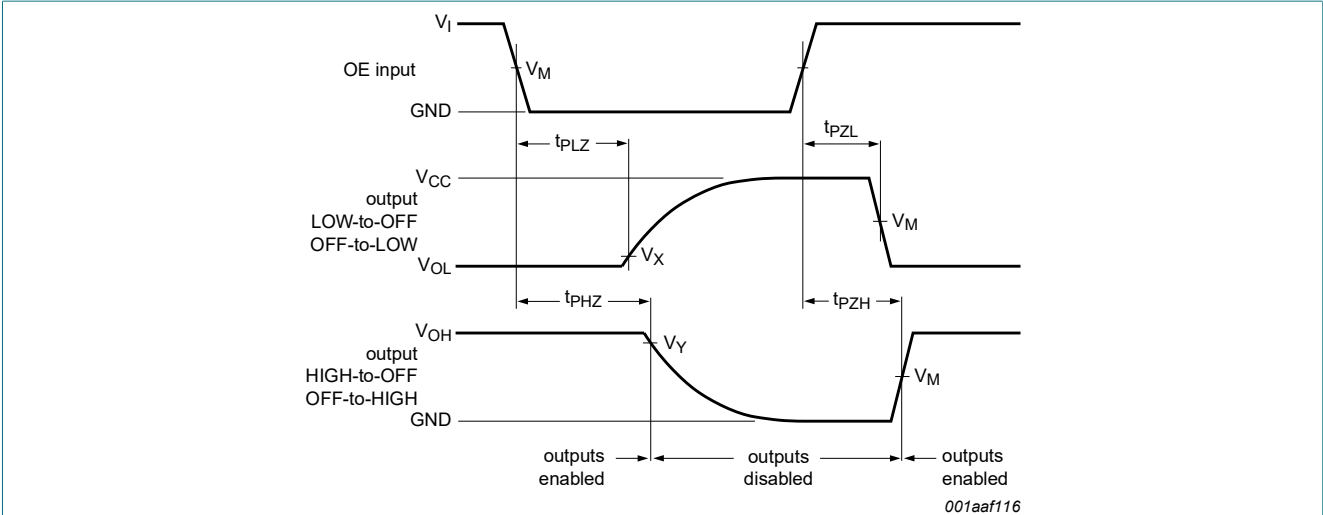
Fig. 6. Propagation delay input (CP) to output (QPn, QS1, QS2), output transition time, clock input (CP) pulse width and the maximum frequency (CP)



Measurement points are given in [Table 8](#).

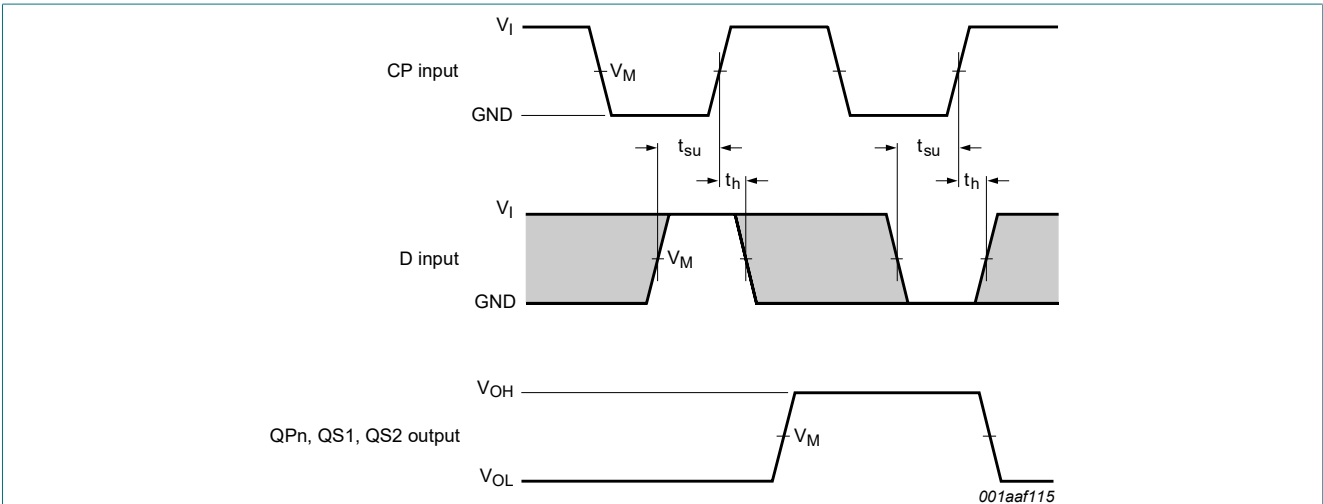
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Propagation delay strobe input (STR) to output (QPn), strobe input (STR) pulse width and the clock set-up and hold times for strobe input



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Enable and disable times

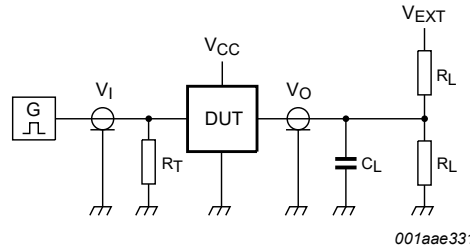
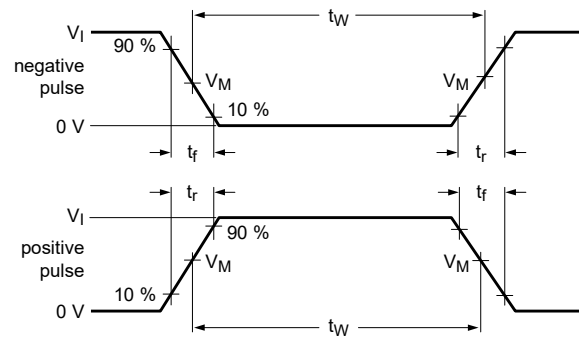


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 9. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



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Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times

Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 k Ω	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 k Ω	open	GND	$2V_{CC}$

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

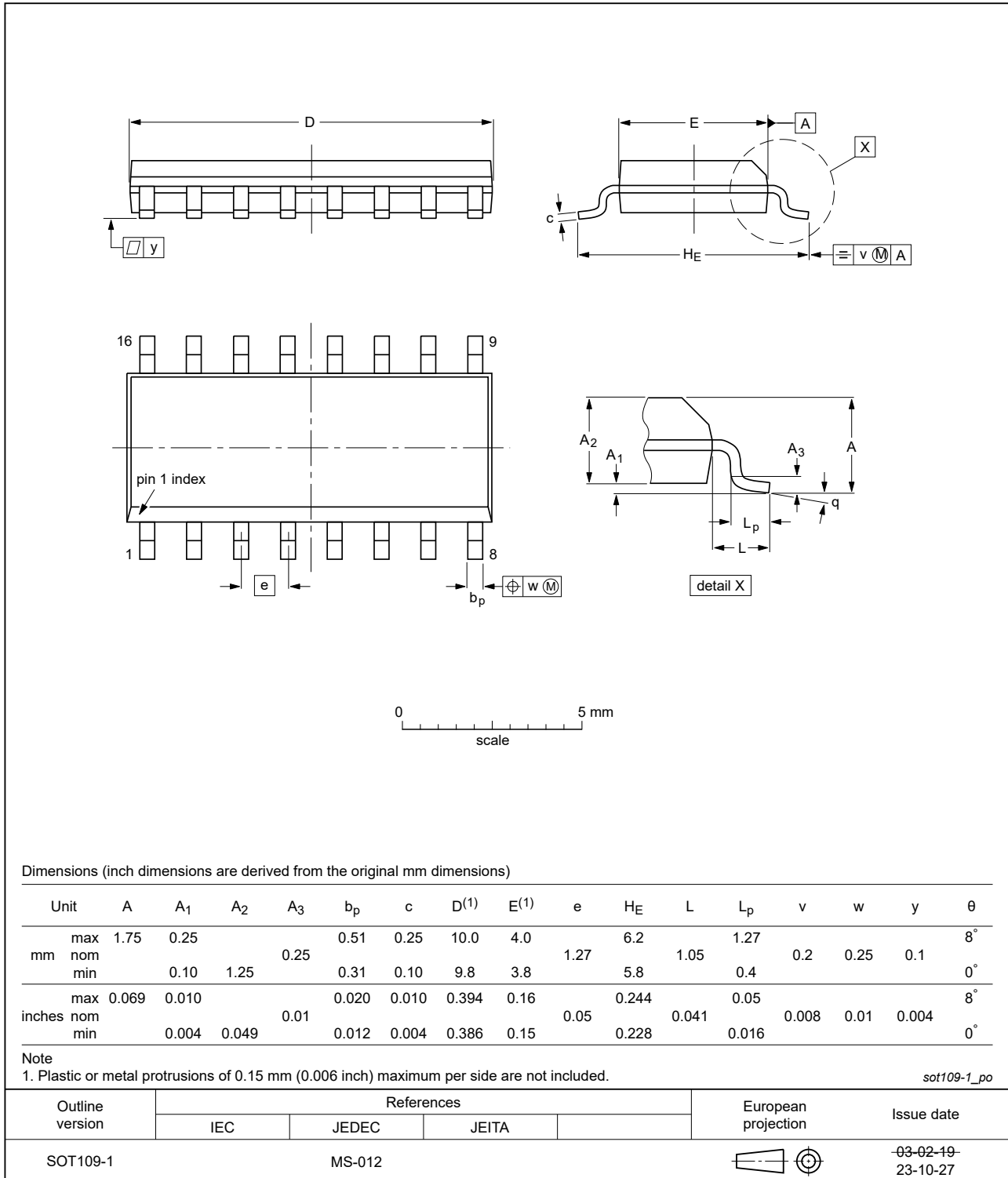


Fig. 11. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

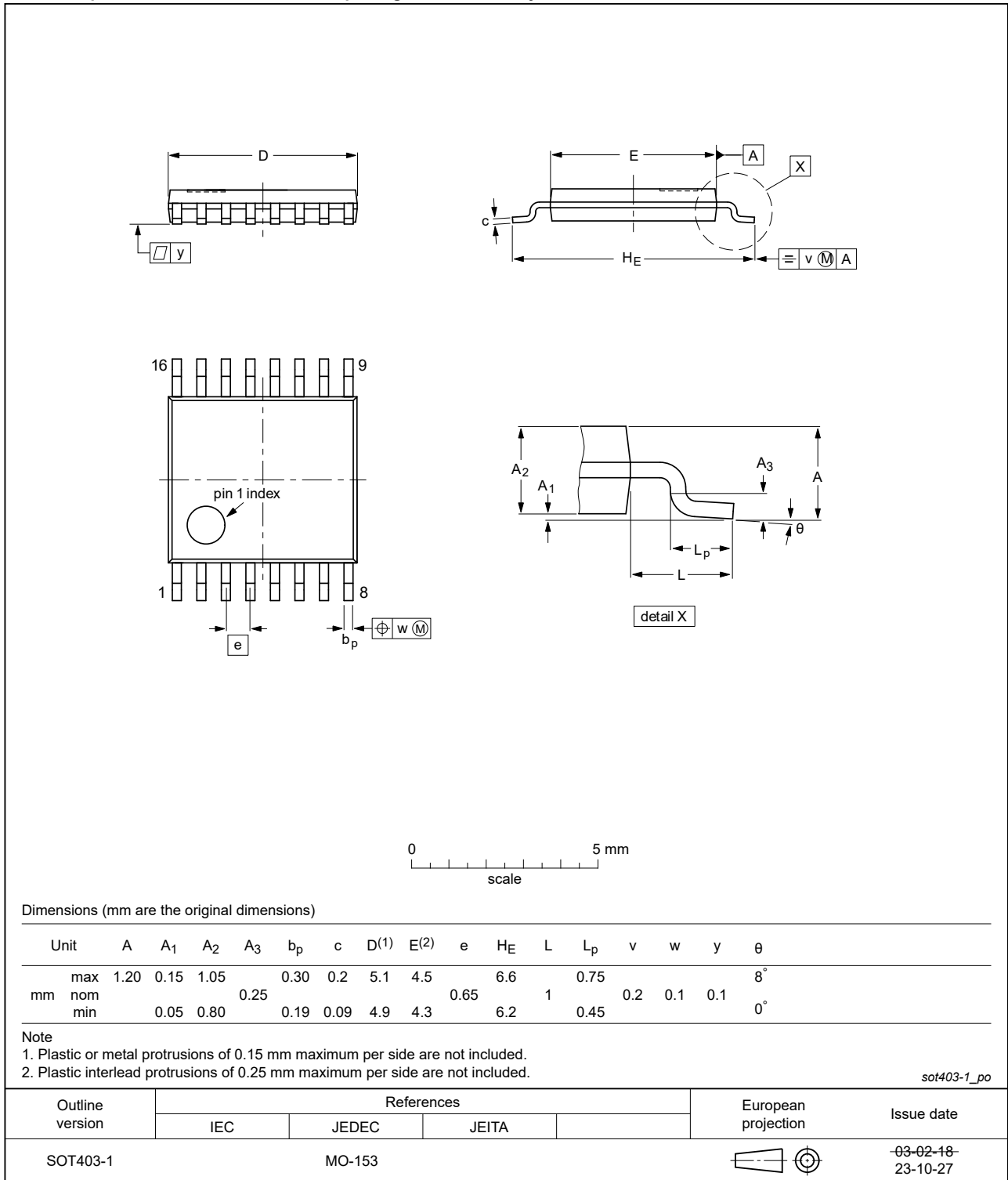


Fig. 12. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4094 v.9	20240528	Product data sheet	-	74LV4094 v.8
Modifications:	<ul style="list-style-type: none"> • Fig. 11, Fig. 12: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard. • Type number 74LV4094DB (SOT338-1 / SSOP16) removed. 			
74LV4094 v.8	20210318	Product data sheet	-	74LV4094 v.7
Modifications:	<ul style="list-style-type: none"> • Type number 74LV4094DB (SOT338-1 / SSOP16) added. 			
74LV4094 v.7	20210205	Product data sheet	-	74LV4094 v.6
Modifications:	<ul style="list-style-type: none"> • Type number 74LV4094DB (SOT338-1 / SSOP16) removed. • Section 1 and Section 2 updated. • Section 8: Derating values for P_{tot} total power dissipation updated. 			
74LV4094 v.6	20181114	Product data sheet	-	74LV4094 v.5
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Fig. 5 corrected. 			
74LV4094 v.5	20160318	Product data sheet	-	74LV4094 v.4
Modifications:	<ul style="list-style-type: none"> • Type number 74LV4094N (SOT38-4) removed. 			
74LV4094 v.4	20111219	Product data sheet	-	74LV4094 v.3
Modifications:	<ul style="list-style-type: none"> • Legal pages updated. 			
74LV4094 v.3	20110307	Product data sheet	-	74LV4094 v.2
74LV4094 v.2	20060629	Product data sheet	-	74LV4094 v.1
74LV4094 v.1	19980623	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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