THE DATASHEET OF

AD5753BCPZ-RL7

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Single-Channel, 16-Bit Current and Voltage DAC with Dynamic Power Control and HART Connectivity

Data Sheet **AD5753**

FEATURES

- 16-bit resolution and monotonicity
- Positive and negative DPC for thermal management
- Current or voltage output available on a single terminal
- Current output ranges: 0 mA to 20 mA, 4 mA to 20 mA, 0 mA to 24 mA, ±20 mA, ±24 mA, and −1 mA to +22 mA
- Voltage output ranges (with 20% overrange): 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V
- User programmable offset and gain
- Advanced on-chip diagnostics, including a 12-bit ADC
- 2 external ADC input pins
- On-chip reference
- Robust architecture, including output fault protection
- −40°C to +115°C temperature range
- 40-lead, 6 mm × 6 mm LFCSP package

APPLICATIONS

- Process control
- Actuator control
- Channel isolated analog outputs
- Programmable logic controller (PLC) and distributed control systems (DCS) applications
- HART network connectivity

GENERAL DESCRIPTION

The AD5753 is a single-channel, voltage and current output digital-to-analog converter (DAC) that operates with a power supply range from a minimum of −33 V on AV_{SS} to a maximum of +33 V on AV_{DD1} with a maximum operating voltage of 60 V between the two rails. On-chip dynamic power control (DPC) minimizes package power dissipation. This minimization is achieved by using buck dc-to-dc converters optimized for minimum on-chip power dissipation to regulate the voltage (V_{DPC+} and V_{DPC-}) that is sent to the VI_{OUT} output driver circuitry from the ±5 V to ±27 V supply voltage. The C_{HART} pin enables a Highway Addressable Remote Transducer® (HART) signal to be coupled on the current output.

The AD5753 uses a versatile, 4-wire, serial peripheral interface (SPI) that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, digital signal processor (DSP), and microcontroller interface standards. The interface features an optional SPI cyclic redundancy check (CRC) and a watchdog timer (WDT). The AD5753 offers improved diagnostic features from earlier versions of similar DACs, such as output current monitoring and an integrated, 12-bit diagnostic analog-to-digital converter (ADC). The inclusion of a line protector on the VI_{OUT}, $+V_{SENSE}$, and $-V_{SENSE}$ pins provides additional robustness.

PRODUCT HIGHLIGHTS

1. Range of advanced diagnostic features, including integrated ADC with two external input pins.
2. DPC, using integrated buck dc-to-dc converters for thermal management, which enables higher channel count in small size module housing.
3. Programmable power control (PPC) mode to enable faster than DPC settling time (15 µs typical).
4. Highly robust with output protection from miswire events (±38 V).
5. HART compliant.

COMPANION PRODUCTS

Product Family: AD5758, AD5755-1, AD5422
HART Modems: AD5700, AD5700-1
External References: ADR431, ADR3425, ADR4525
Digital Isolators: ADuM142D, ADuM141D
Power: LT8300, ADP2360, ADM6339, ADP1031

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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Technical Support www.analog.com

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REVISION HISTORY

5/2019—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

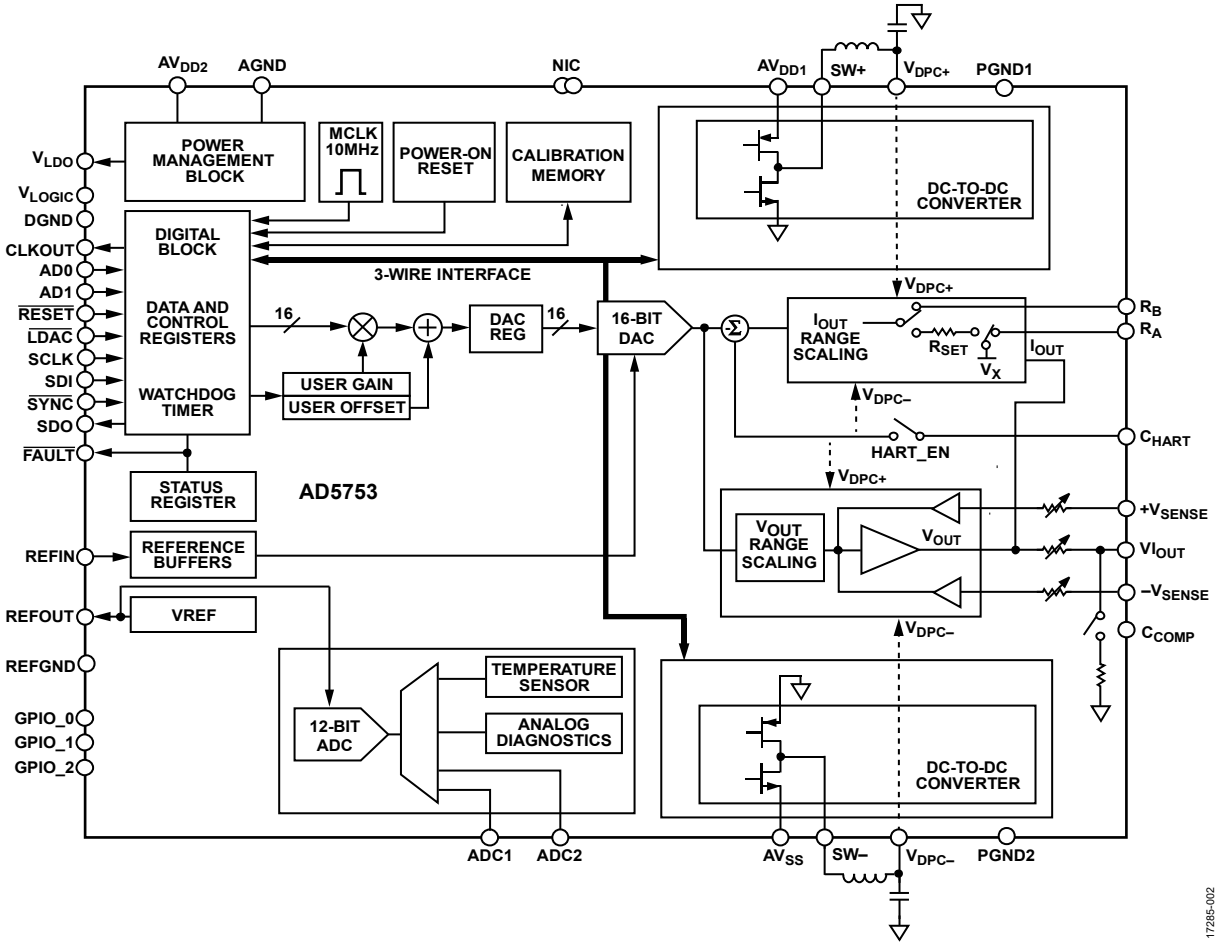


Figure 1.

SPECIFICATIONS

AV_{DD1} = V_{DPC+} = 15 V, dc-to-dc converter disabled, AV_{DD2} = 5 V, AV_{SS} = V_{DPC-} = −15 V, V_{LOGIC} = 1.71 V to 5.5 V, AGND = DGND = REFGND = PGND1 = 0 V, REFIN = 2.5 V external, voltage output: load resistance (R_{LOAD}) = 1 kΩ, load capacitor (C_{LOAD}) = 220 pF, current output: R_{LOAD} = 300 Ω. All specifications at T_A = −40°C to +115°C, T_J (junction temperature) < 125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE (V_{OUT})	0		5	V	Trimmed V_{OUT} ranges
	0		10	V	
	−5		+5	V	
	−10		+10	V	
Output Voltage Overranges	0		6	V	Untrimmed overranges
	0		12	V	
	−6		+6	V	
	−12		+12	V	
Output Voltage Offset Ranges	−0.3		+5.7	V	Untrimmed negatively offset ranges
	−0.4		+11.6	V	
Resolution	16			Bits	
VOLTAGE OUTPUT ACCURACY					Loaded and unloaded, accuracy specifications refer to trimmed V_{OUT} ranges only, unless otherwise noted
Total Unadjusted Error (TUE)	−0.05		+0.05	% FSR	
	−0.01		+0.01	% FSR	T_A = 25°C
TUE Long-Term Stability[1]		15		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		0.35	1.5	ppm FSR/°C	Output drift
Integral Nonlinearity (INL)	−0.006		+0.006	% FSR	All ranges
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic, all ranges
Zero-Scale Error	−0.02	±0.002	+0.02	% FSR	
Zero-Scale Error Temperature Coefficient (TC)[2]		±0.3		ppm FSR/°C	
Bipolar Zero Error	−0.017	+0.001	+0.017	% FSR	±5 V, ±10 V
Bipolar Zero Error TC[2]		±0.4		ppm FSR/°C	±5 V, ±10 V
Offset Error	−0.022	±0.002	+0.022	% FSR	
Offset Error TC[2]		±0.3		ppm FSR/°C	
Gain Error	−0.022	±0.001	+0.022	% FSR	
Gain Error TC[2]		±0.6		ppm FSR/°C	
Full-Scale Error	−0.022	±0.001	+0.022	% FSR	
Full-Scale Error TC[2]		±0.5		ppm FSR/°C	
VOLTAGE OUTPUT CHARACTERISTICS					
Headroom	2			V	Minimum voltage required between VI_{OUT} and V_{DPC+} supply
Footroom	2			V	Minimum voltage required between VI_{OUT} and V_{DPC-} supply
Short-Circuit Current		16		mA	
Load[2]	1			kΩ	For specified performance
Capacitive Load Stability[2]			10	nF	
			2	µF	External compensation capacitor of 220 pF connected
DC Output Impedance		7		mΩ	
DC Power Supply Rejection Ratio (PSRR)		10		µV/V	
V_{OUT} and $-V_{SENSE}$ Common-Mode Rejection Ratio (CMRR)		10		µV/V	Error in V_{OUT} voltage due to changes in $-V_{SENSE}$ voltage

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CURRENT (I_{OUT})	0		24	mA	
	0		20	mA	
	4		20	mA	
	−20		+20	mA	
	−24		+24	mA	
	−1		+22	mA	
Resolution	16			Bits	
CURRENT OUTPUT ACCURACY (EXTERNAL R_{SET})[3]					Assumes ideal 13.7 kΩ resistor
Unipolar Ranges					4 mA to 20 mA, 0 mA to 20 mA, and 0 mA to 24 mA ranges
TUE	−0.05		+0.05	% FSR	
	−0.01		+0.01	% FSR	T_A = 25°C
TUE Long-Term Stability		125		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		2	5	ppm FSR/°C	
INL	−0.007		+0.007	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.03	±0.002	+0.03	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Offset Error	−0.03	±0.001	+0.03	% FSR	
Offset Error TC[2]		±0.7		ppm FSR/°C	
Gain Error	−0.05	±0.002	+0.05	% FSR	
Gain Error TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.05	±0.002	+0.05	% FSR	
Full-Scale Error TC[2]		±3		ppm FSR/°C	
Bipolar Ranges					±20 mA, ±24 mA, and −1 mA to +22 mA ranges
TUE	−0.06		+0.06	% FSR	
	−0.012		+0.012	% FSR	T_A = 25°C
TUE Long-Term Stability[1]		125		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		12	15.5	ppm FSR/°C	
INL	−0.013		+0.013	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.04	±0.003	+0.04	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Bipolar Zero Error	−0.02	±0.003	+0.02	% FSR	
Bipolar Zero Error TC[2]		±0.4		ppm FSR/°C	
Offset Error	−0.04	±0.002	+0.04	% FSR	
Offset Error TC[2]		±0.6		ppm FSR/°C	
Gain Error	−0.06	±0.002	+0.06	% FSR	
Gain Error TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.06	±0.003	+0.06	% FSR	
Full-Scale Error TC[2]		±3		ppm FSR/°C	
CURRENT OUTPUT ACCURACY (INTERNAL R_{SET})					
Unipolar Ranges					4 mA to 20 mA, 0 mA to 20 mA, and 0 mA to 24 mA ranges
TUE	−0.12		+0.12	% FSR	
TUE Long-Term Stability[1]		380		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		3	6	ppm FSR/°C	Output drift
INL	−0.01		+0.01	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.04	±0.001	+0.04	% FSR	
Zero-Scale TC[2]		±0.5		ppm FSR/°C	
Offset Error	−0.04	±0.001	+0.04	% FSR	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Offset Error TC[2]		±1		ppm FSR/°C	
Gain Error	−0.1	±0.003	+0.1	% FSR	
Gain Error TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.12	±0.003	+0.12	% FSR	
Full-Scale Error TC[2]		±3		ppm FSR/°C	
Bipolar Ranges					±20 mA, ±24 mA, and −1 mA to +22 mA ranges
TUE	−0.12		+0.12	% FSR	
TUE Long-Term Stability[1]		380		ppm FSR	Drift after 1000 hours, T_J = 150°C
Output Drift		3	6	ppm FSR/°C	Output drift
INL	−0.02		+0.02	% FSR	
DNL	−1		+1	LSB	Guaranteed monotonic
Zero-Scale Error	−0.06	±0.001	+0.06	% FSR	
Zero-Scale TC[2]		±2		ppm FSR/°C	
Bipolar Zero Error	−0.02	±0.002	+0.02	% FSR	
Bipolar Zero Error TC[2]		±0.3		ppm FSR/°C	
Offset Error	−0.06	±0.001	+0.06	% FSR	
Offset Error TC[2]		±1		ppm FSR/°C	
Gain Error	−0.12	±0.003	+0.12	% FSR	
Gain Error TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.12	±0.003	+0.12	% FSR	
Full-Scale Error TC[2]		±3		ppm FSR/°C	
CURRENT OUTPUT CHARACTERISTICS					
Headroom	2.3			V	Minimum voltage required between VI_{OUT} and V_{DPC+} supply
Footroom	2.3 or 0			V	Minimum voltage required between VI_{OUT} and V_{DPC-} supply; unipolar ranges do not require any footroom and takes on the 0 value
Resistive Load[2]			1000	Ω	The dc-to-dc converter is characterized with a maximum load of 1 kΩ, chosen such that headroom and footroom compliance is not exceeded
Output Impedance		100		MΩ	Midscale output
DC PSRR		0.1		µA/V	
REFERENCE INPUT/OUTPUT					
Reference Input					
Reference Input Voltage[4]		2.5		V	For specified performance
DC Input Impedance	55	120		MΩ	
Reference Output					
Output Voltage	2.495	2.5	2.505	V	T_A = 25°C (including drift after 1000 hours at T_J = 150°C)
Reference TC[2]	−10		+10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[2]		7		µV p-p	
Noise Spectral Density[2]		80		nV/√Hz	At 10 kHz
Capacitive Load[2]			1000	nF	
Load Current		3		mA	
Short-Circuit Current		5		mA	
Line Regulation		1		ppm/V	
Load Regulation		140		ppm/mA	
Thermal Hysteresis[2]		150		ppm	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
V_{LDO} OUTPUT					
Output Voltage		3.3		V	
Output Voltage TC[2]		30		ppm/°C	
Output Voltage Accuracy	−2		+2	%	
Externally Available Current			30	mA	
Short-Circuit Current		55		mA	
Load Regulation		0.8		mV/mA	
Capacitive Load		0.1		µF	Recommended operation
DC-TO-DC					
Start-Up Time		1.25		ms	
Switch					
Peak Current Limit[2]	150		400	mA	User programmable in 50 mA steps via the DCDC_CONFIG2 register
Oscillator					
Oscillator Frequency (f_{SW})		500		kHz	
Minimum Duty Cycle		5		%	
Current Output DPC Mode					Current output dynamic power control mode
V_{DPC+} and V_{DPC-} Voltage Range	±4.95		±27	V	Assuming sufficient supply margin between AV_{DD1} and V_{DPC+}, and AV_{SS} and V_{DPC-}; see the Power Dissipation Control section for further details; maximum operating range of $\lvert V_{DPC+}$ to $V_{DPC-}\rvert$ = 50 V
V_{DPC+} and V_{DPC-} Headroom		2.3	2.5	V	Typical voltage headroom between VI_{OUT} and V_{DPC+} or V_{DPC-}; only applicable when dc-to-dc converter is in regulation, that is, when the load is sufficiently high
Current Output PPC Mode					Programmable power control mode
V_{DPC+} and V_{DPC-} Voltage Range	±5		±25.677	V	Assuming sufficient supply margin between (AV_{DD1} and V_{DPC+}) and (AV_{SS} and V_{DPC-}); see the Power Dissipation Control section for further details; maximum operating range of $\lvert V_{DPC+}$ to $V_{DPC-}\rvert$ = 50 V
V_{DPC+} and V_{DPC-} Voltage Accuracy	−500		+500	mV	Only applicable when dc-to-dc is operating in regulation, that is, when the load is sufficiently high
Voltage Output DPC Mode					Voltage output dynamic power control mode
V_{DPC+} and V_{DPC-} Voltage Range	±5	±15	±25	V	5 V = $-V_{SENSE(MIN)}$ + 15 V; 25 V = $-V_{SENSE(MAX)}$ + 15 V; where $V_{SENSE(MIN)}$ = −10 V and $V_{SENSE(MAX)}$ = +10 V; assuming sufficient supply margin between AV_{DD1} and V_{DPC+}, and AV_{SS} and V_{DPC-}; see the Power Dissipation Control section for further details; maximum operating range of $\lvert V_{DPC+}$ to $V_{DPC-}\rvert$ = 50 V
V_{DPC+} and V_{DPC-} Voltage Accuracy	−250		+250	mV	Only applicable when dc-to-dc is operating in regulation, that is, when the is load sufficiently high
VI_{OUT} LINE PROTECTOR					
On Resistance, R_{ON}		12		Ω	T_A = 25°C
Overvoltage Response Time, $t_{RESPONSE}$		250		ns	
Overvoltage Leakage Current		±100		µA	Line protector fault detect block sinks current for a positive fault and sources current for a negative fault

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC					
Resolution		12		Bits	
Input Voltage Range					
ADC1 Pin	0		0.5	V	ADC_IP_SELECT = 10000
	−0.5		+0.5	V	ADC_IP_SELECT = 10010, AV_{SS} must be ≤ −1 V
	0		1.25	V	ADC_IP_SELECT = 01111
	0		2.5	V	ADC_IP_SELECT = 10001
ADC2 Pin	−15		+15	V	
Total Error					
ADC1 Pin	−0.25		+0.25	% FSR	2.5 V input range
	−0.3		+0.3	% FSR	1.25 V input range
	−0.5		+0.5	% FSR	0 V to 0.5 V and ±0.5 V input ranges
ADC2 Pin	−0.5		+0.5	% FSR	
All other ADC Inputs		±0.3		% FSR	Table 18 lists all ADC input nodes
Conversion Time[2]		100		µs	
GENERAL-PURPOSE INPUT/OUTPUT OUTPUT					
I_{SOURCE} or I_{SINK}[5]		V_{LOGIC}/1 kΩ		mA	Assume 1 kΩ is connected to the GPIO pin
Output Voltage					
Low, V_{OL}			0.4	V	I_{SOURCE} = 2 mA
High, V_{OH}	V_{LOGIC} − 0.2			V	I_{SOURCE} = 2 mA
GPIO INPUT					
Input Voltage					
High, V_{IH}	0.7 × V_{LOGIC}			V	
Low, V_{IL}			0.3 × V_{LOGIC}	V	
Input Current		1.35		µA	
Input Capacitance		2.6		pF	
DIGITAL OUTPUTS					
SDO					
Output Voltage					
Low, V_{OL}			0.4	V	Sinking = 200 µA
High, V_{OH}	V_{LOGIC} − 0.2			V	Sourcing = 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance[2]		2.2		pF	
$\overline{FAULT}$					
Output Voltage					
Low, V_{OL}			0.4	V	10 kΩ pull-up resistor to V_{LOGIC}
		0.6		V	At 2.5 mA
High, V_{OH}	V_{LOGIC} − 0.05			V	10 kΩ pull-up resistor to V_{LOGIC}
DIGITAL INPUTS					
Input Voltage					
3 V ≤ V_{LOGIC} ≤ 5.5 V					
High, V_{IH}	0.7 × V_{LOGIC}			V	
Low, V_{IL}			0.3 × V_{LOGIC}	V	
1.71 V ≤ V_{LOGIC} < 3 V					
High, V_{IH}	0.8 × V_{LOGIC}			V	
Low, V_{IL}			0.2 × V_{LOGIC}	V	
Input Current	−1.5		+1.5	µA	Per pin, internal pull-down on SCLK, SDI, $\overline{RESET}$, and $\overline{LDAC}$; internal pull-up on $\overline{SYNC}$
Pin Capacitance[2]		2.4		pF	Per pin

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Supply Voltages					
AV_{DD1}[6]	7		33	V	Maximum operating range of $\lvert AV_{DD1}$ to $AV_{SS}\rvert = 60$ V
AV_{DD2}	5		33	V	Maximum operating range of $\lvert AV_{DD2}$ to $AV_{SS}\rvert = 50$ V
AV_{SS}[6]	−33		0	V	Maximum operating range of $\lvert AV_{DD1}$ to $AV_{SS}\rvert = 60$ V; for bipolar output ranges, V_{OUT} or I_{OUT} headroom must be obeyed when calculating AV_{SS} maximum; for unipolar current output ranges, AV_{SS} maximum = 0 V; for unipolar voltage output ranges, AV_{SS} maximum = −2.5 V
V_{LOGIC}	1.71		5.5	V	
Supply Quiescent Currents[6]					Quiescent current, assuming no load current
AI_{DD1}[7]		0.05	0.11	mA	Voltage output mode, dc-to-dc converter enabled but not active
		0.05	0.11	mA	Current output mode, dc-to-dc converter enabled but not active
AI_{DD2}[7]		3.3	3.6	mA	Voltage output mode, dc-to-dc converter enabled but not active
		2.9	3.1	mA	Current output mode, dc-to-dc converter enabled but not active
AI_{SS}[7]	−0.11	−0.05		mA	Voltage output mode
	−0.11	0.05		mA	Current output mode
I_{LOGIC}[7]			0.01	mA	$V_{IH} = V_{LOGIC}$, V_{IL} = DGND
I_{DPC+}[7]		1.0	1.3	mA	Voltage output mode
		0.8	1	mA	Unipolar current output mode
		2.3	3.1	mA	Bipolar current output mode
I_{DPC-}[7]	−1.3	−1.0		mA	Voltage output mode
	−0.2	−0.15		mA	Unipolar current output mode
	−3.1	−2.3		mA	Bipolar current output mode
Power Dissipation					Power dissipation assuming an ideal power supply and excluding external load power dissipation, current output DPC mode, negative rail DPC disabled, 0 mA to 20 mA range; see the Example Module Power Calculation section for calculation methodology
		120		mW	AV_{DD1} = 24 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, R_{LOAD} = 1 kΩ, I_{OUT} = 20 mA
		145		mW	AV_{DD1} = 24 V, AV_{DD2} = 5 V, AV_{SS} = −15 V, R_{LOAD} = 0 Ω, I_{OUT} = 20 mA
		180		mW	$AV_{DD1} = AV_{DD2}$ = 24 V, AV_{SS} = −15 V, R_{LOAD} = 1 kΩ, I_{OUT} = 20 mA
		200		mW	$AV_{DD1} = AV_{DD2}$ = 24 V, AV_{SS} = −15 V, R_{LOAD} = 0 Ω, I_{OUT} = 20 mA
		105			AV_{DD1} = 24 V, AV_{DD2} = 5 V, AV_{SS} = −24 V, R_{LOAD} = 1 kΩ, I_{OUT} = −20 mA, negative rail DPC enabled

[1] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[2] Guaranteed by design and characterization; not production tested.
[3] See the Current Output section for more information about the internal and external R_{SET} resistors.
[4] The AD5753 is factory calibrated with an external 2.5 V reference connected to REFIN.
[5] Where I_{SOURCE} is the current source and I_{SINK} is the current sink.
[6] Production tested to AV_{DD1} maximum = 30 V and AV_{SS} minimum = −30 V.
[7] Where AIDD1 is the current on the AV_{DD1} supply, AIDD2 is the current on the AV_{DD2} supply, AI_{SS} is the current on the AV_{SS} supply, I_{LOGIC} is the current on the V_{LOGIC} supply, I_{DPC+} and I_{DPC-} are the currents on the V_{DPC+} and V_{DPC-} supplies, respectively.

AC PERFORMANCE CHARACTERISTICS

AV_{DD1} = V_{DPC+} = 15 V, dc-to-dc converter disabled, AV_{DD2} = 5 V, AV_{SS} = V_{DPC-} = −15 V, V_{LOGIC} = 1.71 V to 5.5 V, AGND = DGND = REFGND = PGND1 = 0 V, REFIN = 2.5 V external, voltage output: R_{LOAD} = 1 kΩ, C_{LOAD} = 220 pF, current output: R_{LOAD} = 300 Ω. All specifications at T_A = −40°C to +115°C, T_J < 125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]					
Voltage Output					
Output Voltage Settling Time					Output voltage settling time specifications also apply to the enabled dc-to-dc converter
		6	20	µs	5 V step to ±0.03% FSR, 0 V to 5 V range
		12	20	µs	10 V step to ±0.03% FSR, 0 V to 10 V range
			15	µs	100 mV step to 1 LSB (16-bit LSB), 0 V to 10 V range
Slew Rate		3		V/µs	0 V to 10 V range, digital slew rate control disabled
Power-On Glitch Energy		25		nV-sec	
Digital-to-Analog Glitch Energy		5		nV-sec	
Glitch Impulse Peak Amplitude		25		mV	
Digital Feedthrough		2		nV-sec	
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.2		LSB p-p	16-bit LSB, 0 V to 10 V range
Output Noise Spectral Density		185		nV/√Hz	Measured at 10 kHz, midscale output, 0 V to 10 V range
AC PSRR		70		dB	200 mV, 50 Hz and 60 Hz sine wave superimposed on power supply voltage
Current Output					
Output Current Settling Time					
		15		µs	To 0.1% FSR (0 mA to 24 mA), dc-to-dc converter disabled
		15		µs	PPC mode, dc-to-dc converter enabled, dc-to-dc current limit = 150 mA
		200		µs	DPC mode, dc-to-dc converter enabled; external inductor and capacitor components as described in Table 10, dc-to-dc current limit = 150 mA
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.2		LSB p-p	16-bit LSB, 0 mA to 24 mA range
Output Noise Spectral Density		0.8		nA/√Hz	Measured at 10 kHz, midscale output, 0 mA to 24 mA range
AC PSRR		80		dB	200 mV, 50 Hz and 60 Hz sine wave superimposed on power supply voltage

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

AV_{DD1} = V_{DPC+} = 15 V, dc-to-dc converter disabled, AV_{DD2} = 5 V, AV_{SS} = V_{DPC-} = −15 V, V_{LOGIC} = 1.71 V to 5.5 V, AGND = DGND = REFGND = PGND1 = 0 V, REFIN = 2.5 V external, voltage output: R_{LOAD} = 1 kΩ, C_{LOAD} = 220 pF, current output: R_{LOAD} = 300 Ω. All specifications at T_A = −40°C to +115°C, T_J < 125°C, unless otherwise noted. The units indicate the minimum or maximum time the action takes to complete.

Table 3.

Parameter[1, 2, 3]	1.71 V ≤ V_{LOGIC} < 3 V	3 V ≤ V_{LOGIC} ≤ 5.5 V	Unit	Description
t_1	33	20	ns minimum	Serial clock input (SCLK) cycle time, write operation
	120	66	ns minimum	SCLK cycle time, read operation
t_2	16	10	ns minimum	SCLK high time, write operation
	60	33	ns minimum	SCLK high time, read operation
t_3	16	10	ns minimum	SCLK low time, write operation
	60	33	ns minimum	SCLK low time, read operation
t_4	10	10	ns minimum	$\overline{SYNC}$ falling edge to SCLK falling edge setup time, write operation
	33	33	ns minimum	$\overline{SYNC}$ falling edge to SCLK falling edge setup time, read operation
t_5	10	10	ns minimum	24th or 32nd SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	500	500	ns minimum	$\overline{SYNC}$ high time (applies to all register writes outside of those listed in this table)
	1.5	1.5	µs minimum	$\overline{SYNC}$ high time (DAC_INPUT register write)
	500	500	µs minimum	$\overline{SYNC}$ high time (DAC_CONFIG register write, where the Range[3:0] bits change; see the Calibration Memory CRC section for more timing information
t_7	5	5	ns minimum	Data setup time
t_8	6	6	ns minimum	Data hold time
t_9	750	750	ns minimum	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge
t_{10}	1.5	1.5	µs minimum	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{11}	250	250	ns minimum	$\overline{LDAC}$ pulse width low
t_{12}	600	600	ns maximum	$\overline{LDAC}$ falling edge to DAC output response time, digital slew rate control disabled.
	2	2	µs maximum	$\overline{LDAC}$ falling edge to DAC output response time, digital slew rate control enabled.
t_{13}	See the AC Performance Characteristics section	See the AC Performance Characteristics section	µs maximum	DAC output settling time
t_{14}	1.5	1.5	µs maximum	$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0)
t_{15}	5	5	µs minimum	$\overline{RESET}$ pulse width
t_{16}	40	28	ns maximum	SCLK rising edge to SDO valid
t_{17}	100	100	µs minimum	$\overline{RESET}$ rising edge to first SCLK falling edge after $\overline{SYNC}$ falling edge (t_{17} does not appear in the timing diagrams)

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{LOGIC}) and timed from a voltage level of 1.2 V. t_R is rise time. t_F is fall time.
[3] See Figure 2, Figure 3, Figure 4, and Figure 5.

Timing Diagrams

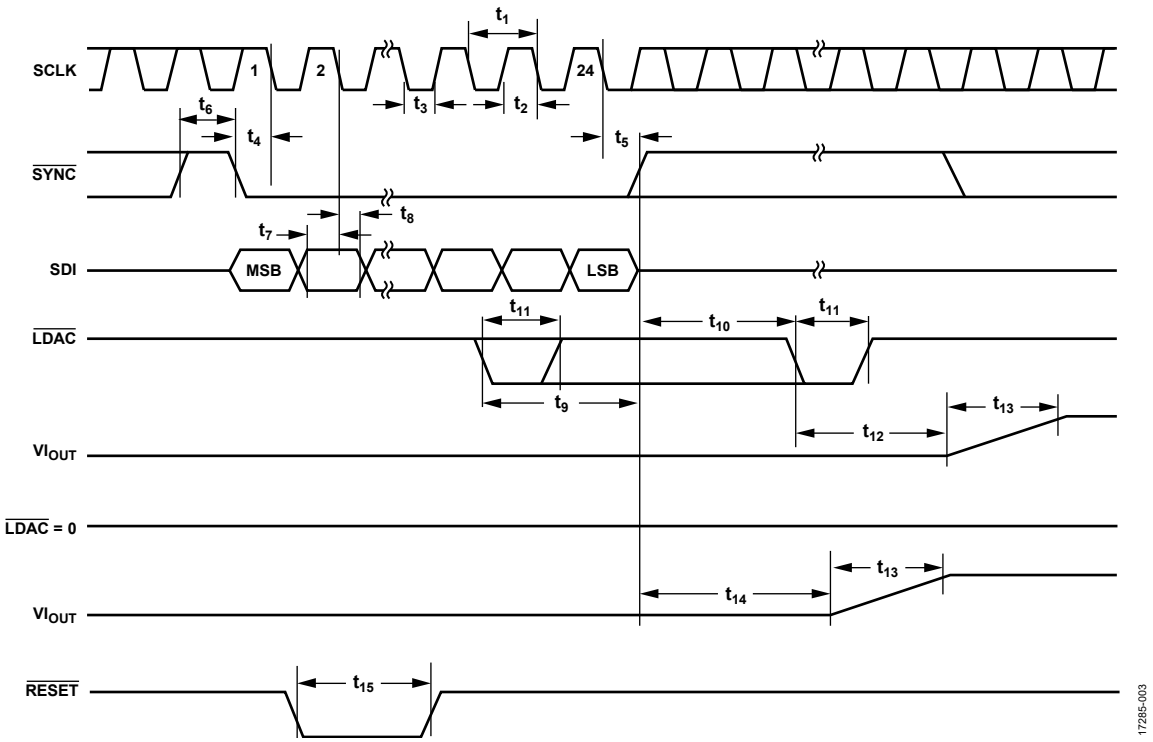


Figure 2. Serial Interface Timing Diagram

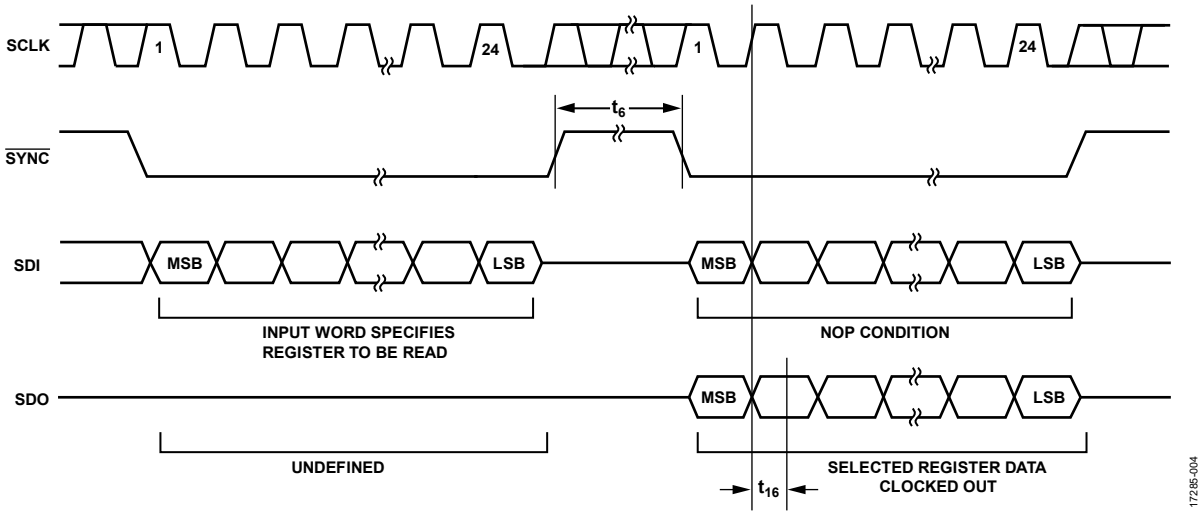
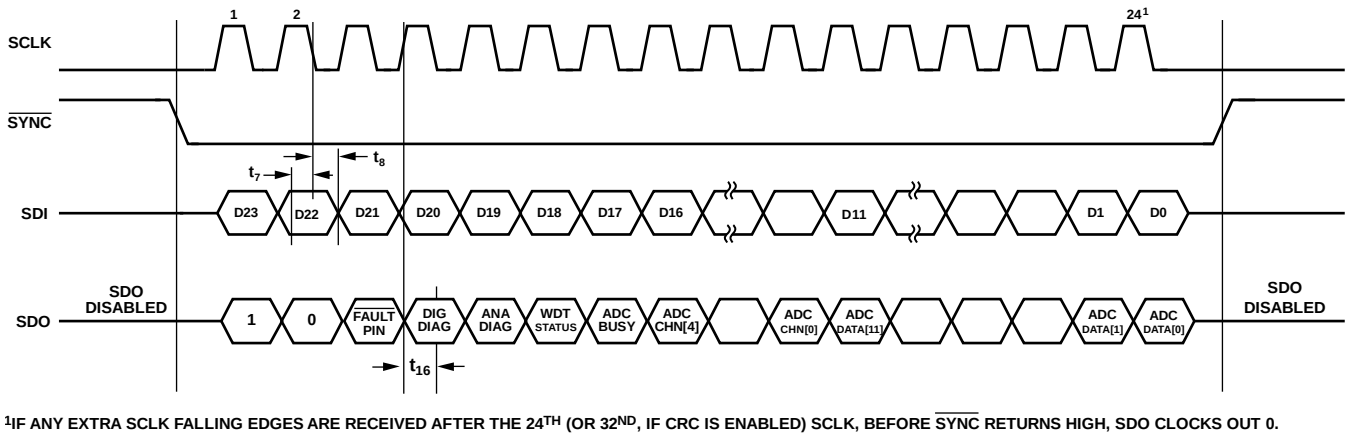


Figure 3. Readback Timing Diagram



[1]IF ANY EXTRA SCLK FALLING EDGES ARE RECEIVED AFTER THE 24TH (OR 32ND, IF CRC IS ENABLED) SCLK, BEFORE SYNC RETURNS HIGH, SDO CLOCKS OUT 0.

Figure 4. Autostatus Readback Timing Diagram

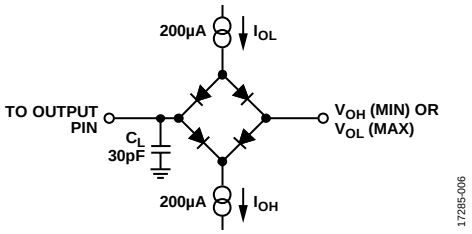


Figure 5. Load Circuit for the SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to ±200 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 4.

Parameter	Rating
AV_{DD1} to AGND, DGND	−0.3 V to +44 V
AV_{SS} to AGND, DGND	+0.3 V to −35 V
AV_{DD1} to AV_{SS}	−0.3 V to +66 V
AV_{DD2}, V_{DPC+} to AGND, DGND	−0.3 V to +35 V
AV_{DD2}, V_{DPC+} to V_{DPC-}	−0.3 V to +55 V
V_{DPC-} to AGND, DGND	+0.3 V to AV_{SS} −0.3 V or −35 V (whichever voltage is less)
V_{LOGIC} to DGND	−0.3 V to +6 V
Digital Inputs to DGND (SCLK, SDI, SYNC, AD0, AD1, RESET, LDAC)	−0.3 V to V_{LOGIC} + 0.3 V or +6 V (whichever voltage is less)
Digital Outputs to DGND (FAULT, SDO, CLKOUT)	−0.3 V to V_{LOGIC} + 0.3 V or +6 V (whichever voltage is less)
GPIO_0, GPIO_1, and GPIO_2 to AGND	−0.3 V to V_{LOGIC} + 0.3 V or +6 V (whichever voltage is less)
REFIN, REFOUT, V_{LDO}, C_{HART} to AGND	−0.3 V to AV_{DD2} + 0.3 V or +6 V (whichever voltage is less)
R_A to AGND	−0.3 V to +4.5 V
R_B to AGND	−0.3 V to +4.5 V
VI_{OUT} to AGND	±38 V
$+V_{SENSE}$ to AGND	±38 V
$-V_{SENSE}$ to AGND	±38 V
C_{COMP} to AGND	AV_{SS} − 0.3 V to V_{DPC+} + 0.3 V
SW+ to AGND	−0.3 V to AV_{DD1} + 0.3 V or +33 V (whichever voltage is less)
SW− to AGND	+0.3 V to AV_{SS} − 0.3 V or −33 V (whichever voltage is less)
AGND, DGND to REFGND	−0.3 V to +0.3 V
AGND, DGND to PGND1, PGND2	−0.3 V to +0.3 V
Industrial Operating Temperature Range (T_A)[1]	−40°C to +115°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	125°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model[2]	±4 kV
Field Induced Charged Device Model[3]	±750 V

[1] Power dissipated on the chip must be derated to keep the junction temperature below 125°C.
[2] As per ANSI/ESDA/JEDEC JS-001, all pins.
[3] As per ANSI/ESDA/JEDEC JS-002, all pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance and Ψ_{JT} is the junction to top of package thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JT}	Unit
CP-40-15[1]	38	0.5	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with thermal vias. See JEDEC and JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

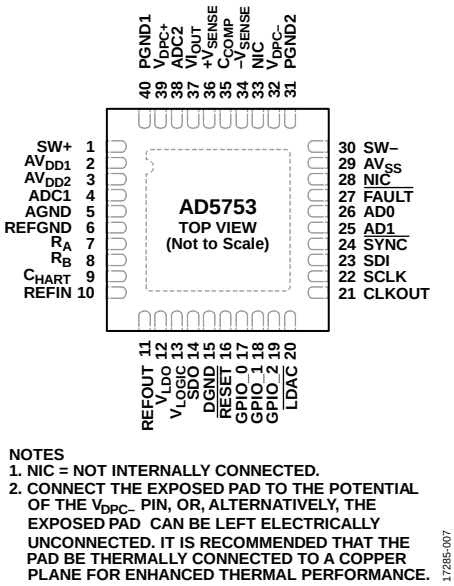


Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SW+	Switching Output for the Positive DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect the external inductor as shown in Figure 77.
2	AV_{DD1}	Positive Analog Supply. The voltage range on this pin is from 7 V to 33 V.
3	AV_{DD2}	Positive Low Voltage Analog Supply. The voltage range on this pin is from 5 V to 33 V.
4	ADC1	Multiplexed ADC External Input 1.
5	AGND	Ground Reference Point for the Analog Circuitry. This pin must be connected to 0 V.
6	REFGND	Ground Reference Point for Internal Reference. This pin must be connected to 0 V.
7	R_A	External Current Setting Resistor. An external precision, low drift, 13.7 kΩ current setting resistor can be connected between R_A and R_B to improve the current output temperature drift performance. It is recommended to place the external resistor as close as possible to the AD5753.
8	R_B	External Current Setting Resistor. An external precision, low drift, 13.7 kΩ current setting resistor can be connected between R_A and R_B to improve the current output temperature drift performance. It is recommended to place the external resistor as close as possible to the AD5753.
9	C_{HART}	HART Input Connection. The HART signal must be ac-coupled to this pin. If the HART signal is not being used, leave this pin unconnected. This pin is disconnected from the HART summing node by default and is connected via the HART_EN bit in the GP_CONFIG1 register.
10	REFIN	External 2.5 V Reference Voltage Input.
11	REFOUT	Internal 2.5 V Reference Voltage Output. REFOUT must be connected to REFIN to use the internal reference. A capacitor between REFOUT and REFGND is not recommended.
12	V_{LDO}	3.3 V Low Dropout (LDO) Output Voltage. V_{LDO} must be decoupled to the AGND with a 0.1 µF capacitor.
13	V_{LOGIC}	Digital Supply. The voltage range on this pin is from 1.71 V to 5.5 V. V_{LOGIC} must be decoupled to DGND with a 0.1 µF capacitor.
14	SDO	Serial Data Output. This pin clocks data from the serial register in readback mode. The maximum SCLK speed for readback mode is 15 MHz and this speed is dependent on the V_{LOGIC} voltage. See Table 3 for the timing specifications.
15	DGND	Digital Ground.
16	$\overline{\text{RESET}}$	Hardware $\overline{\text{Reset}}$. Active low input. Do not write an SPI command within 100 µs of issuing a reset either by using the hardware $\overline{\text{RESET}}$ pin or via software.
17	GPIO_0	General-Purpose Input/Output 0.
18	GPIO_1	General-Purpose Input/Output 1.
19	GPIO_2	General-Purpose Input/Output 2.
20	$\overline{\text{LDAC}}$	Load DAC. $\overline{\text{Active}}$ low input. This pin updates the DAC_OUTPUT register and, consequently, the DAC output. $\overline{\text{Do}}$ not assert $\overline{\text{LDAC}}$ within the 500 ns window before the rising edge of $\overline{\text{SYNC}}$ or 1.5 µs after the rising edge of $\overline{\text{SYNC}}$ (see Table 3 for the timing specifications).

Pin No.	Mnemonic	Description
21	CLKOUT	Optional Clock Output Signal (Disabled by Default). This pin is a divided down version of the internal 10 MHz internal oscillator, which generates the master clock (MCLK), and is configured in the GP_CONFIG1 register.
22	SCLK	Serial Clock Input. Data is clocked to the input shift register on the falling edge of the SCLK. In write mode, this pin operates at clock speeds of up to 50 MHz and this speed is dependent on the V_{LOGIC} voltage. In read mode, the maximum SCLK speed is 15 MHz and this speed is dependent on the V_{LOGIC} voltage. See Table 3 for the timing specifications.
23	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
24	$\overline{\text{SYNC}}$	Frame Synchronization Signal for the Serial Interface. Active low input. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK.
25	AD1	Address Decode 1 for the AD5753 Device.
26	AD0	Address Decode 0 for the AD5753 Device.
27	$\overline{\text{FAULT}}$	Fault Pin. Active low, open-drain output. This pin is high impedance when no faults are detected and is asserted low when certain faults are detected. Some of these faults include an open circuit in current mode, a short circuit in voltage mode, a CRC error, or an overtemperature error (see the Output Fault section). This pin must be connected to V_{LOGIC} with a 10 kΩ pull-up resistor.
28	NIC	Not Internally Connected.
29	AV_{SS}	Negative Analog Supply. The voltage range on this pin is 0 V to −33 V. If using the device solely for unipolar current output purposes, the AV_{SS} can be set to 0 V. For a unipolar voltage output, AV_{SS} (maximum) is −2 V. When using bipolar output ranges, the V_{OUT} or I_{OUT} headroom must be obeyed when calculating the AV_{SS} maximum. For example, for a ±10 V output, the AV_{SS} maximum is −12.5 V. See the AV_{SS} Considerations section for an important note on power supply sequencing.
30	SW−	Switching Output for the Negative DC-to-DC Circuitry. To use the dc-to-dc feature of the device, connect the pin and external inductor as shown in Figure 78.
31	PGND2	Power to Ground.
32	V_{DPC-}	Negative Supply for Current and Voltage Output Stage. To use the dc-to-dc feature of the device, connect the external capacitor as shown in Figure 78.
33	NIC	Not Internally Connected.
34	$-V_{SENSE}$	Sense Connection for Negative Voltage Output Load Connection for V_{OUT} Mode. This pin must stay within ±10 V of AGND for specified operation. For specified operation, V_{DPC-} tracks $-V_{SENSE}$ with respect to AGND. It is recommended to connect a series 1 kΩ resistor to this pin.
35	C_{COMP}	Optional Compensation Capacitor Connection for the Voltage Output Buffer. Connecting a 220 pF capacitor between this pin and the VI_{OUT} pin allows the voltage output to drive up to 2 µF. The addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
36	$+V_{SENSE}$	Sense Connection for Positive Voltage Output Load Connection for Voltage Output Mode. It is recommended to connect a series 1 kΩ resistor to this pin.
37	VI_{OUT}	Voltage or Current Output Pin. VI_{OUT} is a shared pin that provides either a buffered output voltage or current.
38	ADC2	Multiplexed ADC External Input 2.
39	V_{DPC+}	Positive Supply for Current and Voltage Output Stage. To use the dc-to-dc feature of the device, connect the external capacitor as shown in Figure 77.
40	PGND1	Power to Ground.
	EPAD	Exposed Pad. Connect the exposed pad to the potential of the V_{DPC-} pin, or, alternatively, the exposed pad can be left electrically unconnected. It is recommended that the pad be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE OUTPUT

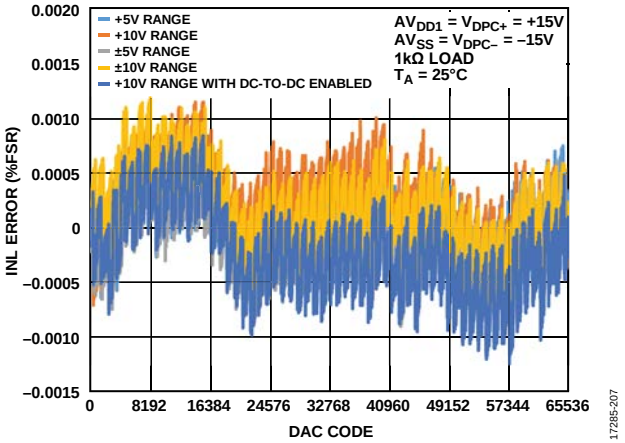


Figure 7. INL Error vs. DAC Code

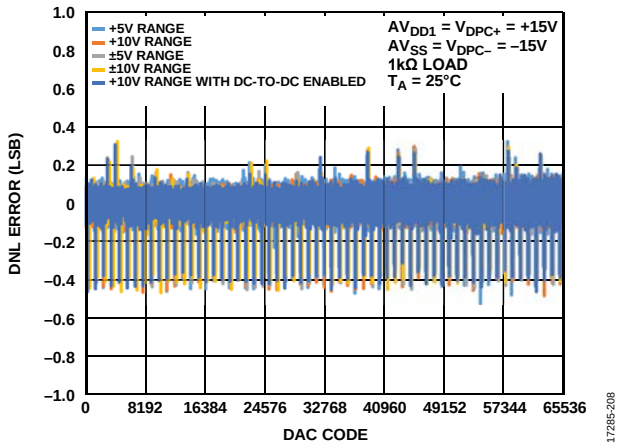


Figure 8. DNL Error vs. DAC Code

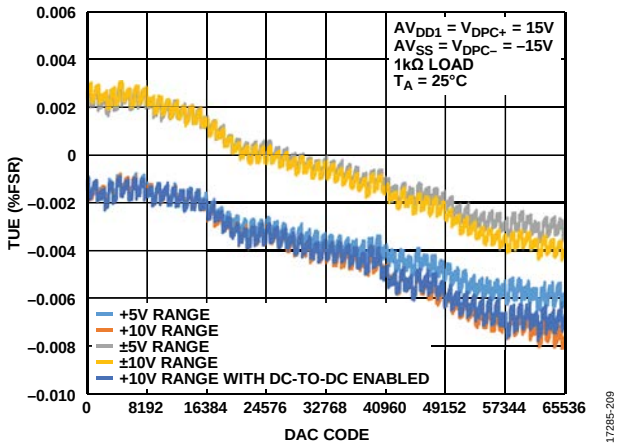


Figure 9. TUE vs. DAC Code

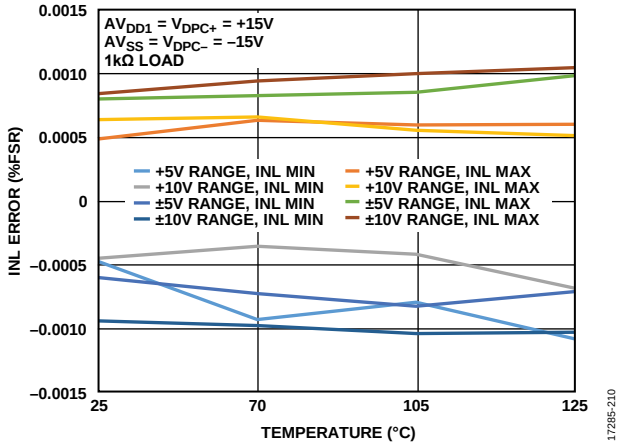


Figure 10. INL Error vs. Temperature

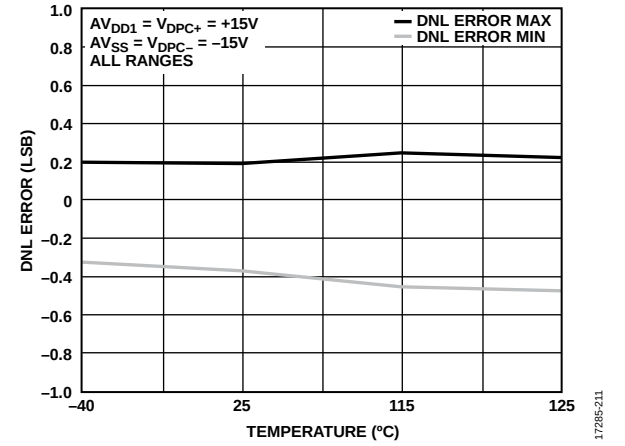


Figure 11. DNL Error vs Temperature

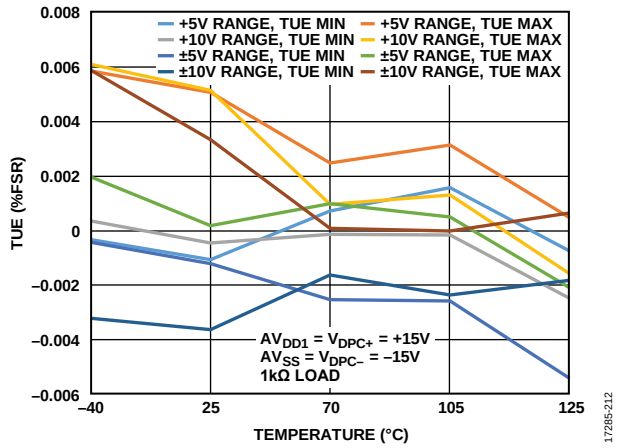


Figure 12. TUE vs. Temperature

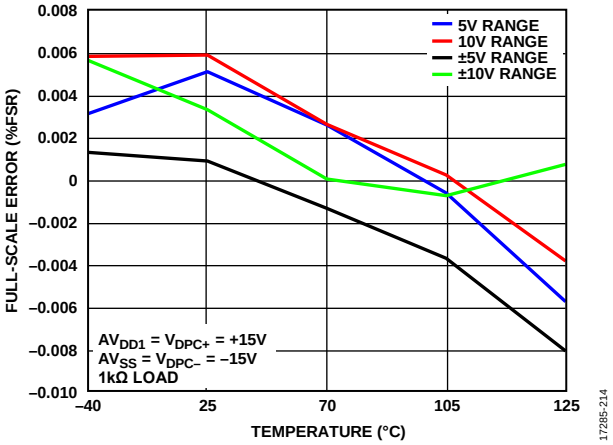


Figure 13. Full-Scale Error vs. Temperature

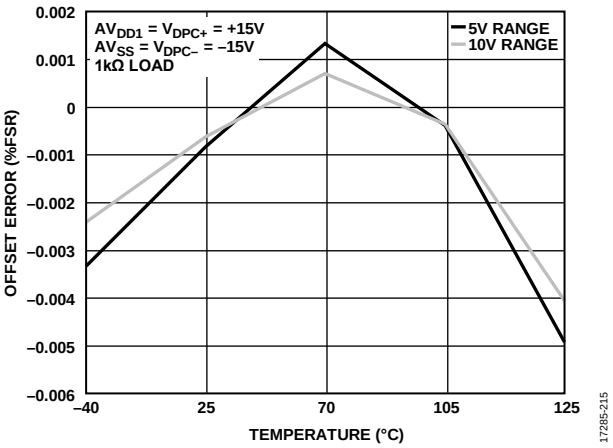


Figure 14. Offset Error vs. Temperature

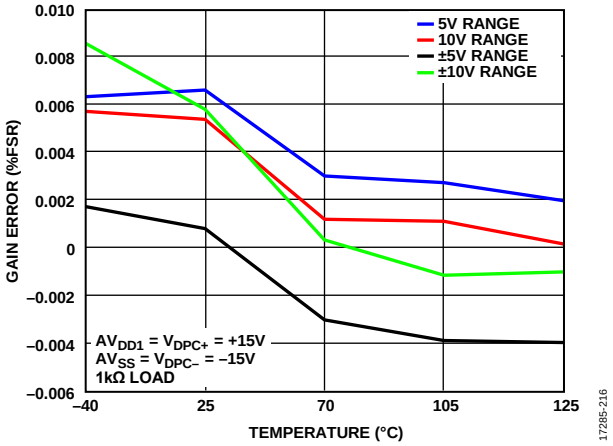


Figure 15. Gain Error vs. Temperature

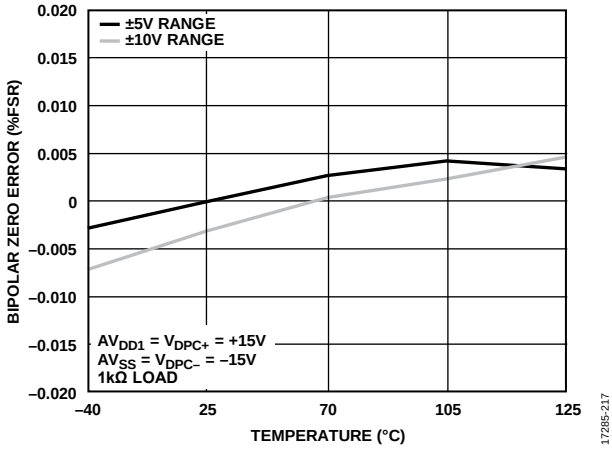


Figure 16. Bipolar Zero Error vs. Temperature

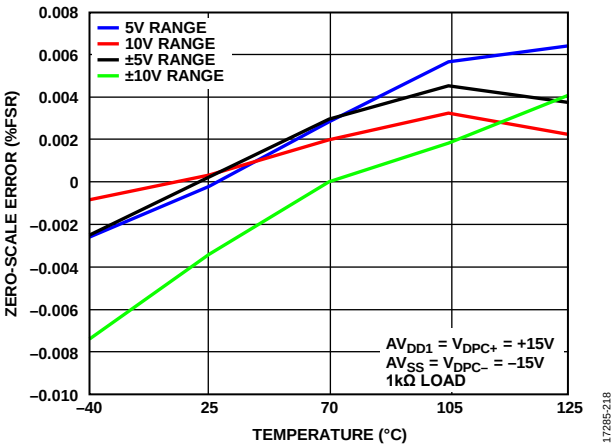


Figure 17. Zero-Scale Error vs. Temperature

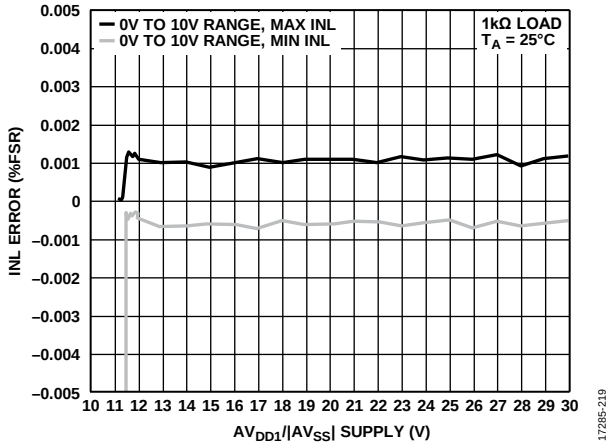


Figure 18. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply

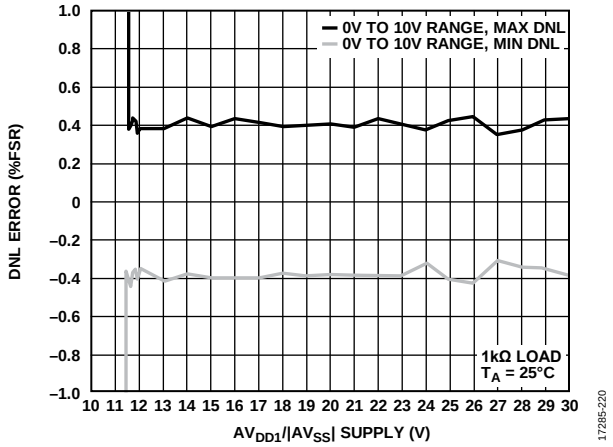


Figure 19. DNL Error vs. AV_{DD1}/|AV_{SS}| Supply

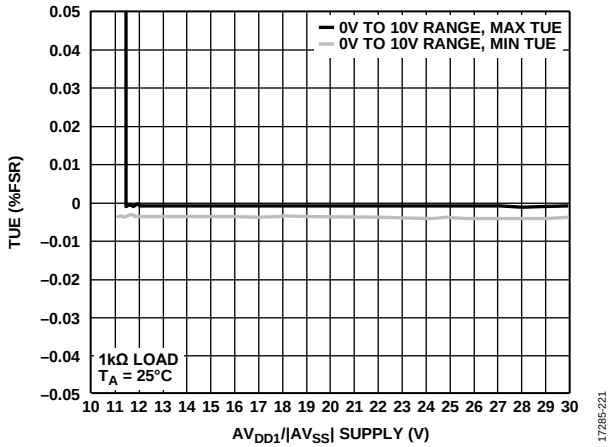


Figure 20. TUE vs. AV_{DD1}/|AV_{SS}| Supply

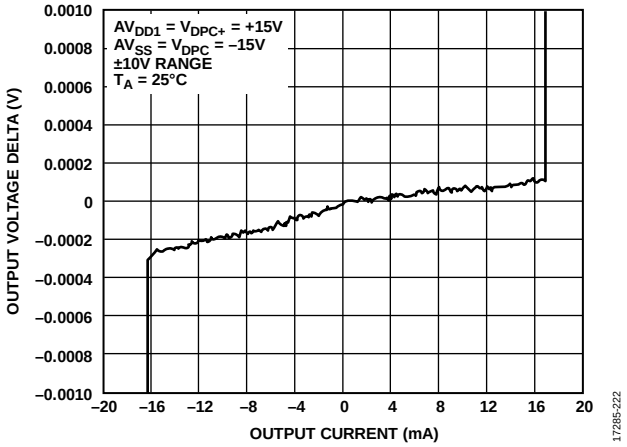


Figure 21. Sink and Source Capability of the Output Amplifier

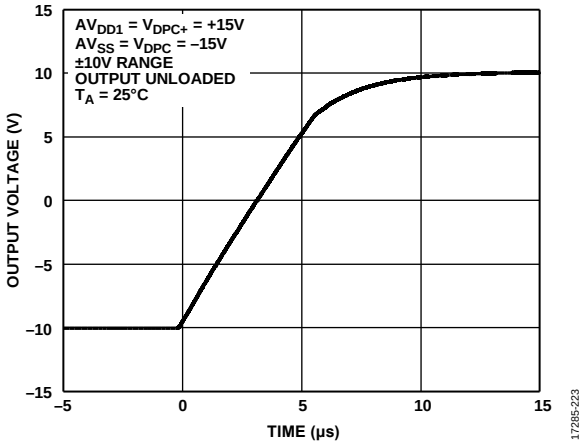


Figure 22. Full-Scale Positive Step

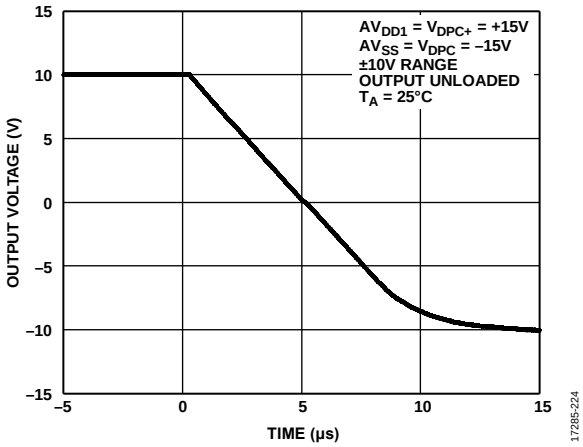


Figure 23. Full-Scale Negative Step

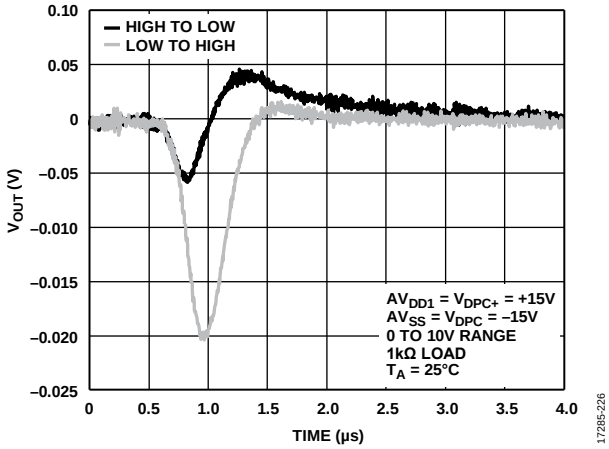


Figure 24. Digital-to-Analog Glitch Major Code Transition

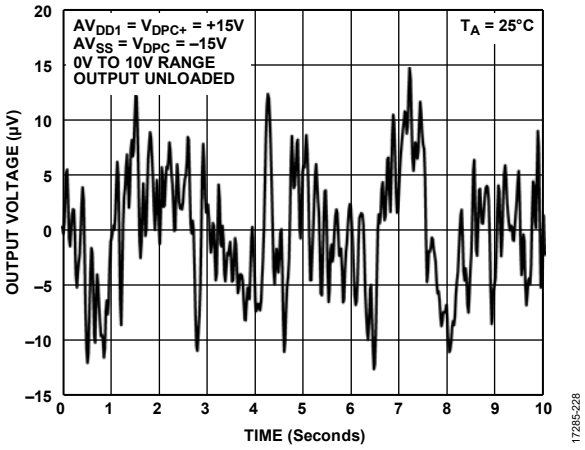


Figure 25. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

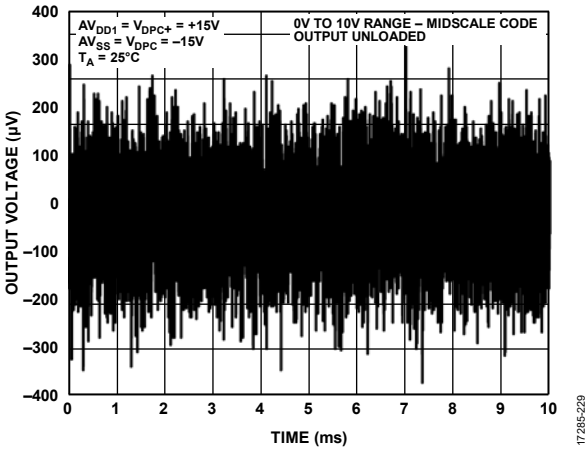


Figure 26. Peak-to-Peak Noise (100 kHz Bandwidth)

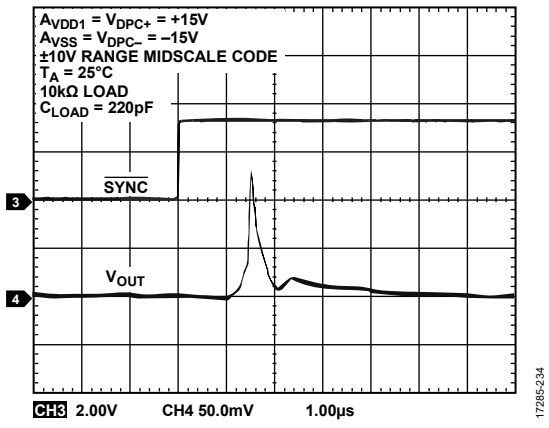


Figure 27. V_{OUT} vs. Time on Output Enable

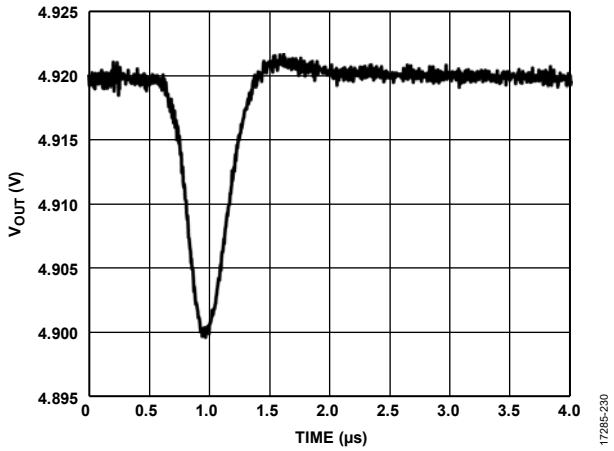


Figure 28. V_{OUT} vs. Time on Power-Up

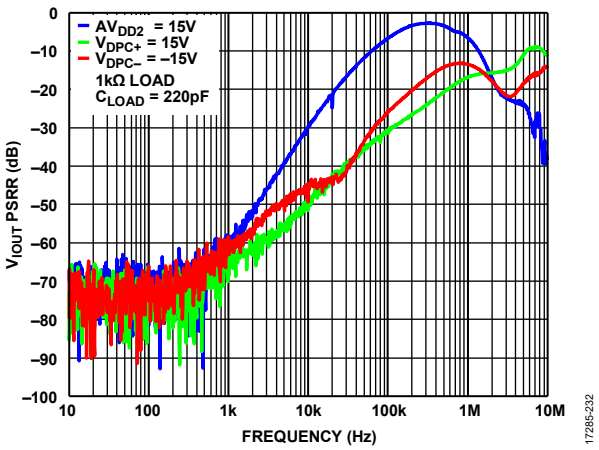


Figure 29. V_{OUT} PSRR vs. Frequency

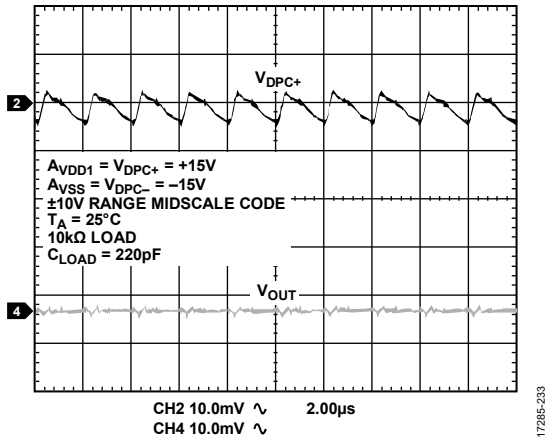


Figure 30. Voltage Output Ripple

CURRENT OUTPUTS

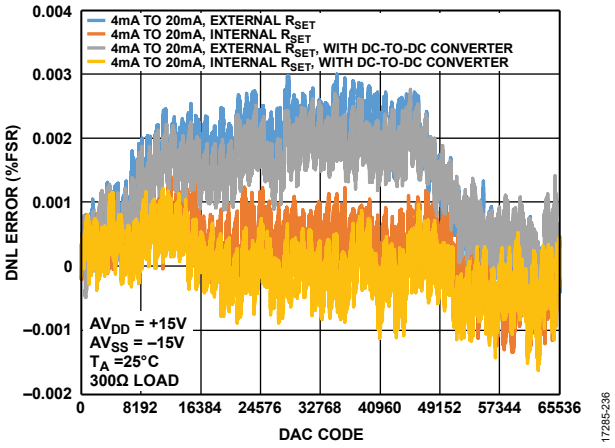


Figure 31. INL Error vs. DAC Code

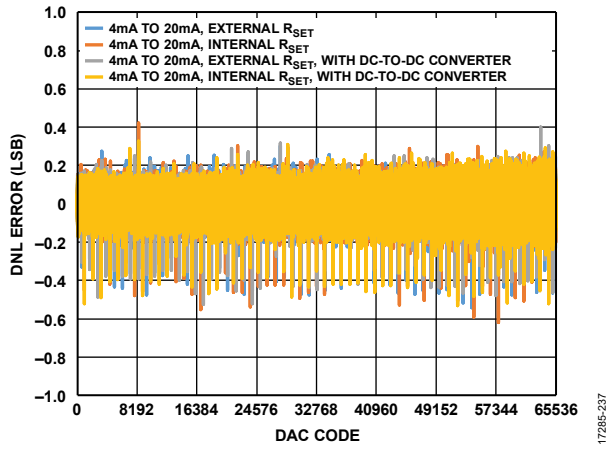


Figure 32. DNL Error vs. DAC Code

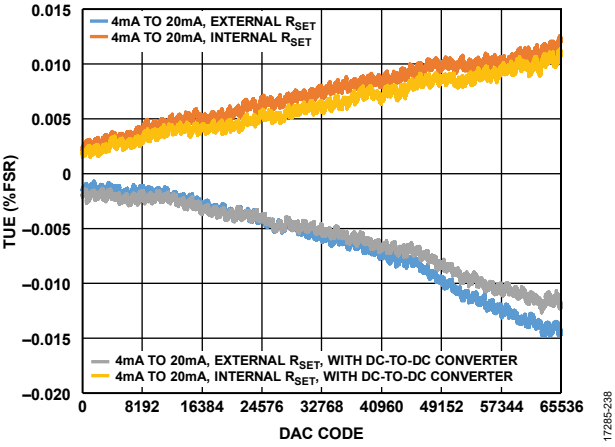


Figure 33. TUE vs. DAC Code

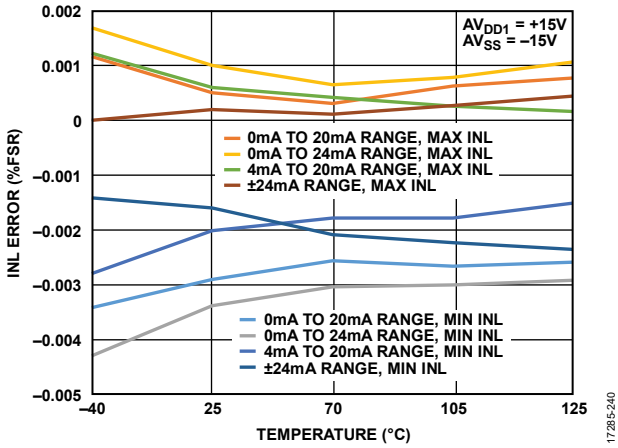


Figure 34. INL Error vs. Temperature, Internal R_{SET}

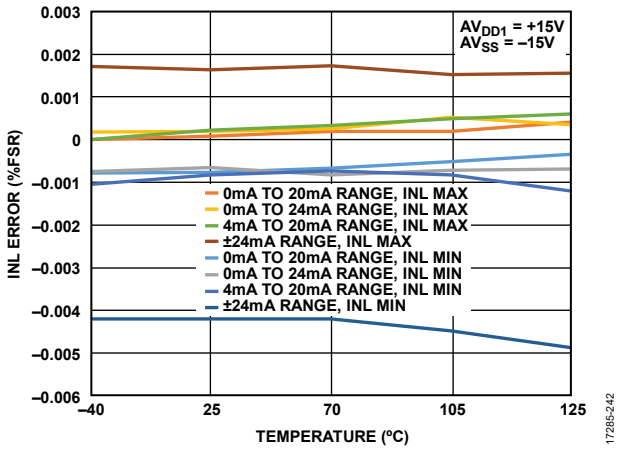


Figure 35. INL Error vs. Temperature, External R_{SET}

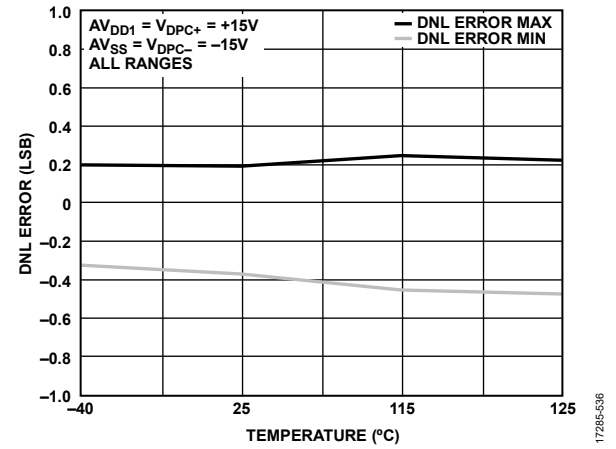


Figure 36. DNL Error vs. Temperature

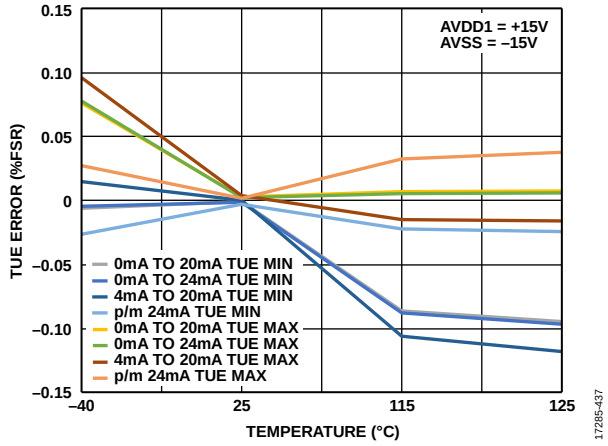


Figure 37. TUE Error vs. Temperature, Internal R_{SET}

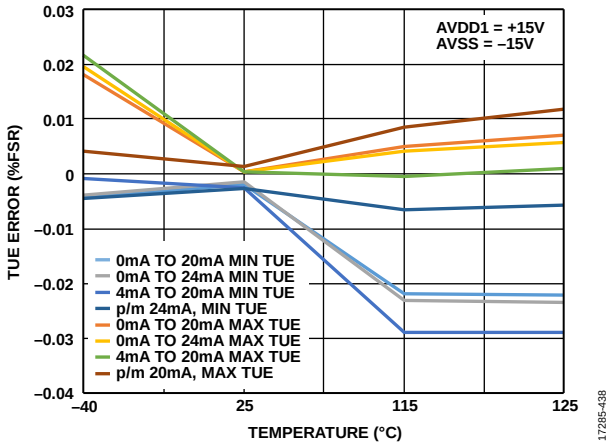


Figure 38. TUE Error vs. Temperature, External R_{SET}

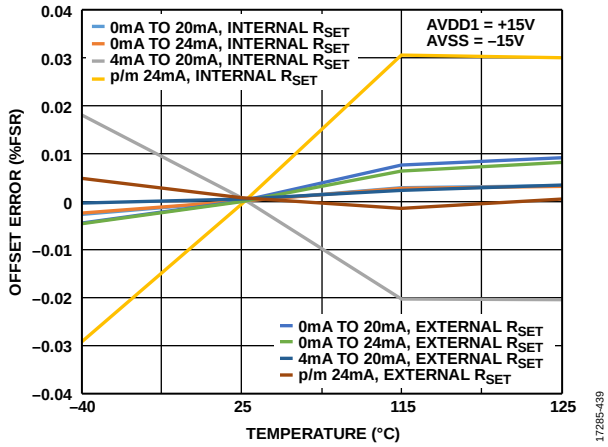


Figure 39. Offset Error vs. Temperature

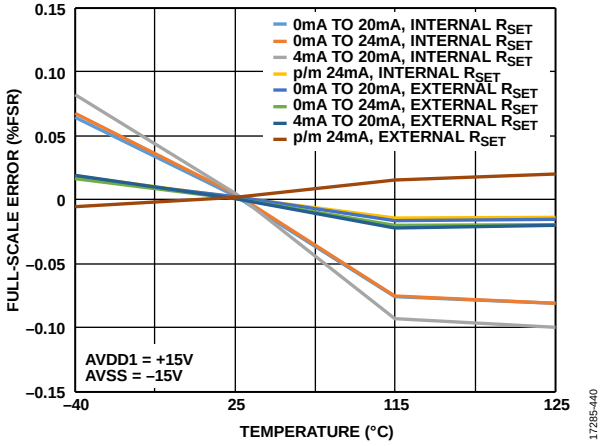


Figure 40. Full-Scale Error vs. Temperature

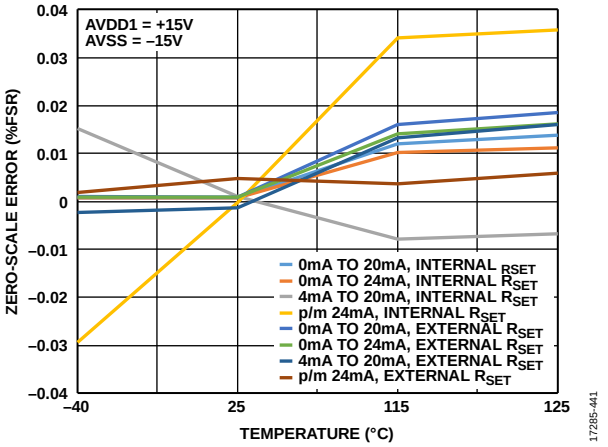


Figure 41. Zero-Scale Error vs. Temperature

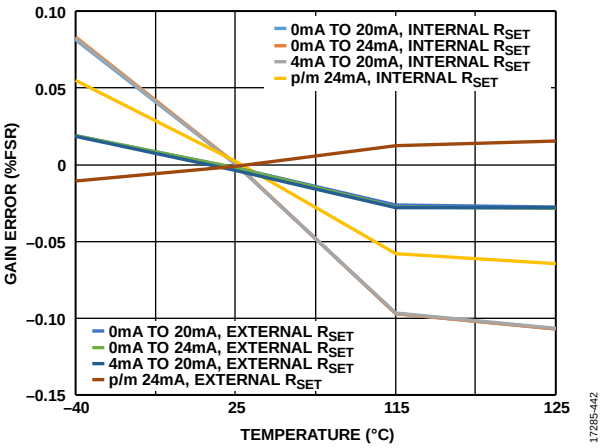


Figure 42. Gain Error vs. Temperature

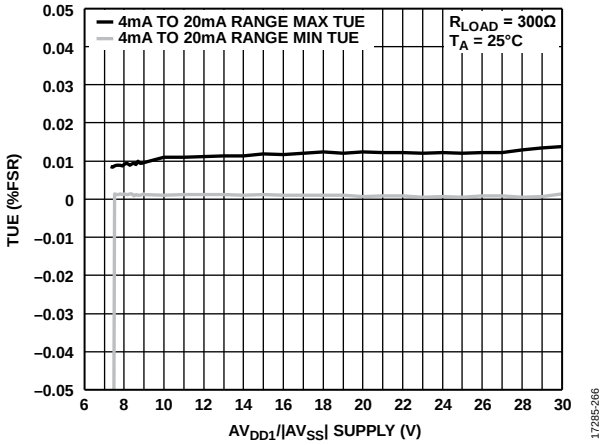


Figure 43. TUE vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

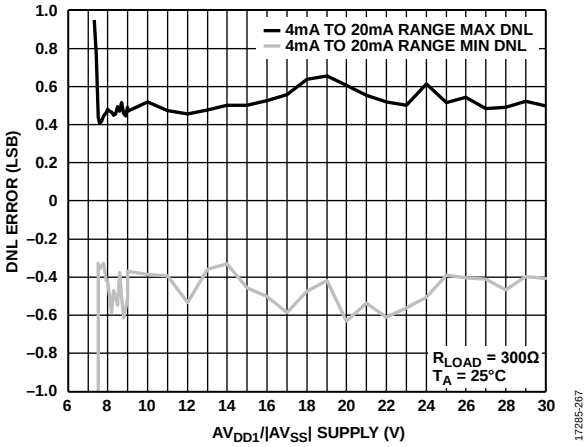


Figure 46. DNL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

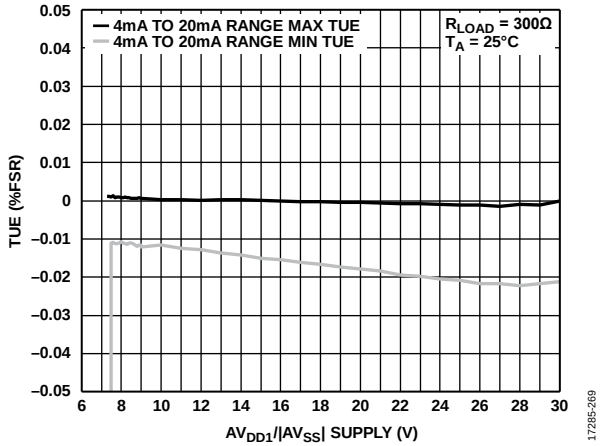


Figure 44. TUE vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

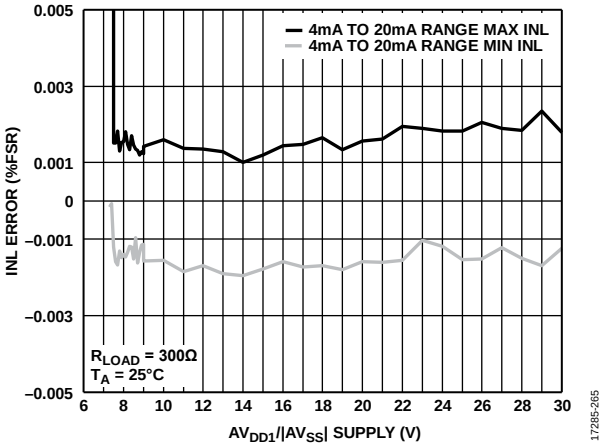


Figure 47. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

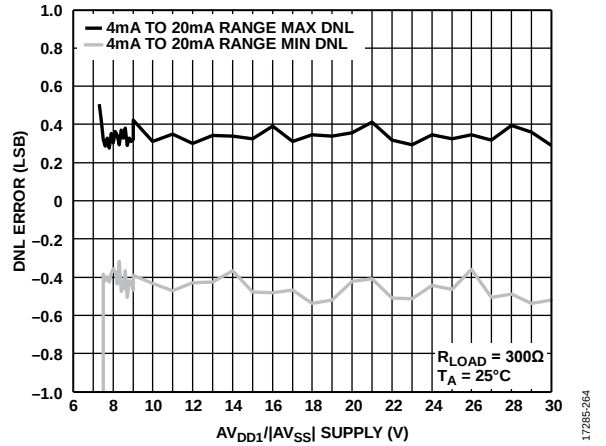


Figure 45. DNL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, Internal R_{SET}

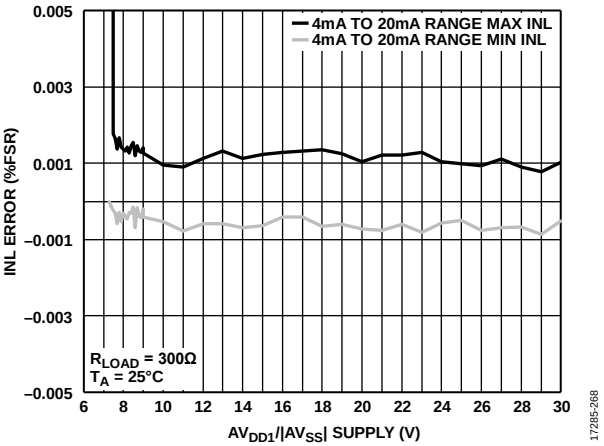


Figure 48. INL Error vs. $AV_{DD1}/|AV_{SS}|$ Supply, External R_{SET}

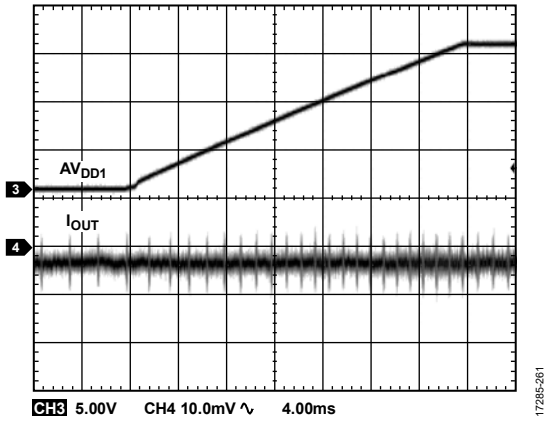


Figure 49. Output Current vs. Time on Power-Up

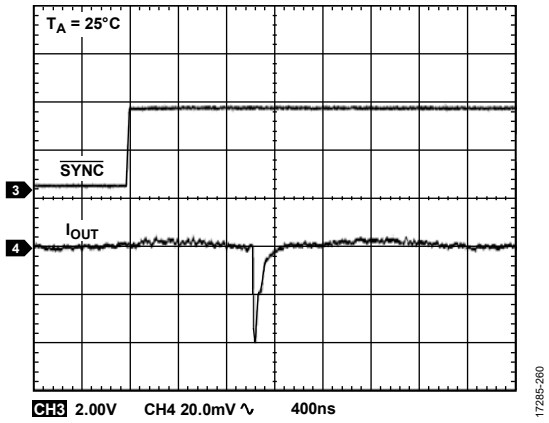


Figure 50. Output Current vs. Time on Output Enable

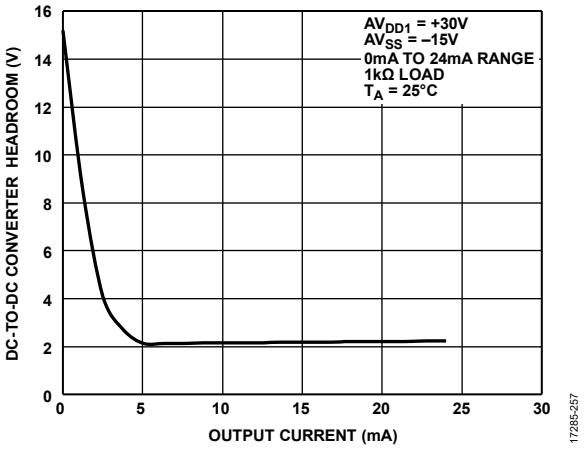


Figure 51. DC-to-DC Converter Headroom vs. Output Current

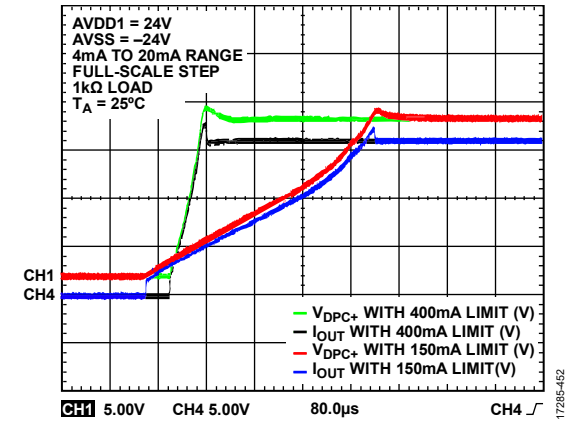


Figure 52. Output Current and V_{DPC+} Settling Time

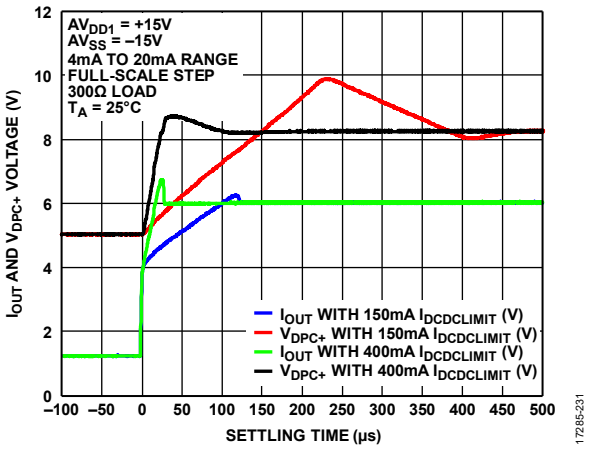


Figure 53. I_{OUT} and V_{DPC+} Voltage vs. Settling Time where $I_{DCDCLIMIT}$ is the DC-to-DC Converter Current Limit

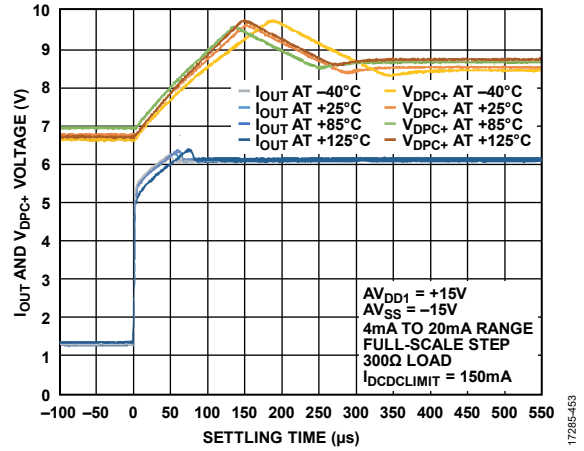


Figure 54. I_{OUT} and V_{DPC+} Voltage vs. Settling Time Including Temperature

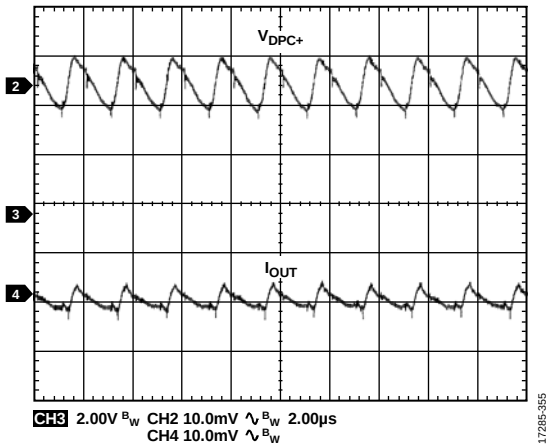


Figure 55. Output Current Ripple vs. Time with DC-to-DC Converter

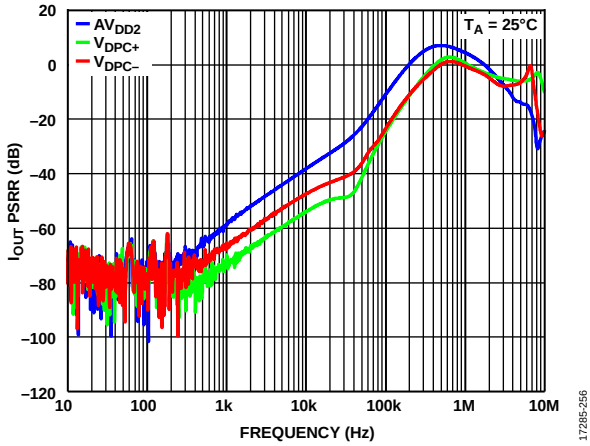


Figure 56. I_{OUT} PSRR vs. Frequency

DC-TO-DC BLOCK

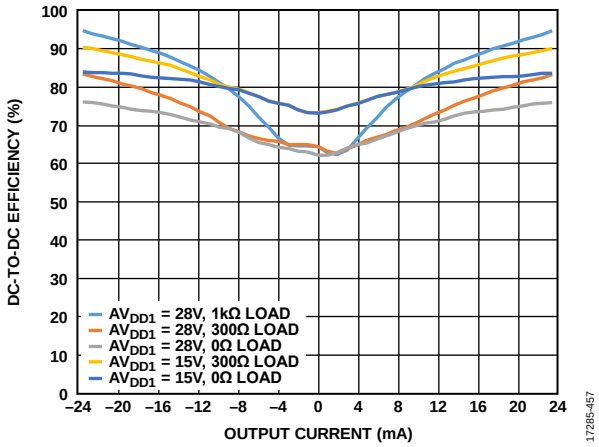


Figure 57. DC-to-DC Efficiency vs. Output Current

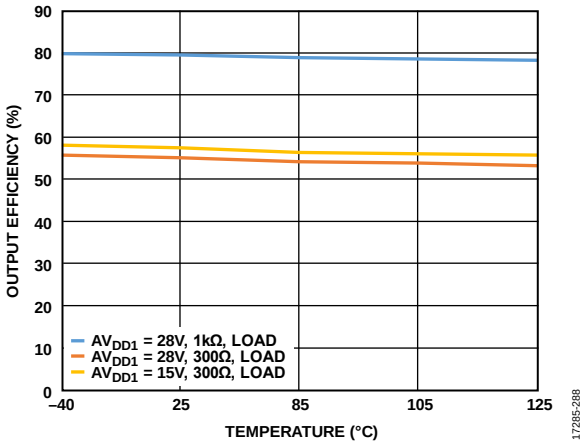


Figure 60. Output Efficiency vs. Temperature

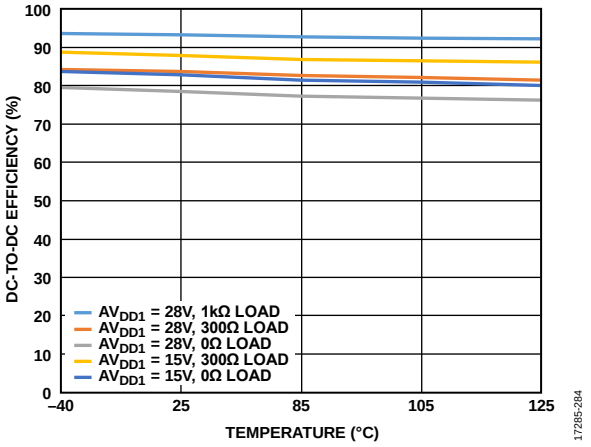


Figure 58. DC-to-DC Efficiency vs. Temperature

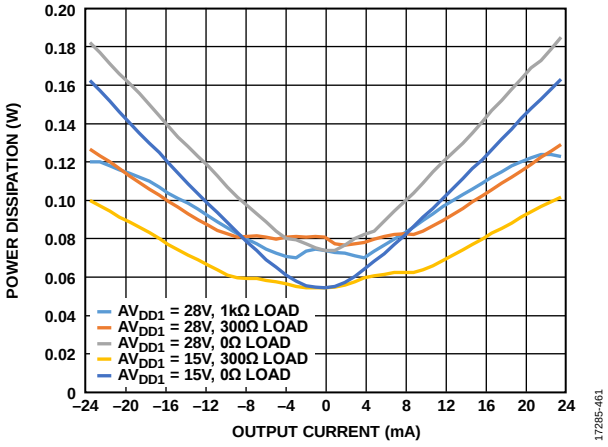


Figure 61. Power Dissipation vs. Output Current

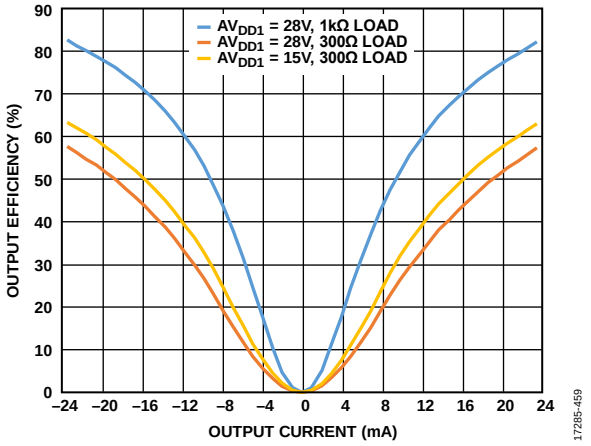


Figure 59. Output Efficiency vs. Output Current

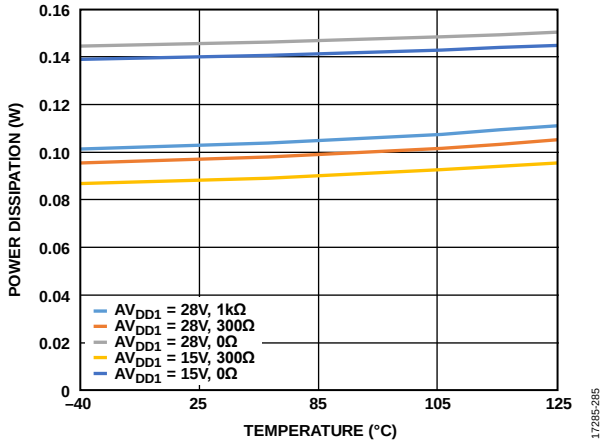


Figure 62. Power Dissipation vs. Temperature

REFERENCE

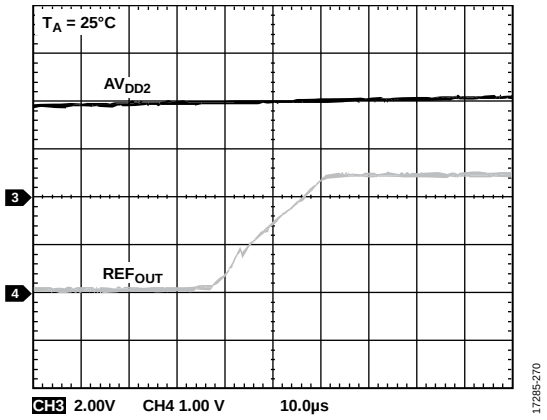


Figure 63. REFOUT Turn On Transient

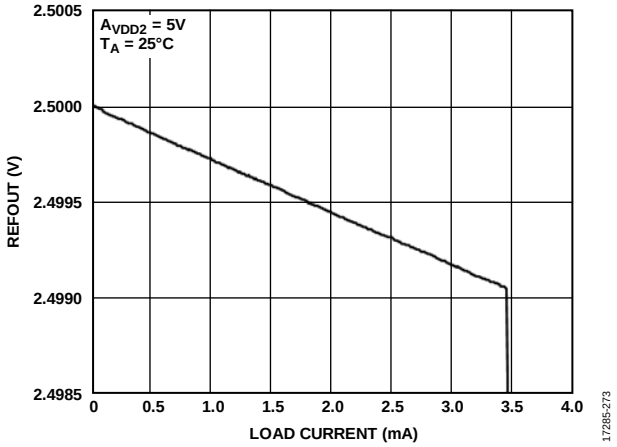


Figure 66. REFOUT vs. Load Current

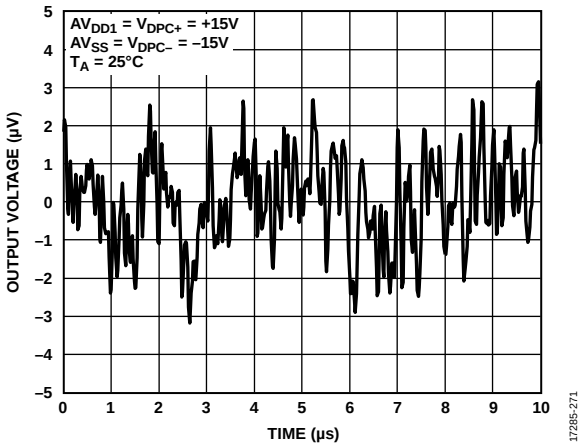


Figure 64. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

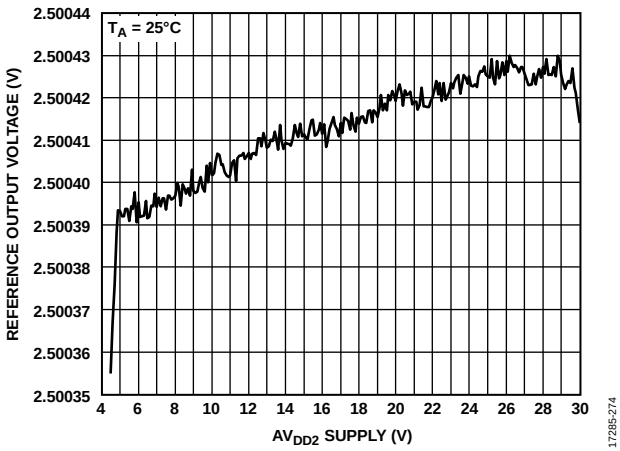


Figure 67. Reference Output Voltage vs. AV_{DD2} Supply

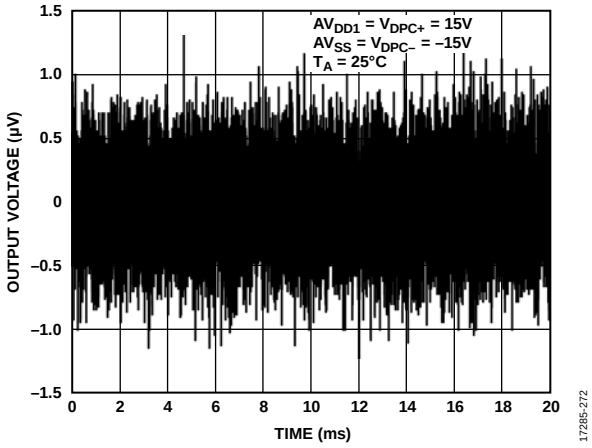


Figure 65. Peak-to-Peak Noise (100 kHz Bandwidth)

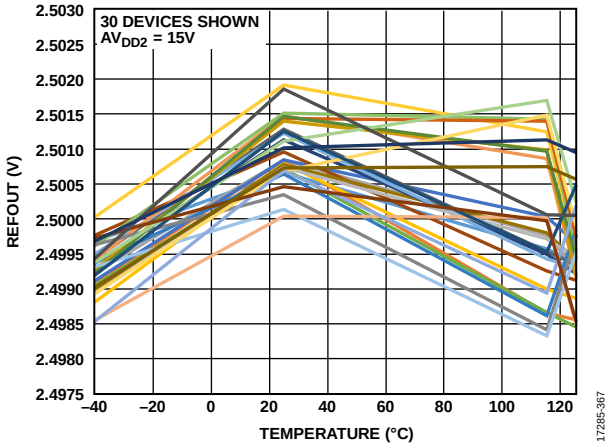


Figure 68. REFOUT vs. Temperature

GENERAL

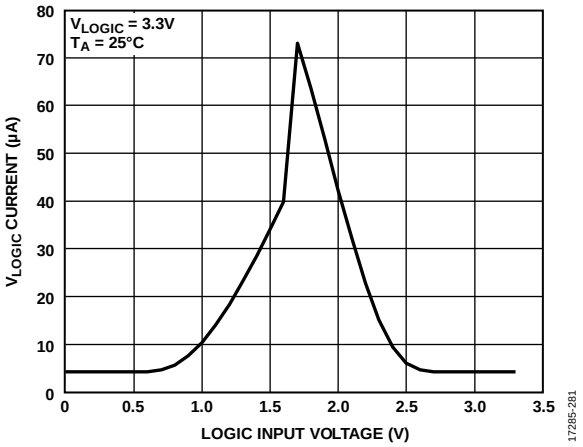


Figure 69. V_{LOGIC} Current vs. Logic Input Voltage

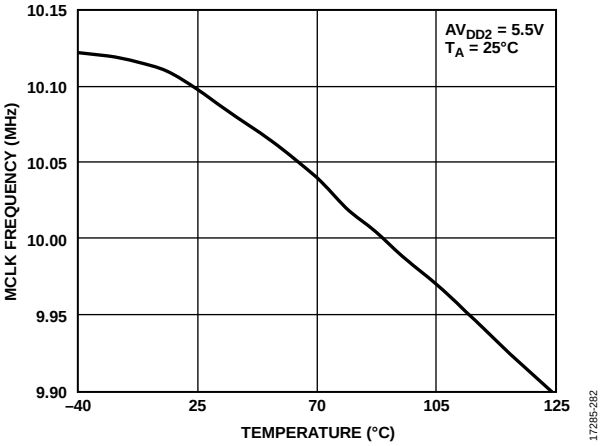


Figure 72. MCLK Frequency vs. Temperature

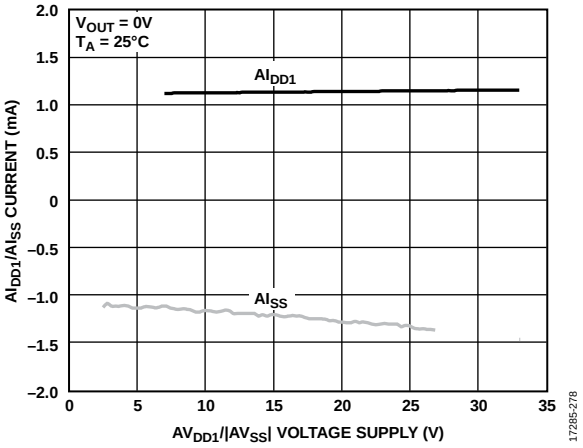


Figure 70. AI_{DD1}/AI_{SS} Current vs. $AV_{DD1}/|AV_{SS}|$ Voltage Supply

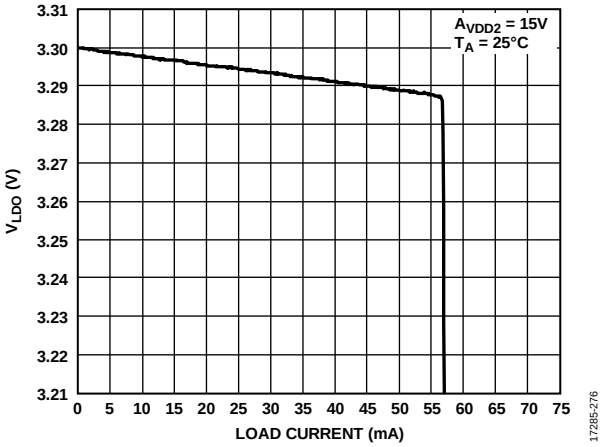


Figure 73. V_{LDO} vs. Load Current

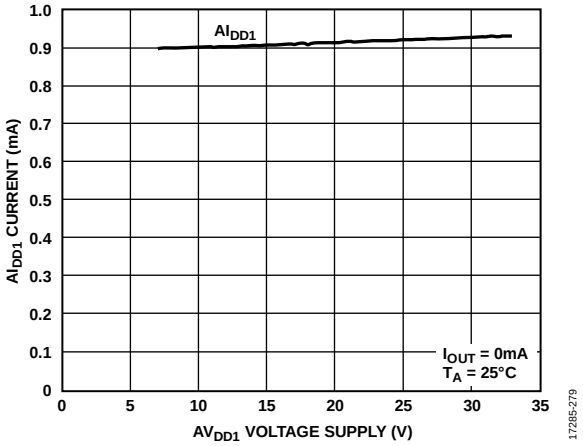


Figure 71. AI_{DD1} Current vs. AV_{DD1} Voltage Supply

TERMINOLOGY

Total Unadjusted Error (TUE)
TUE is a measure of the output error that takes into account various errors, such as INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, also known as INL, is a measure of the maximum deviation, either in LSBs or % FSR, from the best fit line passing through the DAC transfer function.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5753 is monotonic over the full operating temperature range.

Zero-Scale or Negative Full-Scale Error
Zero-scale or negative full-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) is loaded to the DAC output register.

Zero-Scale Temperature Coefficient (TC)
Zero-scale TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC output register is loaded with 0x8000 (straight binary coding).

Bipolar Zero Temperature Coefficient (TC)
Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/°C.

Offset Error
Offset error is the deviation of the analog output from the ideal and is measured using ¼ scale and ¾ scale digital code measurements. It is expressed in % FSR.

Offset Error (TC)
Offset error TC is a measure of the change in the offset error with a change in temperature. It is expressed in ppm FSR/°C.

Gain Error
Gain error is a measure of the span error of the DAC. It is the DAC transfer characteristic slope deviation from the ideal value expressed in % FSR.

Gain Error Temperature Coefficient (TC)
Gain error TC is a measure of the change in gain error with changes in temperature. Gain error TC is expressed in ppm FSR/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC output register. Ideally, the output is full-scale − 1 LSB. Full-scale error is expressed in % FSR.

Headroom
Headroom is the difference between the voltage required at the output, which is the programmed voltage in voltage output mode and the programmed current × R_{LOAD} in current output mode, and the voltage supplied by the positive supply rail, V_{DPC+}. Headroom is relevant when the output is positive with respect to ground.

Footroom
Footroom is the difference between the voltage required at the output, which is the programmed voltage in voltage output mode and the programmed current × R_{LOAD} in current output mode, and the voltage supplied by the negative supply rail, AV_{SS}. Footroom is relevant when the output is negative with respect to ground.

V_{OUT} or $-V_{SENSE}$ Common-Mode Rejection Ratio (CMRR)
V_{OUT} or $-V_{SENSE}$ CMRR is the error in the V_{OUT} voltage that occurs due to changes in the $-V_{SENSE}$ voltage.

Current Loop Compliance Voltage
Current loop compliance voltage is the maximum voltage at the VI_{OUT} pin for which the output current is equal to the programmed value.

Voltage Reference Thermal Hysteresis

Voltage reference thermal hysteresis is the difference in output voltage measured at +25°C compared to the output voltage measured at +25°C after cycling the temperature from +25°C to −40°C to +115°C and then back to +25°C.

Voltage Reference TC
Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated by using the box method. This method defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C and is as follows:

$$TC = \left(\frac{V_{REF_MAX} - V_{REF_MIN}}{V_{REF_NOM} \times Temp\ Range} \right) \times 10^6$$

where:
V_{REF_MAX} is the maximum reference output measured over the total temperature range.
V_{REF_MIN} is the minimum reference output measured over the total temperature range.
V_{REF_NOM} is the nominal reference output voltage, 2.5 V.
Temp Range is the specified temperature range, −40°C to +115°C.

Line Regulation
Line regulation is the change in reference output voltage due to a specified change in power supply voltage. It is expressed in ppm/V.

Load Regulation
Load regulation is the change in reference output voltage due to a specified change in reference load current. It is expressed in ppm/mA.

Dynamic Power Control (DPC)
In DPC mode, the AD5753 circuitry senses the output voltage and dynamically regulates the supply voltage, V_{DPC+}, to meet compliance requirements plus an optimized headroom voltage for the output buffer.

Programmable Power Control (PPC)
In PPC mode, the V_{DPC+} voltage is user programmable to a fixed level that must accommodate the required maximum output load.

Output Voltage Settling Time
Output voltage settling time is the amount of time the output takes to settle to a specified level for a full-scale input change. This specification depends on the manner in which the DPC feature is configured, such as enabled, disabled, or PPC mode enabled, and on the characteristics of the external dc-to-dc inductor and capacitor components used.

Slew Rate
The device slew rate is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage output DAC is usually limited by the slew rate of the amplifier used at the output. Slew rate is measured from 10% to 90% of the output signal and is expressed in V/μs.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5753 is powered on. It is specified as the area of the glitch in nV-sec.

Digital-to-Analog Glitch Energy
Digital-to-analog glitch energy is the energy of the impulse injected into the analog output when the input code in the DAC output register changes state. It is normally specified as the area of the glitch in nV-sec. The worst case usually occurs when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

Glitch Impulse Peak Amplitude

Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC output register changes state. It is specified as the amplitude of the glitch in millivolts and the worst case usually occurs when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the DAC analog output from the DAC digital inputs. However, the digital feedthrough is measured when the DAC output is not updated, which occurs when the $\overline{\text{LDAC}}$ pin is held high. The digital feedthrough is specified in nV-sec and measured with a full-scale code change on the data bus.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

THEORY OF OPERATION

The AD5753 is a single-channel, precision voltage and current output DAC designed to meet the requirements of industrial factory automation and process control applications. The device provides a high precision, fully integrated, single-chip solution for generating a unipolar, bipolar current, or voltage output. Package power dissipation is minimized by incorporating on-chip DPC and then regulating the supply voltage, V_{DPC+} and V_{DPC-}, to the VI_{OUT} output driver from ±4.95 V to ±27 V by using complementary buck dc-to-dc converters optimized for minimum on-chip power dissipation. The AD5753 consists of a two die solution with the dc-to-dc converter circuitry and the VI_{OUT} line protector located on the dc-to-dc die. The remaining circuitry is on the main die. Interdie communication is performed over an internal 3-wire interface.

DAC ARCHITECTURE

The DAC core architecture of the AD5753 consists of a voltage mode R-2R DAC ladder network. The voltage output of the DAC core is converted to either a current or voltage output at the VI_{OUT} pin. Only one mode can be enabled at any one time. Both the voltage and current output stages are supplied by the V_{DPC+} power rail, which is internally generated from AV_{DD1}, and the V_{DPC-} power rail, which is internally generated from AV_{SS}.

Current Output Mode

If current output mode is enabled, the voltage output from the DAC is converted to a current (see Figure 74), which is then mirrored to the supply rail so that the application only sees a current source output.

The available current ranges are 0 mA to 20 mA, 0 mA to 24 mA, 4 mA to 20 mA, ±20 mA, ±24 mA, and −1 mA to +22 mA. An internal or external 13.7 kΩ R_{SET} resistor can be used for the voltage to current conversion.

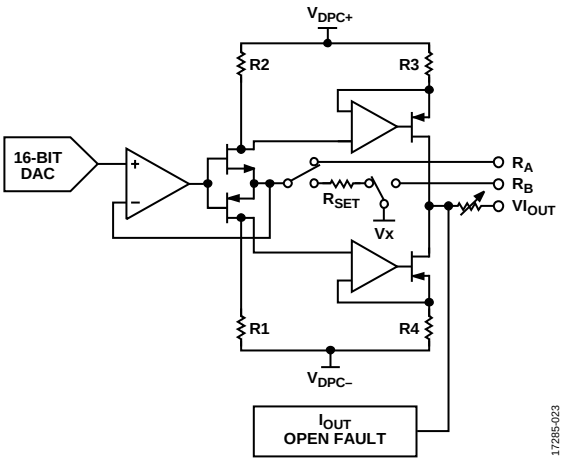


Figure 74. Voltage to Current Conversion Circuitry

Voltage Output Mode

If voltage output mode is enabled, the voltage output from the DAC is buffered and scaled to output a software selectable unipolar or bipolar voltage range (see Figure 75).

The available voltage ranges are 0 V to 5 V, ±5 V, 0 V to 10 V, and ±10 V. A 20% overrange feature is also available via the DAC_CONFIG register, as well as the function to negatively offset the unipolar voltage ranges via the GP_CONFIG1 register (see the General-Purpose Configuration 1 Register section).

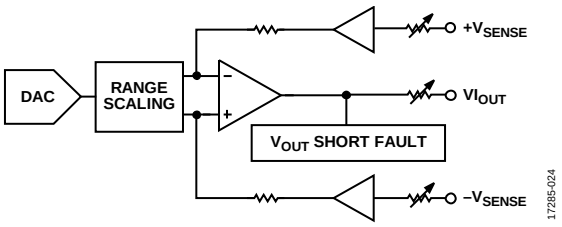


Figure 75. Voltage Output

Reference

The AD5753 can operate either with an external or internal reference. The reference input requires a 2.5 V reference for specified performance. This input voltage is then internally buffered before being applied to the DAC.

The AD5753 contains an integrated buffered 2.5 V voltage reference that is externally available for use elsewhere within the system. The internal reference drives the integrated 12-bit ADC. REFOUT must be connected to REFIN to use the internal reference to drive the DAC.

SERIAL INTERFACE

The AD5753 is controlled over a versatile 4-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP standards. Data coding is always straight binary.

Input Shift Register

With the SPI CRC enabled (default state), the input shift register is 32 bits wide. Data is loaded to the device MSB first as a 32-bit word under the control of a serial clock input, SCLK. Data is clocked in on the falling edge of SCLK. If the CRC is disabled, the serial interface is reduced to 24 bits. A 32-bit frame is still accepted but the last 8 bits are ignored. See the Register Map section for full details on the registers that can be addressed via the SPI interface.

Table 7. Writing to a Register (CRC Enabled)

MSB				LSB
D31	**[D30:D29]**	**[D28:D24]**	**[D23:D8]**	**[D7:D0]**
Slip Bit	AD5753 address	Register address	Data	CRC

Transfer Function

Table 8 shows the input code to ideal output voltage relationship for the AD5753 for straight binary data coding of the ±5 V output range.

Table 8. Ideal Output Voltage to Input Code Relationship

Digital Input, Straight Binary Data Coding				Analog Output
MSB		LSB		V_{OUT}
1111	1111	1111	1111	$2 \times V_{REF} \times (32{,}767/32{,}768)$
1111	1111	1111	1110	$2 \times V_{REF} \times (32{,}766/32{,}768)$
1000	0000	0000	0000	0 V
0000	0000	0000	0001	$-2 \times V_{REF} \times (32{,}767/32{,}768)$
0000	0000	0000	0000	$-2 \times V_{REF}$

POWER-ON STATE OF THE AD5753

On initial power-on or a device reset, the voltage and current output channel is disabled. The switch connecting the VI_{OUT} via a 30 kΩ pull-down resistor to AGND is open. This switch can be configured in the DCDC_CONFIG2 register. V_{DPC+} and V_{DPC-} are internally driven to ±4.8 V upon power-on, until the dc-to-dc converters are enabled.

After device power-on or a device reset, a calibration memory refresh command is required (see the Programming Sequence to Enable the Output section). It is recommended to wait 500 µs at minimum after writing this command before writing further instructions to the device to allow time for internal calibrations to take place.

Power-On Reset

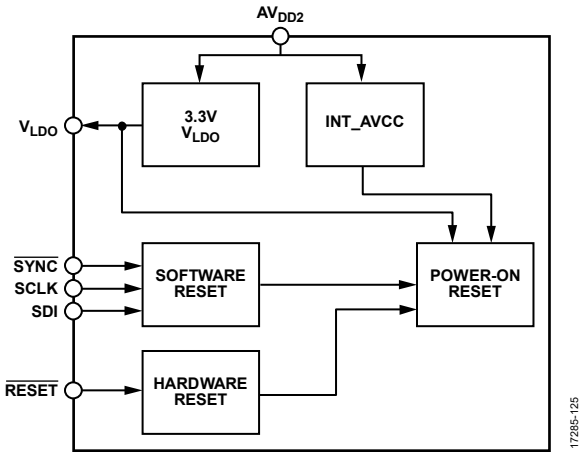


Figure 76. Power-On Reset Block Diagram

The AD5753 incorporates a power-on reset circuit that ensures the AD5753 is held in reset if the power supplies are insufficient enough to allow reliable operation. The power-on reset circuit (see Figure 76) monitors the AV_{DD2} generated V_{LDO}, the INT_AVCC voltages, the $\overline{RESET}$ pin, and the SPI reset signal. The power-on reset circuit keeps the AD5753 in reset until the voltages on the V_{LDO} and an internal AV_{CC} voltage node (INT_AVCC) are sufficient for reliable operation. The AD5753 is reset if the power-on circuit receives a signal from the $\overline{RESET}$ pin or if a software reset is written to the AD5753 via the SPI interface. Do not write SPI commands to the device within 100 µs of a reset event.

POWER SUPPLY CONSIDERATIONS

The AD5753 has the following four supply rails: AV_{DD1}, AV_{DD2}, AV_{SS}, and V_{LOGIC}. See Table 1 for the voltage range of the four supply rails and the associated conditions.

AV_{DD1} Considerations

AV_{DD1} is the supply rail for the positive dc-to-dc converter and can range from 7 V to 33 V. Although the maximum value of AV_{DD1} is 33 V and the minimum value of AV_{SS} is −33 V, the maximum operating range of $|AV_{DD1}$ to $AV_{SS}|$ is 60 V. V_{DPC+} is derived from AV_{DD1} and the value depends on the dc-to-dc converter mode of operation

The dc-to-dc converter requires a sufficient level of margin to be maintained between AV_{DD1} and V_{DPC+} to ensure the dc-to-dc circuitry operates correctly. This margin is 5% of the maximum V_{DPC+} voltage for a given mode of operation.

Table 9. AV_{DD1} to V_{DPC+} Margin

Mode of Operation	V_{DPC+} Maximum
DPC Voltage Mode	15 V
DPC Current Mode	(I_{OUT} maximum × R_{LOAD}) + I_{OUT} headroom
PPC Current Mode	DCDC_CONFIG1[4:0] programmed value

See the Power Dissipation Control section for further details on the dc-to-dc converter modes of operation.

Calculating Supply Voltage

Assuming DPC current mode, use the following equation to calculate the supply voltage:

$$V_{DPC+} \text{ maximum} = I_{OUT} \text{ maximum voltage} + I_{OUT} \text{ headroom} = 22.5 \text{ V}$$

where:

I_{OUT} *maximum* = *20 mA*; R_{LOAD} = 1 kΩ

I_{OUT} *maximum voltage* = I_{OUT} *maximum* × R_{LOAD} = 20 V

I_{OUT} *headroom* = 2.5 V

$|V_{DPC+}$ to $AV_{DD1}|$ headroom is calculated as 5% of 22.5 V = 1.125 V. Therefore, AV_{DD1} (minimum) = 22.5 V + 1.125 V = 23.625 V. Assuming a worst case AV_{DD1} supply rail tolerance of ±10%, this example requires an AV_{DD1} supply rail of approximately 26 V.

AV_{SS} Considerations

AV_{SS} is the negative supply rail and has a range of −33 V to 0 V. As in the case of AV_{DD1}, AV_{SS} must obey the 60 V maximum operating range of $|AV_{DD1}$ to $AV_{SS}|$. V_{DPC-} is derived from AV_{SS} and the value depends on the dc-to-dc converter mode of operation. The dc-to-dc converter requires a sufficient level of margin between AV_{SS} and V_{DPC-} to ensure the dc-to-dc circuitry operates correctly. This margin is 5% of the maximum $|V_{DPC-}|$ voltage for a given mode of operation.

Calculating Supply Voltage

Assuming DPC current mode, use the following equation to calculate the supply voltage:

V_{DPC-} *minimum* = I_{OUT} *minimum voltage* + I_{OUT} *headroom* = −22.5 V

where:

I_{OUT} *minimum* = −20 mA; R_{LOAD} = −20 V

I_{OUT} *minimum voltage* = I_{OUT} *minimum* × R_{LOAD} = −20 V

I_{OUT} *headroom* = −2.5 V

The |V_{DPC-} to AV_{SS}| headroom is calculated as 5% of −22.5 V = −1.125 V. Therefore, AV_{SS} (minimum) = −22.5 V − 1.125 V = −23.625 V. Assuming a worst case AV_{SS} supply rail tolerance of ±10%, this example requires an AV_{SS} supply rail of approximately −26 V.

For unipolar current output ranges, with negative rail DPC disabled, AV_{SS} can be tied to AGND (0 V) and can be connected V_{DPC-} to AV_{SS}. For unipolar voltage output ranges, the maximum AV_{SS} is −2 V to enable sufficient footroom for the internal voltage output circuitry. If negative rail DPC is disabled, connect V_{DPC-} to AV_{SS}. To avoid power supply sequencing issues, a Schottky diode must be placed between V_{DPC-} and ground and the ground supply must always be available.

AV_{DD2} Considerations

AV_{DD2} is the positive low voltage supply rail and has a range of 5 V to 33 V. If only one positive power rail is available, AV_{DD2} can be tied to AV_{DD1}. However, to optimize for reduced power dissipation, supply AV_{DD2} with a separate lower voltage supply.

V_{LOGIC} Considerations

V_{LOGIC} is the digital supply for the device and ranges from 1.71 V to 5.5 V. The 3.3 V V_{LDO} output voltage can be used to drive V_{LOGIC}.

DEVICE FEATURES AND DIAGNOSTICS

POWER DISSIPATION CONTROL

The AD5753 contains integrated buck dc-to-dc converter circuitry that controls the positive and negative (V_{DPC+} and V_{DPC-}) power supply to the output buffers. The converter reduces power consumption from standard designs when using the device in both current and voltage output modes. AV_{DD1} is the supply rail for the dc-to-dc converter and ranges from 7 V to 33 V. V_{DPC+} is also derived from this supply rail. AV_{SS} is the supply rail for the negative rail dc-to-dc converter and ranges from −33 V to 0 V. V_{DPC-} is also derived from this supply rail. The value of both the V_{DPC+} and V_{DPC-} rails depends on the dc-to-dc converter mode of operation as well as the output load, DPC voltage mode, DPC current mode, and PPC current mode.

Figure 77 shows the discrete components needed for the positive dc-to-dc circuitry and Figure 78 shows the components needed for the negative dc-to-dc circuitry. The following sections describe how to select components and circuitry operation. Use the same circuitry on the negative AV_{SS} rail if the negative DPC mode is in use, such as if DCDC_CONFIG2 Bit 1 = 1. If the negative DPC is not in use, tie V_{DPC-} to AV_{SS}.

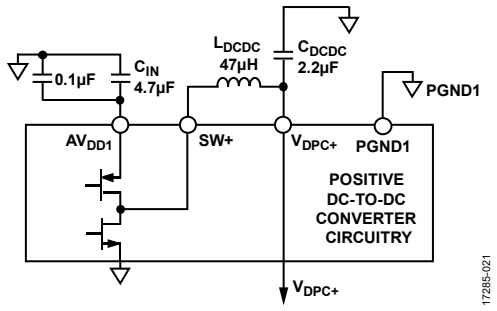


Figure 77. Positive DC-to-DC Circuit

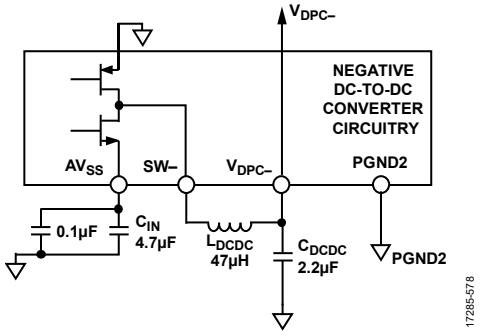


Figure 78. Negative DC-to-DC Circuit

Table 10. Recommended DC-to-DC Components

Symbol	Component	Value	Manufacturer
L_{DCDC}	PA6594-AE	47 µH	Coilcraft
C_{DCDC}	GCM31CR71H225KA55L	2.2 µF	Murata
C_{IN}	GRM31CR71H475KA12L	4.7 µF	Murata

DC-to-DC Converter Operation

The dc-to-dc converter uses a fixed, 500 kHz frequency, peak current mode control scheme to step down the AV_{DD1} and AV_{SS} inputs to produce V_{DPC+} and V_{DPC-} to supply the driver circuitry of the voltage or current output channel. The dc-to-dc converters incorporate a low-side synchronous switch and, therefore, do not require an external Schottky diode. The dc-to-dc converters operate predominantly in discontinuous conduction mode (DCM), where the inductor current goes to zero for an appreciable percentage of the switching cycle. To avoid generating lower frequency harmonics on the V_{DPC+} and V_{DPC-} regulated output voltage rails, the dc-to-dc converters do not skip any cycles. The dc-to-dc converters must therefore transfer a minimum amount of energy to the load, that is, the current or voltage output stage and the respective load, to operate at a fixed frequency. Thus, for light loads, such as a low R_{LOAD} or low I_{OUT}, the V_{DPC+} and V_{DPC-} voltage can rise beyond the target value and stop regulating. This voltage rise is not a fault condition and does not represent the worst case power dissipation condition in an application.

The dc-to-dc converter requires a sufficient level of margin between AV_{DD1} and V_{DPC+}, and between AV_{SS} and V_{DPC-} to ensure that the dc-to-dc circuitry operates correctly. This margin value is 5% of the $V_{DPC+}/|V_{DPC-}|$ maximum.

DPC Voltage Mode

In DPC voltage mode, with the voltage output enabled or disabled, the converter regulates the V_{DPC+} supply to 15 V above the $-V_{SENSE}$ voltage and regulates the V_{DPC-} supply to 15 V below the $-V_{SENSE}$ voltage. This mode allows the full output voltage range to be efficiently applied across remote loads, with corresponding remote grounds at up to ±10 V potential relative to the local ground supply (AGND) for the AD5753.

DPC Current Mode

In standard current input module designs, the combined line and load resistance values typically range from 50 Ω to 750 Ω. Output module systems must provide enough voltage to meet the compliance voltage requirement across the full range of load resistor values. For example, in a 4 mA to 20 mA loop, when driving 20 mA to a 750 Ω load, a compliance voltage of >15 V is required. When driving 20 mA into a 50 Ω load, the required compliance is reduced to >1 V.

In DPC current mode, the AD5753 dc-to-dc circuitry senses the output voltage and regulates the V_{DPC+} and V_{DPC-} supply voltage to meet compliance requirements as well as an optimized headroom voltage for the output buffer. V_{DPC+} is dynamically regulated to 4.95 V or $I_{OUT} \times R_{LOAD}$ + headroom, or whichever voltage is greater, which excludes the light load condition whereby the V_{DPC+} voltage can rise beyond the target value. This same analysis applies to V_{DPC-}, except with the opposite polarity. As previously noted, the exclusion of the light load does not represent the worst case power dissipation condition in an application. The

AD5753 is capable of driving up to 24 mA through a 1 kΩ load for a given input supply (24 V + headroom).

At low output power levels, the regulated headroom increases above 2.3 V due to the fact that the dc-to-dc circuitry uses a minimum on time duty cycle. This behavior is expected and does not impact any worse case power dissipation.

PPC Current Mode

The dc-to-dc converter can also operate in programmable power control mode, where the V_{DPC+} and V_{DPC-} voltages are user programmable to a given level to accommodate the required maximum output load. This mode represents a trade-off between the optimized power efficiency of the DPC current mode and the system settling time with a fixed supply and dc-to-dc disabled. In PPC current mode, V_{DPC+} and V_{DPC-} are regulated to a user programmable level between +5 V and +25.677 V (V_{DPC+}) and −5 V and −25.677 V (V_{DPC-}), with respect to $-V_{SENSE}$ in steps of 0.667 V. This mode is useful if settling time is an important requirement of the design. See the DC-to-DC Converter Settling Time section for information on settling time. If the load is nonlinear in nature, take care in selecting the programmed level of V_{DPC+} and V_{DPC-}. V_{DPC+} and V_{DPC-} must be set high enough to obey the output compliance voltage specification. If the load is unknown, use the external $+V_{SENSE}$ input to the ADC to monitor the VI_{OUT} pin in current mode to determine the user programmable value at which to set V_{DPC+}.

DC-to-DC Converter Settling Time

When in DPC current mode, the settling time is dominated by the dc-to-dc converter settling time and is typically 200 µs without the digital slew rate control feature enabled. To reduce initial VI_{OUT} waveform overshoot without adding a capacitor on VI_{OUT} and thereby affecting HART operation, enable the digital slew rate control feature by using the DAC_CONFIG register (see Table 33 for bit descriptions).

Table 11 shows the typical settling time for each dc-to-dc converter mode. All values shown assume the component uses recommended by Analog Devices, Inc. (see in Table 10). The achievable settling time in any given application is dependent on the choice of external inductor and capacitor components, as well as the dc-to-dc converter current-limit setting.

Table 11. Settling Time vs. DC-to-DC Converter Mode

DC-to-DC Converter Mode	Settling Time (µs)
DPC Current Mode	200
PPC Current Mode	15
DPC Voltage Mode	15

DC-to-DC Converter Inductor Selection

For typical 4 mA to 20 mA applications, a 47 µH inductor (shown in Table 10), combined with the 500 kHz switching frequency, drives up to 24 mA into a load resistance of up to 1 kΩ with a greater than 24 V + headroom AV_{DD1} supply. It is important to ensure that the peak current does not cause the inductor to saturate, especially at the maximum ambient temperature. If the inductor enters saturation mode, a decrease in efficiency results. Larger size inductors translate to lower core losses. The slew rate control feature of the AD5753 can limit peak currents during slewing. Program an appropriate current limit via the DCDC_CONFIG2 register to shut off the internal switch if the inductor current reaches that limit.

DC-to-DC Converter Input and Output Capacitor Selection

The output capacitor, C_{DCDC}, affects the ripple voltage of the dc-to-dc converter and limits the maximum slew rate at which the output current can rise. The ripple voltage is directly related to the output capacitance. The C_{DCDC} capacitor recommended by Analog Devices (see Table 10), combined with the recommended 47 µH inductor, results in a 500 kHz ripple with an amplitude less than 50 mV and a guaranteed stability and operation with HART capability across all operating modes.

For high voltage capacitors, the capacitor size is often an indication of the charge storage ability. It is important to characterize the dc bias voltage vs. the capacitance curve for this capacitor. Any specified capacitance values reference a dc bias corresponding to the maximum V_{DPC+} and V_{DPC-} voltage in the application. The capacitor temperature range, as well as the voltage rating, must be considered for a given application. These considerations are key when selecting the components described in Table 10.

The input capacitor, C_{IN}, provides much of the dynamic current required for the dc-to-dc converter (see Table 10 for details), and a low effective series resistance (ESR) component is recommended as the input capacitor. For the AD5753, it is recommended to use a low ESR tantalum or ceramic capacitor of 4.7 µF (1206 size) in parallel with a 0.1 µF (0402 size) capacitor. Ceramic capacitors must be chosen carefully because they can exhibit an increased sensitivity to dc bias voltages and temperature. X5R or X7R dielectrics are preferred because these capacitors remain stable over wider operating voltage and temperature ranges. Take care if selecting a tantalum capacitor to ensure a low ESR value.

CLKOUT

The AD5753 provides a CLKOUT signal to the system for synchronization purposes. This signal is programmable to eight frequency options between 416 kHz and 588 kHz with the default option being 500 kHz, the same switching frequency of the dc-to-dc converter. This feature is configured in the GP_CONFIG1 register and is disabled by default

INTERDIE 3-WIRE INTERFACE

A 3-wire interface facilitates communication between the two die in the AD5753. The 3-wire interface master is located on the main die and the 3-wire interface slave is on the dc-to-dc die. The three interface signals are data, DCLK (running at MCLK/8), and interrupt.

The main purpose of the 3-wire interface is to read from or write to the DCDC_CONFIG1 and DCDC_CONFIG2 registers. Addressing these registers via the SPI interface initiates an internal 3-wire interface transfer from the main die to the dc-to-dc die. The

3-wire interface master on the main die initiates writes and reads to and from the registers on the dc-to-dc die using DCLK as the serial clock. The slave uses an interrupt signal to the dc-to-dc die to indicate that a read of the dc-to-dc die internal status register is required.

For every 3-wire interface write, an automatic read and compare process can be enabled (default case) to ensure that the contents of the copy of the main die DCDC_CONFIGx registers match the contents of the registers on the dc-to-dc die. This comparison is performed to ensure the integrity of the digital circuitry on the dc-to-dc die. With this feature enabled, a 3-wire interface (3WI) transfer takes approximately 300 µs. When disabled, this transfer time reduces to 30 µs.

The BUSY_3WI flag in the DCDC_CONFIG2 register is asserted during the 3-wire interface transaction. The BUSY_3WI flag is also set when the user updates the DAC range via the range bits (Bits[3:0]) in the DAC_CONFIG register due to the internal calibration memory refresh caused by this action, which requires a 3-wire interface transfer between the two die. A write to either of the DCDC_CONFIGx registers must not be initiated while BUSY_3WI is asserted. If a write occurs while BUSY_3WI is asserted, the new write is delayed until the current 3-wire interface transfer completes.

3-Wire Interface Diagnostics

Any faults on the dc-to-dc die trigger an interrupt to the main die and an automatic status read of the dc-to-dc die is performed. After the read transaction, the main die retains a copy of the dc-to-dc die status bits (VIOUT_OV_ERR, DCDC_P_SC_ERR, and DCDC_P_PWR_ERR). These values are available in both the ANALOG_DIAG_RESULTS register, and via the OR'ed analog diagnostic results bits in the status register. These bits also trigger the $\overline{\text{FAULT}}$ pin.

In response to the interrupt request, the main die (master) performs a 3-wire interface read operation to read the dc-to-dc die status. The interrupt is only asserted again by a subsequent dc-to-dc die fault flag, upon which the 3-wire interface initiates another status read transaction. If an interrupt signal is detected six times in a row, the interrupt detection mechanism is disabled until a 3-wire interface write transaction completes. This disabling prevents the 3-wire interface from being blocked because of the constant dc-to-dc die status reads when the interrupt is toggling. The INTR_SAT_3WI flag in the DCDC_CONFIG2 register indicates when this event occurs, and a write to either DCDC_CONFIGx register resets this bit to 0.

During a 3-wire read or write operation, the address and data bits in the transaction produce parity bits. These parity bits are checked on the receive side and if the bits do not match on both die, the ERR_3WI bit in the DIGITAL_DIAG_RESULTS register is set. If the read and compare process is enabled and a parity error occurs, the 3WI_RC_ERR bit in the DIGITAL_DIAG_ RESULTS register is also set.

VOLTAGE OUTPUT

Voltage Output Amplifier and $\pm V_{SENSE}$ Functionality

The voltage output amplifier is capable of generating both unipolar and bipolar output voltages. The amplifier is also capable of driving a 1 kΩ load in parallel with 2 µF with an external compensation capacitor to AGND. Figure 79 shows the voltage output driving a load, R_{LOAD}, on top of a common-mode voltage (V_{CM}) of ±10 V. An integrated 2 MΩ resistor ensures that the amplifier loop is kept closed and prevents potentially large and destructive voltages on the VI_{OUT} due to the broken amplifier loop in applications where a cable may become disconnected from $+V_{SENSE}$. If remote sensing of the load is not required, connect $+V_{SENSE}$ directly to VI_{OUT} and connect $-V_{SENSE}$ directly to AGND via 1 kΩ series resistors.

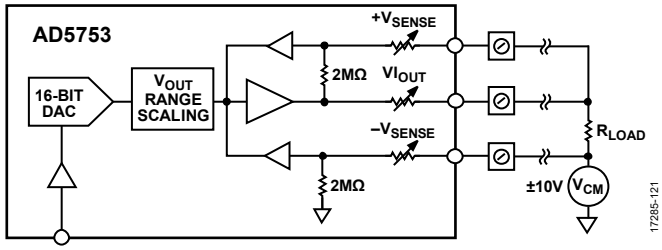


Figure 79. Voltage Output

Driving Large Capacitive Loads

The voltage output amplifier is capable of driving capacitive loads of up to 2 µF with the addition of a 220 pF nonpolarized compensation capacitor. This capacitor, though allowing the AD5753 to drive higher capacitive loads and reduce overshoot, increases the device settling time and, therefore, negatively affects the bandwidth of the system. Without the compensation capacitor, capacitive loads of up to 10 nF can be driven.

Voltage Output Short-Circuit Protection

Under normal operation, the voltage output sinks and sources up to 12 mA and maintains specified operation. The short-circuit current is typically 16 mA. If a short circuit is detected, the $\overline{\text{FAULT}}$ pin goes low and the VOUT_SC_ERR bit in the ANALOG_DIAG_RESULTS register is set.

FAULT PROTECTION

The AD5753 incorporates a line protector on the VI_{OUT} pin, the $+V_{SENSE}$ and $-V_{SENSE}$ pins. The line protector operates by clamping the voltage internal to the line protector to the V_{DPC+} and V_{DPC-} rails, thus protecting the internal circuitry from external voltage faults. If a voltage outside of these limits is detected on the VI_{OUT} pin, an error flag (VIOUT_OV_ERR) located in the ANALOG_DIAG_RESULTS register is set.

CURRENT OUTPUT

External Current Setting Resistor

As shown in Figure 74, R_{SET} is an internal sense resistor that forms part of the voltage to current conversion circuitry. The stability of the output current value over temperature is dependent on the stability of the R_{SET} value. To improve the output current over temperature stability, connect an external 13.7 kΩ, low drift resistor, instead of the internal resistor, between the R_A and R_B pins of the AD5753.

Table 1 shows the AD5753 performance specifications with both the internal R_{SET} resistor and an external 13.7 kΩ R_{SET} resistor. The external R_{SET} resistor specification assumes an ideal resistor. The actual performance depends on the absolute value and temperature coefficient of the resistor used. Therefore, the resistor specifications directly affect the gain error of the output and the TUE.

To arrive at the absolute worst case overall TUE of the output with a particular external R_{SET} resistor, add the percentage of the R_{SET} resistor absolute error (the absolute value of the error) to the TUE of the AD5753 that is using the external R_{SET} resistor shown in Table 1 (expressed in % FSR). Consider the temperature coefficient as well as the specifications of the external reference, if this is the option being used in the system.

The magnitude of the error, derived from summing the absolute error and TC error of the external R_{SET} resistor and external reference with the AD5753 TUE specification, is unlikely to occur because the TC values of the individual components are unlikely to exhibit the same drift polarity and, therefore, an element of cancelation occurs. For this reason, add the TC values with a root of squares method. A further improvement of the TUE specification is gained by performing a two point calibration at zero scale and full scale, thus reducing the absolute errors of the voltage reference and the R_{SET} resistor.

Current Output Open-Circuit Detection

When in current output mode, if the available headroom falls below the compliance range due to an open-loop circuit or an insufficient power supply voltage, the IOUT_OC_ERR flag in the ANALOG_DIAG_RESULTS register is asserted and the $\overline{\text{FAULT}}$ pin goes low.

HART CONNECTIVITY

The AD5753 has a C_{HART} pin onto which a HART signal can be coupled. The HART signal appears on the current output if the HART_EN bit in the GP_CONFIG1 register as well as the VI_{OUT} output is enabled.

Figure 80 shows the recommended circuit for attenuating and coupling the HART signal into the AD5753. To achieve 1 mA p-p at the VI_{OUT} pin, a signal of approximately 125 mV p-p is required at the C_{HART} pin. The HART signal on the VI_{OUT} pin is inverted relative to the signal input at the C_{HART} pin.

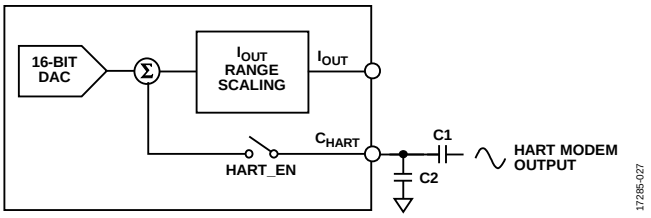


Figure 80. Coupling the HART Signal

As well as their use in attenuating the incoming HART modem signal, a minimum capacitance of the C1 and C2 capacitors is required to ensure the bandwidth presented to the modem output signal allows the 1.2 kHz and 2.2 kHz frequencies through the capacitor. Assuming a HART signal of 500 mV p-p, the recommended values are C1 = 47 nF and C2 = 150 nF. Digitally controlling the output slew rate is necessary to meet the analog rate of change requirements for HART.

If the HART feature is not required, disable the HART_EN bit and leave the C_{HART} pin open circuit. However, if the DAC output signal must be slowed with a capacitor, the HART_EN bit must be enabled and the required C_{SLEW} capacitor must be connected to the C_{HART} pin.

DIGITAL SLEW RATE CONTROL

The AD5753 slew rate control feature allows the user to control the rate at which the output value changes. This feature is available in both current and voltage mode. Disabling the slew rate control feature changes the output value at a rate limited by the output drive circuitry and the attached load. To reduce the slew rate, enable the slew rate control feature. Enabling this feature causes the output to digitally step from one output code to the next at a rate defined by two parameters accessible via the DAC_CONFIG register. These two parameters are SR_CLOCK and SR_STEP. SR_CLOCK and SR_STEP define the rate at which the digital slew is updated. For example, if the selected update rate is 8 kHz, the output updates every 125 µs. In conjunction with SR_CLOCK, SR_STEP defines by how much the output value changes at each update. Together, both parameters define the rate of change of the output value.

The following equation describes the slew rate as a function of the step size, the slew rate frequency, and the LSB size:

$$Slew\ Time = \frac{Output\ Change}{Step\ Size \times Slew\ Rate\ Frequency \times LSB\ Size}$$

where:
Slew Time is expressed in seconds.
Step Size is the change in output.
Output Change is expressed in amps for current output mode or volts for voltage output mode.
Slew Rate Frequency is SR_CLOCK.
LSB Size is SR_STEP.

When the slew rate control feature is enabled, all output changes occur at the programmed slew rate. For example, if the WDT times out and an automatic clear occurs, the output slews to the clear value at the programmed slew rate. However, setting the

CLEAR_NOW_EN bit in the GP_CONFIG1 register overrides this default behavior and causes the output to immediately update to the clear code, rather than at the programmed slew rate.

The slew rate frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range.

ADDRESS PINS

The AD5753 address pins (AD0 and AD1) are used in conjunction with the address bits within the SPI frame (see Table 12) to determine which AD5753 device is being addressed by the system controller. With the two address pins, up to four devices can be independently addressed on one board.

SPI Interface and Diagnostics

The AD5753 is controlled over a 4-wire serial interface with an 8-bit cyclic redundancy check (CRC-8) that is enabled by default. The input shift register is 32 bits wide and data is loaded into the device MSB first under the control of a serial clock input, SCLK. Data is clocked in on the falling edge of SCLK. If CRC is disabled, the serial interface is reduced to 24 bits. A 32-bit frame is still accepted but the last 8 bits are ignored.

Table 12. Writing to a Register (CRC Enabled)

MSB				LSB
D31	**[D30:D29]**	**[D28:D24]**	**[D23:D8]**	**[D7:D0]**
Slip Bit	AD5753 address	Register address	Data	CRC

As shown in Table 12, every SPI frame contains two address bits. These bits must match the AD0 and AD1 pins for a particular device to accept the SPI frame on the bus.

SPI Cyclic Redundancy Check

To verify that data is correctly received in noisy environments, the AD5753 offers a CRC based on a CRC-8. The device, either a micro or a field-programmable gate array (FPGA), controlling the AD5753 generates an 8-bit frame check sequence by using the following polynomial:

$$C(x) = x^8 + x^2 + x^1 + 1$$

This 8-bit frame check sequence is added to the end of the data-word and 32 bits are sent to the AD5753 before taking $\overline{\text{SYNC}}$ high.

If the SPI_CRC_EN bit is set high (default state), the user must supply a frame that is exactly 32 bits wide that contains the 24 data bits and the 8-bit CRC. If the CRC check is valid, the data is written to the selected register. If the CRC check fails, the data is ignored, the $\overline{\text{FAULT}}$ pin goes low, and the $\overline{\text{FAULT}}$ pin status bit and digital diagnostic status bit (DIG_DIAG_STATUS) in the status register are asserted. A subsequent readback of the DIGITAL_DIAG_RESULTS register shows that the SPI_CRC_ERR bit is also set. This register is per individual bits, a write one per bit clears the register (see the Sticky Diagnostic Results Bits section for more details). Therefore, the SPI_CRC_ERR bit is cleared by writing a 1 to Bit D0 of the DIGITAL_DIAG_RESULTS register. Writing a 1 clears the SPI_CRC_ERR bit and causes the $\overline{\text{FAULT}}$ pin to return high, assuming that there are no other active faults. When configuring the FAULT_PIN_CONFIG register, the user decides whether the SPI CRC error affects the $\overline{\text{FAULT}}$ pin. See the $\overline{\text{FAULT}}$ Pin Configuration Register section for further details. The SPI CRC feature is used for both transmitting and receiving data packets.

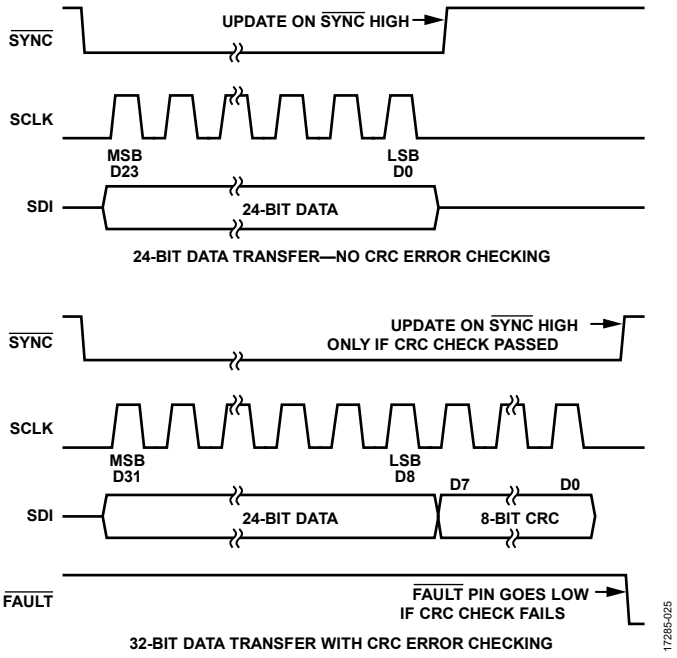


Figure 81. CRC Timing (Assume $\overline{\text{LDAC}}$ = 0)

SPI Interface Slip Bit

Adding the slip bit enhances the interface robustness. The MSB of the SPI frame must equal the inverse of MSB − 1 for the frame to be considered valid. If an incorrect slip bit is detected, the data is ignored and the SLIPBIT_ERROR bit in the DIGITAL_DIAG_RESULTS register is asserted.

SPI Interface SCLK Count Feature

An SCLK count feature is also built into the SPI diagnostics, meaning that only SPI frames with exactly 32 SCLK falling edges (24 if SPI CRC is disabled) are accepted by the interface as a valid write. SPI frames lengths other than 32 are ignored and the SCLK_COUNT_ERR flag asserts in the DIGITAL_DIAG_RESULTS register.

Readback Modes

The AD5753 offers the following four readback modes:

- Two-stage readback mode
- Autostatus readback mode
- Shared $\overline{\text{SYNC}}$ autostatus readback mode
- Echo mode

The two-stage readback consists of a write to a dedicated register, TWO_STAGE_READBACK_SELECT, to select the register location to be read back. This write is followed by a no operation (NOP) command during which the contents of the selected register are available on the SDO pin.

Table 13. SDO Contents for Read Operation

MSB				LSB
[D31:D30]	D29	[D28:24]	[D23:D8]	[D7:D0]
0b10	$\overline{\text{FAULT}}$ pin status	Register address	Data	CRC

Bits[D31:D30] = 0b10 are used for synchronization purposes during readback.

If autostatus readback mode is selected, the contents of the status register are available on the SDO line during every SPI transaction. This feature allows the user to continuously monitor the status register and to act quickly if a fault occurs. The AD5753 powers up with this feature disabled. When this feature is enabled, the normal two-stage readback feature is not available. Only the status register is available on SDO. To read back other registers, first disable the automatic readback feature before following the two-stage readback sequence. The automatic status readback can be reenabled after the register is read back.

The shared AD5753 $\overline{\text{SYNC}}$ autostatus readback is a special version of the autostatus readback mode used to avoid SDO bus contention when multiple devices share the same $\overline{\text{SYNC}}$ line.

Echo mode behaves similarly to autostatus readback mode, except that every second readback consists of an echo (a repetition) of the previous command written to the AD5753 (see Figure 82). See the Reading from Registers section for further details on the readback modes.

Figure 82. SDO Contents, Echo Mode

WDT

The WDT feature ensures that communication is not lost between the system controller and the AD5753, and that the SPI datapath lines function as expected.

When enabled, the WDT alerts the system if the AD5753 has not received a specific SPI frame in the user programmable timeout period. When the specific SPI frame is received, the watchdog resets the timer controlling the timeout alert. The SPI frame used to reset the WDT is configurable as one of the two following choices:

- A specific key code write to the key register (default).
- A valid SPI write to any register.

When a watchdog timeout event occurs, there are two user configurable actions the AD5753 takes. The first is to load the DAC output with a user defined clear code stored in the CLEAR_CODE register. The second is to perform a software reset. These two actions can be enabled via Bit 10 and Bit 9, respectively, in the WDT_CONFIG register. On a watchdog timeout event, regardless if Bit 10 or Bit 9 is enabled, a dedicated WDT_STATUS bit in the status register, as well as a WDT_ERR bit in the DIGITAL_DIAG_RESULTS register, alerts the user that the WDT is timed out. After a WDT timeout occurs, all writes to the DAC_INPUT register, as well as the hardware or software $\overline{\text{LDAC}}$ events, are ignored until the active WDT fault flag within the DIGITAL_DIAG_RESULTS register clears.

After the active WDT fault flag clears, the WDT restarts by performing a subsequent WDT reset command.

On power-up, the WDT is disabled by default. The default timeout setting is 1 sec. The default method to reset the WDT is to write one specific key. On timeout, the default action is to set the relevant WDT_ERR flag bits and the $\overline{\text{FAULT}}$ pin. See Table 42 for the specific register bit details to support the configurability of the WDT operation.

USER DIGITAL OFFSET AND GAIN CONTROL

The AD5753 has a USER_GAIN register and a USER_OFFSET register that trim the gain and offset errors from the entire signal chain. The 16-bit USER_GAIN register allows the user to adjust the gain of the DAC channel in steps of 1 LSB. The USER_GAIN register coding is straight binary, as shown in Table 14. The default code in the USER_GAIN register is 0xFFFF, which results in a no gain factor applied to the programmed output. In theory, the gain can be tuned across the full range of the output. In practice, the maximum recommended gain trim is approximately 50% of the programmed range to maintain accuracy.

Table 14. Gain Register Adjustment

Gain Adjustment Factor	D15	[D14:D1]	D0
1	1	1	1
65,535/65,536	1	1	0
…	…	…	…
2/65,536	0	0	1
1/65,536	0	0	0

The 16-bit USER_OFFSET register allows the user to adjust the offset of the DAC channel from −32,768 LSBs to +32,768 LSBs in steps of 1 LSB. The USER_OFFSET register coding is straight binary, as shown in Table 15. The default code in the USER_OFFSET register is 0x8000, which results in zero offset programmed to the output.

Table 15. Offset Register Adjustment

Gain Adjustment	D15	[D13:D2]	D0
+32,768 LSBs	1	1	1
+32,767 LSBs	1	1	0
…	…	…	…
No Adjustment (Default)	1	0	0
…	…	…	…
−32,767 LSBs	0	0	1
−32,768 LSBs	0	0	0

The decimal value that is written to the internal DAC register (DAC code) is calculated with the following equation:

$$DAC\ code = D \times \frac{(M+1)}{2^{16}} + C - 2^{15}$$

where:
D is the code loaded to the DAC_INPUT register.
M is the code in the USER_GAIN register (default code = $2^{16} - 1$).
C is the code in the USER_OFFSET register (default code = 2^{15}).

Data from the DAC_INPUT register is processed by a digital multiplier and adder and both are controlled by the contents of the user gain and user offset registers, respectively. The calibrated DAC data is then loaded to the DAC. The loading of the DAC data is dependent on the state of the $\overline{\text{LDAC}}$ pin.

Each time data is written to the USER_GAIN or USER_OFFSET register, the DAC output is not automatically updated. Instead, the next write to the DAC_INPUT register uses these user gain and user offset values to perform a new calibration and to automatically update the output channel. The read only DAC_OUTPUT register represents the value currently available at the DAC output, except in the case of user gain and user offset calibration. In this case, the DAC_OUTPUT register contains the DAC data input by the user, on which the calibration is performed and not the result of the calibration.

Both the USER_GAIN register and the USER_OFFSET register have 16 bits of resolution. The correct method to calibrate the gain and offset is to first calibrate the gain and then calibrate the offset.

DAC OUTPUT UPDATE AND DATA INTEGRITY DIAGNOSTICS

Figure 83 shows a simplified version of the DAC input loading circuitry. If used, the USER_GAIN and USER_OFFSET registers must be updated before writing to the DAC_INPUT register.

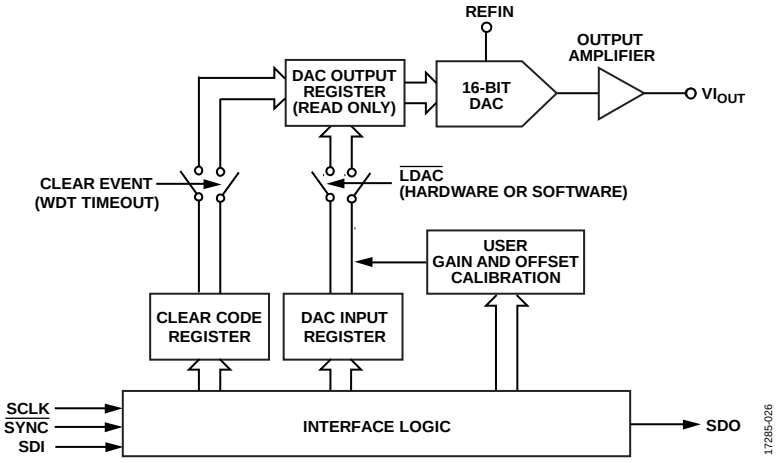


Figure 83. Simplified Serial Interface of Input Loading Circuitry

The DAC_OUTPUT register, and ultimately the DAC output, updates in any of the following cases:

- If a write is performed to the DAC_INPUT register with the hardware $\overline{\text{LDAC}}$ pin tied low, the DAC_OUTPUT register is updated on the rising edge of $\overline{\text{SYNC}}$ and is subject to the timing specifications shown in Table 2.
- If the hardware $\overline{\text{LDAC}}$ pin is tied high and the DAC_INPUT register is written to, the DAC_OUTPUT register does not update until a software $\overline{\text{LDAC}}$ instruction is issued or the hardware $\overline{\text{LDAC}}$ pin is pulsed low.
- If a WDT timeout occurs with the CLEAR_ON_WDT_FAIL bit set, the CLEAR_CODE register contents are loaded into the DAC_OUTPUT register.
- If the slew rate control feature is enabled, the DAC_OUTPUT register contains the dynamic value of the DAC as the register slews between values.

While a WDT fault is active, all writes to the DAC_INPUT register, as well as hardware or software $\overline{\text{LDAC}}$ events, are ignored. If the CLEAR_ON_WDT_FAIL bit is set such that the output is set to the clear code, after the WDT fault flag clears, the DAC_INPUT register must be written to before the DAC_OUTPUT register updates. The DAC_INPUT register must be written to because performing a software or hardware $\overline{\text{LDAC}}$ only reloads the DAC with the clear code. As described in this section, after configuring the DAC range via the DAC_CONFIG register, the DAC_INPUT register must be written to, even if the contents of the DAC_INPUT register are not changing from the current value.

The GP_CONFIG2 register contains a bit to enable a global software LDAC mode, which ignores the device under test (DUT) address bits of the SW_LDAC command, thus enabling multiple AD5753 devices to be simultaneously updated by using a single SW_$\overline{\text{LDAC}}$ command. This feature is useful if the hardware $\overline{\text{LDAC}}$ pin is not being used in a system containing multiple AD5753 devices.

DAC Data Integrity Diagnostics

To protect against transient changes to the internal digital circuitry, the digital block stores both the digital DAC value and an inverted copy of the digital DAC value. A check is completed to ensure that the two values correspond to each other before the DAC is strobed to update to the DAC code. This matching feature is enabled by default via the INVERSE_DAC_CHECK_EN bit in the DIGITAL_DIAG_CONFIG register.

Outside of the digital block, the DAC code is stored in latches, as shown in Figure 84. These latches are potentially vulnerable to the same transient events that affect the digital block. To protect the DAC latches against such transients, enable the DAC latch monitor feature via the DAC_LATCH_MON_EN bit within the DIGITAL_DIAG_CONFIG register. This latch monitor feature monitors the actual digital code driving the DAC and compares the code with the digital code generated within the digital block. Any difference between the two codes sets the DAC_LATCH_MON_ERR flag in the DIGITAL_DIAG_RESULTS register.

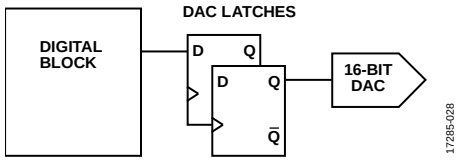


Figure 84. DAC Data Integrity

GPIO PINS

The AD5753 provides the following three GPIO pins: GPIO_0, GPIO_1, and GPIO_2. Using the GP_CONFIG register, each of these pins can be configured as a digital output, a digital input, or as a 100 kΩ to DGND (default). When configured as a digital input or output, the GPIO_DATA register is used to read or write from or to the relevant pins.

USE OF KEY CODES

Key codes are used via the key register for the following functions (see the Key Register section for full details):

- Initiating calibration memory refresh.
- Initiating a software reset.
- Initiating a single ADC conversion.
- WDT reset key.

Using specific keys to initiate actions such as a calibration memory refresh or a device reset provides extra system robustness because the keys reduce the probability of either task being initiated in error.

SOFTWARE RESET

A software reset requires two consecutive writes of 0x15FA and 0xAF51 respectively to the key register. A device reset can be initiated via the hardware $\overline{\text{RESET}}$ pin, the software reset keys, or automatically after a WDT timeout (if configured to do so). The RESET_OCCURRED bit in the DIGITAL_DIAG_RESULTS register is set when the device is reset. This RESET_OCCURRED bit defaults to 1 on power-up. Both of the diagnostic results registers implement a write 1 to clear the function that is, a 1 must be written to this bit to clear it (see the Sticky Diagnostic Results Bits section).

CALIBRATION MEMORY CRC

For every calibration memory refresh cycle, which is either initiated via a key code write to the key register or automatically initiated when the Range[3:0] bits of the DAC_CONFIG register, is changed, an automatic CRC is calculated on the contents of the calibration memory shadow registers. The result of this CRC is compared with the factory stored reference CRC value. If the CRC values match, the read of the entire calibration memory is considered valid. If the values do not match, the CAL_MEM_CRC_ERR bit in the DIGITAL_DIAG_RESULTS register is set to 1. This calibration memory CRC feature is enabled by default and can be disabled via the CAL_MEM_CRC_EN bit in the DIGITAL_DIAG_CONFIG register.

Two-stage readback commands are permitted while this calibration memory refresh cycle is active. However, a write to any register other than the TWO_STAGE_READBACK_SELECT register or the NOP register sets the INVALID_SPI_ACCESS_ERR bit in the DIGITAL_DIAG_RESULTS register. As described in the Programming Sequence to Enable the Output section, a wait period of 500 µs is recommended after a calibration memory refresh cycle is initiated.

INTERNAL OSCILLATOR DIAGNOSTICS

An internal frequency monitor uses the internal MCLK to increment a 16-bit counter at a rate of 1 kHz (MCLK/10,000). The counter value can be read in the FREQ_MONITOR register. The user can poll this register periodically and use it as a diagnostic tool for the internal oscillator (to monitor that the oscillator is running), and to measure the oscillator frequency. This counter feature is enabled by default via the FREQ_MON_EN bit in the DIGITAL_DIAG_CONFIG register.

If the MCLK stops, the AD5753 sends a specific code of 0x07DEAD to the SDO line for every SPI frame. This oscillator dead code feature is enabled by default and is disabled by clearing the OSC_STOP_DETECT_EN bit in the GP_CONFIG1 register. This feature is limited to the maximum readback timing specifications described in Table 3.

STICKY DIAGNOSTIC RESULTS BITS

The AD5753 contains the following two diagnostic results registers: digital and analog (see Table 47 and Table 48, respectively for the diagnostic error bits). The diagnostic result bits contained within these registers are sticky (R/W-1-C), that is, each bit needs a 1 to be written to it to clear the error bit. However, if the fault is still present, even after writing a 1 to the bit in question, the error bit does not clear to 0. Upon writing Logic 1 to the bit, it updates to the latest value, which is Logic 1 if the fault is still present and Logic 0 if the fault is no longer present.

These are the two following exceptions to this R/W-1-C access within the DIGITAL_DIAG_RESULTS register: CAL_MEM_UNREFRESHED and SLEW_BUSY. These flags automatically clear when the calibration memory refreshes or the output slew is complete.

The status register contains a DIG_DIAG_STATUS and ANA_DIAG_STATUS bit and both bits are the result of a logical OR of the diagnostic results bits contained in each diagnostic results registers. All analog diagnostic flag bits are included in the logical OR of the ANA_DIAG_STATUS bit and all digital diagnostic flag bits, with the exception of the SLEW_BUSY bit, are included in the logical OR of the DIG_DIAG_STATUS bit. The OR'ed bits within the status register are read only and not sticky (R/W-1-C).

BACKGROUND SUPPLY AND TEMPERATURE MONITORING

Excessive die temperature and overvoltage are known to be related to common cause failures. These conditions can be monitored in a continuous fashion by using comparators, which eliminates the requirement to poll the ADC.

Both die have a built-in temperature sensor with a ±5°C accuracy. The die temperature is monitored by a comparator and the background temperature comparators are permanently enabled. Programmable trip points corresponding to 142°C, 127°C, 112°C, and 97°C can be configured in the GP_CONFIG1 register. If the temperature of either die exceeds the programmed limit, the relevant status bit in the ANALOG_DIAG_RESULTS register is set and the $\overline{\text{FAULT}}$ pin is asserted low.

The low voltage supplies on the AD5753 are monitored via low power static comparators. This monitoring function is disabled by default and is enabled via the COMPARATOR_CONFIG bits in the GP_CONFIG2 register. The INT_EN bit in the DAC_CONFIG register must be set for the REFIN buffer to be powered up and for this node to be available to the REFIN comparator. The monitored nodes are REFIN, REFOUT, V_{LDO}, and INT_AVCC. There is a status bit in the ANALOG_DIAG_RESULTS register that corresponds to each monitored node. If any of the monitored node supplies exceed the upper or lower threshold values (see Table 16 for the threshold values), the corresponding status bit is set. Note that if a REFOUT fault occurs, the REFOUT_ERR status bit is set. The INT_AVCC, V_{LDO}, and temperature comparator status bits can then also be set because REFOUT is used as the comparison voltage for these nodes. Like all the other status bits in the ANALOG_DIAG_RESULTS register, these bits are sticky and need a 1 to be written to them to clear them, assuming that the error condition is subsided. If the error condition is still present, the flag remains high even after a 1 is written to clear it.

Table 16. Comparator Supply Activation Thresholds

Supply	Lower Threshold (V)	Nominal Value/Range (V)	Upper Threshold (V)
INT_AVCC	3.8	4 to 5	5.2
V_{LDO}	2.8	3 to 3.6	3.8
REFIN	2.24	2.5	2.83
REFOUT	2.24	2.5	2.83

OUTPUT FAULT

The AD5753 is equipped with a $\overline{\text{FAULT}}$ pin. This pin is an active low, open-drain output that connects several AD5753 devices together to one pull-up resistor for global fault detection. This pin is high impedance when no faults are detected and is asserted low when certain faults, such as an open circuit in current mode, a short circuit in voltage mode, a CRC error, or an overtemperature error, are detected. Table 17 shows the fault conditions that automatically force the $\overline{\text{FAULT}}$ pin active and highlights the user maskable fault bits available via the FAULT_PIN_CONFIG register (see Table 45). All registers contain a

corresponding $\overline{\text{FAULT}}$ pin status bit, FAULT_PIN_STATUS, that mirrors the inverted current state of the $\overline{\text{FAULT}}$ pin. For example, if the $\overline{\text{FAULT}}$ pin is active, the FAULT_PIN_STATUS bit is 1.

Table 17. $\overline{\text{FAULT}}$ Pin Trigger Sources[1]

Fault Type	Mapped to $\overline{\text{FAULT}}$ Pin	Mask Ability
Digital Diagnostic Faults		
Oscillator Stop Detect	Yes	Yes
Calibration Memory Not Refreshed	No	N/A
Reset Detected	No	N/A
3-Wire Interface Error	Yes	No
WDT Error	Yes	Yes
3-Wire Read and Compare Parity Error	Yes	No
DAC Latch Monitor Error	Yes	Yes
Inverse DAC Check Error	Yes	Yes
Calibration Memory CRC Error	Yes	No
Invalid SPI Access	Yes	Yes
SCLK Count Error	Yes	No[2]
Slip Bit Error	Yes	Yes
SPI CRC Error	Yes	Yes
Analog Diagnostic Faults		
VI_{OUT} Overvoltage Error	Yes	Yes
DC-to-DC Short-Circuit Error	Yes	Yes
DC-to-DC Power Error	Yes	No
Current Output Open Circuit Error	Yes	Yes
Voltage Output Short-Circuit Error	Yes	Yes
DC-to-DC Die Temperature Error	Yes	Yes
Main Die Temperature Error	Yes	Yes
REFFOUT Comparator Error	Yes	No
REFIN Comparator Error	Yes	No
INT_AVCC Comparator Error	Yes	No
V_{LDO} Comparator Error	Yes	No

[1] N/A means not applicable.
[2] Although the SCLK count error cannot be masked in the FAULT_PIN_CONFIG register, it can be excluded from the $\overline{\text{FAULT}}$ pin by enabling the SPI_DIAG_QUIET_EN bit (Bit D3 in the GP_CONFIG1 register).

The DIG_DIAG_STATUS, ANA_DIAG_STATUS, and WDT_STATUS bits of the status register are used in conjunction with the $\overline{\text{FAULT}}$ pin and the FAULT_PIN_STATUS bit to inform the user which fault condition is causing the $\overline{\text{FAULT}}$ pin or which FAULT_PIN_STATUS bit to activate.

ADC MONITORING

The AD5753 incorporates a 12-bit ADC to provide diagnostic information on user selectable inputs such as supplies, grounds, internal die temperatures, references, and external signals. See Table 18 for a full list of these selectable inputs. The ADC reference is derived from REFOUT and provides independence from the DAC reference (REFIN) if necessary. The ADC_CONFIG register configures the ADC mode of operation, either user initiated individual conversions or sequence mode, and selects the multiplexed ADC input channel via the ADC_IP_SELECT bits (see Table 44).

ADC Transfer Function Equations

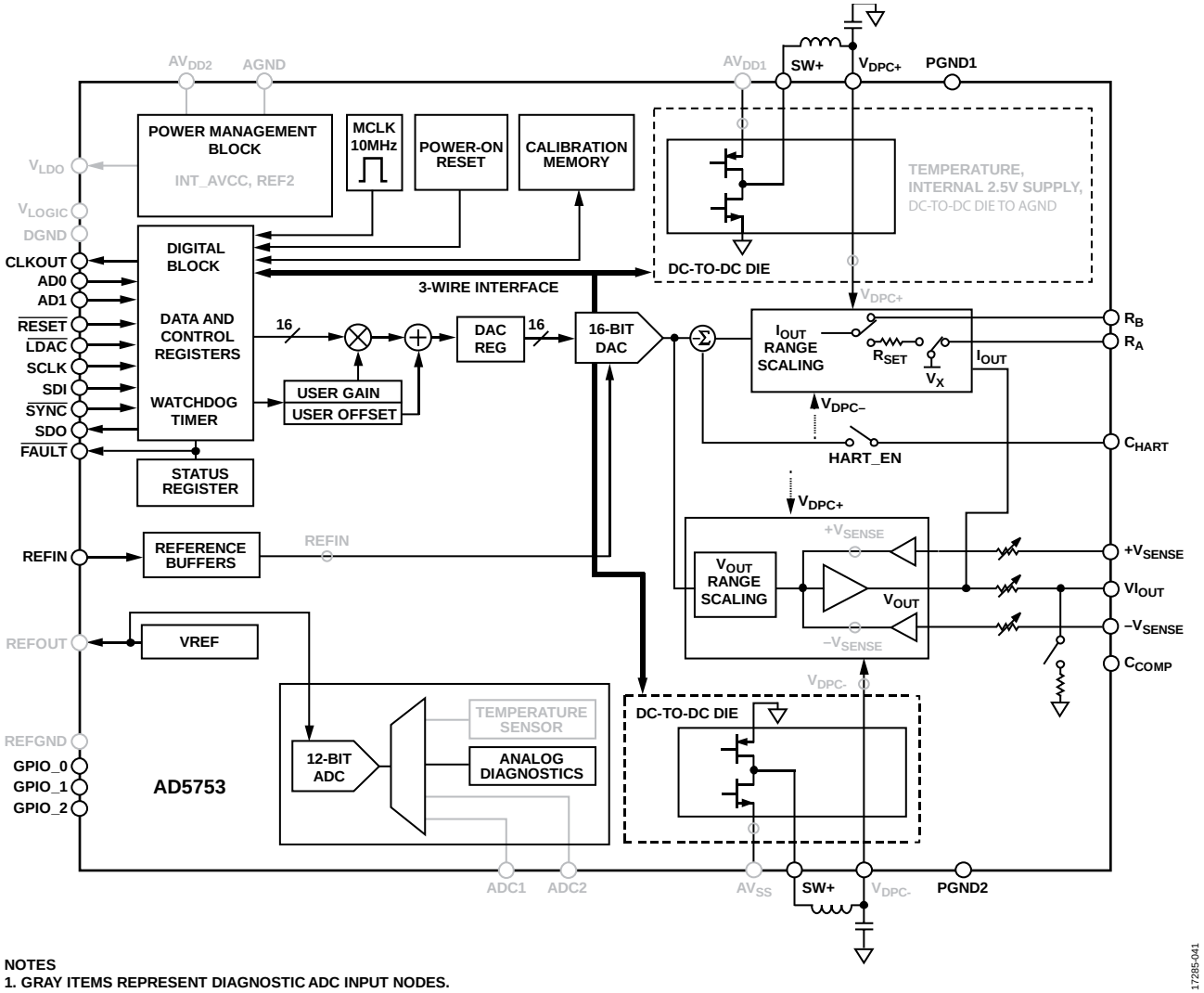
The ADC has an input range of 0 V to 2.5 V and can be used to digitize a variety of different nodes. The set of inputs to the ADC encompasses both unipolar and bipolar ranges, varying from high to low voltage values. Therefore, to be able to digitize the voltage values, the voltage ranges outside of the 0 V to 2.5 V ADC input range must be divided down.

The ADC transfer function equation is dependent on the selected ADC input node. See Table 18 for a summary of all transfer function equations).

Table 18. ADC Input Node Summary

ADC_IP_SELECT	V_{IN} Node Description	ADC Transfer Function
00000	Main die temperature	T (°C) = (−0.09369 × D) + 307 where D = ADC_CODE (the ADC result)
00001	DC-to-dc die temperature	T (°C) = (−0.11944 × D) + 436
00010	Reserved	Reserved
00011	REFIN	REFIN (V) = $(D/2^{12}) \times 2.75$
00100	Internal 1.23 V reference voltage (REF2)	REF2 (V) = $(D/2^{12}) \times 2.5$
00101	Reserved	Reserved
00110	Reserved	Reserved
01100	ADC2 pin input (±15 V input range)	ADC2 (V) = $(30 \times D)/2^{12} - 15$
01101	Voltage on the $+V_{SENSE}$ buffer output	$+V_{SENSE}$ (V) = $((50 \times D)/2^{12}) - 25$
01110	Voltage on the $-V_{SENSE}$ buffer output	$-V_{SENSE}$ (V) = $((50 \times D)/2^{12}) - 25$
01111	ADC1 pin input (0 – 1.25 V input range)	ADC1 (V) = $D/2^{12} \times 1.25$
10000	ADC1 pin input (0 – 0.5 V input range)	ADC1 (V) = $D/2^{12} \times 2.5 \times 1/5 = D/2^{12} \times 0.5$
10001	ADC1 pin input (0 – 2.5 V input range)	ADC1 (V) = $D/2^{12} \times 2.5$
10010	ADC1 pin input (± 0.5 V input range)	ADC1 (V) = $D/2^{12}$ - 0.5

ADC_IP_SELECT	V_{IN} Node Description	ADC Transfer Function
10011	Reserved	Reserved
10100	INT_AVCC	INT_AVCC (V) = D/2^{12} × 10
10101	V_{LDO}	V_{LDO} (V) = D/2^{12} × 10
10110	V_{LOGIC}	V_{LOGIC} (V) = D/2^{12} × 10
11000	REFGND	REFGND (V) = D/2^{12} × 2.5
11001	AGND	AGND (V) = D/2^{12} × 2.5
11010	DGND	DGND (V) = D/2^{12} × 2.5
11011	V_{DPC+}	V_{DPC+} (V) = D/2^{12} × 37.5
11100	AV_{DD2}	AV_{DD2} (V) = D/2^{12} × 37.5
11101	V_{DPC-}	V_{DPC-} (V) = (15 × D/2^{12} − 14) × 2.5
11110	DC-to-dc die node; configured in the DCDC_CONFIG2 register	
	00: AGND on dc-to-dc die	AGND (dc-to-dc) (V) = (D/2^{12}) × 2.5
	01: Internal 2.5 V supply on dc-to-dc die	Internal 2.5 V (dc-to-dc) (V) = (D/2^{12}) × 5
	10: AV_{DD1}	AV_{DD1} (V) = D/2^{12} × 37.5
	11: AV_{SS}	AV_{SS} (V) = (15 × D/2^{12} − 14) × 2.5
11111	REFOUT	REFOUT (V) = (D/2^{12}) × 2.5



NOTES
1. GRAY ITEMS REPRESENT DIAGNOSTIC ADC INPUT NODES.

17285-041

Figure 85. Diagnostic ADC Input Nodes

ADC Configuration

The ADC is configured using the ADC_CONFIG register via the SEQUENCE_COMMAND bits (Bits[10:8]), the SEQUENCE_DATA bits (Bits[7:5]), and the ADC_IP_SELECT bits (Bits[4:0]). Table 19 shows the contents of the ADC_CONFIG register.

Table 19. ADC Configuration Register

[D10:D8]	[D7:D5]	[D4:D0]
Command	Data	ADC input select

The ADC can be set up to either monitor a single node of interest or configured to sequence through up to eight nodes of interest. The sequential conversions can be initiated automatically after every valid SPI frame is received by the device (automatic sequence mode), or in a more controlled manner via a specific key code written to the key register (key sequence mode). When a conversion is complete, the ADC result is available in the status register and, if in sequence mode, the sequencer address is advanced. If autostatus readback mode is used in conjunction with either sequence mode, the last completed ADC conversion data is available on the SDO during every SPI frame written to the device.

The sequencer command has a maximum channel depth of eight channels. Each channel in the sequencer must be configured with the required ADC input for that sequencer channel via the ADC_IP_SELECT bits. The number of configured channels must equal the channel depth. If the active sequencer channel location is not configured correctly, the sequencer stores the previously loaded channel value and defaults all other enabled sequencer channels 0b00000 for all sequencer channels. To avoid any 3-wire interface related delays between ADC conversions if a dc-to-dc die node is required to be part of the ADC sequencer, perform this configuration using the DCDC_ADC_CONTROL_DIAG bits in the DCDC_CONFIG2 register before configuring the ADC sequencer. If multiple nodes from the dc-to-dc die are required within the sequence, key sequencing mode must be used rather than automatic sequencing mode because the DCDC_ADC_CONTROL_DIAG bits must be updated between ADC conversions to configure the next dc-to-dc die node required by the sequence.

The four ADC modes of operation are key sequencing, automatic sequencing, single immediate conversion, and single key conversion. The sequencing modes are mutually exclusive so if the key sequencing mode is enabled, it disables the automatic sequencing mode and vice versa.

Key Sequencing (Command 010)

Writing Command 010 to the command bits in the ADC_CONFIG register enables key sequencing mode. Key sequencing starts with a write to the key register with Key Code 0x1 ADC and starts on Channel 0, continuing to Channel N − 1, where N is the channel depth with every 0x1ADC command. This mode enables users to control channel switching during sequencing because the switch only occurs every specific key code command, rather than for every valid SPI frame, which occurs in automatic sequencing mode. When the sequence is completed, it starts again with Channel 0 until disabled. Before Command 0b010 is issued, Command 000 and Command 001 must be used to configure all the required channels to enable key sequencing mode (see Figure 86). If the sequencing is disabled and later reenabled, the sequencer is reset to recommence converting on the first channel in the sequence.

Automatic Sequencing (Command 011)

Sequencing starts on the next valid SPI frame and starts with Channel 0, continuing to Channel N − 1 where N is the channel depth on every valid SPI frame. When the sequence is complete, it starts again with Channel 0 until disabled. As with the key sequencing mode, before Command 011 is issued, Command 000 and Command 001 must be used to configure all the required channels to enable automatic sequencing mode (see Figure 86). If the sequencing is disabled and later reenabled, the sequencer is reset to recommence converting on the first channel in the sequence. When reenabled, the channels do not need to be reconfigured unless the desired list of nodes changes. Use automatic sequencing in conjunction with the autostatus readback mode to ensure that the latest ADC result is available.

Single Immediate Conversion (Command 100)

Single immediate conversion mode initiates a single conversion on the node currently selected in the ADC_IP_SELECT bits of the ADC_CONFIG register. Selecting this command stops any active automatic sequence, which means the sequencer must be reenabled if required. The sequencer does not need to be reconfigured because the configuration of the sequencer depth and channels is stored.

Single Key Conversion (Command 101)

Single key conversion mode sets up an individual ADC input node to be converted when the user initiates the mode by writing the 0x1ADC key code to the key register.

Sequencing Mode Setup

A list of the relevant ADC sequencer commands are shown in Table 20. These commands are available in the ADC_CONFIG register; see Table 44 for the ADC_CONFIG register bits. The default depth (000) is equivalent to one diagnostic channel up to a binary depth value of 111, which is equivalent to eight channels.

Table 20. Command Bits

Value	Description
000	Set the sequencer depth (0 to 7)
001	Load the sequencer Channel N with the selected ADC input
010	Enable or disable key sequencer
011	Enable or disable automatic sequencer
100	Perform a single conversion on the currently selected ADC input
101	Set up single key conversion, that is, select the ADC mux input to be used when the 0x1ADC key is written with a write to the key register (this conversion is outside of the key sequencing mode)

Use the following procedure to set up the sequencer:

1. Select the depth.
2. Load the channels to the sequencer N times for N channels.
3. Enable the sequencer. Enabling the sequencer also starts the first conversion.

An example of configuring the sequencer to monitor three ADC nodes is shown in Figure 86.

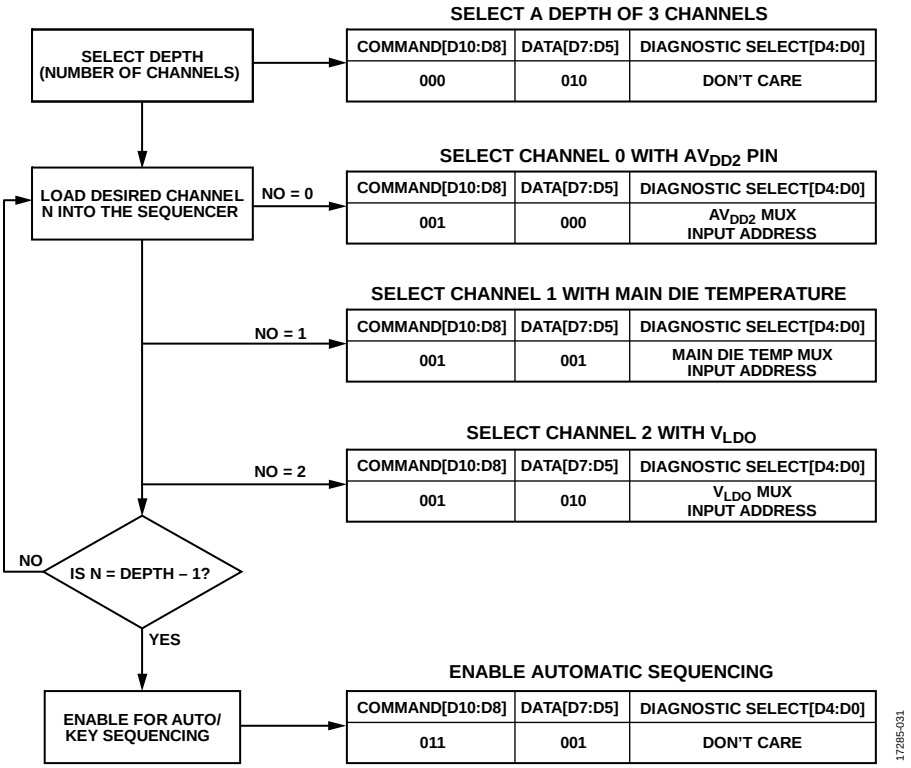


Figure 86. Example Automatic Sequence Mode Setup for Three ADC Input Nodes

ADC Conversion Timing

Figure 87 shows an example where autostatus readback mode is enabled. The status register always contains the last completed ADC conversion result together with the associated mux address, ADC_IP_SELECT.

This example is applicable irrespective of the ADC conversion mode in use (key sequencing, automatic sequencing, single immediate conversion, or single key conversion). During the first ADC conversion command shown, the contents of the status register are available on the SDO line. The ADC portion of this data contains the conversion result of the previously converted ADC node (ADC Conversion Result 0), as well as the associated channel address. If another SPI frame is not received while the ADC is busy converting due to Command 1, the next data to appear on the SDO line contains the associated conversion result, ADC Conversion Result 1. However, if an SPI frame is received while the ADC is busy, the status register contents available on SDO still contain the previous conversion result and indicates that the ADC_BUSY flag is high. Any new ADC conversion instructions received while the ADC_BUSY bit is active are ignored. If using a sequencer mode, the sequencer address is updated after the conversion completes.

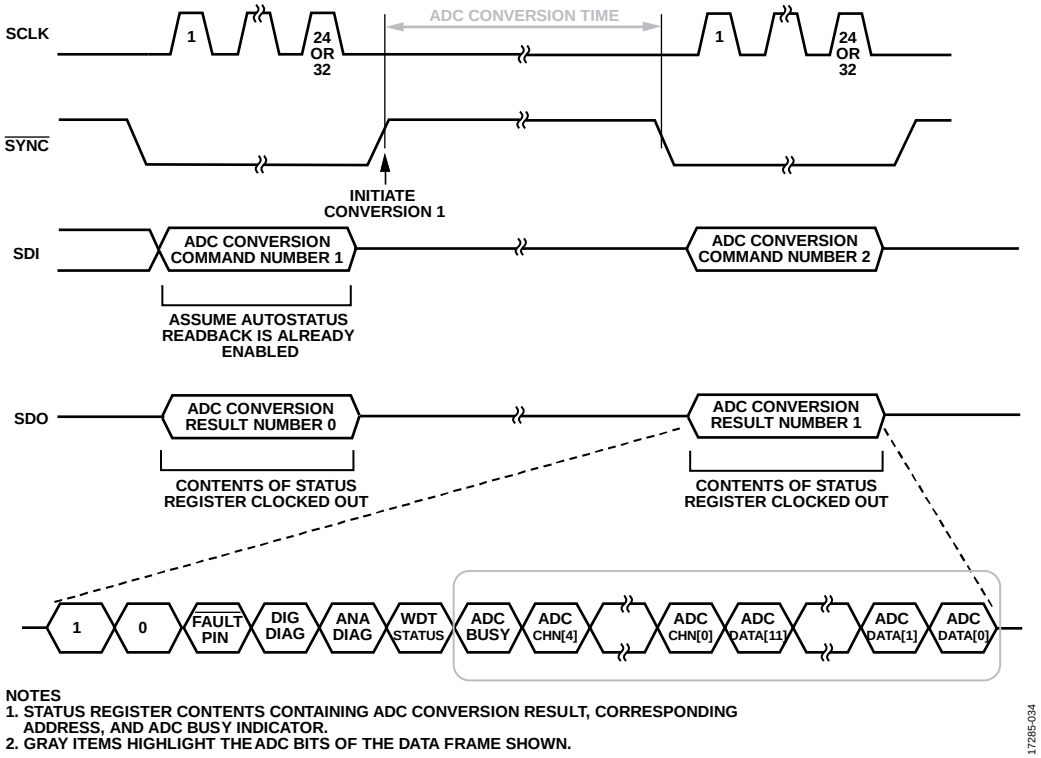


Figure 87. ADC Conversion Timing Example

REGISTER MAP

The AD5753 is controlled and configured via 29 on-chip registers described in the Register Details section. The four possible access permissions are as follows:

- R/W: read or write
- R: read only
- R/W-1-C: read or write 1 to clear
- R0: read zero
- R0/W: read zero or write

Reading from and writing to reserved registers is flagged as an invalid SPI access. When accessing registers with reserved bit fields, the default value of those bit fields must be written. These values are listed in the Reset column of Table 27 to Table 52.

WRITING TO REGISTERS

Use the format data frame in Table 21 when writing to any register. By default, the SPI CRC is enabled, and the input register is 32 bits wide with the last eight bits corresponding to the CRC code. Only frames of exactly 32 bits wide are accepted as valid. If the CRC is disabled, the input register is 24 bits wide, and 32-bit frames are also accepted, with the final 8 bits ignored. Table 22 describes the bit names and functions of Bit D23 to Bit D16. Bit D15 to Bit D0 depend on the register that is being addressed.

Table 21. Writing to a Register

MSB **LSB**

D23	D22	D21	D20	D19	D18	D17	D16	[D15:D0]
$\overline{AD1}$	AD1	AD0	REG_ADR4	REG_ADR3	REG_ADR2	REG_ADR1	REG_ADR0	Data

Table 22. Input Register Decode

Bit	Description
$\overline{AD1}$	Slip bit. This bit must equal the inverse of Bit D22, that is, AD1.
AD1, AD0	Used in association with the external pins, AD1 and AD0, to determine which AD5753 device is being addressed by the system controller. Up to four unique devices can be addressed, corresponding to the AD1 and AD0 addresses of 0b00, 0b01, 0b10, and 0b11.
REG_ADR4, REG_ADR3, REG_ADR2, REG_ADR1, REG_ADR0	Selects which register is written to. See Table 26 for a summary of the available registers.

READING FROM REGISTERS

The AD5753 has four options for readback mode that can be configured in the TWO_STAGE_READBACK_SELECT register (see Table 46). These options are as follows:

- Two-stage readback
- Autostatus readback
- Shared $\overline{\text{SYNC}}$ autostatus readback
- Echo mode

Two-Stage Readback Mode

Two-stage readback mode consists of a write to the TWO_STAGE_READBACK_SELECT register to select the register location to be read back, followed by a NOP command. To perform a NOP command, write all zeros to Bits[D15:D0] of the NOP register (see Table 27). During the NOP command, the contents of the selected register are available on the SDO pin in the data frame format shown in Table 23. It is also possible to write a new two-stage readback command during the second frame, such that the corresponding new data is available on the SDO pin in the subsequent frame (see Figure 88). Bits[D31:D30] (or Bits[D23:D22], if SPI CRC is not enabled) = 0b10 are used as part of the synchronization during readback. The contents of the first write instruction to the TWO_STAGE_READBACK_SELECT register is shown in Table 24.

Table 23. SDO Contents for Read Operation

MSB			LSB
[D23:D22]	**D21**	**[D20:16]**	**[D15:D0]**
0b10	$\overline{\text{FAULT}}$ pin status	Register address	Data

Table 24. Reading from a Register Using Two-Stage Readback Mode

MSB													LSB
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**[D15:D5]**	**D4**	**D3**	**D2**	**D1**	**D0**
$\overline{\text{AD1}}$	AD1	AD0	0x13					Reserved	READBACK_SELECT[4:0]				

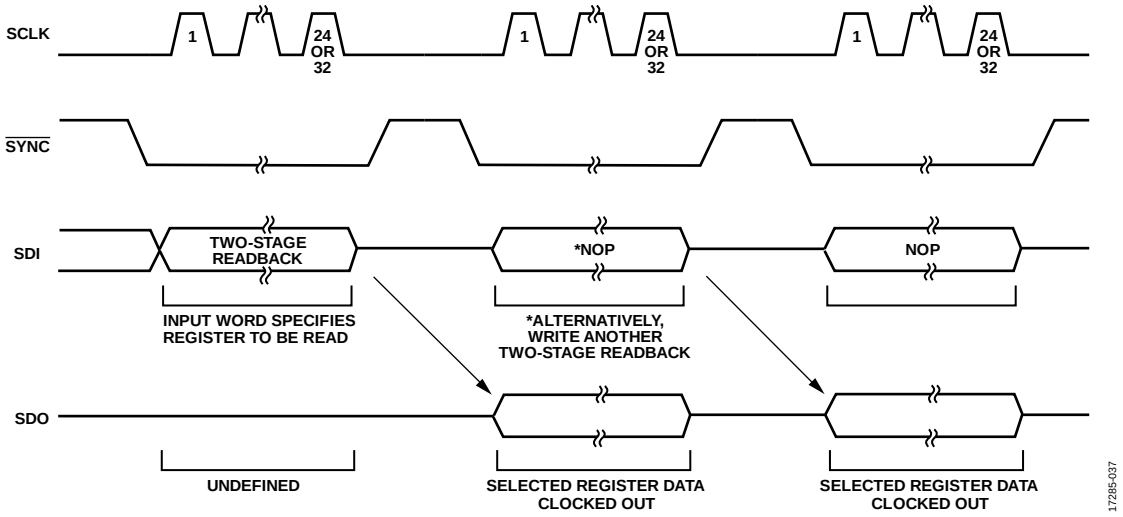


Figure 88. Two-Stage Readback Example

Autostatus Readback Mode

If autostatus readback mode is selected, the contents of the status register are available on the SDO line during every SPI transaction. When reading back the status register, the SDO contents differ from the data frame format shown in Table 23. The contents of the status register are shown in Table 25.

The autostatus readback mode can be used in conjunction with the ADC sequencer to consecutively monitor up to eight different ADC inputs. See the ADC Monitoring section for further details on the ADC sequencer. The autostatus readback mode can be configured via the READBACK_MODE bits in the TWO_STAGE_READBACK_SELECT register (see the Two-Stage Readback Select Register section). Figure 89 shows an example of the data frames for an autostatus readback.

Table 25. SDO Contents for a Read Operation on the Status Register

MSB **LSB**

D23	D22	D21	D20	D19	D18	D17	[D16:D12]	[D11:D0]
1	0	FAULT_PIN_STATUS	DIG_DIAG_STATUS	ANA_DIAG_STATUS	WDT_STATUS	ADC_BUSY	ADC_CH[4:0]	ADC_DATA[11:0]

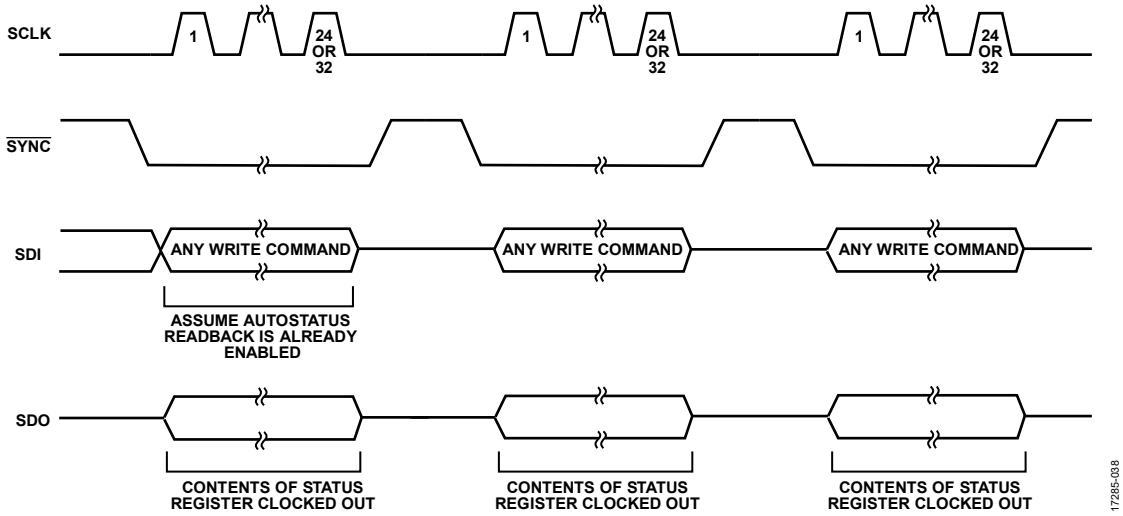


Figure 89. Autostatus Readback Example

Shared $\overline{\text{SYNC}}$ Autostatus Readback Mode

The shared $\overline{\text{SYNC}}$ autostatus readback is a special version of the autostatus readback mode that is used to avoid SDO bus contention when multiple AD5753 devices are sharing the same $\overline{\text{SYNC}}$ line. If this scenario occurs, the AD5753 devices are distinguished from each other using the hardware address pins. An internal flag is set after each valid write to a device and the flag is cleared on the subsequent falling edge of $\overline{\text{SYNC}}$. The shared $\overline{\text{SYNC}}$ autostatus readback mode behaves in a similar manner to the normal autostatus readback mode, except the device does not output the status register contents on SDO when $\overline{\text{SYNC}}$ goes low, unless the internal flag is set, which occurs when the previous SPI write is valid. Refer to the example shown in Figure 90. Configure the shared $\overline{\text{SYNC}}$ autostatus readback mode via the READBACK_MODE bits in the two-stage readback select register (see the Two-Stage Readback Select Register section).

Echo Mode

Echo mode behaves in a similar manner to the autostatus readback mode, except that every second readback consists of an echo of the previous command written to the AD5753. Echo mode is useful for checking which SPI instruction is received in the previous SPI frame. Echo mode can be configured via the READBACK_MODE bits in the two-stage readback select register (see the Two-Stage Readback Select Register section).

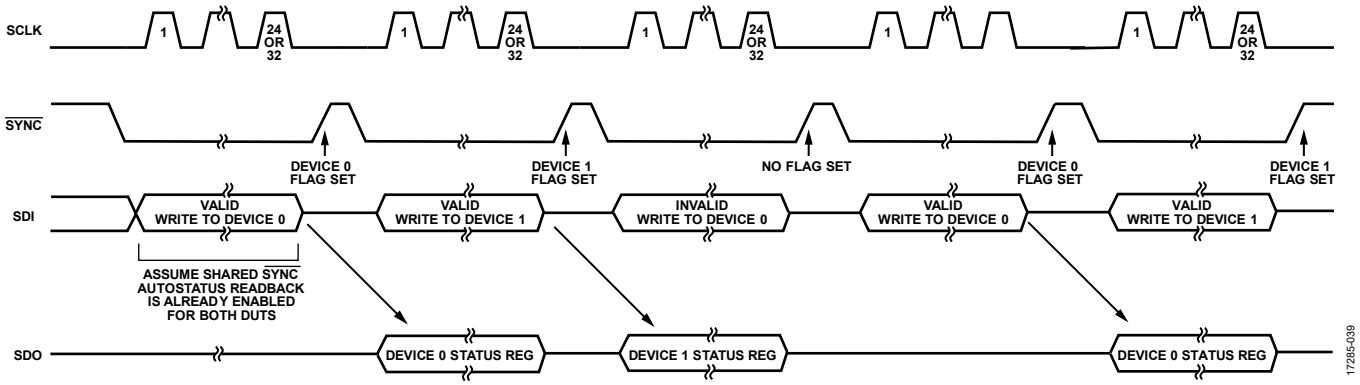


Figure 90. Shared $\overline{\text{SYNC}}$ Autostatus Readback Example

Figure 91. SDO Contents—Echo Mode

PROGRAMMING SEQUENCE TO ENABLE THE OUTPUT

To write to and set up the AD5753 from a power-on or reset condition, take the following steps:

1. Perform a hardware or software reset and wait 100 µs.
2. Perform a calibration memory refresh by writing 0xFCBA to the key register. Wait a minimum of 500 µs before proceeding to Step 3 to allow time for the internal calibrations to complete. As an alternative to waiting 500 µs for the refresh cycle to complete, poll the CAL_MEM_UNREFRESHED bit in the DIGITAL_DIAG_RESULTS register until it is 0.
3. Write 1 to Bit D13 in the DIGITAL_DIAG_RESULTS register to clear the RESET_OCCURRED flag.
4. If the CLKOUT signal is required, configure and enable CLKOUT via the GP_CONFIG1 register. It is important to configure this feature before enabling the dc-to-dc converter.
5. Write to the DCDC_CONFIG2 register to set the dc-to-dc current limit and enable the negative dc-to-dc converter (if using negative DPC). Wait 300 µs to allow the 3-wire interface communication to complete. As an alternative to waiting 300 µs for the 3-wire interface communication to complete, poll the BUSY_3WI bit in the DCDC_CONFIG2 register until it is 0.
6. Write to the DCDC_CONFIG1 register to set up the dc-to-dc converter mode, which enables the dc-to-dc converter. Wait 300 µs to allow the 3-wire interface communication to complete. As an alternative to waiting 300 µs for the 3-wire interface communication to complete, poll the BUSY_3WI bit in the DCDC_CONFIG2 register until it is 0.
7. Write to the DAC_CONFIG register to set the INT_EN bit, which powers up the DAC and internal amplifiers without enabling the channel output, and configure the output range, internal or external R_{SET}, and slew rate. Keep the OUT_EN bit disabled at this point. Wait for a minimum of 500 µs before proceeding to Step 8 to allow the internal calibrations to complete. As an alternative to waiting 500 µs for the internal calibrations to complete, poll the CAL_MEM_UNREFRESHED bit in the DIGITAL_DIAG_RESULTS register until it reads 0.
8. Write a zero-scale DAC code to the DAC_INPUT register. If a bipolar range is selected in Step 7, then a DAC code that represents a 0 mA/0 V output must be written to the DAC_INPUT register. It is important that this step be completed even if the contents of the DAC_INPUT register are not changing.
9. If the LDAC functionality is being used, perform either a software or hardware LDAC command.
10. Rewrite the same word, used in Step 7, to the DAC_CONFIG register with the OUT_EN bit enabled. Allow a minimum of 1.25 ms to pass between Step 6 and Step 9, which is the time from when the dc-to-dc is enabled to when the VI_{OUT} output is enabled.
11. Write the required DAC code to the DAC_INPUT register.

Figure 92 shows an example of a change to the programming sequence.

Changing and Reprogramming the Range

After the output is enabled, take the following steps to change the output range:

1. Write to the DAC_INPUT register. Set the output to 0 mA or 0 V.
2. Write to the DAC_CONFIG register. Disable the output (OUT_EN = 0) and set the new output range. Keep the INT_EN bit set. Wait 500 µs minimum before proceeding to Step 3 to allow time for internal calibrations to complete.
3. Write Code 0x0000 or the case of bipolar ranges, write Code 0x8000 to the DAC_INPUT register. It is important that this step be completed even if the contents of the DAC_INPUT register do not change.
4. Reload the DAC_CONFIG register word from Step 2 and set the OUT_EN bit to 1 to enable the output.
5. Write the required DAC code to the DAC_INPUT register.

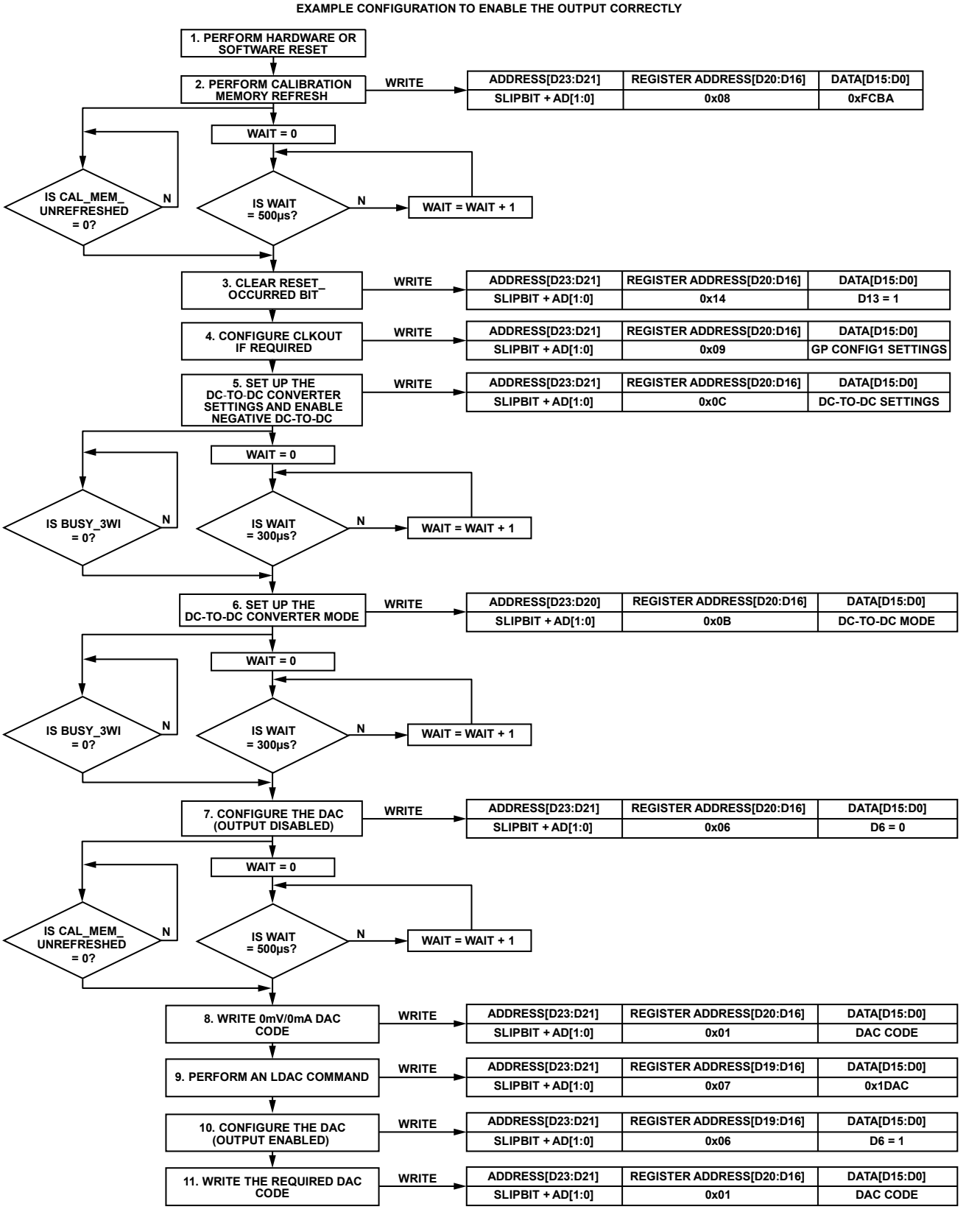


Figure 92. Example Configuration to Enable the Output Correctly (CRC Disabled for Simplicity)

REGISTER DETAILS

Table 26. Register Summary

Address	Name	Description	Reset	Access
0x00	NOP	NOP register.	0x000000	R0/W
0x01	DAC_INPUT	DAC input register.	0x010000	R/W
0x02	DAC_OUTPUT	DAC output register.	0x020000	R
0x03	CLEAR_CODE	Clear code register.	0x030000	R/W
0x04	USER_GAIN	User gain register.	0x04FFFF	R/W
0x05	USER_OFFSET	User offset register.	0x058000	R/W
0x06	DAC_CONFIG	DAC configuration register.	0x060C00	R/W
0x07	SW_LDAC	Software LDAC register.	0x070000	R0/W
0x08	Key	Key register.	0x080000	R0/W
0x09	GP_CONFIG1	General-Purpose Configuration 1 register.	0x090204	R/W
0x0A	GP_CONFIG2	General-Purpose Configuration 2 register.	0x0A0200	R/W
0x0B	DCDC_CONFIG1	DC-to-DC Configuration 1 register.	0x0B0000	R/W
0x0C	DCDC_CONFIG2	DC-to-DC Configuration 2 register.	0x0C0100	R/W
0x0D	GPIO_CONFIG	GPIO configuration register.	0x0D0000	R/W
0x0E	GPIO_DATA	GPIO data register.	0x0E0000	R/W
0x0F	WDT_CONFIG	WDT configuration register.	0x0F0009	R/W
0x10	DIGITAL_DIAG_CONFIG	Digital diagnostic configuration register.	0x10005D	R/W
0x11	ADC_CONFIG	ADC configuration register.	0x110000	R/W
0x12	FAULT_PIN_CONFIG	$\overline{\text{FAULT}}$ pin configuration register.	0x120000	R/W
0x13	TWO_STAGE_READBACK_SELECT	Two stage readback select register.	0x130000	R/W
0x14	DIGITAL_DIAG_RESULTS	Digital diagnostic results register.	0x14A000	R/W-1-C
0x15	ANALOG_DIAG_RESULTS	Analog diagnostic results register.	0x150000	R/W-1-C
0x16	Status	Status register.	0x100000	R
0x17	CHIP_ID	Chip ID register.	0x170101	R
0x18	FREQ_MONITOR	Frequency monitor register.	0x180000	R
0x19	Reserved	Reserved.	0x190000	R
0x1A	Reserved	Reserved.	0x1A0000	R
0x1B	Reserved	Reserved.	0x1B0000	R
0x1C	DEVICE_ID_3	Generic ID register.	0x1C0000	R

NOP Register

Address: 0x00, Reset: 0x000000, Name: NOP

Write 0x0000 to Bits[D15:D0] at this address to perform a no operation (NOP) command. Bits[D15:D0] (see Table 21) of this register always read back as 0x0000.

Table 27. Bit Descriptions for NOP

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	NOP command	Write 0x0000 to perform a NOP command.	0x0	R0/W

DAC Input Register

Address: 0x01, Reset: 0x010000, Name: DAC_INPUT

Bits[D15:D0] consists of the 16-bit data to be written to the DAC. If the $\overline{\text{LDAC}}$ pin is tied low (active), the DAC_INPUT register contents are written directly to the DAC_OUTPUT register without any $\overline{\text{LDAC}}$ functionality dependence. If the $\overline{\text{LDAC}}$ pin is tied high, the contents of the DAC_INPUT register are written to the DAC_OUTPUT register when the $\overline{\text{LDAC}}$ pin is brought low or when the software $\overline{\text{LDAC}}$ command is written.

Table 28. Bit Descriptions for DAC_INPUT

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	DAC_INPUT_DATA	DAC input data.	0x0	R/W

DAC Output Register

Address: 0x02, Reset: 0x020000, Name: DAC_OUTPUT

DAC_OUTPUT is a read only register and contains the latest calibrated 16-bit DAC output value. If a clear event occurs due to a WDT fault, this register contains the clear code until the DAC is updated to another code.

Table 29. Bit Descriptions for DAC_OUTPUT

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	DAC_OUTPUT_DATA	DAC output data. For example, the last calibrated 16-bit DAC output value.	0x0	R

Clear Code Register

Address: 0x03, Reset: 0x030000, Name: CLEAR_CODE

When writing to the CLEAR_CODE register, Bits[D15:D0] consist of the clear code that clears the DAC when a clear event occurs (for example, a WDT fault). After a clear event, the DAC_INPUT register must be rewritten to with the 16-bit data to be written to the DAC, even if it is the same data as previously written before the clear event. Performing an LDAC write to the hardware or software does not update the DAC_OUTPUT register to a new code until the DAC_INPUT register is first written to.

Table 30. Bit Descriptions for CLEAR_CODE

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	CLEAR_CODE	Clear code. The DAC clears to this code upon a clear event, for example, a WDT fault.	0x0	R/W

User Gain Register

Address: 0x04, Reset: 0x04FFFF, Name: USER_GAIN

The 16-bit USER_GAIN register allows the user to adjust the gain of the DAC channel in steps of 1 LSB. The USER_GAIN register coding is straight binary. The default code is 0xFFFF. Theoretically, the gain can be tuned across the full range of the output. However, the maximum recommended gain trim is approximately 50% of the programmed range to maintain accuracy.

Table 31. Bit Descriptions for USER_GAIN

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	USER_GAIN	User gain correction code.	0xFFFF	R/W

User Offset Register

Address: 0x05, Reset: 0x058000, Name: USER_OFFSET

The 16-bit USER_OFFSET register allows the user to adjust the offset of the DAC channel by −32,768 LSBs to +32,768 LSBs in steps of 1 LSB. The USER_OFFSET register coding is straight binary. The default code is 0x8000, which results in zero offset programmed to the output.

Table 32. Bit Descriptions for USER_OFFSET

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	USER_OFFSET	User offset correction code.	0x8000	R/W

DAC Configuration Register

Address: 0x06, Reset: 0x060C00, Name: DAC_CONFIG

The DAC_CONFIG register configures the DAC (range, internal or external R_{SET}, and output enable), enables the output stage circuitry, and configures the slew rate control function.

Table 33. Bit Descriptions for DAC_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:13]	SR_STEP	Slew rate step. In conjunction with the slew rate clock, the slew rate step defines how much the output value changes at each update. Together, both parameters define the rate of change of the output value. 000: 4 LSB (default). 001: 12 LSB. 010: 64 LSB. 011: 120 LSB. 100: 256 LSB. 101: 500 LSB. 110: 1820 LSB. 111: 2048 LSB.	0x0	R/W
[12:9]	SR_CLOCK	Slew rate clock. Slew rate clock defines the rate at which the digital slew is updated. 0000: 240 kHz. 0001: 200 kHz. 0010: 150 kHz. 0011: 128 kHz. 0100: 64 kHz. 0101: 32 kHz. 0110: 16 kHz (default). 0111: 8 kHz. 1000: 4 kHz. 1001: 2 kHz. 1010: 1 kHz. 1011: 512 Hz. 1100: 256 Hz. 1101: 128Hz. 1110: 64 Hz. 1111: 16 Hz.	0x6	R/W
8	SR_EN	Enables slew rate control. 0: disable (default). 1: enable.	0x0	R/W
7	RSET_EXT_EN	Enables external current setting resistor. 0: select internal R_{SET} resistor (default). 1: select external R_{SET} resistor.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
6	OUT_EN	Enables VI_{OUT}. 0: disable VI_{OUT} output (default). 1: enable VI_{OUT} output.	0x0	R/W
5	INT_EN	Enables internal buffers. 0: disable (default). 1: enable. Setting this bit powers up the DAC and internal amplifiers but does not enable the output. It is recommended to set this bit and allow a >200 µs delay before enabling the output. This delay results in a reduced output enable glitch.	0x0	R/W
4	OVRNG_EN	Enables 20% voltage overrange. 0: disable (default). 1: enable.	0x0	R/W
[3:0]	Range	Selects output range. Note that changing the contents of the range bits initiates an internal calibration memory refresh and. Consequently, a subsequent SPI write must not be performed until the CAL_MEM_UNREFRESHED bit in the DIGITAL_DIAG_RESULTS register returns to 0. Writes to invalid range codes are ignored. 0000: 0 V to 5 V voltage range (default). 0001: 0 V to 10 V voltage range. 0010: ±5 V voltage range. 0011: ±10 V voltage range. 1000: 0 mA to 20 mA current range. 1001: 0 mA to 24 mA current range. 1010: 4 mA to 20 mA current range. 1011: ±20 mA current range. 1100: ±24 mA current range. 1101: −1 mA to +22 mA current range.	0x0	R/W

Software LDAC Register

Address: 0x07, Reset: 0x070000, Name: SW_LDAC

Writing 0x1DAC to the SW_LDAC register performs a software LDAC update on the device matching the DUT_ADDRESS, the device address bits AD1 and AD0, bits within the SPI frame. If the GLOBAL_SW_LDAC bit in the GP_CONFIG2 register is set, the DUT_ADDRESS bits are ignored and all devices sharing the same SPI bus are updated via the SW_LDAC command. Bits[15:0] of this register always read back as 0x0000.

Table 34. Bit Descriptions for SW_LDAC

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	LDAC_COMMAND	Software LDAC. Write 0x1DAC to this register to perform a software LDAC instruction.	0x0	R0/W

Key Register

Address: 0x08, Reset: 0x080000, Name: Key

The key register accepts specific key codes to perform tasks such as calibration memory refresh and software reset. Bits[15:0] of this register always read back as 0x0000. All unlisted key codes are reserved.

Table 35. Bit Descriptions for Key

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	KEY_CODE	Key code. 0x15FA: first of two keys to initiate a software reset. 0xAF51: second of two keys to initiate a software reset. 0x1ADC: key to initiate a single ADC conversion on the selected ADC channel. 0x0D06: key to reset the WDT. 0xFCBA: key to initiate a calibration memory refresh to the shadow registers. This key is only valid the first time it is run and has no effect if subsequent writes occur within a given system reset cycle.	0x0	R0/W

General-Purpose Configuration 1 Register

Address: 0x09, Reset: 0x090204, Name: GP_CONFIG1

The GP_CONFIG register configures functions such as the temperature comparator threshold and CLKOUT, as well as enabling other miscellaneous features.

Table 36. Bit Descriptions for GP_CONFIG1

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:14]	RESERVED	Reserved. (Do not alter the default value of this bit)	0x0	R
[13:12]	SET_TEMP_THRESHOLD	Sets the temperature comparator threshold value. 00: 142°C (default). 01: 127°C. 10: 112°C. 11: 97°C.	0x0	R/W
[11:10]	CLKOUT_CONFIG	Configures the CLKOUT pin. 00: disable. No clock is output on the CLKOUT pin (default). 01: enable. Clock is output on the CLKOUT pin according to the CLKOUT_FREQ bits (Bits[9:7]). 10: reserved. Do not select this option. 11: reserved. Do not select this option.	0x0	R/W
[9:7]	CLKOUT_FREQ	Configure the frequency of CLKOUT. 000: 416 kHz. 001: 435 kHz. 010: 454 kHz. 011: 476 kHz. 100: 500 kHz (default). 101: 526 kHz. 110: 555 kHz. 111: 588 kHz.	0x4	R/W
6	HART_EN	Enables the path to the C_{HART} pin. 0: output of the DAC drives the output stage directly (default). 1: C_{HART} path is coupled to the DAC output to allow a HART modem connection or connection of a slew capacitor.	0x0	R/W
5	NEG_OFFSET_EN	Enables negative offset in unipolar V_{OUT} mode. When set, this bit offsets the currently enabled unipolar output range. This bit is only applicable to the 0 V to 6 V range and the 0 V to 12 V range. The 0 V to 6 V range becomes −300 mV to +5.7 V. The 0 V to 12 V range becomes −400 mV to +11.6 V. 0: disable (default). 1: enable.	0x0	R/W
4	CLEAR_NOW_EN	Enables clear to occur immediately, even if the output slew feature is currently enabled. 0: disable (default). 1: enable.	0x0	R/W
3	SPI_DIAG_QUIET_EN	Enables SPI diagnostic quiet mode. When this bit is enabled, SPI_CRC_ERR, SLIPBIT_ERR, and SCLK_COUNT_ERR are not included in the logical OR calculation, which creates the DIG_DIAG_STATUS bit in the status register. They are also masked from affecting the $\overline{\text{FAULT}}$ pin if this bit is set. 0: disable (default). 1: enable.	0x0	R/W
2	OSC_STOP_DETECT_EN	Enables automatic 0x07DEAD code on SDO if the MCLK stops. 0: disable. 1: enable (default).	0x1	R/W
1	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
0	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W

General-Purpose Configuration 2 Register

Address: 0x0A, Reset: 0x0A0200, Name: GP_CONFIG2

The GP_CONFIG2 register configures and enables functions such as the voltage comparators and the global software LDAC.

Table 37. Bit Descriptions for GP_CONFIG2

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the FAULT pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
15	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R0
[14:13]	COMPARATOR_CONFIG	Enables or disables the voltage comparator inputs for test purposes. The temperature comparator is permanently enabled. See the Background Supply and Temperature Monitoring section. 00: disable voltage comparators (default). 01: reserved. 10: reserved. 11: enable voltage comparators. The INT_EN bit in the DAC_CONFIG register must be set to power-up the REFIN buffer and make the REFIN buffer available to the REFIN comparator.	0x0	R/W
12	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
11	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
10	GLOBAL_SW_LDAC	When enabled, the DUT address bits are ignored when performing a software LDAC command, enabling multiple devices to be simultaneously updated using one SW_LDAC command. 0: disable (default). 1: enable.	0x0	R/W
9	FAULT_TIMEOUT	Enables reduced fault detect timeout. This bit configures the delay from when the analog block indicates a VI_{OUT} fault has been detected to the associated change of the relevant bit in the ANALOG_DIAG_RESULTS register. This feature provides flexibility to accommodate a variety of output load values. 0: fault detect timeout = 25 ms. 1: fault detect timeout = 6.5 ms (default).	0x1	R/W
[8:5]	Reserved	Reserved. Do not alter the default value of these bits.	0x0	R/W
4	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
3	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
2	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
1	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
0	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W

DC-to-DC Configuration 1 Register

Address: 0x0B, Reset: 0x0B0000, Name: DCDC_CONFIG1

The DCDC_CONFIG1 register configures the dc-to-dc controller mode.

Table 38. Bit Descriptions for DCDC_CONFIG1

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:8]	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R0
7	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
[6:5]	DCDC_MODE	These two bits configure the dc-to-dc converters. 00: dc-to-dc converter powered off (default). 01: DPC current mode. The positive and negative DPC rails tracks the headroom and footroom of the current output buffer. 10: DPC voltage mode. The positive DPC rail is regulated to 15 V with respect to $-V_{SENSE}$. If enabled, the negative DPC rail is also regulated to −15 V with respect to $-V_{SENSE}$. 11: PPC current mode. V_{DPC+} and V_{DPC-} (if enabled) is regulated to a user programmable level between ±5 V and ±25.677 V (depending on the DCDC_VPROG bits, Bits[4:0]) with respect to $-V_{SENSE}$. If the V_{DPC-} is disabled, the ENABLE_PPC_BUFFERS bit (Bit 11 in the ADC_CONFIG register) must be set prior to enabling PPC current mode.	0x0	R/W
[4:0]	DCDC_VPROG	DC-to-dc programmed voltage in PPC mode. V_{DPC+} and V_{DPC-} is regulated to a user programmable level between ±5 V (0b00000) and ±25.677 V (0b11111), in steps of 0.667 V with respect to $-V_{SENSE}$.	0x0	R/W

DC-to-DC Configuration 2 Register

Address: 0x0C, Reset: 0x0C0100, Name: DCDC_CONFIG2

The DCDC_CONFIG2 register configures various dc-to-dc die features, such as the dc-to-dc converter current limit and the dc-to-dc die node, to be multiplexed to the ADC.

Table 39. Bit Descriptions for DCDC_CONFIG2

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:13]	Reserved	Reserved. Do not alter the default value of these bits.	0x0	R0
12	BUSY_3WI	Three-wire interface busy indicator. 0: 3-wire interface not currently active. 1: 3-wire interface busy.	0x0	R
11	INTR_SAT_3WI	Three-wire interface saturation flag. This flag is set to 1 when the interrupt detection circuitry is automatically disabled due to six consecutive interrupt signals. A write to either of the dc-to-dc configuration registers clears this bit to 0.	0x0	R
10	DCDC_READ_COMP_DIS	Disables 3-wire interface read and compare cycle. This read and compare cycle ensures that copied contents of the dc-to-dc configuration registers on the main die match the dc-to-dc die contents on the. 0: enable automatic read and compare cycle (default). 1: when set, this bit disables the automatic read and compare cycle after each 3-wire interface write.	0x0	R/W
[9:8]	Reserved	Reserved. Do not alter the default value of these bits.	0x1	R/W
7	VIOUT_OV_ERR_DEGLITCH	Adjusts the deglitch time on VI_{OUT} overvoltage error flag. 0: deglitch time set to 1.02 ms (default). 1: deglitch time set to 128 µs.	0x0	R/W
6	VIOUT_PULLDOWN_EN	Enables the 30 kΩ resistor to ground on VI_{OUT}. 0: disable (default). 1: enable.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[5:4]	DCDC_ADC_CONTROL_DIAG	Selects which dc-to-dc die node is multiplexed to the ADC on the main die. 00: AGND on dc-to-dc die. 01: internal 2.5 V supply on dc-to-dc die. 10: AV_{DD1}. 11: reserved. Do not select this option.	0x0	R/W
[3:1]	DCDC_ILIMIT	These three bits set the dc-to-dc converter current limit. 000: 150 mA (default). 001: 200 mA. 010: 250 mA. 011: 300 mA. 100: 350 mA. 101: 400 mA. 110: 400 mA. 111: 400 mA.	0x0	R/W
0	DCDC_NEG_EN	Enables negative dc-to-dc. 0: disable (default). 1: enable.	0x0	R/W

GPIO Configuration Register

Address: 0x0D, Reset: 0x0D0000, Name: GPIO_CONFIG

The GPIO_CONFIG register configures the GPIO pins as either inputs, outputs or 100 kΩ to DGND.

Table 40. Bit Descriptions for GPIO_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:6]	Reserved	Reserved.	0x0	R0
[5:4]	GPIO_2_CFG	Configuration bits for GPIO_2. 00: 100 kΩ to DGND (default). 01: GPO mode. GPIO_2 pin goes to the value of the GPO_2_WRITE bit. 10: GPI mode. GPO_2_READ is the value of the GPIO_2 pin. 11: reserved.	0x0	R/W
[3:2]	GPIO_1_CFG	Configuration bits for GPIO_1. 00: 100 kΩ to DGND (default). 01: GPO mode. GPIO_1 pin goes to value in GPO_1_WRITE bit. 10: GPI mode. GPO_1_READ is the value of the GPI_1 pin. 11: reserved.	0x0	R/W
[1:0]	GPIO_0_CFG	Configuration bits for GPIO_0. 00: 100 kΩ to DGND (default). 01: GPO mode. GPIO_0 pin goes to value in GPO_0_WRITE bit. 10: GPI mode. GPO_0_WRITE is the value of the GPIO_0 pin. 11: reserved.	0x0	R/W

GPIO Data Register

Address: 0x0E, Reset: 0x0E0000, Name: GPIO_DATA

The GPIO_DATA register is used to read and write from and to the GPIO_0, GPIO_1, and GPIO_2 pins.

Table 41. Bit Descriptions for GPIO_DATA

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:6]	Reserved	Reserved.	0x0	R0
5	GPI_2_READ	User readable bit. This bit reflects the logic value on the GPIO_2 pin in GPO and GPI mode.	0x0	R
4	GPO_2_WRITE	User writable bit. This bit reflects the GPIO_2 pin logic value in GPO mode.	0x0	R/W
3	GPI_1_READ	User readable bit. This bit reflects the logic value on the GPIO_1 pin in GPO and GPI mode.	0x0	R
2	GPO_1_WRITE	User writable bit. This bit reflects the GPIO_1 pin logic value in GPO mode.	0x0	R/W
1	GPI_0_READ	User readable bit. This bit reflects the logic value on the GPIO_0 pin in GPO and GPI mode.	0x0	R
0	GPO_0_WRITE	User writable bit. This bit reflects the GPIO_0 pin logic value in GPO mode.	0x0	R/W

WDT Configuration Register

Address: 0x0F, Reset: 0x0F0009, Name: WDT_CONFIG

The WDT_CONFIG register configures the WDT timeout values. This register also configures the acceptable resets for WDT setup and configures the resulting response to a WDT fault, for example, clears the output or resets the device.

Table 42. Bit Descriptions for WDT_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:11]	Reserved	Reserved. Do not alter the default value of these bits.	0x0	R
10	CLEAR_ON_WDT_FAIL	Enable clear on WDT fault. If the WDT times out, a clear event occurs, whereby the output is loaded with the clear code stored in the CLEAR_CODE register. 0: disable (default). 1: enable.	0x0	R/W
9	RESET_ON_WDT_FAIL	Enables a software reset to automatically occur if the WDT times out. 0: disable (default). 1: enable.	0x0	R/W
8	KICK_ON_VALID_WRITE	Enables any valid SPI command to reset the WDT. Any active WDT error flags must be cleared before the WDT can be restarted. 0: disable (default). 1: enable.	0x0	R/W
7	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
6	WDT_EN	Enables the WDT, then starts the WDT, assuming there are no active WDT fault flags. 0: disable (default). 1: enable.	0x0	R/W
[5:4]	Reserved	Reserved. Do not alter the default value of these bits.	0x0	R/W
[3:0]	WDT_TIMEOUT	Sets the WDT timeout value. Setting WDT_TIMEOUT to a binary value beyond 0b1010 results in the default setting of 1 sec. 0000: 1 ms. 0001: 5 ms. 0010: 10 ms. 0011: 25 ms. 0100: 50 ms. 0101: 100 ms. 0110: 250 ms.	0x9	R/W

Bits	Bit Name	Description	Reset	Access
		0111: 500 ms. 1000: 750 ms. 1001: 1 sec (default). 1010: 2 sec.		

Digital Diagnostic Configuration Register

Address: 0x10, Reset: 0x10005D, Name: DIGITAL_DIAG_CONFIG

The DIGITAL_DIAG_CONFIG register configures various digital diagnostic features of interest.

Table 43. Bit Descriptions for DIGITAL_DIAG_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:9]	Reserved	Reserved. Do not alter the default value of these bits.	0x0	R0
[8:7]	Reserved	Reserved. Do not alter the default value of these bits.	0x0	R/W
6	DAC_LATCH_MON_EN	Enables a diagnostic monitor on the DAC latches. This feature monitors the actual digital code driving the DAC and compares the code with the digital code generated within the digital block. Any difference between the two codes causes the DAC_LATCH_MON_ERR flag to be set in the DIGITAL_DIAG_RESULTS register. 0: disable. 1: enable (default).	0x1	R/W
5	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
4	INVERSE_DAC_CHECK_EN	Enables check for DAC code vs. inverse DAC code error. 0: disable. 1: enable (default).	0x1	R/W
3	CAL_MEM_CRC_EN	Enables the CRC of calibration memory on a calibration memory refresh. 0: disable. 1: enable (default).	0x1	R/W
2	FREQ_MON_EN	Enables the internal frequency monitor on the MCLK. 0: disable. 1: enable (default).	0x1	R/W
1	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
0	SPI_CRC_EN	Enables the SPI CRC function. 0: disable. 1: enable (default).	0x1	R/W

ADC Configuration Register

Address: 0x11, Reset: 0x110000, Name: ADC_CONFIG

The ADC_CONFIG register configures the ADC to one of the following four modes of operation: key sequencing, automatic sequencing, single immediate conversion of the currently selected ADC_IP_SELECT node, and single-key conversion.

Table 44. Bit Descriptions for ADC_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address. Do not alter the default value.	0x0	R
[15:12]	Reserved	Reserved. Do not alter the default value of these bits.	0x0	R/W
11	ENABLE_PPC_BUFFERS	Enable the sense buffers for PPC mode.	0x0	R/W
[10:8]	SEQUENCE_COMMAND	ADC sequence command bits. 000: set the depth of the sequencer. The contents of the SEQUENCE_DATA bits correspond to the depth of the sequencer (000 = 1 channel, 001 = 2 channels,…, 111 = 8 channels). 001: set the SEQUENCE_DATA[7:5] bits with the channel number for the selected ADC input, ADC_IP_SELECT[4:0].	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		010: Enable or disable key sequencer mode, depending on the contents of the SEQUENCE_DATA[7:5] bits. SEQUENCE_DATA[7:5] = 001 enables the key sequencer. SEQUENCE_DATA[2:0] ≠ 001 disables the key sequencer. 011: enable/disable automatic sequencer mode, depending on the contents of the SEQUENCE_DATA[2:0] bits. SEQUENCE_DATA[2:0] = 001: enables the automatic sequencer. SEQUENCE_DATA[2:0] ≠ 001: disables the automatic sequencer. 100: initiate a single conversion on the ADC_IP_SELECT (Bits[4:0]) input. This disables autosequencing. The SEQUENCE_DATA bits, Bits[7:5], are not applicable for this command. 101: set up the ADC for future individual ADC conversions (if not using the key sequencer) using the 0x1ADC key code. The SEQUENCE_DATA bits, Bits[7:5], are not applicable for this command. 110: reserved. Do not select this option. 111: reserved. Do not select this option.		
[7:5]	SEQUENCE_DATA	The function of the contents of this field is dependent on the command being issued by the SEQUENCE_COMMAND bits.	0x0	R/W
[4:0]	ADC_IP_SELECT	Selects which node to multiplex to the ADC. All unlisted 5-bit codes are reserved and return an ADC result of zero. 00000: main die temperature. 00001: dc-to-dc die temperature. 00010: reserved. Do not select this option. 00011: REFIN. The INT_EN bit in the DAC_CONFIG register must be set for the REFIN buffer to be powered up and this node to be available to the ADC. 00100: REF2; internal 1.23 V reference voltage. 00101: reserved. Do not select this option. 00110: reserved. Do not select this option. 01100: ADC2 pin input (±15 V input range). 01101: voltage on the $+V_{SENSE}$ buffer output. 01110: voltage on the $-V_{SENSE}$ buffer output 01111: ADC1 pin input (0 V to 1.25 V input range). 10000: ADC1 pin input (0 V to 0.5 V input range). 10001: ADC1 pin input (0 V to 2.5 V input range). 10010: ADC1 pin input (±0.5 V input range). 10011: reserved. Do not select this option. 10100: INT_AVCC. 10101: V_{LDO}. 10110: V_{LOGIC}. 11000: REFGND. 11001: AGND. 11010: DGND. 11011: V_{DPC+}. 11100: AV_{DD2}. 11101: V_{DPC-}. 11110: dc-to-dc die node. Configured in the DCDC_CONFIG2 register. 11111: REFOUT.	0x0	R/W

$\overline{\text{FAULT}}$ Pin Configuration Register

Address: 0x12, Reset: 0x120000, Name: FAULT_PIN_CONFIG

The $\overline{\text{FAULT}}$ register masks particular fault bits from the $\overline{\text{FAULT}}$ pin, if so desired.

Table 45. Bit Descriptions for FAULT_PIN_CONFIG

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
15	INVALID_SPI_ACCESS_ERR	If this bit is set, do not map the INVALID_SPI_ACCESS_ERR fault flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
14	VIOUT_OV_ERR	If this bit is set, do not map the VIOUT_OV_ERR fault flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
13	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
12	INVERSE_DAC_CHECK_ERR	If this bit is set, do not map the INVERSE_DAC_CHECK_ERR flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
11	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
10	OSCILLATOR_STOP_DETECT	If this bit is set, do not map the clock stop error to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
9	DAC_LATCH_MON_ERR	If this bit is set, do not map the DAC_LATCH_MON_ERR fault flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
8	WDT_ERR	If this bit is set, do not map the WDT_ERR flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
7	SLIPBIT_ERR	If this bit is set, do not map the SLIPBIT_ERR error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
6	SPI_CRC_ERR	If this bit is set, do not map the SPI_CRC_ERR error flag to the pin.	0x0	R/W
5	Reserved	Reserved. Do not alter the default value of this bit.	0x0	R/W
4	DCDC_P_SC_ERR	If this bit is set, do not map the positive rail dc-to-dc short circuit error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
3	IOUT_OC_ERR	If this bit is set, do not map the current output open-circuit error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
2	VOUT_SC_ERR	If this bit is set, do not map the voltage output short-circuit error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
1	DCDC-DIE_TEMP_ERR	If this bit is set, do not map the dc-to-dc die temperature error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W
0	MAIN_DIE_TEMP_ERR	If this bit is set, do not map the main die temperature error flag to the $\overline{\text{FAULT}}$ pin.	0x0	R/W

Two-Stage Readback Select Register

Address: 0x13, Reset: 0x130000, Name: TWO_STAGE_READBACK_SELECT

The TWO_STAGE_READBACK_SELECT register selects the address of the register required for a two-stage readback operation. The address of the register selected for readback is stored in Bits[D4:D0].

Table 46. Bit Descriptions for TWO_STAGE_READBACK_SELECT

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:7]	Reserved	Reserved.	0x0	R
[6:5]	READBACK_MODE	These bits control the SPI readback mode. 0: two-stage SPI readback mode (default). 01: autostatus readback mode. The status register contents are shifted out on SDO for every SPI frame. 10: shared $\overline{\text{SYNC}}$ autostatus readback mode. This mode allows the use of a shared $\overline{\text{SYNC}}$ line on multiple devices (distinguished using the hardware address pins). After each valid write to a device, a flag is set. This mode behaves similar to the normal autostatus readback mode, except that the device does not output the status register contents on SDO as $\overline{\text{SYNC}}$ goes low, unless the internal flag is set (previous SPI write is valid). 11: the status register contents and the previous SPI frame instruction are alternately available on SDO.	0x0	R/W
[4:0]	READBACK_SELECT	Selects readback address for a two-stage readback. 0x00: NOP register (default). 0x01: DAC_INPUT register. 0x02: DAC_OUTPUT register. 0x03: CLEAR_CODE register. 0x04: USER_GAIN register.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0x05: USER_OFFSET register. 0x06: DAC_CONFIG register. 0x07: SW_LDAC register. 0x08: key register. 0x09: GP_CONFIG1 register. 0x0A: GP_CONFIG2 register. 0x0B: DCDC_CONFIG1 register. 0x0C: DCDC_CONFIG2 register. 0x0D: GPIO_CONFIG register. 0x0E: GPIO_DATA register. 0x0F: WDT_CONFIG register. 0x10: DIGITAL_DIAG_CONFIG register. 0x11: ADC_CONFIG register. 0x12: FAULT_PIN_CONFIG register. 0x13: TWO_STAGE_READBACK_SELECT register. 0x14: DIGITAL_DIAG_RESULTS register. 0x15: ANALOG_DIAG_RESULTS register. 0x16: Status register. 0x17: CHIP_ID register. 0x18: FREQ_MONITOR register. 0x19: reserved. Do not select this option. 0x1A: reserved. Do not select this option. 0x1B: reserved .Do not select this option. 0x1C: DEVICE_ID_3 register.		

Digital Diagnostic Results Register

Address: 0x14, Reset: 0x14A000, Name: DIGITAL_DIAG_RESULTS

The DIGITAL_DIAG_RESULTS register contains an error flag for the on-chip digital diagnostic features, most of which are configurable using the digital diagnostic configuration register. This register also contains a flag to indicate that a reset occurred, as well as a flag to indicate that the calibration memory has not refreshed or an invalid SPI access attempted. With the exception of the CAL_MEM_UNREFRESHED and SLEW_BUSY flags, all of these flags require a 1 to be written to them to update them to their current value. The CAL_MEM_UNREFRESHED and SLEW_BUSY flags automatically clear when the calibration memory refresh or output slew, respectively, is complete. When the corresponding enable bits in the DIGITAL_DIAG_CONFIG register are not enabled, the respective flag bits read as zero.

Table 47. Bit Descriptions for DIGITAL_DIAG_RESULTS

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
15	CAL_MEM_UNREFRESHED	Calibration memory unrefreshed flag. Modifying the range bits in the DAC_CONFIG register also initiates a calibration memory refresh, which asserts this bit. Unlike the R/W-1-C bits in this register, this bit is automatically cleared after the calibration memory refresh completes. 0: calibration memory is refreshed. 1: calibration memory is unrefreshed (default on power-up). This bit asserts if the range bits are modified in the DAC_CONFIG register.	0x1	R
14	SLEW_BUSY	This flag is set to 1 when the DAC is actively slewing. Unlike the R/W-1-C bits in this register, this bit is automatically cleared when slewing is complete.	0x0	R
13	RESET_OCCURRED	This bit flags that a reset occurred (default on power-up is therefore Logic 1).	0x1	R/W-1-C
12	ERR_3WI	This bit flags an error in the interdie 3-wire interface communications.	0x0	R/W-1-C
11	WDT_ERR	This bit flags a WDT fault.	0x0	R/W-1-C
10	Reserved	Reserved.	0x0	R/W-1-C
9	3WI_RC_ERR	This bit flags an error if the 3-wire read and compare process is enabled and a parity error occurs.	0x0	R/W-1-C
8	DAC_LATCH_MON_ERR	This bit flags if the output of the DAC latches does not match the input.	0x0	R/W-1-C

Bits	Bit Name	Description	Reset	Access
7	Reserved	Reserved.	0x0	R/W-1-C
6	INVERSE_DAC_CHECK_ERR	This bit flags if a fault it detected between the DAC code driven by the digital core and an inverted copy.	0x0	R/W-1-C
5	CAL_MEM_CRC_ERR	This bit flags a CRC error for the CRC calculation of the calibration memory upon refresh.	0x0	R/W-1-C
4	INVALID_SPI_ACCESS_ERR	This bit flags if an invalid SPI access is attempted, such as writing to or reading from an invalid or reserved address. This bit also flags if an SPI write is attempted directly after powering up but before a calibration memory refresh is performed or if an SPI write is attempted while a calibration memory refresh is in progress. Performing a two stage readback is permitted during a calibration memory refresh and does not cause this flag to set. Attempting to write to a read only register also causes this bit to assert.	0x0	R/W-1-C
3	Reserved	Reserved.	0x0	R/W-1-C
2	SCLK_COUNT_ERR	This bit flags an SCLK falling edge count error. 32 clocks are required if SPI CRC is enabled and 24 clocks or 32 clocks are required if SPI CRC is not enabled.	0x0	R/W-1-C
1	SLIPBIT_ERR	This bit flags an SPI frame slip bit error, that is, the MSB of the SPI word is not equal to the inverse of MSB − 1.	0x0	R/W-1-C
0	SPI_CRC_ERR	This bit flags an SPI CRC error.	0x0	R/W-1-C

Analog Diagnostic Results Register

Address: 0x15, Reset: 0x150000, Name: ANALOG_DIAG_RESULTS

The ANALOG_DIAG_RESULTS register contains an error flag corresponding to the four voltage nodes (V_{LDO}, INT_AVCC, REFIN, and REFOUT) monitored in the background by comparators, as well as a flag for the main die temperature, which is also monitored by a comparator. Voltage output short circuit, current output open circuit, and dc-to-dc error flags are also contained in this register. Like the DIGITAL_DIAG_RESULTS register, all of the flags contained in this register require a 1 to be written to them to update or clear them. When the corresponding diagnostic features are not enabled, the respective error flags are read as zero.

Table 48. Bit Descriptions for ANALOG_DIAG_RESULTS

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:14]	Reserved	Reserved.	0x0	R0
13	VIOUT_OV_ERR	This bit flags if the voltage at the VI_{OUT} pin goes outside of the V_{DPC+} rail or AV_{SS} rail.	0x0	R/W-1-C
12	Reserved	Reserved.	0x0	R/W-1-C
11	DCDC_P_SC_ERR	This bit flags a dc-to-dc short-circuit error for the positive rail dc-to-dc circuit.	0x0	R/W-1-C
10	Reserved	Reserved.	0x0	R/W-1-C
9	DCDC_P_PWR_ERR	This bit flags a dc-to-dc regulation fault, that is, the dc-to-dc circuitry cannot reach the target V_{DPC+} voltage due to an insufficient AV_{DD1} voltage.	0x0	R/W-1-C
8	Reserved	Reserved.	0x0	R/W-1-C
7	IOUT_OC_ERR	This bit flags a current output open circuit error. This error bit is set in the case of a current output open circuit and in the case where there is insufficient headroom available to the internal current output driver circuitry to provide the programmed output current.	0x0	R/W-1-C
6	VOUT_SC_ERR	This bit flags a voltage output short-circuit error.	0x0	R/W-1-C
5	DCDC_DIE_TEMP_ERR	This bit flags an overtemperature error for the dc-to-dc die.	0x0	R/W-1-C
4	MAIN_DIE_TEMP_ERR	This bit flags an overtemperature error for the main die.	0x0	R/W-1-C
3	REFOUT_ERR	This bit flags that the REFOUT node is outside of the comparator threshold levels or if the short-circuit current limit occurs.	0x0	R/W-1-C
2	REFIN_ERR	This bit flags that the REFIN node is outside of the comparator threshold levels.	0x0	R/W-1-C
1	INT_AVCC_ERR	This bit flags that the INT_AVCC node is outside of the comparator threshold levels.	0x0	R/W-1-C
0	VLDO_ERR	This bit flags that the V_{LDO} node is outside of the comparator threshold levels or if the short-circuit current limit occurs.	0x0	R/W-1-C

Status Register

Address: 0x16, Reset: 0x100000, Name: Status

The Status register contains ADC data and status bits, as well as the WDT, OR'ed analog and digital diagnostics, and the $\overline{\text{FAULT}}$ pin status bits.

Table 49. Bit Descriptions for Status

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
20	DIG_DIAG_STATUS	This bit represents the result of a logical OR of the contents of Bits[15:0] in the DIGITAL_DIAG_RESULTS register, with the exception of the SLEW_BUSY bit. Therefore, if any of these bits are high, the DIG_DIAG_STATUS bit is high. Note that this bit is high on power-up due to the active RESET_OCCURRED flag. A quiet mode is also available (SPI_DIAG_QUIET_EN in the GP_CONFIG1 register), such that the logical OR function only incorporates Bits[D15:D3] of the DIGITAL_DIAG_RESULTS register (with the exception of the SLEW_BUSY bit). If an SPI CRC, SPI slip bit, or SCLK count error occurs, the DIG_DIAG_STATUS bit is not set high.	0x1	R
19	ANA_DIAG_STATUS	This bit represents the result of a logical OR of the contents of Bits[13:0] in the ANALOG_DIAG_RESULTS register. Therefore, if any bit in this register is high, the ANA_DIAG_STATUS bit is high.	0x0	R
18	WDT_STATUS	WDT status bit.	0x0	R
17	ADC_BUSY	ADC busy status bit.	0x0	R
[16:12]	ADC_CH	Address of the ADC channel represented by the ADC_DATA bits in the status register.	0x0	R
[11:0]	ADC_DATA	12 bits of ADC data representing the converted signal addressed by the ADC_CH bits, Bits[16:12].	0x0	R

Chip ID Register

Address: 0x17, Reset: 0x170101, Name: CHIP_ID

The CHIP_ID register contains the silicon revision ID of both the main die and the dc-to-dc die.

Table 50. Bit Descriptions for CHIP_ID

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:11]	Reserved	Reserved.	0x0	R0
[10:8]	DCDC_DIE_CHIP_ID	These bits reflect the silicon revision number of the dc-to-dc die.	0x2	R
[7:0]	MAIN_DIE_CHIP_ID	These bits reflect the silicon revision number of the main die.	0x2	R

Frequency Monitor Register

Address: 0x18, Reset: 0x180000, Name: FREQ_MONITOR

An internal frequency monitor uses the MCLK to create a pulse at a frequency of 1 kHz (MCLK/10,000). This pulse is used to increment a 16-bit counter. The value of the counter is available to read in the FREQ_MONITOR register. The user can poll this register periodically and use it both as a diagnostic tool for the internal oscillator (to monitor that the oscillator is running) and to measure the frequency. This feature is enabled by default via the FREQ_MON_EN bit in the DIGITAL_DIAG_CONFIG register.

Table 51. Bit Descriptions for FREQ_MONITOR

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:0]	FREQ_MONITOR	Internal clock counter value.	0x0	R

Generic ID Register

Address: 0x1C, Reset: 0x1C0000, Name: DEVICE_ID_3

Table 52. Bit Descriptions for DEVICE_ID_3

Bits	Bit Name	Description	Reset	Access
21	FAULT_PIN_STATUS	The FAULT_PIN_STATUS bit reflects the inverted current status of the $\overline{\text{FAULT}}$ pin.	0x0	R
[20:16]	REGISTER_ADDRESS	Register address.	0x0	R
[15:8]	Reserved	Reserved.	0x0	R
[7:3]	Reserved	Reserved.	0x0	R
[2:0]	Generic ID	Generic ID. 000: reserved. 001: reserved. 010: AD5753. 011: reserved. 100: reserved. 101: reserved. 110: reserved. 111: reserved.	0x0	R

APPLICATIONS INFORMATION

EXAMPLE MODULE POWER CALCULATION

Using the example module shown in Figure 93, the power dissipation (excluding the power dissipated in the load) of the module can be calculated using the methodology shown in the Power Calculation Methodology (R_{LOAD} = 1 kΩ) section. Assuming a maximum I_{OUT} value of 20 mA and R_{LOAD} value of 1 kΩ, the total module power is calculated as approximately 226 mW. The power associated with the external digital isolation is not included in the calculations because this power is dependent on the choice of component used.

Replacing the 1 kΩ load with a short circuit, the power dissipation calculation is shown in the Power Calculation Methodology (R_{LOAD} = 0 Ω) section, which shows that the total module power becomes approximately 206 mW in a short-circuit load condition.

Power Calculation Methodology (R_{LOAD} = 1 kΩ)

Table 53. Quiescent Current Power Calculation

Voltage (V)	Current (mA)	Power (mW)
AV_{DD1} = 24	AI_{DD1} = 0.05	1.2
AV_{DD2} = 5	AI_{DD2} = 2.9	14.5
AV_{SS} = −15	AI_{SS} = 0.23	3.45
V_{LOGIC} = 3.3	I_{LOGIC} = 0.01	0.033

Using the voltage and current values in Table 53, the total quiescent current power is 19.18 mW.

Next, perform the following calculation:

$$(V_{DPC+}) \times (20\ mA + I_{DPC+}) = 22.5\ V \times 20.5\ mA = 461.25\ mW$$

Assume the dc-to-dc converter is at 90% efficiency. Therefore, V_{DPC+} power = 512.5 mW. The total input power at the AD5753 side of the isolated dc-to-dc power module is therefore 512.5 mW + 19.18 mW = 531.68 mW. Subtracting the 400 mW load power from this value gives the power associated only with the AD5753, which is 131.68 mW.

Assuming an 85% efficiency isolated, dc-to-dc power module, the total input power becomes 625.5 mW (see Figure 93).

Total Module Power = Input Power − Load Power

Therefore, the equation is as follows:

625.5 mW − 400 mW = 225.5 mW

Power Calculation Methodology (R_{LOAD} = 0 Ω)

Using the voltage and current values in Table 53, the total quiescent current power is 19.18 mW.

Next, use the following equation:

$$(V_{DPC+}) \times (20\ mA + I_{DPC+}) = 4.95\ V \times 20.5\ mA = 101.5\ mW$$

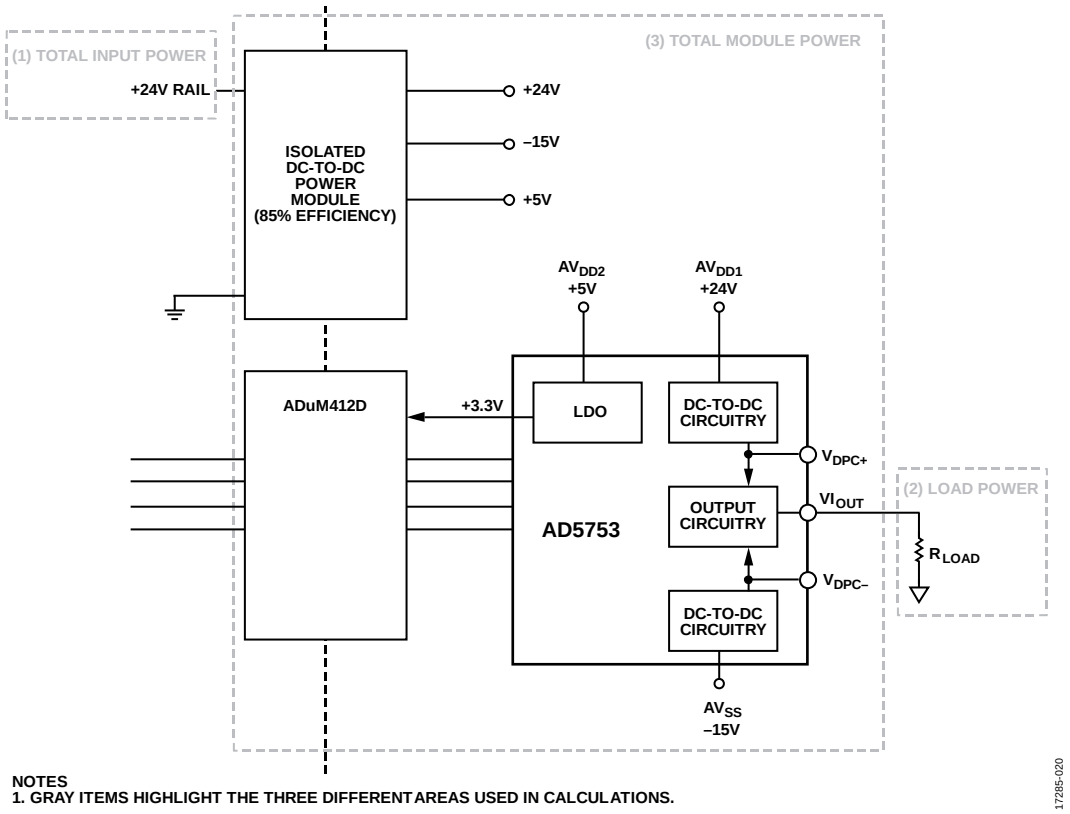
Assume dc-to-dc converter at 65% efficiency. Therefore, V_{DPC+} power = 156.2 mW. The total input power at the AD5753 side of the isolated dc-to-dc power module is therefore 156.2 mW + 19.18 mW = 175.38 mW. Subtracting the 0 mW load power from this value gives the power associated only with the AD5753, which is 175.38 mW.

Assuming an 85% efficiency isolated, dc-to-dc power module, the total input power becomes 206.33 mW (see Figure 93).

Total Module Power = Input Power − Load Power

Therefore, the equation is as follows:

206.33 mW − 0 mW = 206.33 mW



NOTES
1. GRAY ITEMS HIGHLIGHT THE THREE DIFFERENT AREAS USED IN CALCULATIONS.

Figure 93. Example Module Containing the AD5753

OUTLINE DIMENSIONS

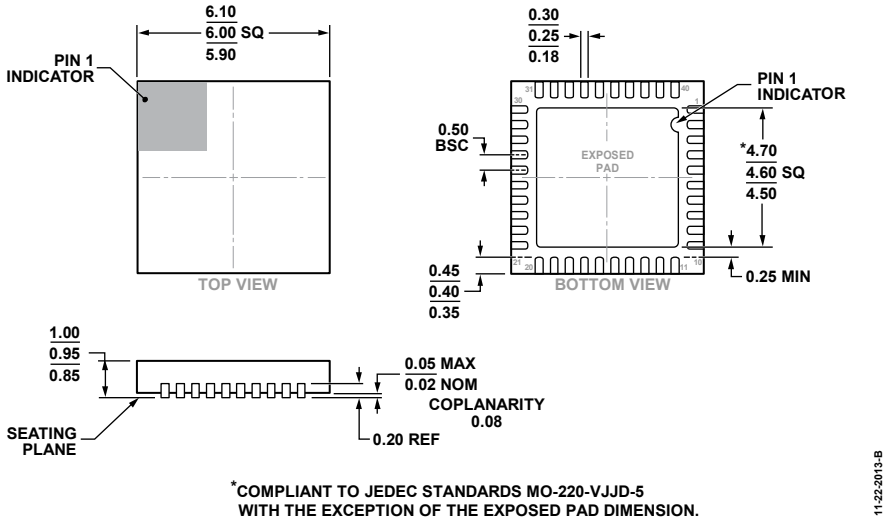


Figure 94. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-40-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5753BCPZ-REEL	−40°C to +115°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
AD5753BCPZ-RL7	−40°C to +115°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
EVAL-AD5753SDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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