THE DATASHEET OF

ADG1409SRUZ-EP

4 Ω R_{ON}, 4-/8-Channel ±15 V/+12 V/±5 V *i*CMOS Multiplexers

Enhanced Product

ADG1408-EP/ADG1409-EP

FEATURES

- 4.7 Ω maximum on resistance @ 25°C
- 0.5 Ω on resistance flatness
- Up to 190 mA continuous current
- Fully specified at ±15 V/+12 V/±5 V
- 3 V logic-compatible inputs
- Rail-to-rail operation
- Break-before-make switching action
- 16-lead TSSOP

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- One assembly and test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

FUNCTIONAL BLOCK DIAGRAM

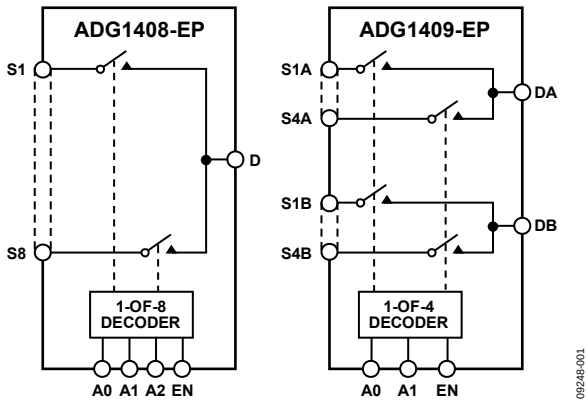

Figure 1.

GENERAL DESCRIPTION

The ADG1408-EP/ADG1409-EP are monolithic *i*CMOS® analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG1408-EP switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2. The ADG1409-EP switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines, A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off.

The *i*CMOS (industrial CMOS) modular manufacturing process combines high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow on resistance and on resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications where low distortion is critical. *i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

Full details about this enhanced product are available in the ADG1408/ADG1409 data sheet, which should be consulted in conjunction with this data sheet.

PRODUCT HIGHLIGHTS

1. 4 Ω on resistance
2. 0.5 Ω on resistance flatness
3. 3 V logic-compatible digital input, V_{INH} = 2.0 V, V_{INL} = 0.8 V
4. 16-lead TSSOP package

Rev. B

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REVISION HISTORY

11/2017—Rev. A to Rev. B

Changes to Ordering Guide 16

8/2017—Rev. 0 to Rev. A

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3/2011—Revision 0: Initial Version

SPECIFICATIONS

15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	4		Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 12
	4.7	6.7	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between	0.2		Ω typ	V_S = ±10 V, I_S = −10 mA
Channels (ΔR_{ON})	0.78	1.1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	V_S = ±10 V, I_S = −10 mA
	0.72	0.92	Ω max	
LEAKAGE CURRENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.04		nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 13
	±0.2	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.04		nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 13
	±0.45	±30	nA max	
Channel On Leakage, I_D, I_S (On)	±0.1		nA typ	V_S = V_D = ±10 V; see Figure 14
	±1.5	±30	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current	±0.005		μA typ	V_{IN} = V_{GND} or V_{DD}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	4		pF typ	
DYNAMIC CHARACTERISTICS[1]				
Transition Time, $t_{TRANSITION}$	140		ns typ	R_L = 100 Ω, C_L = 35 pF
	170	240	ns max	V_S = 10 V, see Figure 15
Break-Before-Make Time Delay, t_{BBM}	50		ns typ	R_L = 100 Ω, C_L = 35 pF
		19	ns min	V_{S1} = V_{S2} = 10 V; see Figure 16
t_{ON} (EN)	100		ns typ	R_L = 100 Ω, C_L = 35 pF
	120	165	ns max	V_S = 10 V; see Figure 17
t_{OFF} (EN)	100		ns typ	R_L = 100 Ω, C_L = 35 pF
	120	170	ns max	V_S = 10 V; see Figure 17
Charge Injection	−50		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 18
Off Isolation	−70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
Channel-to-Channel Crosstalk	−70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 20
Total Harmonic Distortion, THD + N	0.025		% typ	R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 22
−3 dB Bandwidth				R_L = 50 Ω, C_L = 5 pF; see Figure 21
ADG1408-EP	60		MHz typ	
ADG1409-EP	115		MHz typ	
Insertion Loss	0.24		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 21
C_S (Off)	14		pF typ	f = 1 MHz
C_D (Off)				
ADG1408-EP	80		pF typ	f = 1 MHz
ADG1409-EP	40		pF typ	f = 1 MHz
C_D, C_S (On)				
ADG1408-EP	135		pF typ	f = 1 MHz
ADG1409-EP	90		pF typ	f = 1 MHz

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.002		µA typ	Digital inputs = 0 V or V_{DD}
		1	µA max	
	220		µA typ	Digital inputs = 5 V
		420	µA max	
I_{SS}	0.002		µA typ	Digital inputs = 0 V, 5 V or V_{DD}
		1	µA max	
V_{DD}/V_{SS}		±4.5/±16.5	V min/max	

[1] Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance (R_{ON})	6		Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 12
	8	11.2	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match	0.2		Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
Between Channels (ΔR_{ON})	0.82	1.1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	1.5		Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	2.5	2.8	Ω max	
LEAKAGE CURRENTS				V_{DD} = 13.2 V
Source Off Leakage, I_S (Off)	±0.04		nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 13
	±0.2	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.04		nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 13
	±0.45	±37	nA max	
Channel On Leakage, I_D, I_S (On)	±0.06		nA typ	V_S = V_D = 1 V or 10 V; see Figure 14
	±0.44	±32	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current	±0.005		μA typ	V_{IN} = V_{GND} or V_{DD}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	5		pF typ	
DYNAMIC CHARACTERISTICS[1]				
Transition Time, $t_{TRANSITION}$	200		ns typ	R_L = 100 Ω, C_L = 35 pF
	260	380	ns max	V_S = 8 V; see Figure 15
Break-Before-Make Time Delay, t_{BBM}	90		ns typ	R_L = 100 Ω, C_L = 35 pF
		40	ns min	V_{S1} = V_{S2} = 8 V; see Figure 16
t_{ON} (EN)	160		ns typ	R_L = 100 Ω, C_L = 35 pF
	210	285	ns max	V_S = 8 V; see Figure 17
t_{OFF} (EN)	115		ns typ	R_L = 100 Ω, C_L = 35 pF
	145	200	ns max	V_S = 8 V; see Figure 17
Charge Injection	−12		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 18
Off Isolation	−70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
Channel-to-Channel Crosstalk	−70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 20
−3 dB Bandwidth				R_L = 50 Ω, C_L = 5 pF; see Figure 21
ADG1408-EP	36		MHz typ	
ADG1409-EP	72		MHz typ	
Insertion Loss	0.5		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 21
C_S (Off)	25		pF typ	f = 1 MHz
C_D (Off)				
ADG1408-EP	165		pF typ	f = 1 MHz
ADG1409-EP	80		pF typ	f = 1 MHz
C_D, C_S (On)				
ADG1408-EP	200		pF typ	f = 1 MHz
ADG1409-EP	120		pF typ	f = 1 MHz

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS				V_{DD} = 13.2 V
I_{DD}	0.002		µA typ	Digital inputs = 0 V or V_{DD}
		1	µA max	
	220		µA typ	Digital inputs = 5 V
		420	µA max	
V_{DD}		5/16.5	V min/max	V_{SS} = 0 V, GND = 0 V

[1] Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	7		Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 12
	9	12	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance Match Between	0.3		Ω typ	V_S = ±4.5 V, I_S = −10 mA
Channels (ΔR_{ON})	0.78	1.1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	1.5		Ω typ	V_S = ±4.5 V; I_S = −10 mA
	2.5	3	Ω max	
LEAKAGE CURRENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.02		nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 13
	±0.2	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.02		nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 13
	±0.45	±20	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04		nA typ	V_S = V_D = ±4.5 V; see Figure 14
	±0.3	±22	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current	±0.005		μA typ	V_{IN} = V_{GND} or V_{DD}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	5		pF typ	
DYNAMIC CHARACTERISTICS[1]				
Transition Time, $t_{TRANSITION}$	330		ns typ	R_L = 100 Ω, C_L = 35 pF
	440	550	ns max	V_S = 5 V; see Figure 15
Break-Before-Make Time Delay, t_{BBM}	100		ns typ	R_L = 100 Ω, C_L = 35 pF
		45	ns min	V_{S1} = V_{S2} = 5 V; see Figure 16
t_{ON} (EN)	245		ns typ	R_L = 100 Ω, C_L = 35 pF
	330	440	ns max	V_S = 5 V; see Figure 17
t_{OFF} (EN)	215		ns typ	R_L = 100 Ω, C_L = 35 pF
	285	370	ns max	V_S = 5 V; see Figure 17
Charge Injection	−10		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 18
Off Isolation	−70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
Channel-to-Channel Crosstalk	−70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 20
Total Harmonic Distortion, THD + N	0.06		% typ	R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 22
−3 dB Bandwidth				R_L = 50 Ω, C_L = 5 pF; see Figure 21
ADG1408-EP	40		MHz typ	
ADG1409-EP	80		MHz typ	
Insertion Loss	0.5		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 21
C_S (Off)	20		pF typ	f = 1 MHz
C_D (Off)				
ADG1408-EP	130		pF typ	f = 1 MHz
ADG1409-EP	65		pF typ	f = 1 MHz
C_D, C_S (On)				
ADG1408-EP	180		pF typ	f = 1 MHz
ADG1409-EP	120		pF typ	f = 1 MHz

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001		µA typ	Digital inputs = 0 V or V_{DD}
		1	µA max	
I_{SS}	0.001		µA typ	Digital inputs = 0 V, 5 V or V_{DD}
		1	µA max	
V_{DD}/V_{SS}		±4.5/±16.5	V min/max	

[1] Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 4.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, S or D[1]					
15 V Dual Supply					V_{DD} = +13.5 V, V_{SS} = −13.5 V
ADG1408-EP	190	105	50	mA max	
ADG1409-EP	140	85	45	mA max	
12 V Single Supply					V_{DD} = 10.8 V, V_{SS} = 0 V
ADG1408-EP	160	95	50	mA max	
ADG1409-EP	120	75	40	mA max	
5 V Dual Supply					V_{DD} = +4.5 V, V_{SS} = −4.5 V
ADG1408-EP	155	90	45	mA max	
ADG1409-EP	115	70	40	mA max	

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs, Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Continuous Current, S or D	Table 4 data + 10%
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	350 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA}	150.4°C/W
θ_{JC}	50°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

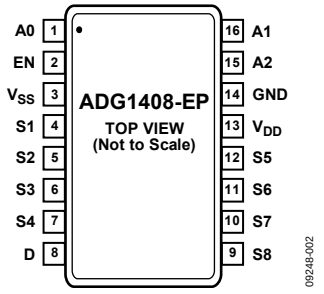

Figure 2. ADG1408-EP Pin Configuration

Table 6. ADG1408-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single supply applications, it can be connected to ground.
4	S1	Source Terminal 1. Can be an input or an output.
5	S2	Source Terminal 2. Can be an input or an output.
6	S3	Source Terminal 3. Can be an input or an output.
7	S4	Source Terminal 4. Can be an input or an output.
8	D	Drain Terminal. Can be an input or an output.
9	S8	Source Terminal 8. Can be an input or an output.
10	S7	Source Terminal 7. Can be an input or an output.
11	S6	Source Terminal 6. Can be an input or an output.
12	S5	Source Terminal 5. Can be an input or an output.
13	V_{DD}	Most Positive Power Supply Potential.
14	GND	Ground (0 V) Reference.
15	A2	Logic Control Input.
16	A1	Logic Control Input.

Table 7. ADG1408-EP Truth Table

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

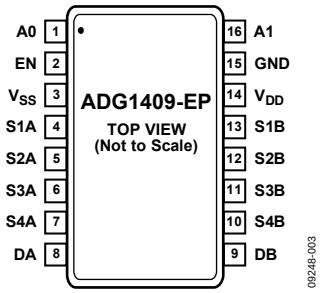

Figure 3. ADG1409-EP Pin Configuration (TSSOP)

Table 8. ADG1409-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single supply applications, it can be connected to ground.
4	S1A	Source Terminal 1A. Can be an input or an output.
5	S2A	Source Terminal 2A. Can be an input or an output.
6	S3A	Source Terminal 3A. Can be an input or an output.
7	S4A	Source Terminal 4A. Can be an input or an output.
8	DA	Drain Terminal A. Can be an input or an output.
9	DB	Drain Terminal B. Can be an input or an output.
10	S4B	Source Terminal 4B. Can be an input or an output.
11	S3B	Source Terminal 3B. Can be an input or an output.
12	S2B	Source Terminal 2B. Can be an input or an output.
13	S1B	Source Terminal 1B. Can be an input or an output.
14	V_{DD}	Most Positive Power Supply Potential.
15	GND	Ground (0 V) Reference.
16	A1	Logic Control Input.

Table 9. ADG1409-EP Truth Table

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TYPICAL PERFORMANCE CHARACTERISTICS

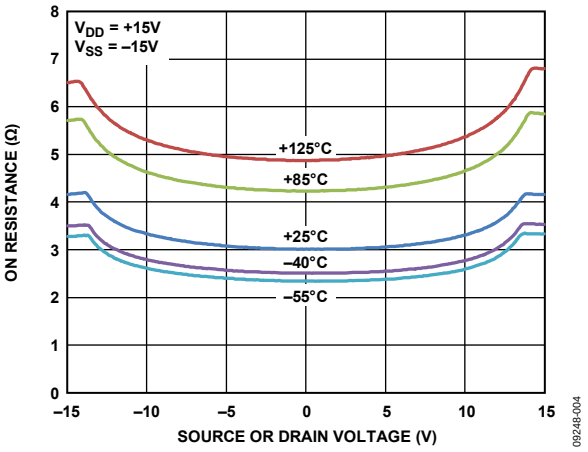

Figure 4. On Resistance vs. V_D, V_S for Different Temperatures; 15 V Dual Supply

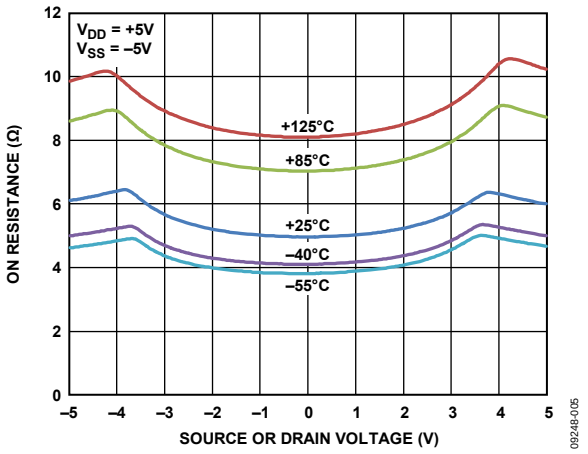

Figure 5. On Resistance vs. V_D, V_S for Different Temperatures; 5 V Dual Supply

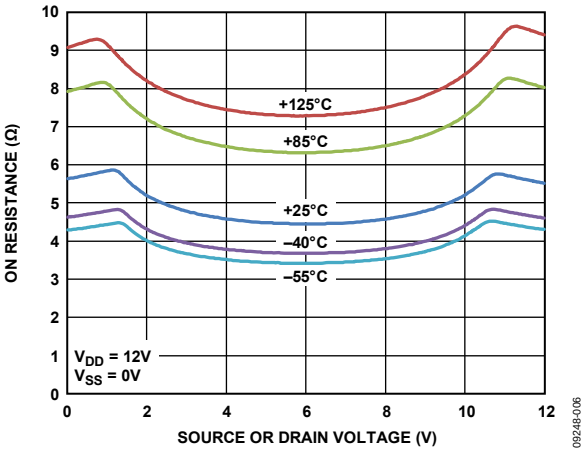

Figure 6. On Resistance vs. V_D, V_S for Different Temperatures; 12 V Single Supply

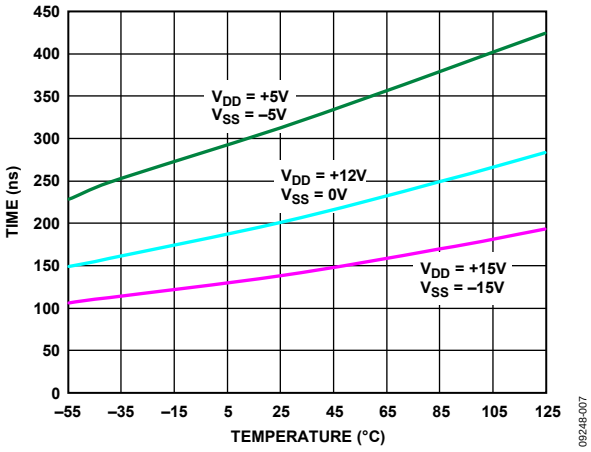

Figure 7. Transition Time vs. Temperature

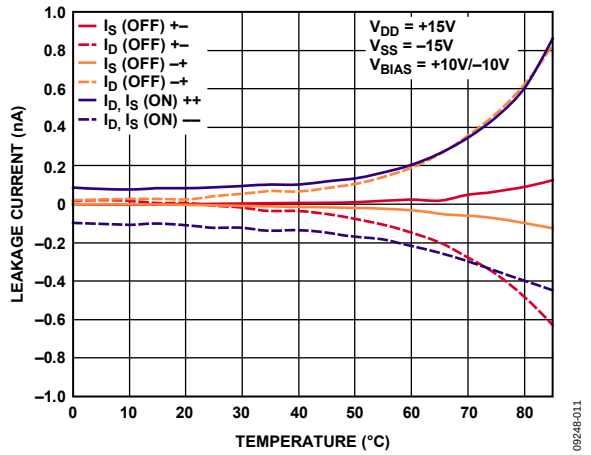

Figure 8. Leakage Current vs. Temperature; 15 V Dual Supply

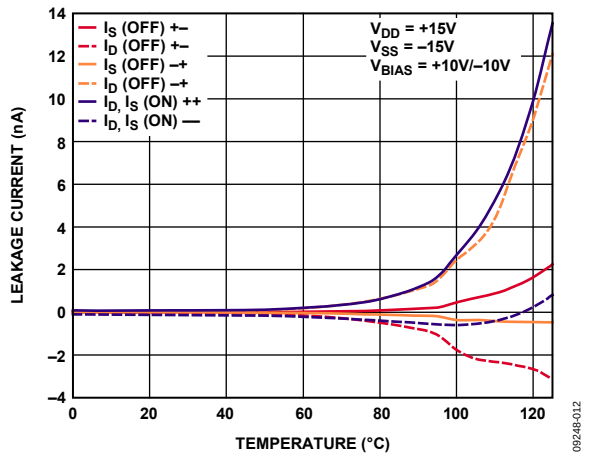

Figure 9. Leakage Current vs. Temperature; 15 V Dual Supply

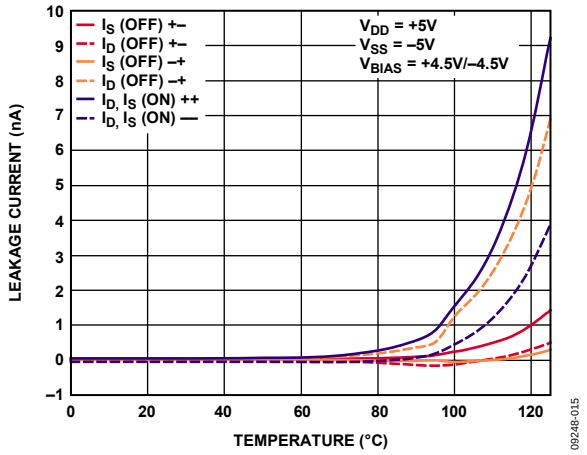

Figure 10. Leakage Current vs. Temperature; 5 V Dual Supply

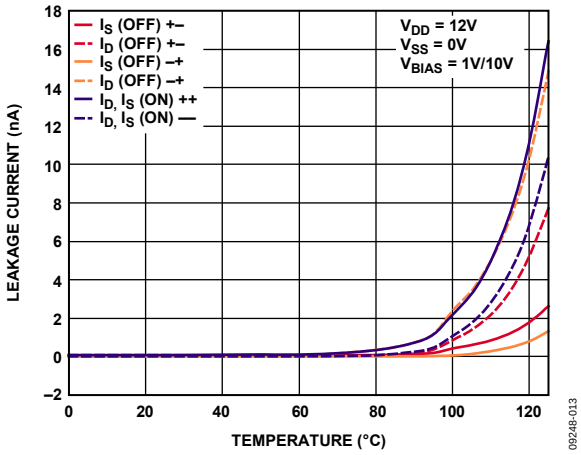

Figure 11. Leakage Current vs. Temperature; 12 V Single Supply

TEST CIRCUITS

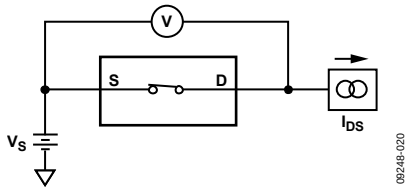

Figure 12. On Resistance

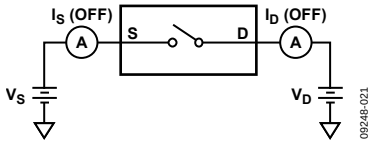

Figure 13. Off Leakage

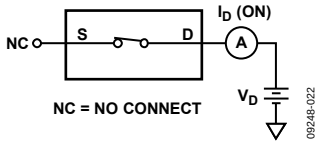

Figure 14. On Leakage

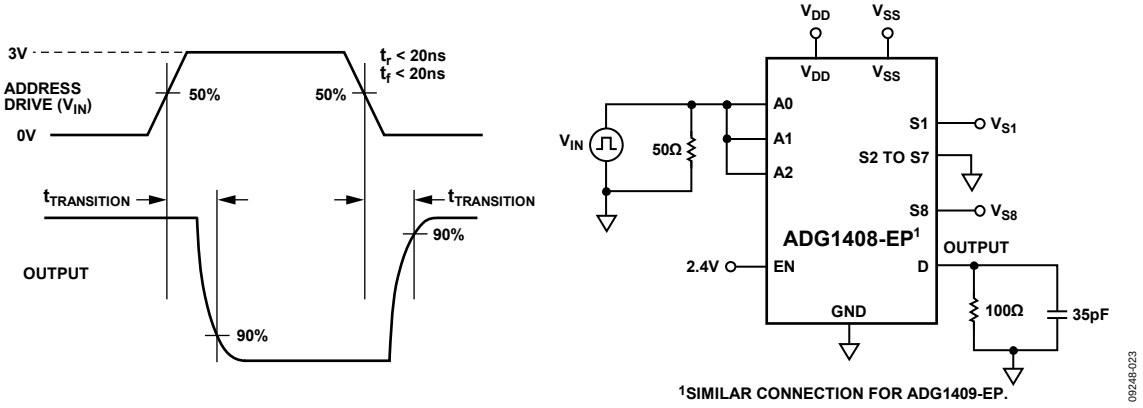

Figure 15. Address to Output Switching Times, $t_{TRANSITION}$

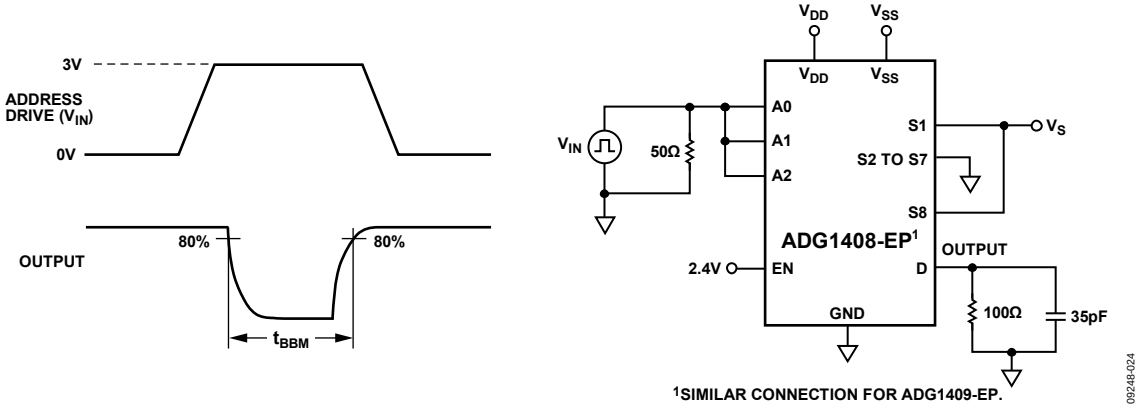

Figure 16. Break-Before-Make Delay, t_{BBM}

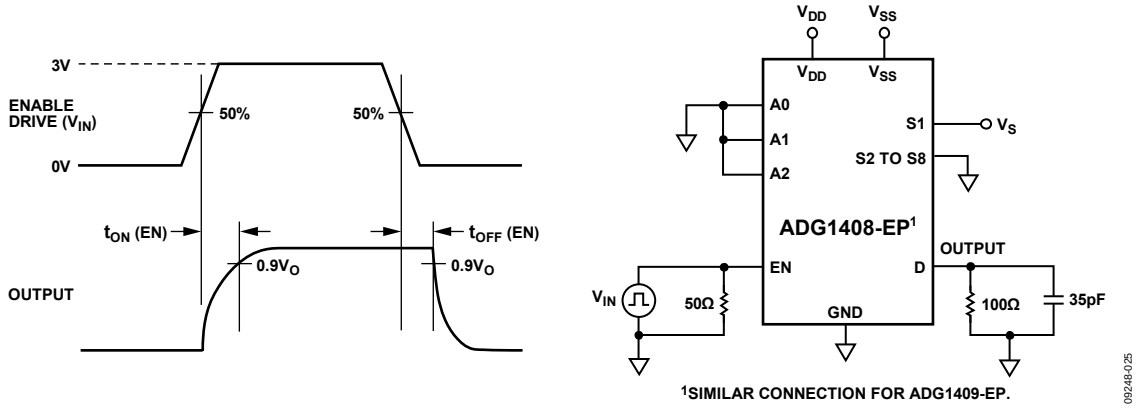

Figure 17. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

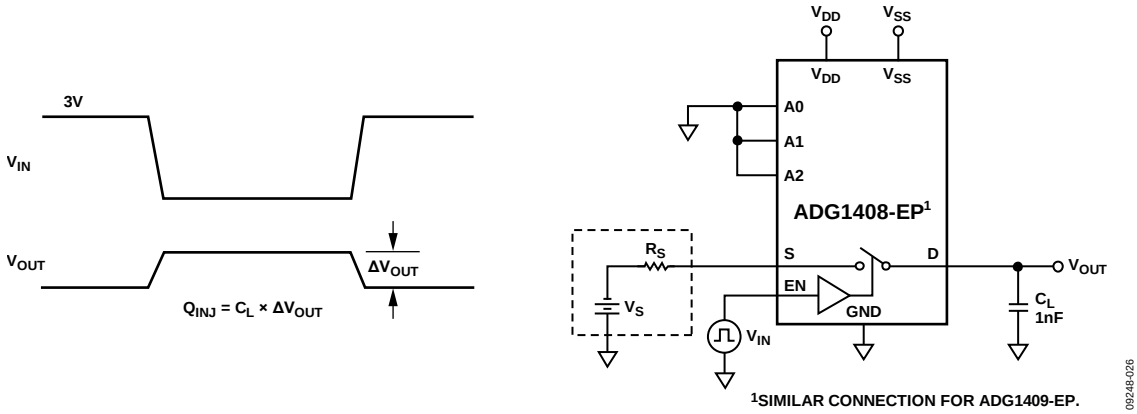

Figure 18. Charge Injection

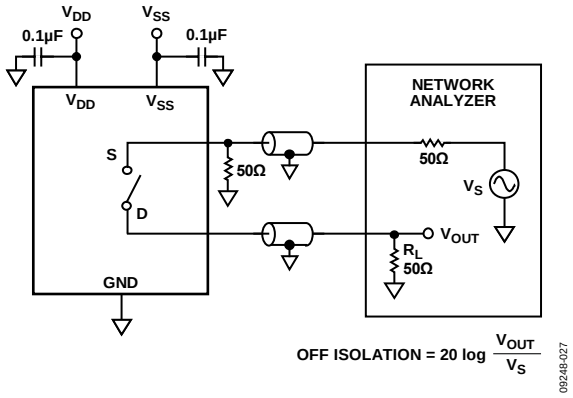

Figure 19. Off Isolation

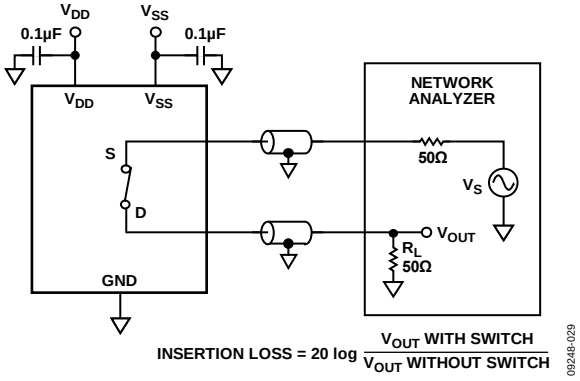

Figure 21. Insertion Loss

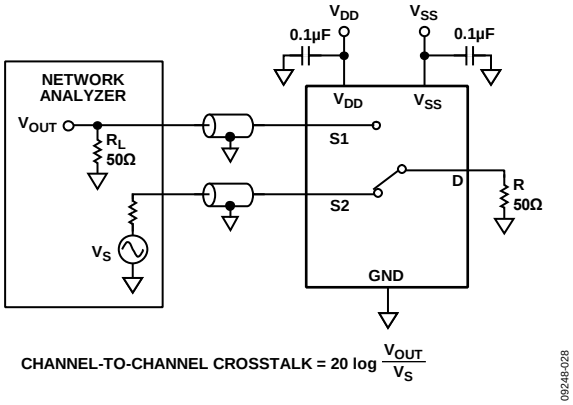

Figure 20. Channel-to-Channel Crosstalk

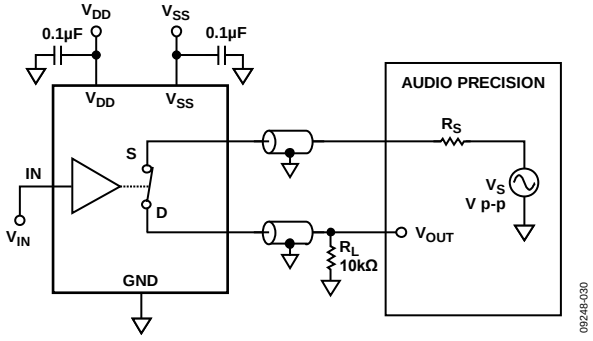

Figure 22. THD + Noise

OUTLINE DIMENSIONS

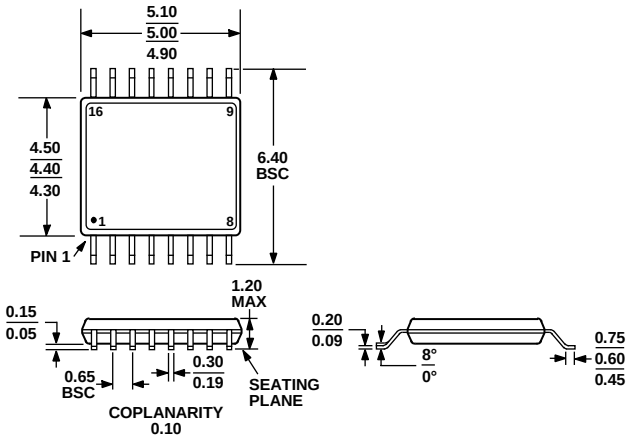

Figure 23. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG1408SRUZ-EP	−55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1408SRUZ-EP-RL7	−55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1408SRU-EP	−55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1408SRU-EP-RL7	−55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1409SRUZ-EP	−55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1409SRUZ-EP-RL7	−55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1409SRU-EP	−55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1409SRU-EP-RL7	−55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

[1] Z = RoHS Compliant Part.

D09248-0-11/17(B)

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