



# THE DATASHEET OF BSC0909NS

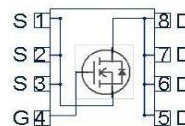


**OptiMOS™ Power-MOSFET**
**Features**

- Optimized for 5V driver application (Notebook, VGA, POL)
- Low FOM<sub>SW</sub> for High Frequency SMPS
- 100% Avalanche tested
- Improved switching behaviour
- N-channel
- Very low on-resistance  $R_{DS(on)}$  @  $V_{GS}=4.5\text{ V}$
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Superior thermal resistance
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

**Product Summary**

$V_{DS}$		34	V
$R_{DS(on),max}$	$V_{GS}=10\text{ V}$	9.2	mΩ
	$V_{GS}=4.5\text{ V}$	11.8	
$I_D$		44	A

**PG-TDSON-8**


Type	Package	Marking
BSC0909NS	PG-TDSON-8	0909NS

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	44	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	28	
		$V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$	39	
		$V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$	24	
		$V_{GS}=4.5\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$	12	
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	176	
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	$T_C=25\text{ °C}$	35	
Avalanche energy, single pulse	$E_{AS}$	$I_D=25\text{ A}, R_{GS}=25\text{ Ω}$	10	mJ
Gate source voltage	$V_{GS}$		±20	V

<sup>1)</sup> J-STD20 and JESD22

Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	27	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=50\text{ K/W}^2)$	2.5	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Thermal characteristics

Thermal resistance, junction - case	$R_{\text{thJC}}$	bottom	-	-	4.6	K/W
		top	-	-	20	
Device on PCB	$R_{\text{thJA}}$	6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	50	

Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified

### Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}$ , $I_{\text{D}}=1\text{ mA}$	34	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}$ , $I_{\text{D}}=250\text{ }\mu\text{A}$	1.2	-	2	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=34\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=25\text{ °C}$	-	0.1	1	$\mu\text{A}$
		$V_{\text{DS}}=34\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=16\text{ V}$ , $V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}$ , $I_{\text{D}}=15\text{ A}$	-	9.4	11.8	m $\Omega$
		$V_{\text{GS}}=10\text{ V}$ , $I_{\text{D}}=20\text{ A}$	-	7.7	9.2	
Gate resistance	$R_{\text{G}}$		1.5	3	6.0	$\Omega$
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$ , $I_{\text{D}}=30\text{ A}$	25	50	-	S

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See figure 3 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V}, f=1\text{ MHz}$	-	1100	1500	pF
Output capacitance	$C_{oss}$		-	390	520	
Reverse transfer capacitance	$C_{rss}$		-	25	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=4.5\text{ V}, I_D=30\text{ A}, R_{G,ext}=1.6\ \Omega$	-	9.6	-	ns
Rise time	$t_r$		-	4.4	-	
Turn-off delay time	$t_{d(off)}$		-	8.9	-	
Fall time	$t_f$		-	5.4	-	

**Gate Charge Characteristics<sup>5)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=15\text{ V}, I_D=30\text{ A}, V_{GS}=0\text{ to }4.5\text{ V}$	-	3.8	5.1	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.7	-	
Gate to drain charge	$Q_{gd}$		-	1.8	2.3	
Switching charge	$Q_{sw}$		-	3.8	-	
Gate charge total	$Q_g$		-	7.2	9.6	
Gate plateau voltage	$V_{plateau}$		-	3.3	-	V
Gate charge total	$Q_g$	$V_{DD}=15\text{ V}, I_D=30\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	15	20	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }4.5\text{ V}$	-	6.2	-	
Output charge	$Q_{oss}$	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	10	13	

**Reverse Diode**

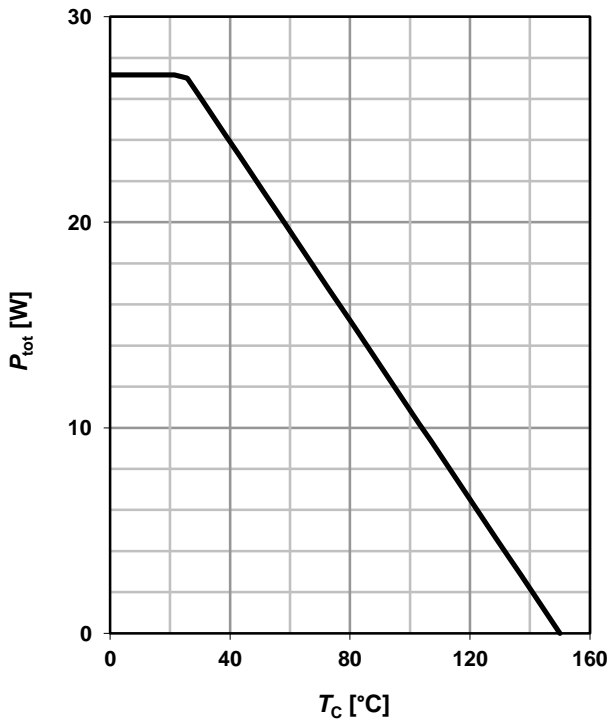
Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	25	A
Diode pulse current	$I_{S,pulse}$		-	-	176	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=30\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.92	-	V
Reverse recovery charge	$Q_{rr}$	$V_R=15\text{ V}, I_F=I_S, di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

<sup>4)</sup> See figure 13 for more detailed information

<sup>5)</sup> See figure 16 for gate charge parameter definition

### 1 Power dissipation

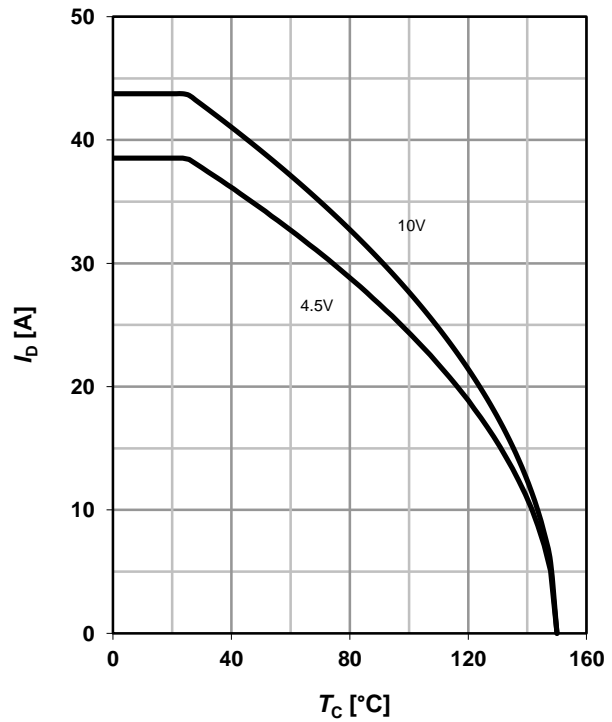
$$P_{tot}=f(T_C)$$



### 2 Drain current

$$I_D=f(T_C)$$

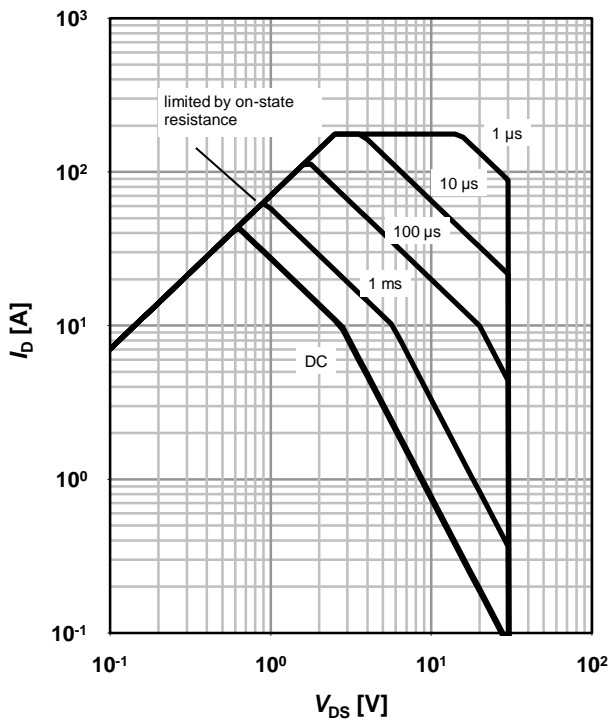
parameter:  $V_{GS}$



### 3 Safe operating area

$$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$$

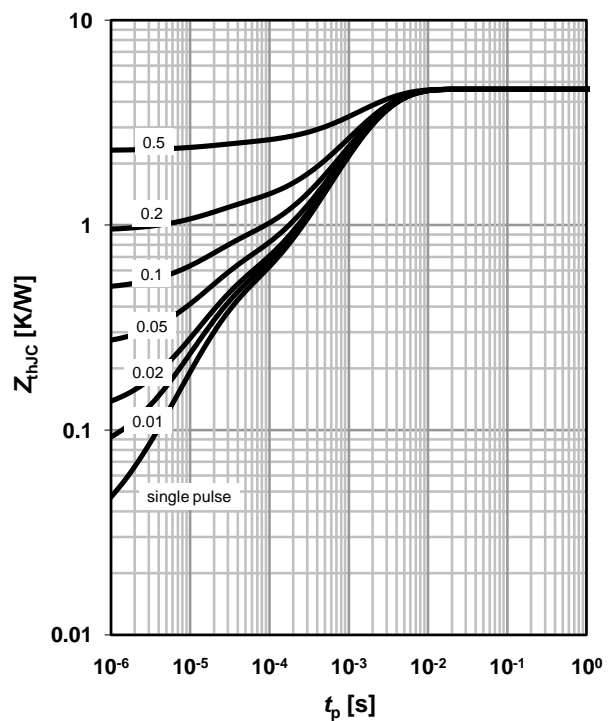
parameter:  $t_p$



### 4 Max. transient thermal impedance

$$Z_{thJC}=f(t_p)$$

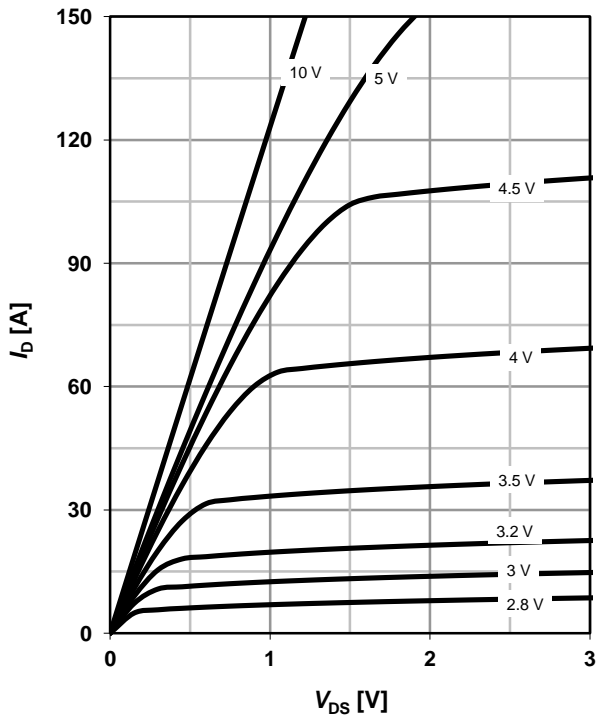
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

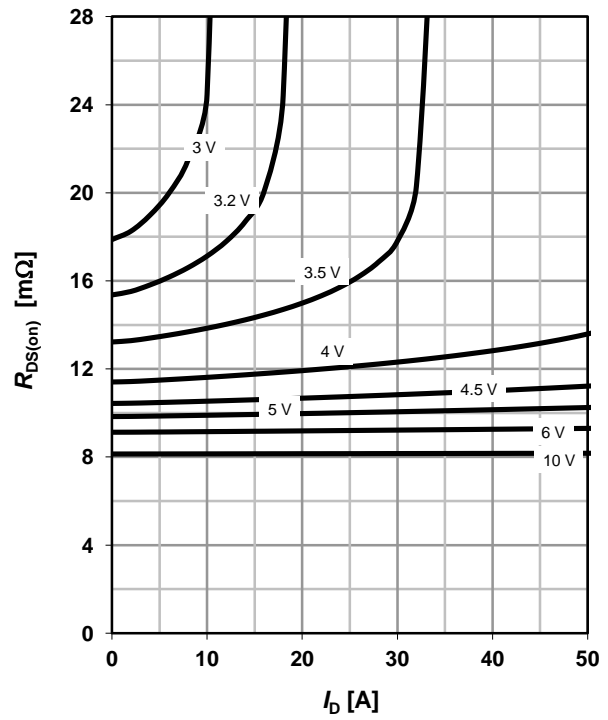
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

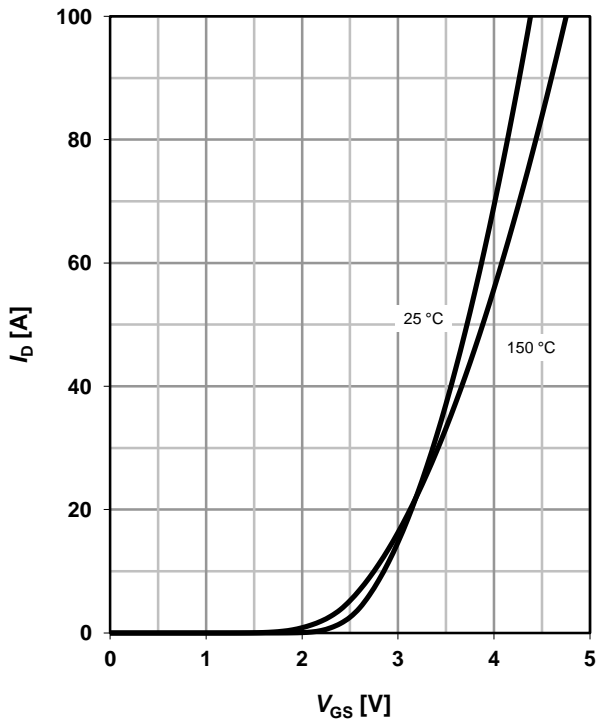
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

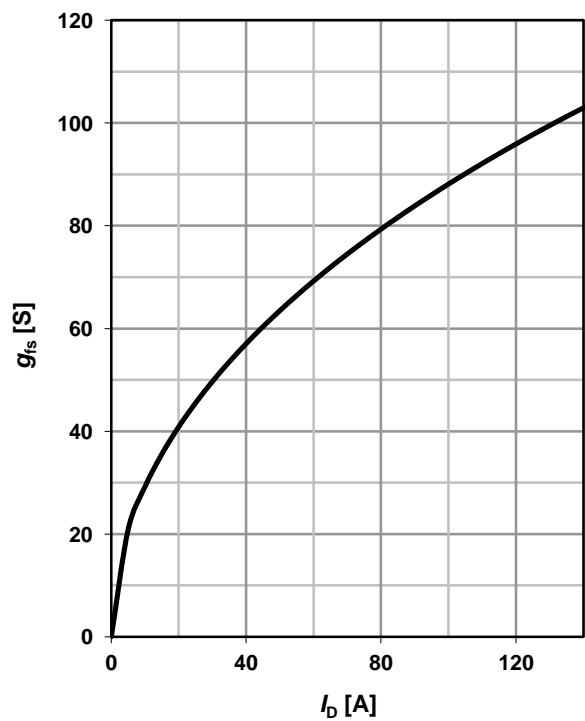
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



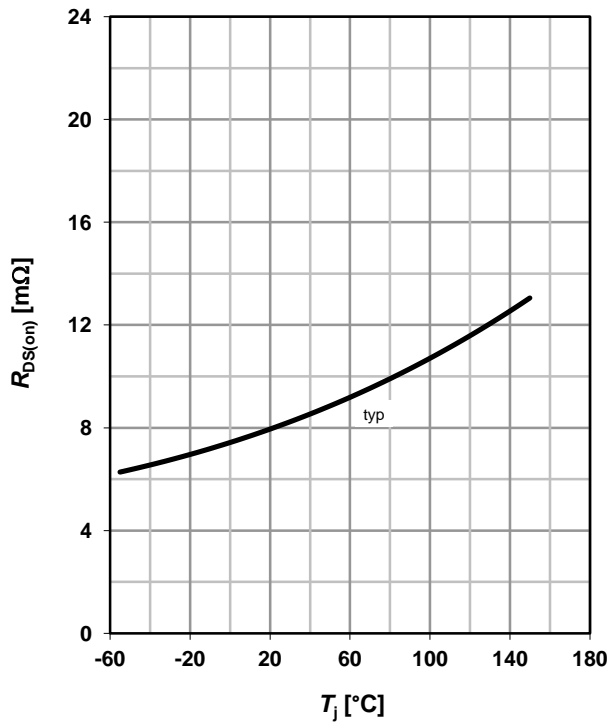
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



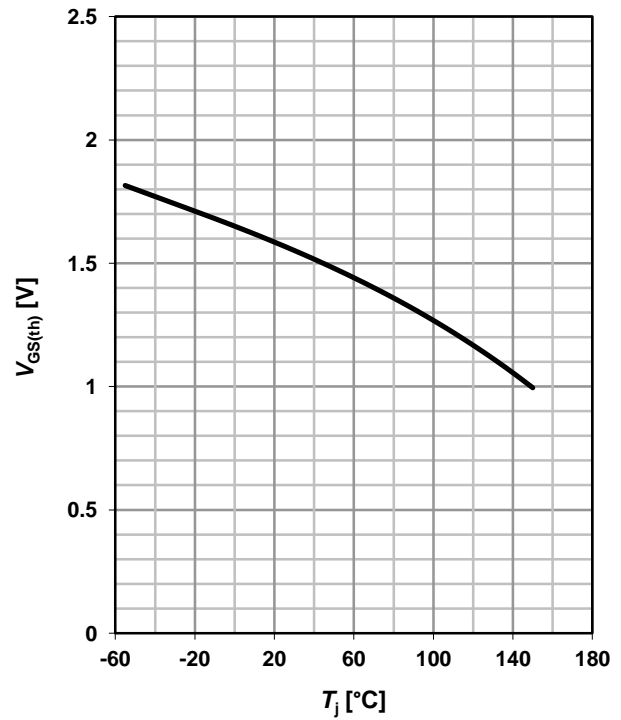
**9 Drain-source on-state resistance**

$R_{DS(on)}=f(T_j); I_D=30\text{ A}; V_{GS}=10\text{ V}$



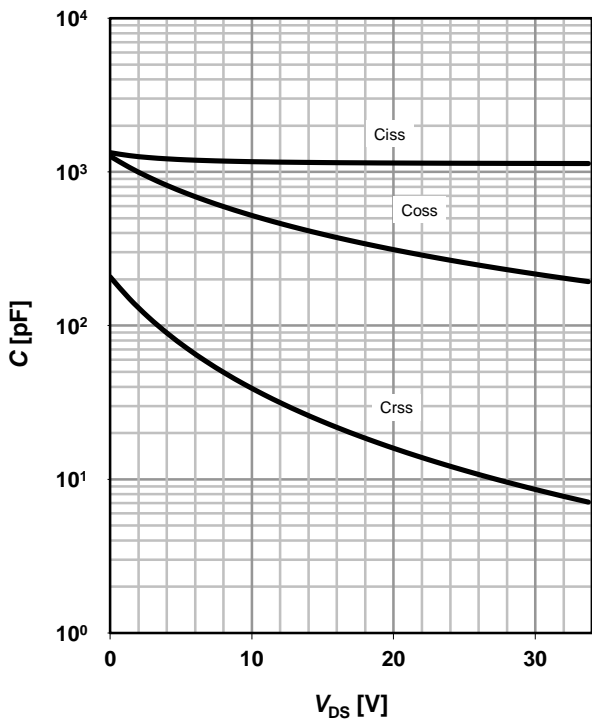
**10 Typ. gate threshold voltage**

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}; I_D=250\text{ }\mu\text{A}$



**11 Typ. capacitances**

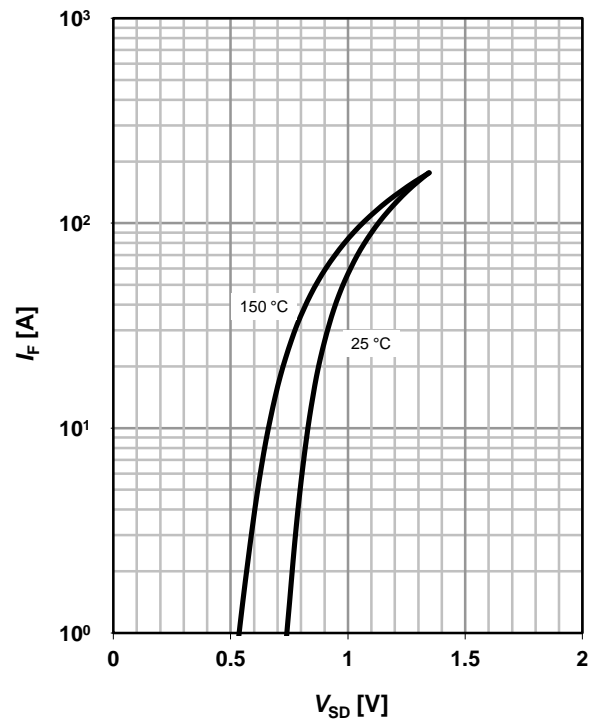
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

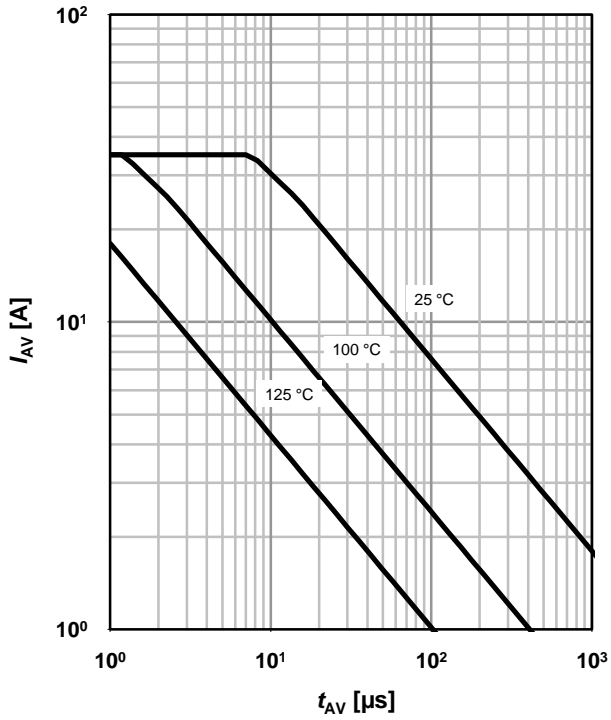
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

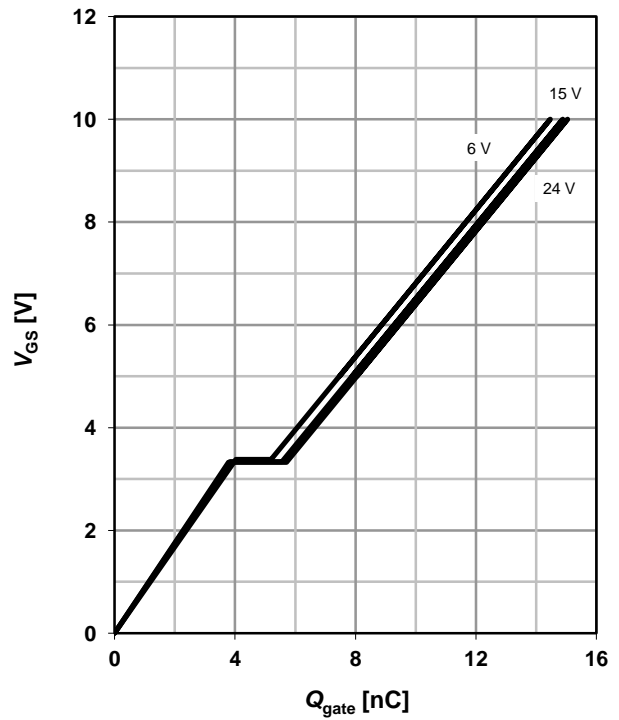
parameter:  $T_{j(\text{start})}$



**14 Typ. gate charge**

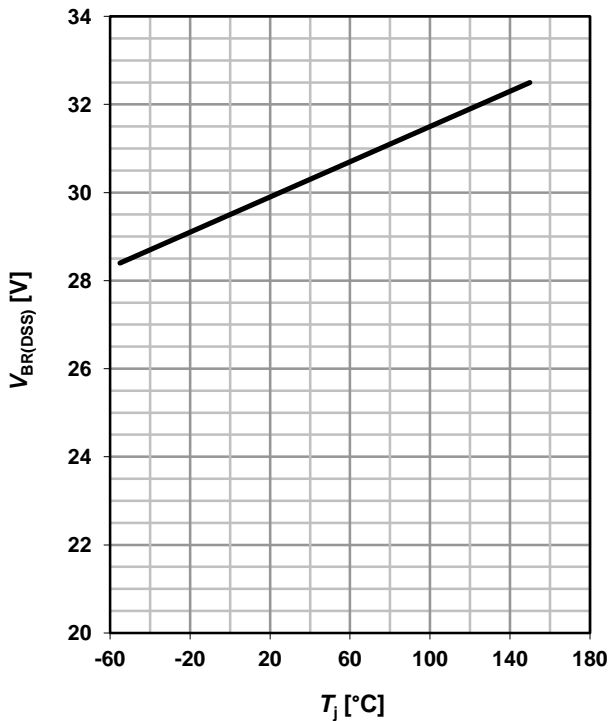
$V_{GS}=f(Q_{\text{gate}}); I_D=30 \text{ A pulsed}$

parameter:  $V_{DD}$

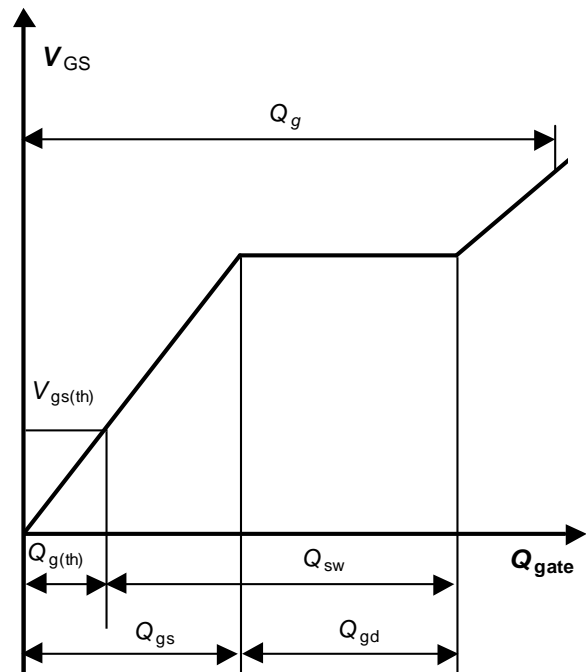


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



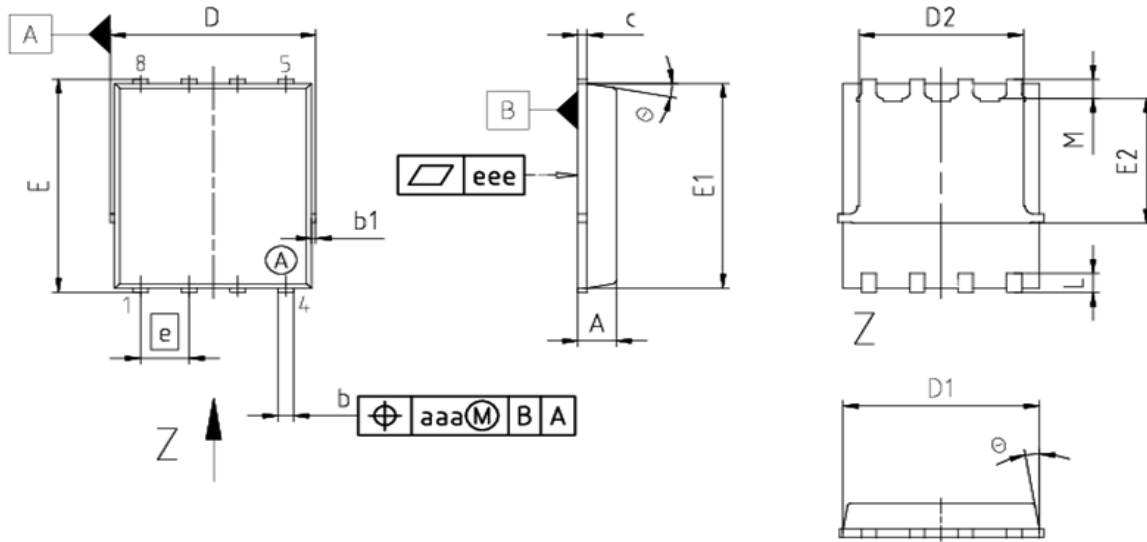
**16 Gate charge waveforms**



Package Outline

PG-TDSON-8

PG-TDSON-8-5: Outline



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
theta	8.5°	12°
aaa	0.25	
eee	0.08	

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